

NLV74HC11ADR2G Datasheet



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DiGi Electronics Part Number NLV74HC11ADR2G-DG

Manufacturer onsemi

Manufacturer Product Number NLV74HC11ADR2G

Description IC GATE AND 3CH 3-INP 14SOIC

Detailed Description AND Gate IC 3 Channel 14-SOIC



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DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NLV74HC11ADR2G	onsemi
Series:	Product Status:
74HC	Obsolete
Logic Type:	Number of Circuits:
AND Gate	3
Number of Inputs:	Features:
3	
Voltage - Supply:	Current - Quiescent (Max):
2V ~ 6V	1 μΑ
Current - Output High, Low:	Input Logic Level - Low:
5.2mA, 5.2mA	0.5V ~ 1.8V
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
1.5V ~ 4.2V	25ns @ 6V, 50pF
Operating Temperature:	Grade:
-55°C ~ 125°C	Automotive
Qualification:	Mounting Type:
AEC-Q100	Surface Mount
Supplier Device Package:	Package / Case:
14-SOIC	14-SOIC (0.154", 3.90mm Width)
Base Product Number:	
7411C11	

Environmental & Export classification

8542.39.0001

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	



Triple 3-Input AND Gate

High-Performance Silicon-Gate CMOS

MC74HC11A

The MC74HC11A is identical in pinout to the LS11. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 V to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

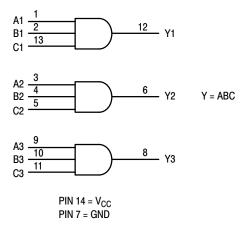


Figure 1. Logic Diagram

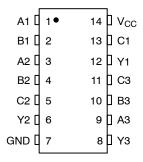
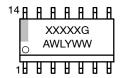


Figure 2. Pinout Diagram

MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G



XXXX = Specific Device Code
A = Assembly Location

WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs			Output
Α	В	С	Υ
L	Х	Х	L
X	L	X	L
X	X	L	L.
Н	Н	Н	Н

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
V _{IN}	DC Input Voltage		-0.5 to V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage		-0.5 to V _{CC} + 0.5	V
I _{IN}	DC Input Current, per Pin		±20	mA
I _{OUT}	DC Output Current, per Pin		±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins		±50	mA
I _{IK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})		±20	mA
I _{OK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})		±20	mA
T _{STG}	Storage Temperature		-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
TJ	Junction Temperature Under Bias		±150	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 1)	SOIC-14 TSSOP-14	116 150	°C/W
P _D	Power Dissipation in Still Air at 25°C	SOIC-14 TSSOP-14	1077 833	mW
MSL	Moisture Sensitivity		Level 1	-
F _R	Flammability Rating Ox	kygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model harged Device Model	>2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
 HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND) (Note 3)	0	V _{CC}	V	
T _A	Operating Free-Air Temperature			+125	°C
t _r , t _f	V	_{CC} = 2.0 V _{CC} = 4.5 V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

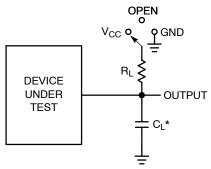
				Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V _{CC} V	– 55 to 25°C	≤ 85 °C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $ I_{out} \le 20 \mu A$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $ I_{out} \le 20 \mu A$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$ \begin{aligned} V_{in} = V_{IH} \text{ or } V_{IL} & & I_{out} \leq 2.4 \text{ mA} \\ & & I_{out} \leq 4.0 \text{ mA} \\ & & I_{out} \leq 5.2 \text{ mA} \end{aligned} $	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$ \begin{aligned} V_{in} = V_{IH} \text{ or } V_{IL} & & I_{out} \leq 2.4 \text{ mA} \\ & & I_{out} \leq 4.0 \text{ mA} \\ & & I_{out} \leq 5.2 \text{ mA} \end{aligned} $	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
l _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	1	10	40	μΑ

AC ELECTRICAL CHARACTERISTICS

			Guaranteed Limit			
Symbol	Parameter	V _{CC} V	– 55 to 25°C	≤ 85 °C	≤ 125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, (A, B, or C) to Y (Figures 3 and 4)	2.0 3.0 4.5 6.0	95 45 19 16	120 60 24 20	145 75 29 25	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C _{in}	Maximum Input Capacitance	-	10	10	10	pF

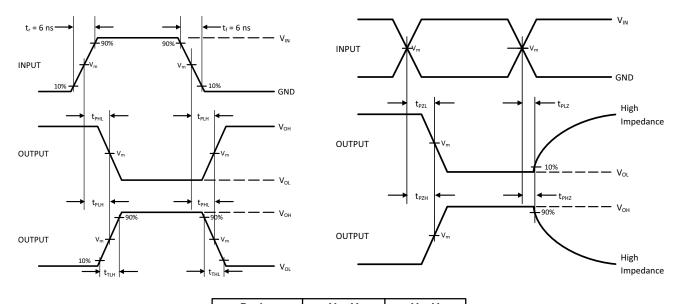
		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	27	pF

^{*}Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC} 2f + I_{CC} V_{CC}$.



Test	Switch Position	CL	R_{L}
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 3. Test Circuit



 Device
 V_{IN}, V
 V_m, V

 MC74HC11A
 V_{CC}
 50% x V_{CC}

Figure 4. Switching Waveforms

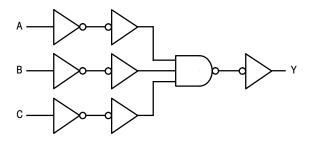


Figure 5. Expanded Logic Diagram (1/3 of the Device)

^{*}C_L Includes probe and jig capacitance

ORDERING INFORMATION

Device	Package	Marking	Shipping [†]
MC74HC11ADG	SOIC-14	HC11A	55 Units / Rail
MC74HC11ADG-Q*	SOIC-14	HC11A	55 Units / Rail
MC74HC11ADR2G	SOIC-14	HC11A	2500 / Tape & Reel
MC74HC11ADR2G-Q*	SOIC-14	HC11A	2500 / Tape & Reel
MC74HC11ADTR2G	TSSOP-14	HC 11A	2500 / Tape & Reel
MC74HC11ADTR2G-Q*	TSSOP-14	HC 11A	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



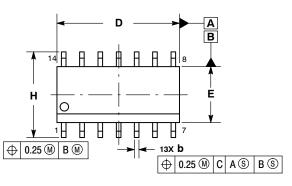
MECHANICAL CASE OUTLINE

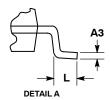
PACKAGE DIMENSIONS

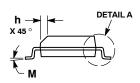


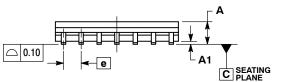
SOIC-14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016









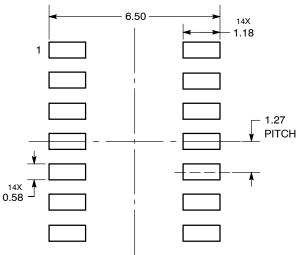
- ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT
- MAXIMUM MATERIAL CONDITION.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

NOTES:
1. DIMENSIONING AND TOLERANCING PER

5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE

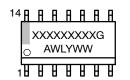
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
АЗ	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
е	1.27 BSC		0.050	BSC
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7°	0 °	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code Α = Assembly Location

WL = Wafer Lot Υ = Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC-14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

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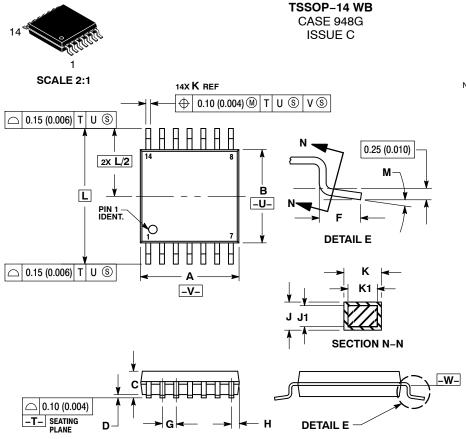
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

DATE 17 FEB 2016



- NOTES.

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

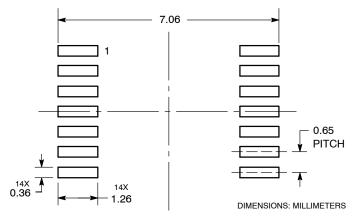
 3. DIMENSION A DOES NOT INCLUDE MOLD
- FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
- INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
- INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR DEFERENCE ONLY
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE
- DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	o°	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



= Assembly Location

= Wafer Lot = Year = Work Week W

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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