NLV74HC139ADR2G Datasheet
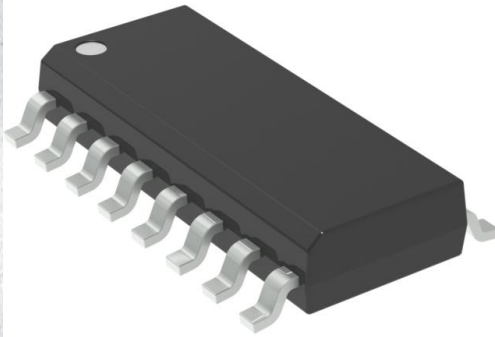
DiGi Electronics Part Number	NLV74HC139ADR2G-DG
Manufacturer	onsemi
Manufacturer Product Number	NLV74HC139ADR2G
Description	IC DECODER/DEMUX 1X2:4 16SOIC
Detailed Description	Decoder/Demultiplexer 1 x 2:4 16-SOIC

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NLV74HC139ADR2G	onsemi
Series:	Product Status:
74HC	Obsolete
Type:	Circuit:
Decoder/Demultiplexer	1 x 2:4
Independent Circuits:	Current - Output High, Low:
2	5.2mA, 5.2mA
Voltage Supply Source:	Voltage - Supply:
Single Supply	2V ~ 6V
Operating Temperature:	Mounting Type:
-55°C ~ 125°C	Surface Mount
Package / Case:	Supplier Device Package:
16-SOIC (0.154", 3.90mm Width)	16-SOIC
Base Product Number:	
74HC139	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

Dual 1-of-4 Decoder/ Demultiplexer

High−Performance Silicon−Gate CMOS

MC74HC139A

The MC74HC139A is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.

This device consists of two independent 1−of−4 decoders, each of which decodes a two−bit Address to one−of−four active−low outputs. Active−low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
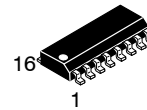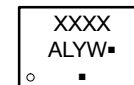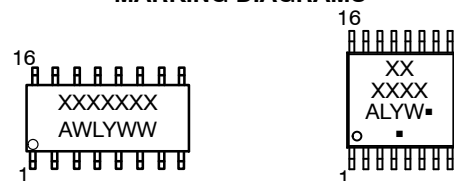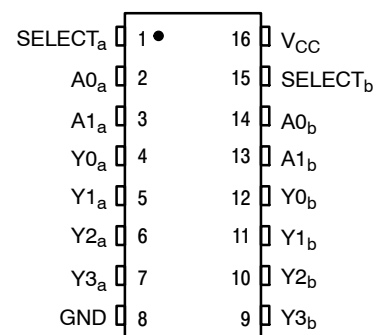
SOIC−16
D SUFFIX
CASE 751B
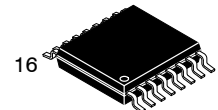
TSSOP−16
DT SUFFIX
CASE 948F

QFN16
MN SUFFIX
CASE 485AW

MARKING DIAGRAMS

XXXXXXX
AWLYWW

XX
XXXX
ALYW▪

XXXX
ALYW▪

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

SELECT$_a$	1	16	V$_{CC}$
A0$_a$	2	15	SELECT$_b$
A1$_a$	3	14	A0$_b$
Y0$_a$	4	13	A1$_b$
Y1$_a$	5	12	Y0$_b$
Y2$_a$	6	11	Y1$_b$
Y3$_a$	7	10	Y2$_b$
GND	8	9	Y3$_b$

ORDERING INFORMATION

MC74HC139A

ADDRESS INPUTS { A0$_a$ — 2
A1$_a$ — 3

4 — Y0$_a$
5 — Y1$_a$
6 — Y2$_a$
7 — Y3$_a$ } ACTIVE–LOW OUTPUTS

SELECT$_a$ — 1

PIN 16 = V$_{CC}$
PIN 8 = GND

ADDRESS INPUTS { A0$_b$ — 14
A1$_b$ — 13

12 — Y0$_b$
11 — Y1$_b$
10 — Y2$_b$
9 — Y3$_b$ } ACTIVE–LOW OUTPUTS

SELECT$_b$ — 15

Figure 1. Logic Diagram
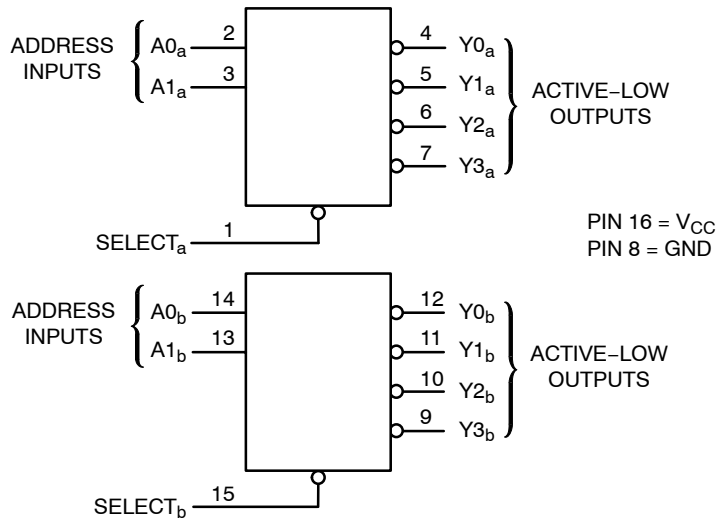
FUNCTION TABLE

Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care

MC74HC139A

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		±150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−16 QFN16 TSSOP−16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
4. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

MC74HC139A

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55°C to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V $|I_{OUT}| \leq$ 20 µA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V $|I_{OUT}| \leq$ 20 µA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $|I_{OUT}| \leq$ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $\quad |I_{OUT}| \leq$ 4.0 mA $|I_{OUT}| \leq$ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $|I_{OUT}| \leq$ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $\quad |I_{OUT}| \leq$ 4.0 mA $|I_{OUT}| \leq$ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0 µA	6.0	4	40	160	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55°C to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 2 and 3)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF

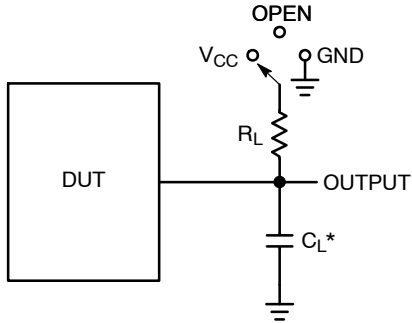|		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Decoder) (Note 5)	55	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

MC74HC139A

SWITCHING WAVEFORMS AND TEST CIRCUIT

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

*C_L Includes probe and jig capacitance

Figure 2. Test Circuit
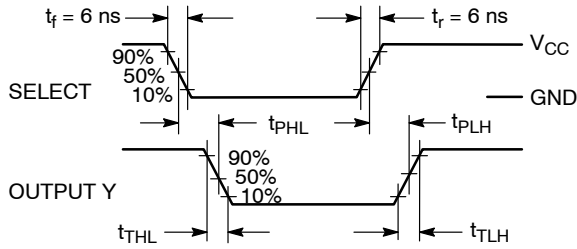
Figure 3. Switching Waveform
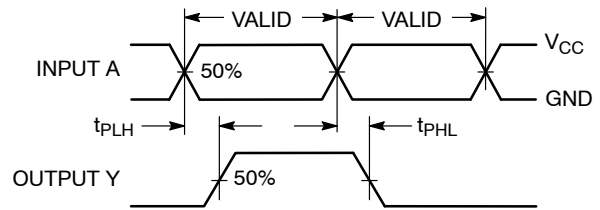
Figure 4. Switching Waveform

PIN DESCRIPTIONS

ADDRESS INPUTS

A0$_a$, A1$_a$, A0$_b$, A1$_b$ (Pins 2, 3, 14, 13)

Address inputs. These inputs, when the respective 1−of−4 decoder is enabled, determine which of its four active−low outputs is selected.

CONTROL INPUTS

Select$_a$, Select$_b$ (Pins 1, 15)

Active−low select inputs. For a low level on this input, the outputs for that particular decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

OUTPUTS

Y0$_a$ – Y3$_a$, Y0$_b$ – Y3$_b$ (Pins 4 – 7, 12, 11, 10, 9)

Active−low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.
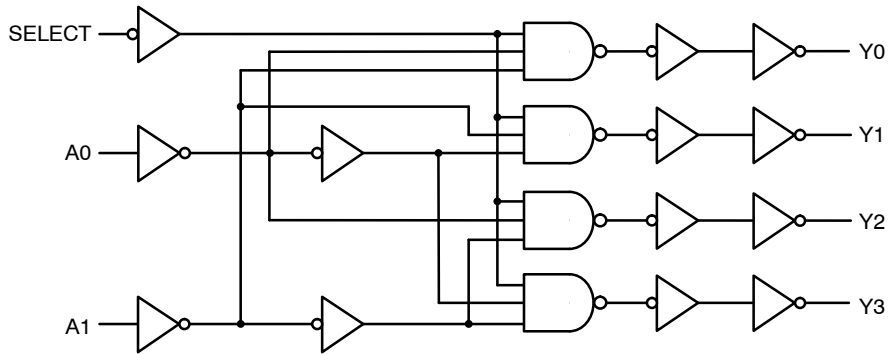
Figure 5. Expanded Logic Diagram
(1/2 of Device)

MC74HC139A

ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
MC74HC139ADR2G	HC139AG	SOIC−16	2500 / Tape & Reel
MC74HC139ADR2G−Q*	HC139AG	SOIC−16	2500 / Tape & Reel
MC74HC139ADTR2G	HC 139A	TSSOP−16	2500 / Tape & Reel
MC74HC139ADTR2G−Q*	HC 139A	TSSOP−16	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC74HC139A

PACKAGE DIMENSIONS

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

DATE 11 DEC 2008

SCALE 2:1

TOP VIEW

PIN ONE
REFERENCE

2X � 0.15 C

2X � 0.15 C

D ← → A
B
E

SIDE VIEW

0.10 C
16X � 0.08 C
NOTE 4

DETAIL B

A
(A3)
A1
C SEATING PLANE

BOTTOM VIEW

0.15 C A B
D2
16X L
K
DETAIL A
8
10   0.15 C A B
E2
2
15   16X b
1
e
e/2

0.10 C A B
0.05 C   NOTE 3
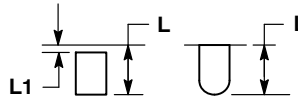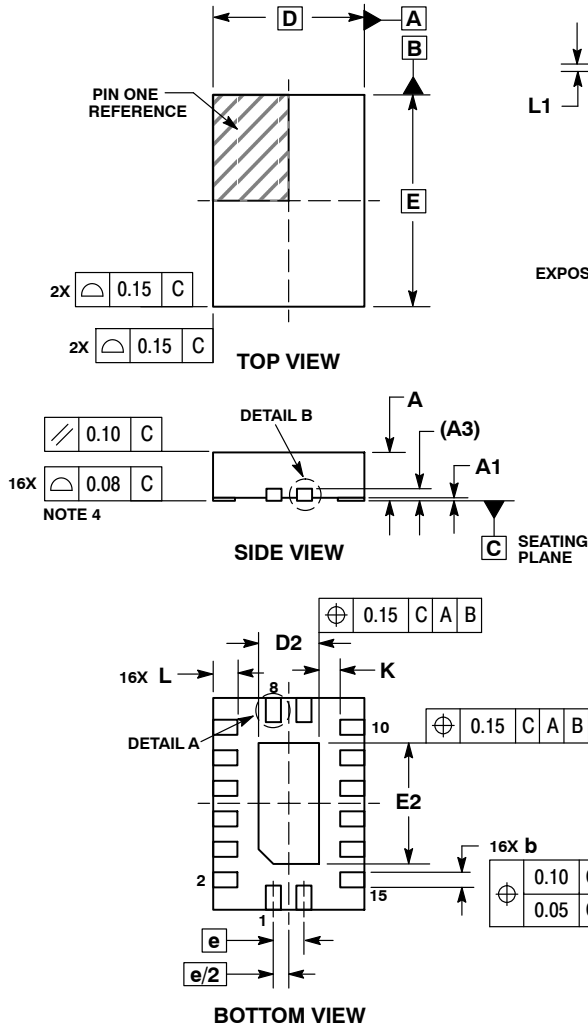
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

L
L
L1
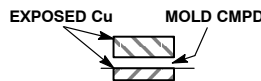
DETAIL B
ALTERNATE
CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
---	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*
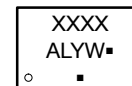
XXXX
ALYW▪

XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*
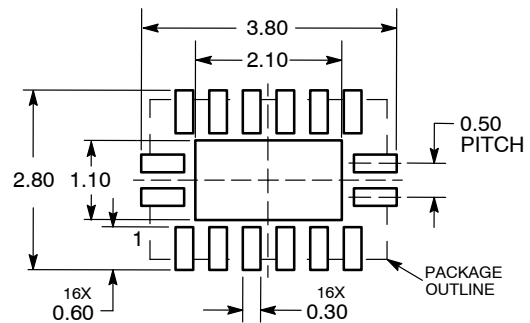
3.80
2.10
2.80   1.10
1
16X
0.60
16X
0.30
0.50
PITCH
PACKAGE
OUTLINE

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
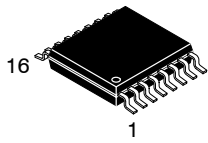
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

onsemi
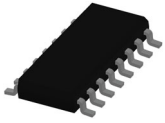
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

TOP VIEW

SEATING PLANE

SIDE VIEW

END VIEW

DETAIL "A"

0.25 GAUGE PLANE

DETAIL "A"
Scale 3:1
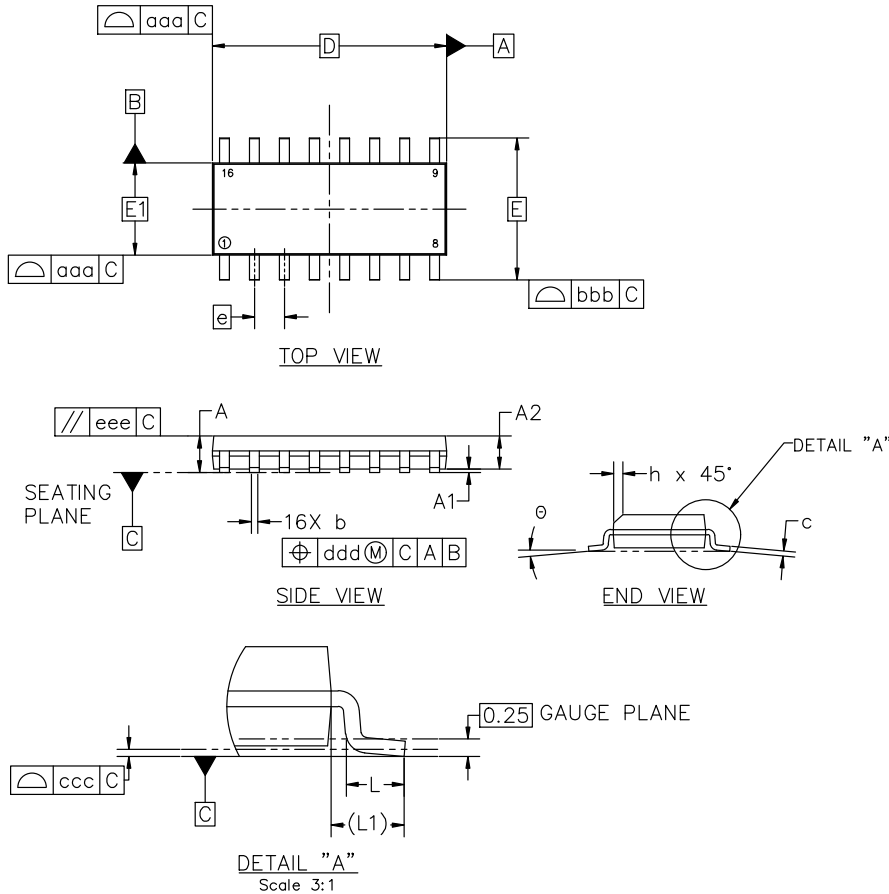
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		

8X
6.40

16X
0.58

1.270
PITCH

1.120
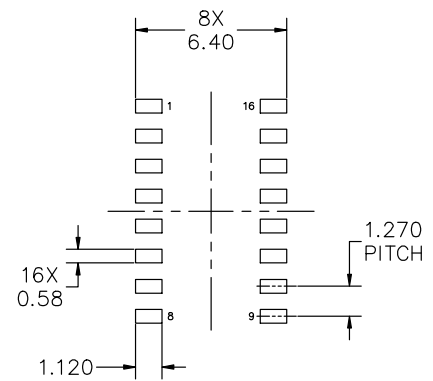
RECOMMENDED MOUNTING FOOTPRINT
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16 9.90X3.90X1.37 1.27P		PAGE 1 OF 2

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

**GENERIC
MARKING DIAGRAM***

```
16 ┌─────────────────┐
   │ XXXXXXXXXXXXG   │
   │ XXXXXXXXXXXXX   │
   │     AWLYWW      │
 1 └─────────────────┘
```
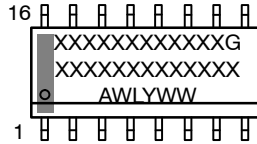
XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
Y   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to
 device data sheet for actual part marking.
 Pb−Free indicator, "G" or microdot "▪", may
 or may not be present. Some products may
 not follow the Generic Marking.

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. EMITTER	3. NO CONNECTION	3. EMITTER, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. EMITTER	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. EMITTER, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. EMITTER	10. ANODE	10. BASE, #3	10. EMITTER, #4
11. NO CONNECTION	11. NO CONNECTION	11. EMITTER, #3	11. BASE, #3
12. EMITTER	12. CATHODE	12. COLLECTOR, #3	12. EMITTER, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. EMITTER, #2
15. EMITTER	15. ANODE	15. EMITTER, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. EMITTER, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

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DESCRIPTION:	SOIC−16 9.90X3.90X1.37 1.27P		PAGE 2 OF 2

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

SCALE 2:1

16X K REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

◺ | 0.15 (0.006) | T U Ⓢ

2X L/2

L

16
9

PIN 1
IDENT.

B
−U−

1
8

◺ | 0.15 (0.006) | T U Ⓢ

A
−V−

K
K1

J1

J

SECTION N−N

N

0.25 (0.010)

M

N

F

DETAIL E

C

◺ | 0.10 (0.004)

−T− SEATING PLANE

D

G

H

−W−

DETAIL E
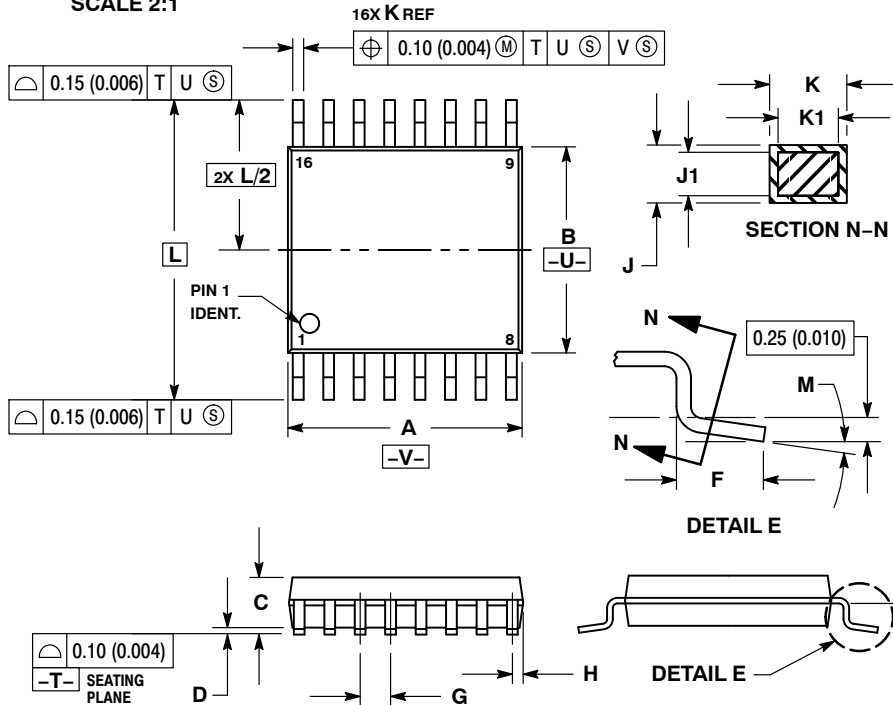
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*
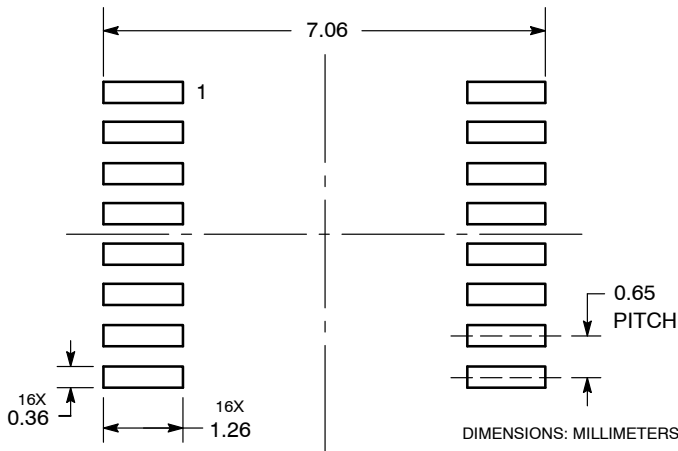
7.06

1

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

16

XXXX
XXXX
ᵒ ALYW

1
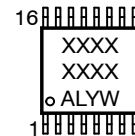
XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP−16		PAGE 1 OF 1

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