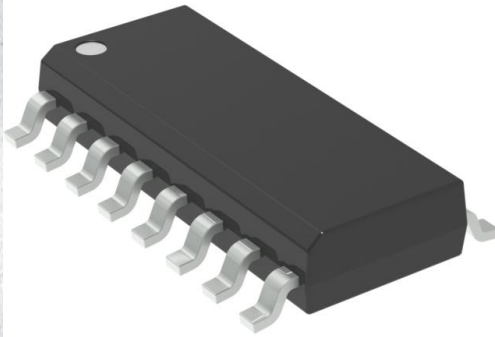


NLV74HC157ADR2G Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	NLV74HC157ADR2G-DG
Manufacturer	onsemi
Manufacturer Product Number	NLV74HC157ADR2G
Description	IC DATA SEL/MULTPL 4X2:1 16SOIC
Detailed Description	Data Selector/Multiplexer 4 x 2:1 16-SOIC



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

NLV74HC157ADR2G

Series:

74HC

Type:

Data Selector/Multiplexer

Independent Circuits:

1

Voltage Supply Source:

Single Supply

Operating Temperature:

-55°C ~ 125°C

Package / Case:

16-SOIC (0.154", 3.90mm Width)

Base Product Number:

74HC157

Manufacturer:

onsemi

Product Status:

Obsolete

Circuit:

4 x 2:1

Current - Output High, Low:

7.8mA, 7.8mA

Voltage - Supply:

2V ~ 6V

Mounting Type:

Surface Mount

Supplier Device Package:

16-SOIC

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

Quad 2-Input Data Selectors/Multiplexers

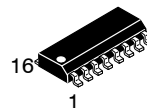
MC74HC157A

The MC74HC157A is identical in pinout to the LS157. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

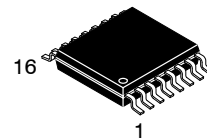
This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



SOIC-16
D SUFFIX
CASE 751B

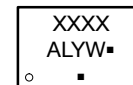
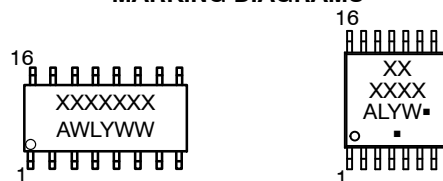


TSSOP-16
DT SUFFIX
CASE 948F



QFN16
MN SUFFIX
CASE 485AW

MARKING DIAGRAMS



- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

MC74HC157A

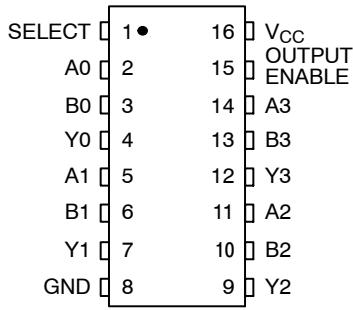


Figure 1. Pin Assignment

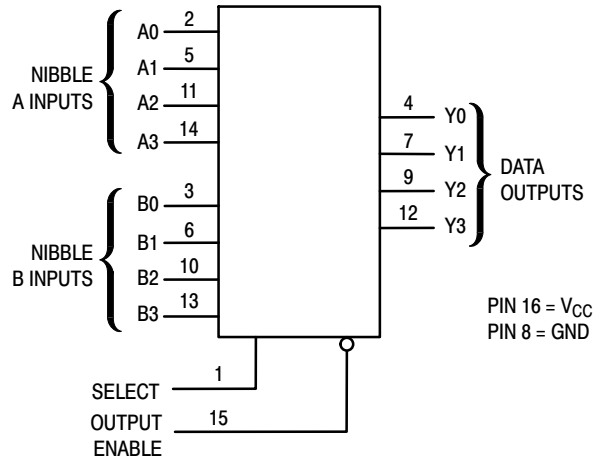


Figure 2. Logic Diagram

FUNCTION TABLE

Inputs		Outputs Y0 - Y3
Output Enable	Select	
H	X	L
L	L	A0 - A3
L	H	B0 - B3

X = don't care
 A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

MC74HC157A**MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V	
V _{IN}	DC Input Voltage	-0.5 to V _{CC} + 0.5	V	
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V	
I _{IN}	DC Input Current, per Pin	±20	mA	
I _{OUT}	DC Output Current, per Pin	±25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA	
I _{IK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})	±20	mA	
I _{OK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})	±20	mA	
T _{STG}	Storage Temperature	-65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C	
T _J	Junction Temperature Under Bias	±150	°C	
θ _{JA}	Thermal Resistance (Note 1)	SOIC-16 QFN16 TSSOP-16	126 118 159	°C/W
P _D	Power Dissipation in Still Air at 25°C	SOIC-16 QFN16 TSSOP-16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	-
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Note 3)	0	V _{CC}	V
T _A	Operating Free-Air Temperature	-55	+125	°C
t _r , t _f	Input Rise or Fall Time	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74HC157A**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		I _{OUT} ≤ 2.4 mA I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	3.0	2.48	2.34	2.2	
			4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V _{OL}	Minimum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		I _{OUT} ≤ 2.4 mA I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	3.0	0.26	0.33	0.4	
			4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND	6.0	4.0	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

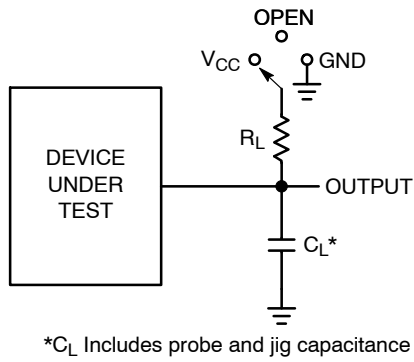
MC74HC157A**AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y	2.0	105	130	160	ns
		3.0	65	85	115	
		4.5	21	26	32	
		6.0	18	22	27	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Select to Output Y	2.0	110	140	165	ns
		3.0	70	90	115	
		4.5	22	28	33	
		6.0	19	24	28	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Output Enable to Output Y	2.0	100	125	150	ns
		3.0	60	80	110	
		4.5	20	25	30	
		6.0	17	21	26	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	-	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 4)	5.0	Typical @ 25°C		pF
			33		

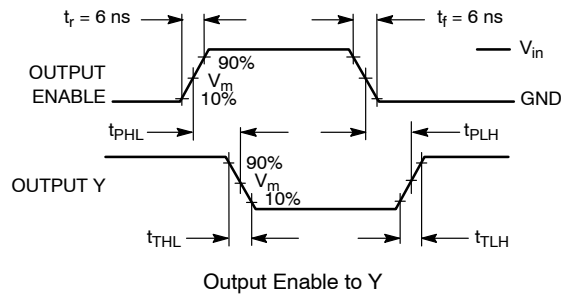
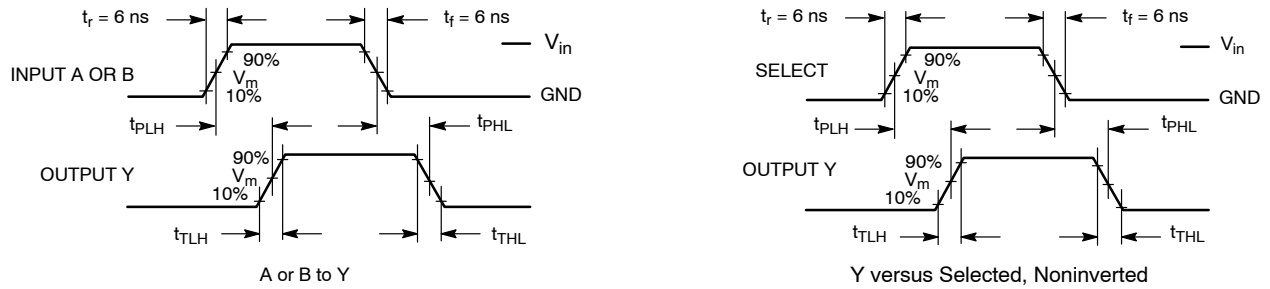
4. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f + I_{CC} \times V_{CC}$.

MC74HC157A



Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 3. Test Circuit



Device	V _{IN} , V	V _m , V
MC74HC157A	V _{CC}	50% x V _{CC}

Figure 4. Switching Waveforms

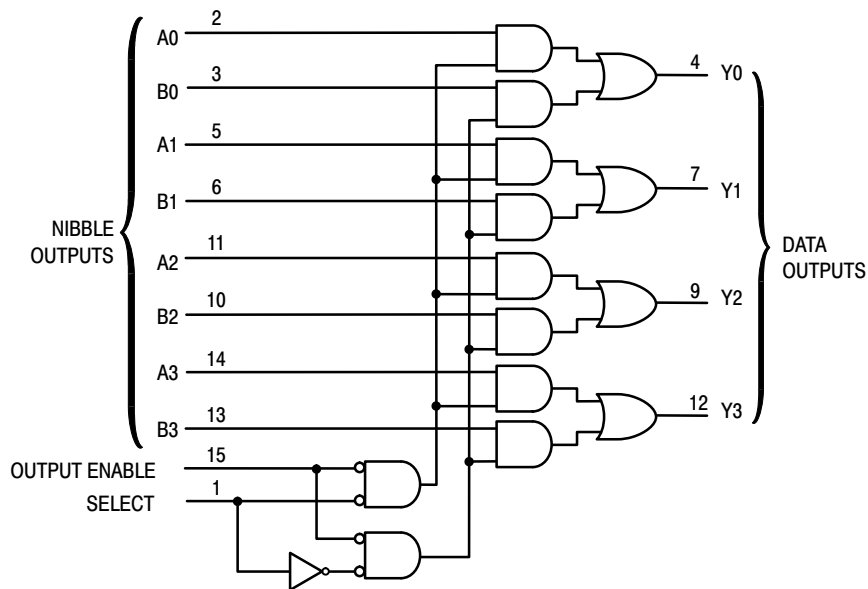
MC74HC157A

Figure 5. Expanded Logic Diagram

PIN DESCRIPTIONS**INPUTS****A0, A1, A2, A3 (Pins 2, 5, 11, 14)**

Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

B0, B1, B2, B3 (Pins 3, 6, 10, 13)

Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

OUTPUTS**Y0, Y1, Y2, Y3 (Pins 4, 7, 9, 12)**

Data outputs. The selected input Nibble is presented at these outputs when the Output Enable input is at a low level.

The data present on these pins is in its noninverted form. For the Output Enable input at a high level, the outputs are at a low level.

CONTROL INPUTS**Select (Pin 1)**

Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

Output Enable (Pin 15)

Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level.

MC74HC157A**ORDERING INFORMATION**

Device	Package	Marking	Shipping†
MC74HC157ADG	SOIC-16	HC157AG	1000 Units / Tape & Reel
MC74HC157ADR2G	SOIC-16	HC157AG	1000 Units / Tape & Reel
MC74HC157ADR2G-Q*	SOIC-16	HC157AG	1000 Units / Tape & Reel
MC74HC157ADTR2G	TSSOP-16	HC 157A	2500 Units / Tape & Reel
MC74HC157ADTR2G-Q*	TSSOP-16	HC 157A	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC74HC157A

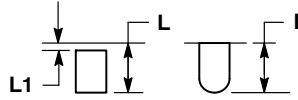
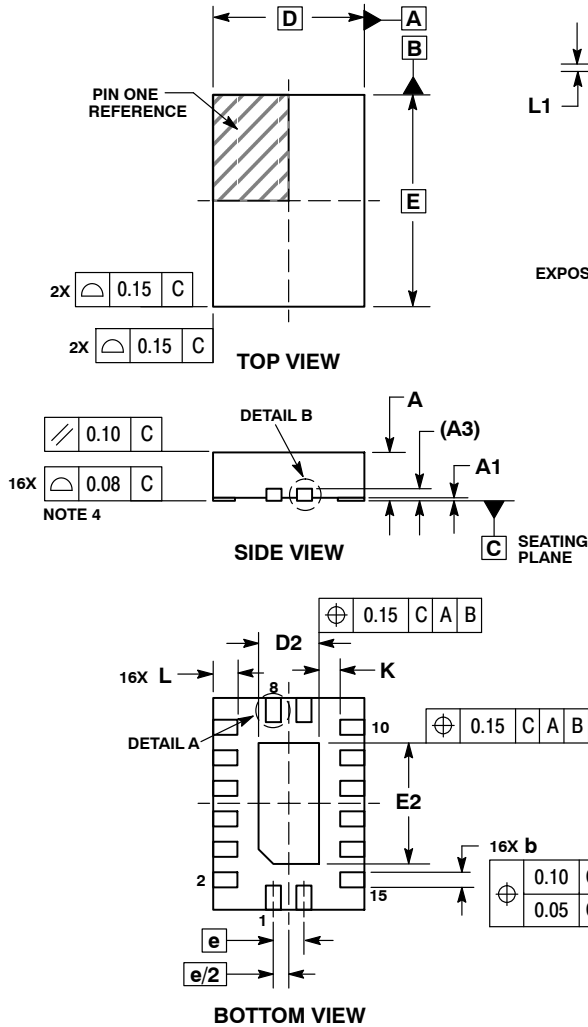
PACKAGE DIMENSIONS



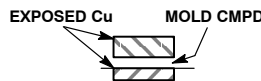
SCALE 2:1

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

DATE 11 DEC 2008



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



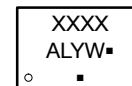
DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.50	BSC
D2	0.85	1.15
E	3.50	BSC
E2	1.85	2.15
e	0.50	BSC
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*

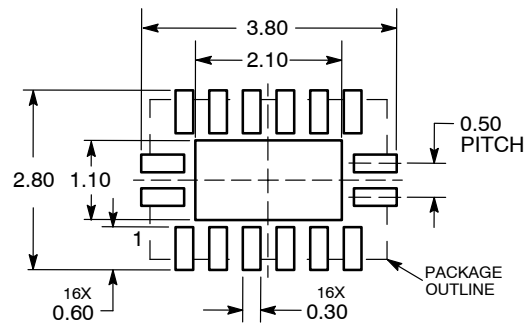


- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*

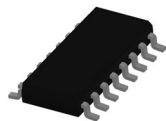


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**

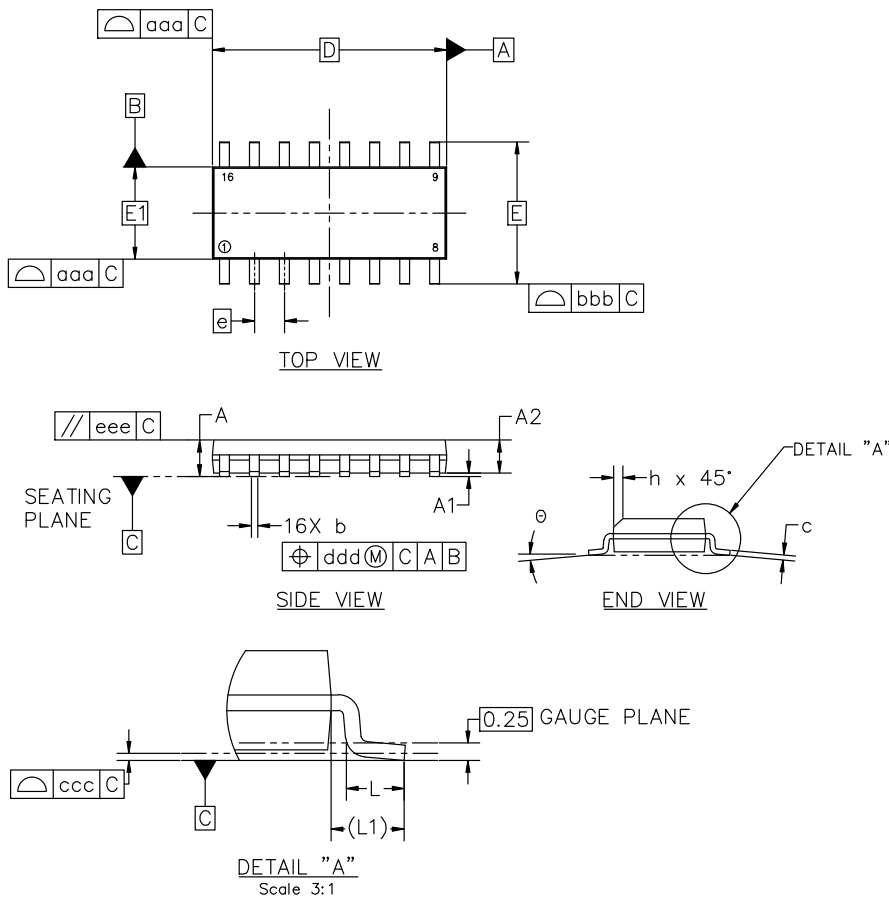


**SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M**

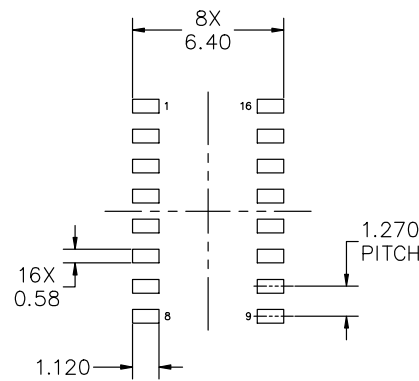
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

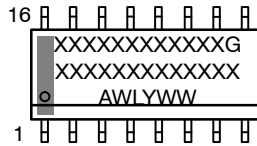
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DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 1 OF 2

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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

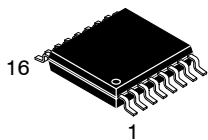
<p>STYLE 1:</p> <p>PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH</p>	

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DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 2 OF 2

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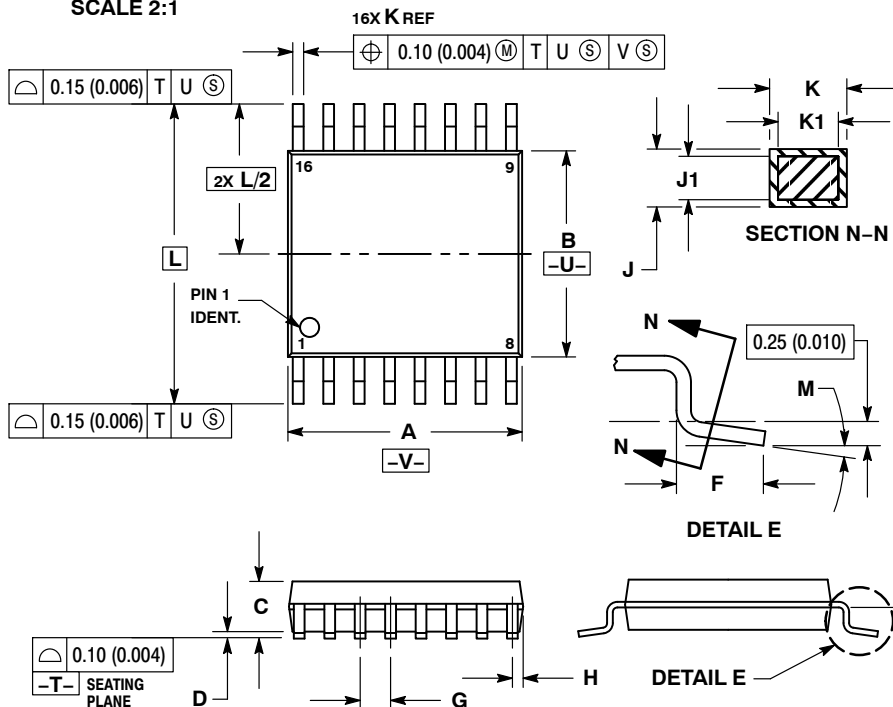


**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



**TSSOP-16 WB
CASE 948F
ISSUE B**

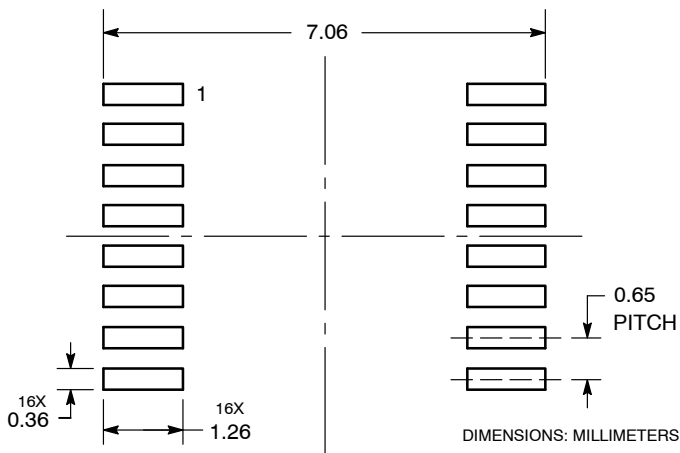
DATE 19 OCT 2006



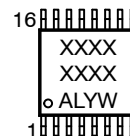
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***



**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

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