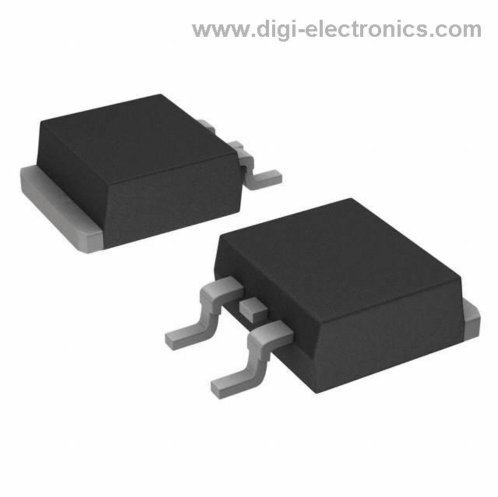
NTD85N02R Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	NTD85N02R-DG
Manufacturer	onsemi
Manufacturer Product Number	NTD85N02R
Description	MOSFET N-CH 24V 12A/85A DPAK
Detailed Description	N-Channel 24 V 12A (Ta), 85A (Tc) 1.25W (Ta), 78.1 W (Tc) Surface Mount DPAK

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NTD85N02R	onsemi
Series:	Product Status:
-	Obsolete
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
24 V	12A (Ta), 85A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	5.2mOhm @ 20A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2V @ 250µA	17.7 nC @ 5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	2050 pF @ 20 V
FET Feature:	Power Dissipation (Max):
-	1.25W (Ta), 78.1W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
DPAK	TO-252-3, DPAK (2 Leads + Tab), SC-63
Base Product Number:	
NTD85	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
RoHS non-compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

NTD85N02R

Power MOSFET, 85 A, 24 V, N-Channel DPAK/IPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Low Gate Charge to Minimize Switching Losses
- Pb−Free Packages are Available

Applications

- CPU Power Delivery
- DC−DC Converters
- Low Side Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	24	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	17	A
		T_A = 85°C		12	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.4	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	I_D	12	A
		T_A = 85°C		8.8	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	1.25	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	85	A
		T_C = 85°C		58	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	78.1	W
Pulsed Drain Current	T_A = 25°C, t_p = 10μs		I_{DM}	192	A
Current Limited by Package		T_A = 25°C	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	78	A
Drain to Source dV/dt			dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy T_J = 25°C, V_{DD} = 30 V, V_{GS} = 10 V, I_L = 13 A_{pk}, L = 1.0 mH, R_G = 25 Ω)			EAS	85	mJ
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

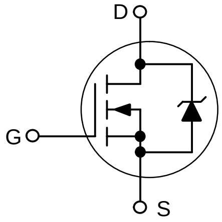
1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

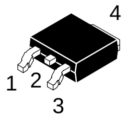
ON Semiconductor®

http://onsemi.com

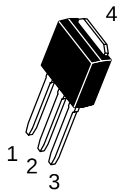
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
24 V	5.2 mΩ @ 10 V	85 A

N−Channel



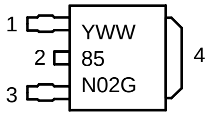


DPAK
CASE 369AA
STYLE2

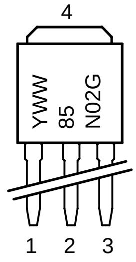


DPAK−3
CASE 369D
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



1 Gate
2 Drain
3 Source
4 Drain



Y = Year
WW = Work Week
85N02R = Specific Device Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	1.6	°C/W
Junction−to−TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	52	
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	100	

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		24	28		V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				20.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25 °C			1.5	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0	1.5	2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4		mV/°C
Drain−to−Source on Resistance	$R_{DS(ON)}$	V_{GS} = 10 V	I_D = 20 A		4.8	5.2	mΩ
		V_{GS} = 4.5 V	I_D = 20 A		6.5		
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 15 A			38		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 20 V			2050		pF
Output Capacitance	C_{OSS}				871		
Reverse Transfer Capacitance	C_{RSS}				359		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 5.0 V, V_{DS} = 10 V; I_D = 10 A			17.7		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.6		
Gate−to−Source Charge	Q_{GS}				2.6		
Gate−to−Drain Charge	Q_{GD}				7.1		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 10 V; I_D = 10 A			35.1		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 10 V, I_D = 30 A, R_G = 3.0 Ω			6.3		ns
Rise Time	t_r				77		
Turn−Off Delay Time	$t_{d(OFF)}$				25		
Fall Time	t_f				12		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.81	1.0	V
			T_J = 125°C		0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 20 A			37.5		ns
Charge Time	t_a				16.8		
Discharge Time	t_b				20.7		
Reverse Recovery Charge	Q_{RR}				27		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			2.49		nH
Drain Inductance, DPAK	L_D				0.0164		
Drain Inductance, IPAK*	L_D				1.88		
Gate Inductance	L_G				3.46		
Gate Resistance	R_G				1.2		Ω

*Assume standoff of 110 mils.

ORDERING INFORMATION

Device	Package	Shipping†
NTD85N02R	DPAK	75 Units / Rail
NTD85N02RG	DPAK (Pb−Free)	
NTD85N02R−001	IPAK	800 / Tape & Reel
NTD85N02R−1G	IPAK (Pb−Free)	
NTD85N02RT4	DPAK	2500 / Tape & Reel
NTD85N02RT4G	DPAK (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

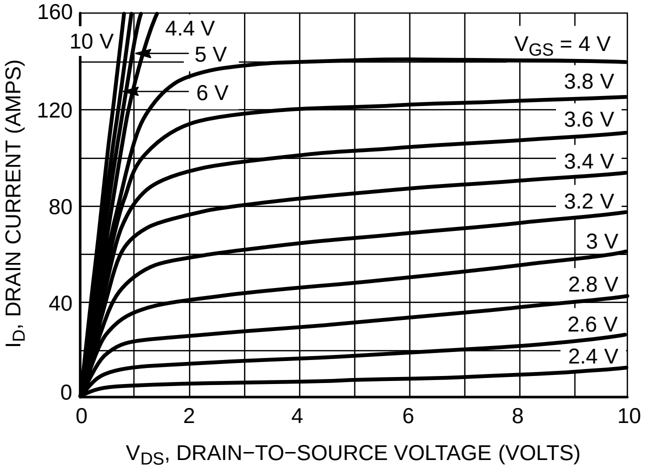


Figure 1. On−Region Characteristics

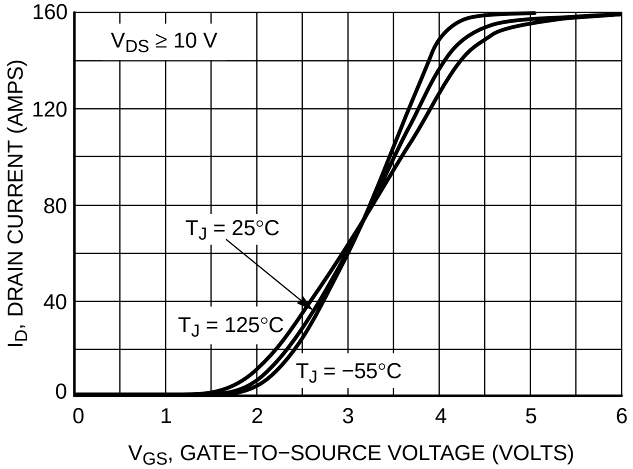


Figure 2. Transfer Characteristics

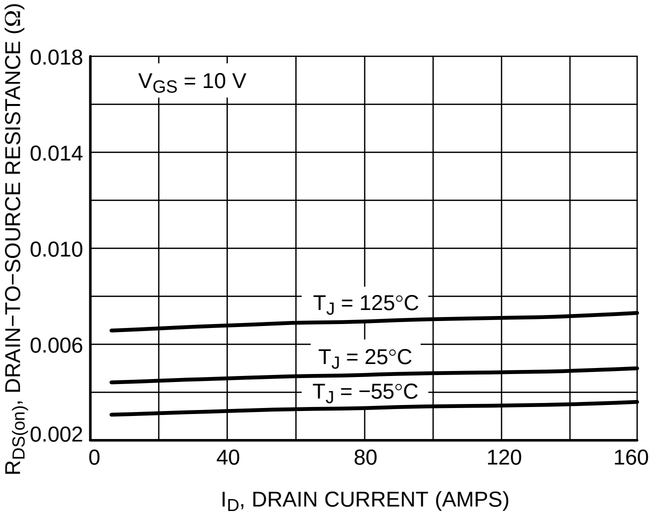


Figure 3. On−Resistance versus Drain Current and Temperature

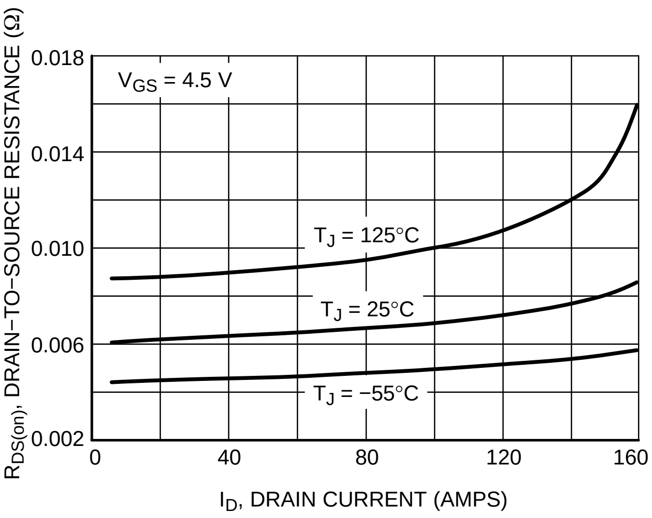


Figure 4. On−Resistance versus Drain Current and Temperature

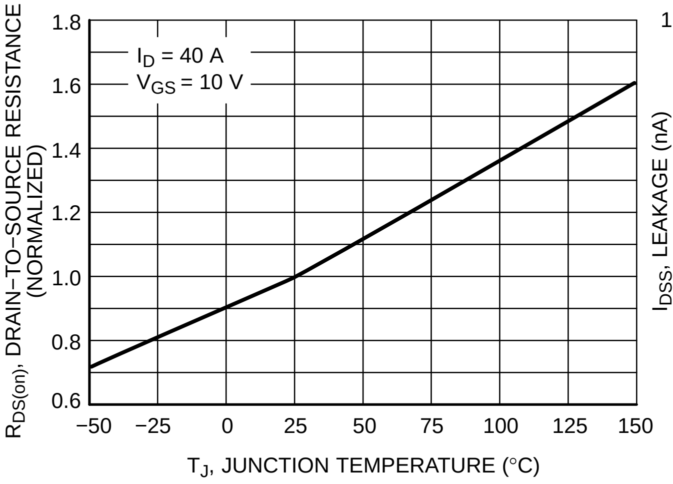


Figure 5. On−Resistance Variation with Temperature

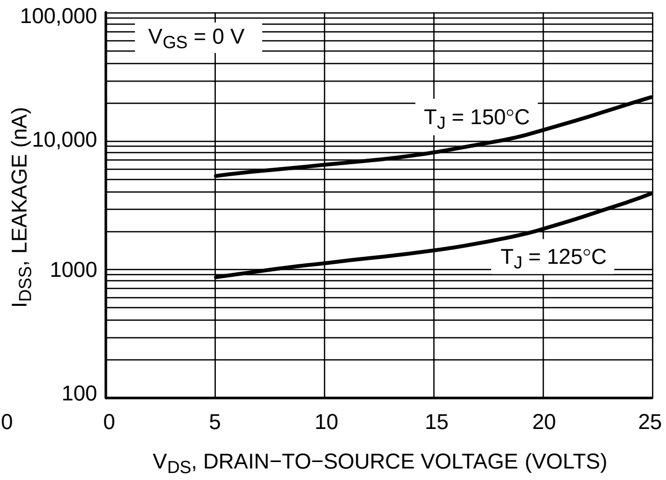


Figure 6. Drain−to−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

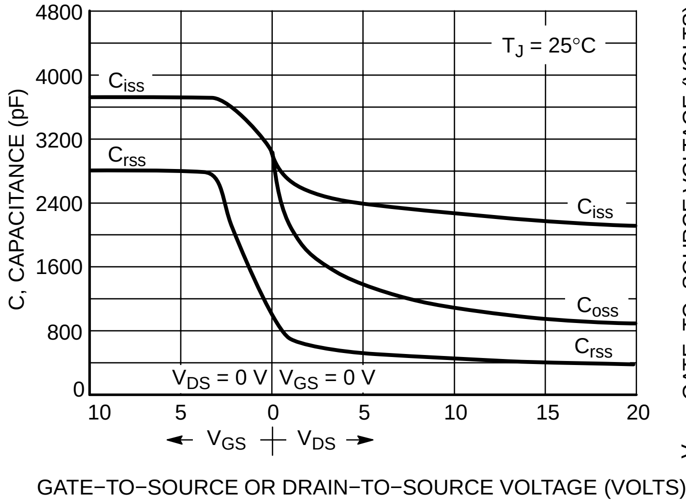


Figure 7. Capacitance Variation

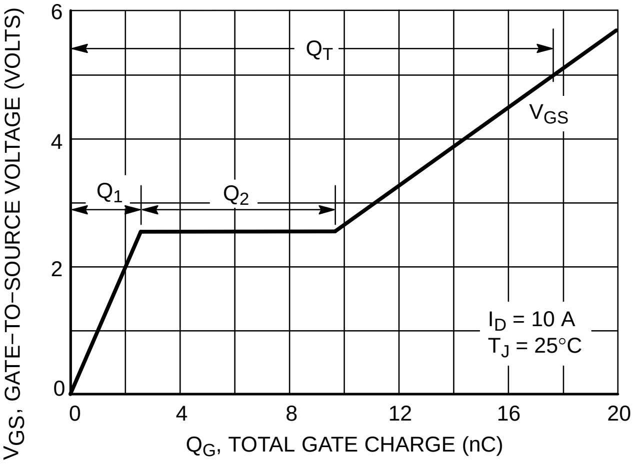


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

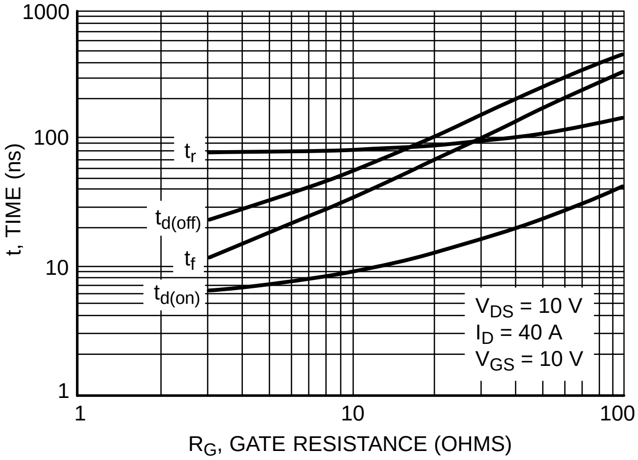


Figure 9. Resistive Switching Time Variation versus Gate Resistance

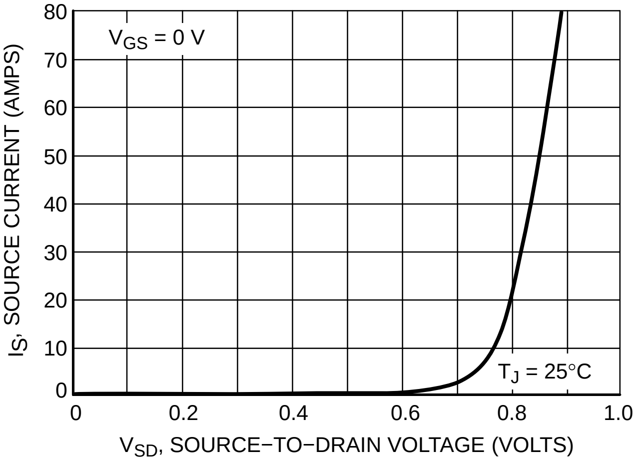


Figure 10. Diode Forward Voltage versus Current

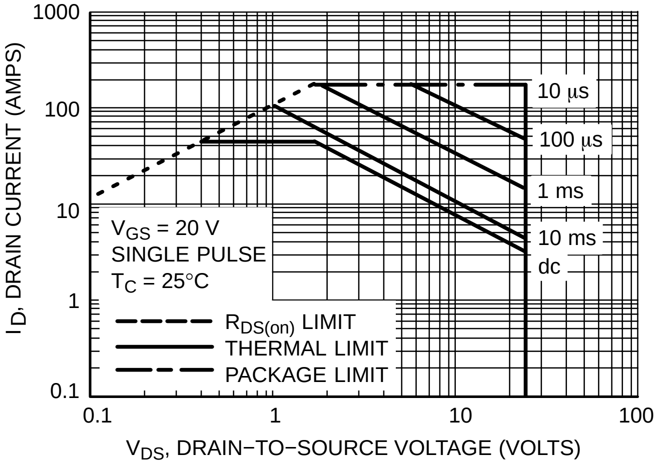


Figure 11. Maximum Rated Forward Biased Safe Operating Area

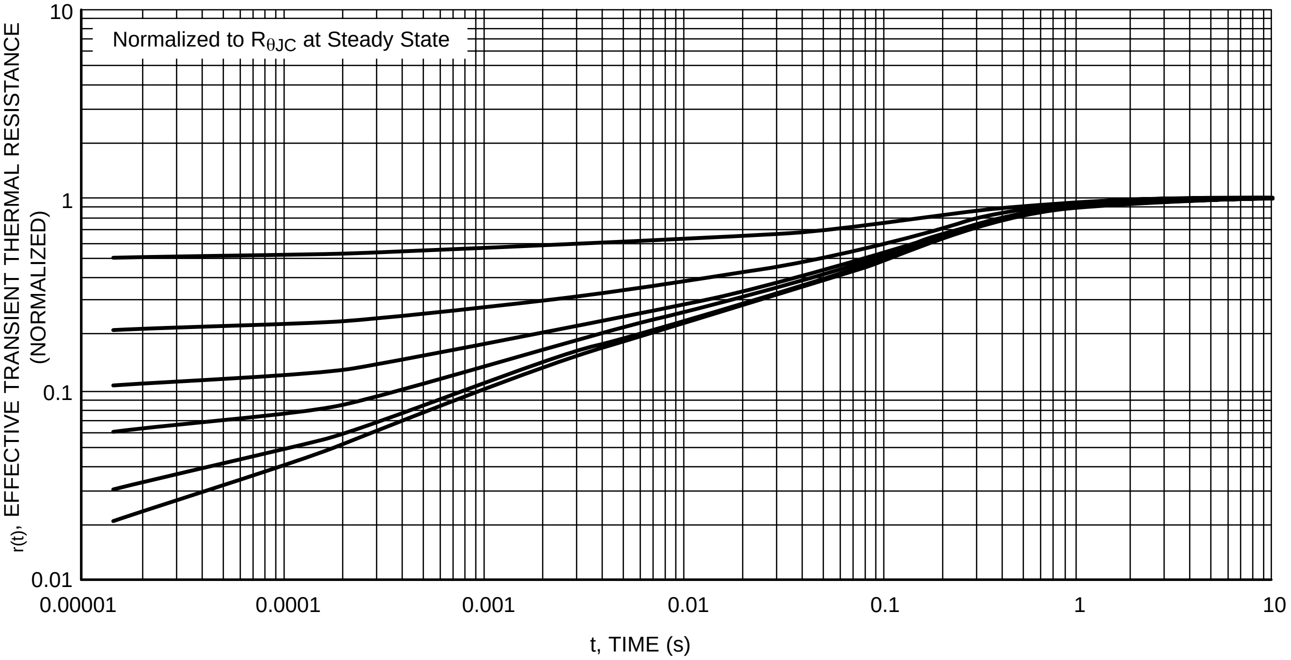


Figure 12. Thermal Response

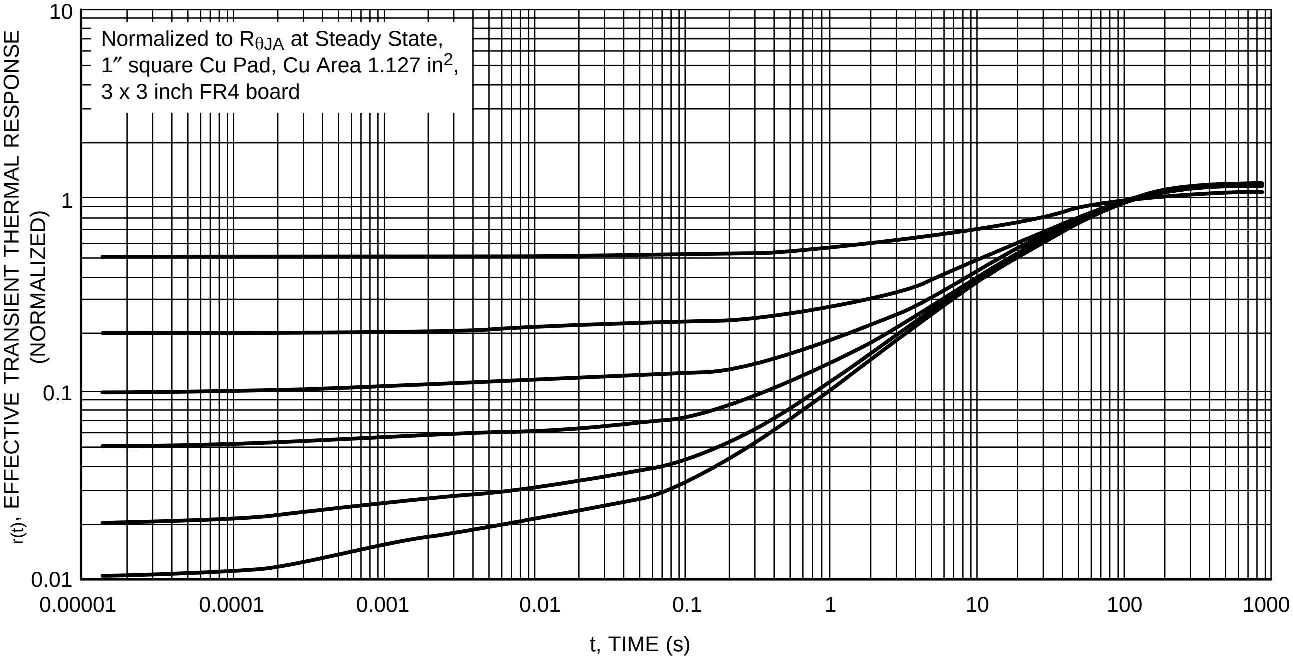
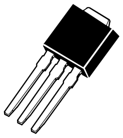


Figure 13. Thermal Response

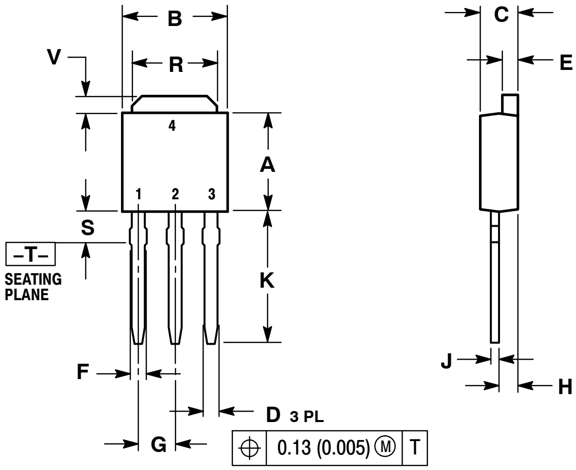
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

DPAK INSERTION MOUNT
CASE 369
ISSUE O

DATE 02 JAN 2000



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

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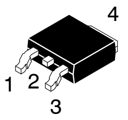
DESCRIPTION:	**DPAK INSERTION MOUNT**	**PAGE 1 OF 1**

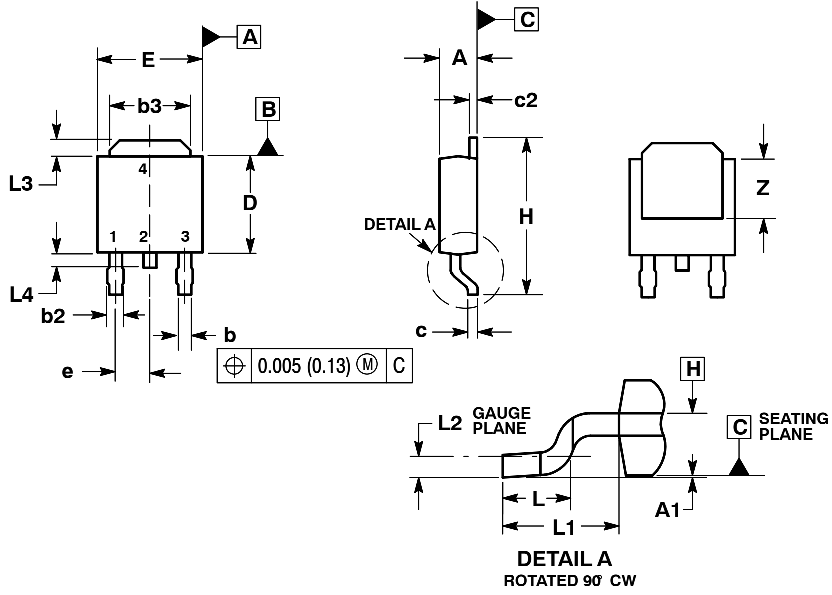
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

DPAK (SINGLE GUAGE)
CASE 369AA
ISSUE B

DATE 03 JUN 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

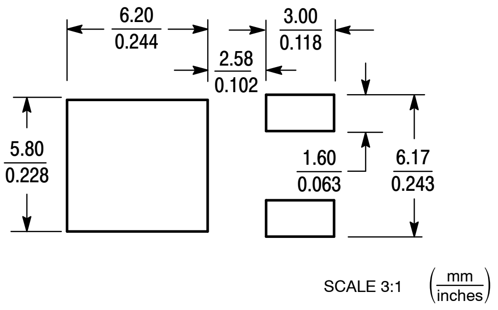
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

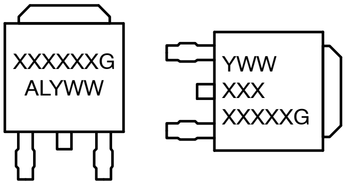
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**

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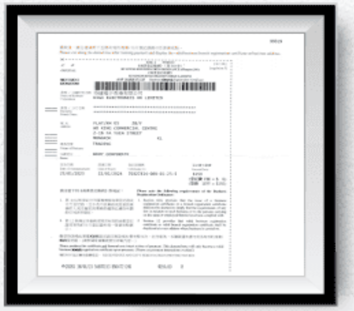

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