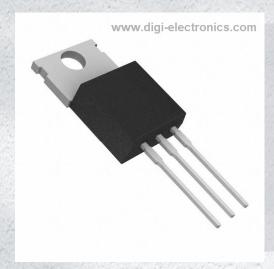


# NTP90N02 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number NTP90N02-DG

Manufacturer onsemi

Manufacturer Product Number NTP90N02

Description MOSFET N-CH 24V 90A TO220AB

Detailed Description N-Channel 24 V 90A (Ta) 85W (Tc) Through Hole TO

-220



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RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



### **Purchase and inquiry**

Manufacturer Product Number:	Manufacturer:
NTP90N02	onsemi
Series:	Product Status:
	Obsolete
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
24 V	90A (Ta)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ ld, Vgs:
4.5V, 10V	5.8mOhm @ 90A, 10V
Vgs(th) (Max) @ ld:	Gate Charge (Qg) (Max) @ Vgs:
3V @ 250μA	29 nC @ 4.5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	2120 pF @ 20 V
FET Feature:	Power Dissipation (Max):
	85W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Through Hole
Supplier Device Package:	Package / Case:
TO-220	TO-220-3
Base Product Number:	
NTP90N	

### **Environmental & Export classification**

8541.29.0095

RoHS Status:	Moisture Sensitivity Level (MSL):
RoHS non-compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

### Power MOSFET 90 Amps, 24 Volts

### N-Channel D<sup>2</sup>PAK and TO-220

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### **Features**

• Pb-Free Packages are Available

#### **Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	24	Vdc
Gate-to-Source Voltage - Continuous	V <sub>GS</sub>	±20	Vdc
Drain Current - Continuous @ $T_A = 25^{\circ}C$ - Single Pulse ( $t_p = 10 \mu s$ )	I <sub>D</sub> I <sub>DM</sub>	90* 200	A A
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	85 0.66	W/°C
Operating and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ ( $V_{DD} = 28$ Vdc, $V_{GS} = 10$ Vdc, $L = 5.0$ mH, $I_{L(pk)} = 17$ A, RG = $25 \Omega$ )	E <sub>AS</sub>	733	mJ
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1)	R <sub>θJC</sub> R <sub>θJA</sub>	1.55 70	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).
- When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).
- \*Chip current capability limited by package.

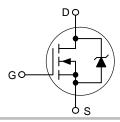


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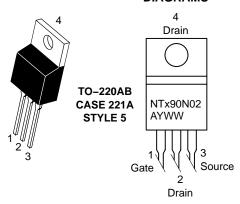
#### http://onsemi.com

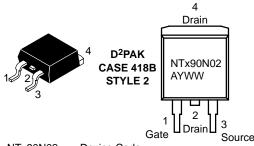
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
24 V	5.0 mΩ @ 10 V	90 A
211	7.5 mΩ @ 4.5 V	0071

#### **N-Channel**



#### MARKING DIAGRAMS





NTx90N02 = Device Code

x = P or B

A = Assembly Location

Y = Year

WW = Work Week

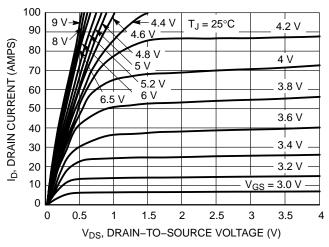
#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

CI	Symbol	Min	Тур	Max	Unit	
Characteristic Symbol Min Typ I  OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 µAdc) Temperature Coefficient (Positive)		V <sub>(BR)DSS</sub>	24 -	27 25	- -	Vdc mV/°C
Zero Gate Voltage Drain Currer $(V_{DS}=24~\text{Vdc},~V_{GS}=0~\text{Vdc})\\ (V_{DS}=24~\text{Vdc},~V_{GS}=0~\text{Vdc},$		I <sub>DSS</sub>	_ _	- -	1.0 10	μAdc
Gate-Body Leakage Current (V	$V_{GS} = \pm 20 \text{Vdc},  V_{DS} = 0 \text{Vdc})$	I <sub>GSS</sub>	_	-	±100	nAdc
ON CHARACTERISTICS (Note	3)					
Gate Threshold Voltage (Note 3 $(V_{DS} = V_{GS}, I_D = 250 \mu Adc)$ Threshold Temperature Coeffici	•	V <sub>GS(th)</sub>	1.0	1.9 -3.8	3.0	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) $ (V_{GS} = 10 \text{ Vdc}, I_D = 90 \text{ Adc}) $ $ (V_{GS} = 4.5 \text{ Vdc}, I_D = 40 \text{ Adc}) $ $ (V_{GS} = 10 \text{ Vdc}, I_D = 20 \text{ Adc}) $ $ (V_{GS} = 4.5 \text{ Vdc}, I_D = 20 \text{ Adc}) $ $ (V_{GS} = 4.5 \text{ Vdc}, I_D = 20 \text{ Adc}) $		R <sub>DS(on)</sub>	- - - -	5.0 7.5 5.0 7.5	5.8 9.0 5.8 9.0	mΩ
Forward Transconductance (No	9FS	-	25	-	mhos	
DYNAMIC CHARACTERISTICS	3	•		•		
Input Capacitance	$(V_{DS} = 20 \text{ Vdc}, V_{GS} = 0 \text{ Vdc},$	C <sub>iss</sub>	_	2120	-	pF
Output Capacitance	f = 1.0 MHz)	C <sub>oss</sub>	_	900	-	
Transfer Capacitance		C <sub>rss</sub>	_	360	-	
SWITCHING CHARACTERISTIC	CS (Note 4)					
Turn-On Delay Time	$(V_{DD} = 20 \text{ Vdc}, I_D = 20 \text{ Adc},$	t <sub>d(on)</sub>	_	16	_	ns
Rise Time	$V_{GS} = 4.5 \text{ Vdc}, R_G = 2.5 \Omega)$	t <sub>r</sub>	-	90	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	28	-	
Fall Time		t <sub>f</sub>	-	60	-	
Gate Charge	$(V_{DS} = 20 \text{ Vdc}, I_{D} = 20 \text{ Adc},$	Q <sub>T</sub>	_	29	_	nC
	V <sub>GS</sub> = 4.5 Vdc) (Note 3)	Q <sub>1</sub>	-	8.0	-	
			_	20	-	
SOURCE-DRAIN DIODE CHAR	RACTERISTICS					
Forward On-Voltage	$ \begin{array}{c} (I_S = 2.3 \; \text{Adc},  V_{GS} = 0 \; \text{Vdc}) \\ (I_S = 40 \; \text{Adc},  V_{GS} = 0 \; \text{Vdc}) \; (\text{Note 3}) \\ (I_S = 2.3 \; \text{Adc},  V_{GS} = 0 \; \text{Vdc},  T_J = 150^{\circ}\text{C}) \end{array} $	V <sub>SD</sub>	- - -	0.75 1.2 0.65	1.0 - -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 2.3 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	_	40	_	ns
		ta	_	21	_	
		t <sub>b</sub>	_	18	_	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	_	0.036	_	μC

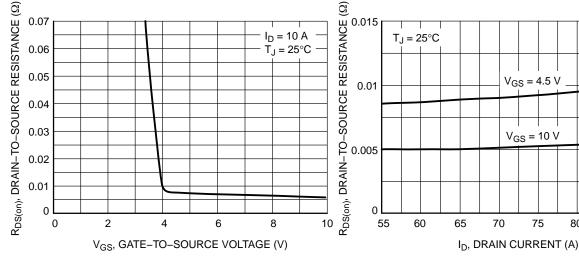
<sup>3.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2%. 4. Switching characteristics are independent of operating junction temperatures.



160 150  $V_{DS} \ge 24 \text{ V}$ 140 130 120 **DRAIN CURRENT (AMPS)** 110 100 90 80 70  $T_J = 25^{\circ}C$ 60 50 40  $T_J = 125^{\circ}C$ 30 20 -55°C ے 0 3 2 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



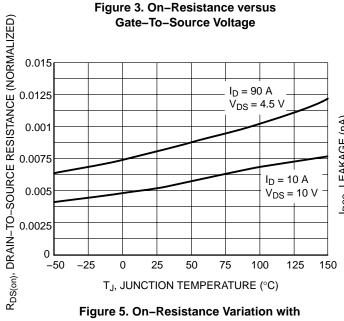
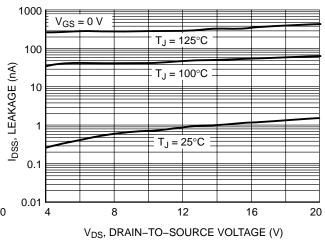


Figure 4. On-Resistance versus Drain Current and Gate Voltage

80

90

85



**Temperature** 

Figure 6. Drain-To-Source Leakage **Current versus Voltage** 

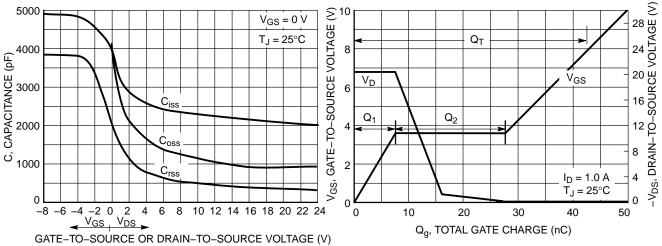


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

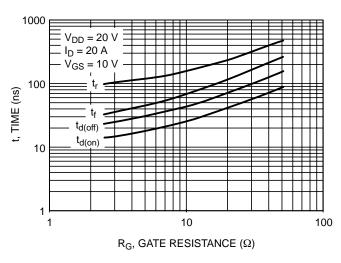


Figure 9. Resistive Switching Time Variation versus Gate Resistance

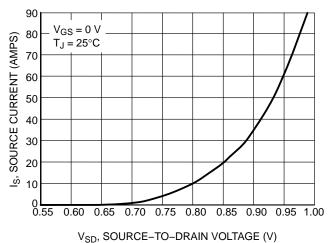


Figure 10. Diode Forward Voltage versus Current

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTP90N02	TO-220AB	50 Units / Rail
NTP90N02G	TO-220AB (Pb-Free)	50 Units / Rail
NTB90N02	D <sup>2</sup> PAK	50 Units / Rail
NTB90N02G	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NTB90N02T4	D <sup>2</sup> PAK	800 Tape & Reel
NTB90N02T4G	D <sup>2</sup> PAK (Pb-Free)	800 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### **POWER MOSFET SWITCHING**

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{SGP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_{\Gamma} = Q_2 \times R_2/10(V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_2/V_{GSP}$$

where:

 $V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$ 

 $R_G$  = the gate drive resistance and  $Q_2$  and  $V_{GSP}$  are read from the gate charge curve.

During the turn—on and turn—off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network.

The equations are:

$$t_{d(on)} = R_G C_{iss} ln [V_{GG}/(V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G C_{iss} In (V_{GG}/V_{GSP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on–state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.



### **MECHANICAL CASE OUTLINE**

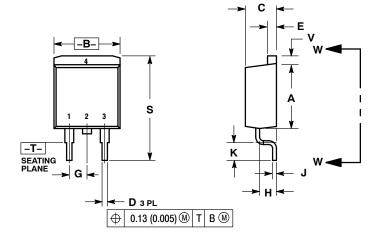
PACKAGE DIMENSIONS



D<sup>2</sup>PAK 3 CASE 418B-04 **ISSUE L** 

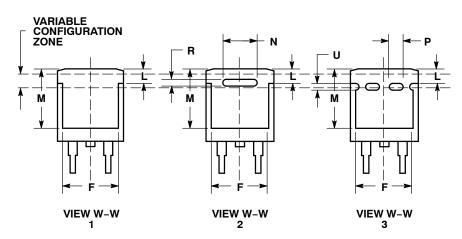
**DATE 17 FEB 2015** 

#### SCALE 1:1



- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
   CONTROLLING DIMENSION: INCH.
- 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

	INCHES		MILLIMETER	
DIM	MIN	MAX	MIN	MAX
Α	0.340	0.380	8.64	9.65
В	0.380	0.405	9.65	10.29
С	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
Е	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
Н	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
Р	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
٧	0.045	0.055	1.14	1.40



STYLE 1: PIN 1. BASE 2. COLLECTOR
3. EMITTER
4. COLLECTOR STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN STYLE 3:

PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE

STYLE 4: PIN 1. GATE 2. COLLECTOR

3. EMITTER 4. COLLECTOR

STYLE 5: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

STYLE 6: PIN 1. NO CONNECT 2. CATHODE 3. ANODE 4. CATHODE

#### **MARKING INFORMATION AND FOOTPRINT ON PAGE 2**

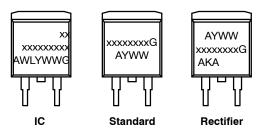
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#### D<sup>2</sup>PAK 3 CASE 418B-04 ISSUE L

**DATE 17 FEB 2015** 

## GENERIC MARKING DIAGRAM\*

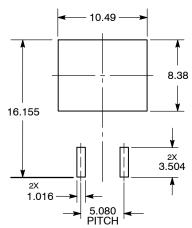


xx = Specific Device Code A = Assembly Location

WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package
AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

#### **SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

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<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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