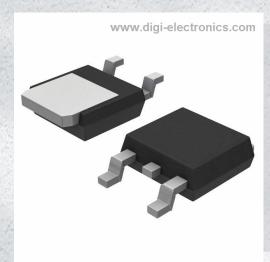


NVD5C434NT4G Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number NVD5C434NT4G-DG

Manufacturer onsemi

Manufacturer Product Number NVD5C434NT4G

Description MOSFET N-CHANNEL 40V 163A DPAK

Detailed Description N-Channel 40 V 163A (Tc) 117W (Tc) Surface Mount

DPAK



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NVD5C434NT4G	onsemi
Series:	Product Status:
	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
40 V	163A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	2.1mOhm @ 50A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 250μA	80.6 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	5400 pF @ 25 V
FET Feature:	Power Dissipation (Max):
	117W (Tc)
Operating Temperature:	Grade:
-55°C ~ 175°C (TJ)	Automotive
Qualification:	Mounting Type:
AEC-Q101	Surface Mount
Supplier Device Package:	Package / Case:
DPAK	TO-252-3, DPAK (2 Leads + Tab), SC-63
Base Product Number:	
NVD5C434	

Environmental & Export classification

8541.29.0095

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

MOSFET - Power, Single, **N-Channel** 40 V, 2.1 mΩ, 163 A

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Cur-		T _C = 25°C	I _D	163	Α
rent R _{θJC} (Notes 1 & 3)	Steady	T _C = 100°C		115	
Power Dissipation R _{θJC}	State	T _C = 25°C	P_{D}	117	W
(Note 1)		T _C = 100°C		58	
Continuous Drain		T _A = 25°C	I _D	26	Α
Current R _{θJA} (Notes 1, 2 & 3)	Steady State	T _A = 100°C		22	
Power Dissipation R _{θJA}		T _A = 25°C	P_{D}	3.2	W
(Notes 1 & 2)		T _A = 100°C		2.2	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I _{DM}	900	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	°C
Source Current (Body Diode)			I _S	130	Α
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25$ °C, $I_{L(pk)} = 25$ A)			E _{AS}	420	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	1.28	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	48	

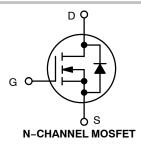
- 1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
 Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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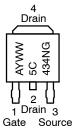
V _{(BR)DSS}	R _{DS(on)}	I _D	
40 V	2.1 mΩ @ 10 V	163 A	





DPAK CASE 369C STYLE 2

MARKING DIAGRAM **& PIN ASSIGNMENT**



= Assembly Location

= Year WW = Work Week 5C434N= Device Code = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS					•	•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				18		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	$T_J = 25^{\circ}C$			10	μΑ
		$V_{DS} = 40 \text{ V}$	T _J = 125°C			250	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	_S = 20 V			100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D =$	= 250 μΑ	2.0		4.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				7.9		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D	= 50 A		1.7	2.1	mΩ
Forward Transconductance	9FS	$V_{DS} = 3 \text{ V}, I_{D}$	= 50 A		155		S
CHARGES, CAPACITANCES AND GATE RE	SISTANCES						
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 25 \text{ V}$			5400		pF
Output Capacitance	C _{oss}				3000		
Reverse Transfer Capacitance	C _{rss}				71		
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 10 \text{ V}, V_{DS} = 32 \text{ V},$ $I_{D} = 50 \text{ A}$			80.6		nC
Threshold Gate Charge	Q _{G(TH)}				15.2		
Gate-to-Source Charge	Q _{GS}				25.2		
Gate-to-Drain Charge	Q_{GD}				15.4		
Plateau Voltage	V_{GP}				4.8		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	t _{d(on)}				15		ns
Rise Time	t _r	Vcc = 10 V. Vp.	c = 32 V		78		
Turn-Off Delay Time	t _{d(off)}	V_{GS} = 10 V, V_{DS} = 32 V, I_{D} = 50 A, R_{G} = 2.5 Ω			43		
Fall Time	t _f				14		
DRAIN-SOURCE DIODE CHARACTERISTIC	s						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.8	1.2	V
		I _S = 50 A	T _J = 125°C		0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dls/dt = 100 A/μs,			73		ns
Charge Time	ta				36		
Discharge Time	tb	$I_S = 50$			37		
Reverse Recovery Charge	Q _{RR}				120		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

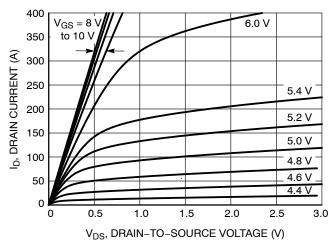


Figure 1. On-Region Characteristics

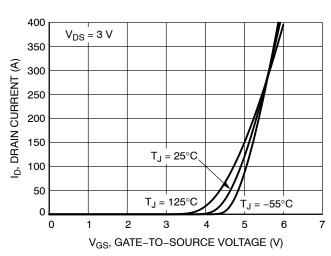


Figure 2. Transfer Characteristics

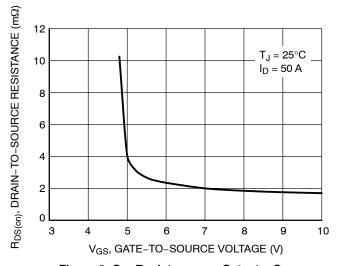


Figure 3. On-Resistance vs. Gate-to-Source Voltage

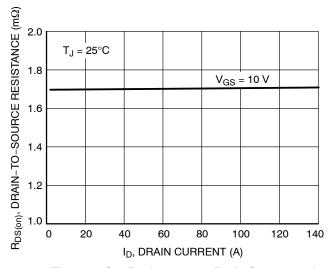


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

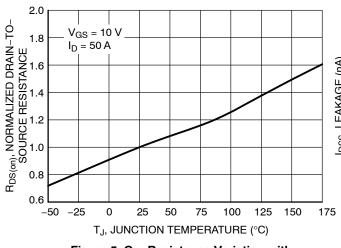


Figure 5. On–Resistance Variation with Temperature

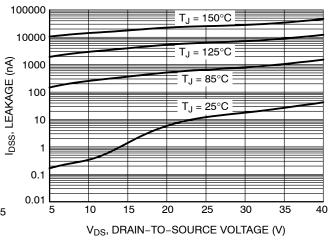


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

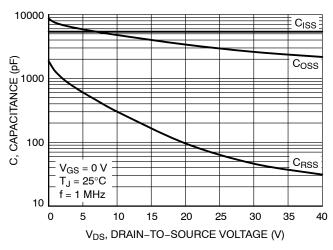


Figure 7. Capacitance Variation

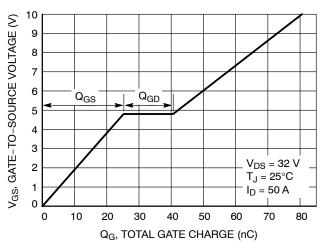


Figure 8. Gate-to-Source vs. Total Charge

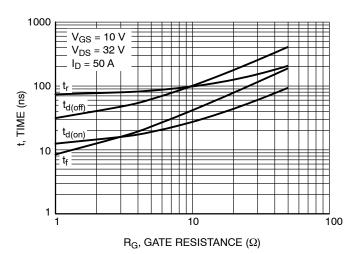


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

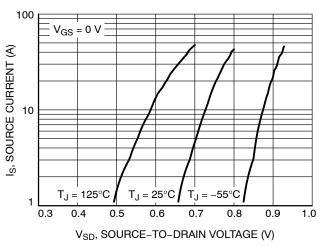


Figure 10. Diode Forward Voltage vs. Current

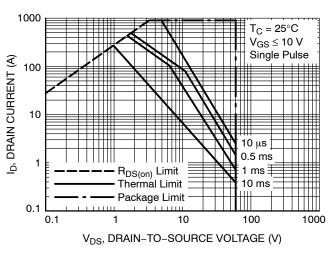


Figure 11. Maximum Rated Forward Biased Safe Operating Area

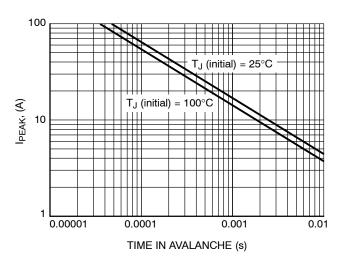


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

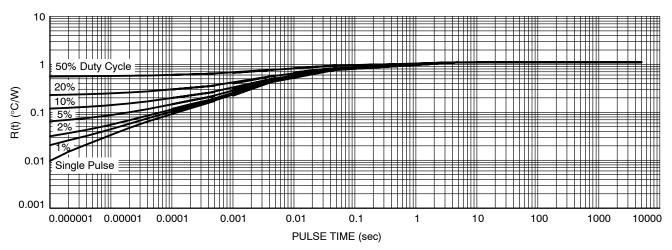


Figure 13. Thermal Characteristics

ORDERING INFORMATION

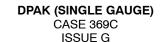
Order Number	Package	Shipping [†]
NVD5C434NT4G	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

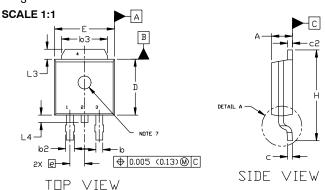


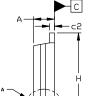
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



DATE 31 MAY 2023





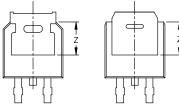
NUTES:

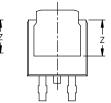
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS 63,
- L3. AND Z. L3, AND Z.

 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
 PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR
 GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
 DIMENSIONS D AND E ARE DETERMINED AT THE
 OUTERMOST EXTREMES OF THE PLASTIC BODY.
 DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
 DETININAL MOLD ESCALUPE.

- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIM	MILLIMETERS		
ויונע	MIN.	MAX.	MIN.	MAX.		
Α	0.086	0.094	2.18	2.38		
A1	0.000	0.005	0.00	0.13		
b	0.025	0.035	0.63	0.89		
b2	0.028	0.045	0.72	1.14		
b3	0.180	0.215	4.57	5.46		
С	0.018	0.024	0.46	0.61		
c2	0.018	0.024	0.46	0.61		
D	0.235	0.245	5.97	6.22		
Ε	0.250	0.265	6.35	6.73		
е	0.090 BSC		2.29 BSC			
Н	0.370	0.410	9.40	10.41		
L	0.055	0.070	1.40	1.78		
L1	0.114	0.114 REF		REF		
L2	0.020 BSC		0.51	BSC		
L3	0.035	0.050	0.89	1.27		
L4		0.040		1.01		
Z	0.155		3.93			





BOTTOM VIEW

2.58

[0.102]

1.60

[0.063]

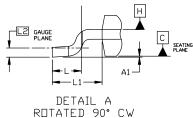
5.80

6.17 [0.243] RECOMMENDED MOUNTING FOOTPRINT*

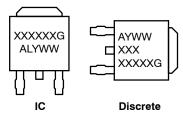
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DUWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

BOTTOM VIEW AL TERNATE

CONSTRUCTIONS [0.228] 6.20 -L2 GAUGE PLANE [0.244] 3.00 [0.118] ROTATED 90°



GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
Α	= Assembly Location
L	= Wafer Lot
Υ	= Year
WW	= Work Week
G	= Pb-Free Package

STYLE 1: PIN 1. BASE STYLE 2: PIN 1. GATE STYLE 3: PIN 1. ANODE STYLE 4: PIN 1. CATHODE STYLE 5: PIN 1. GATE 2. COLLECTOR 2. DRAIN 2. CATHODE 2. ANODE 3 SOURCE 3 FMITTER 3 ANODE 3 GATE

2. ANODE 3 CATHODE COLLECTOR 4. DRAIN CATHODE 4. ANODE ANODE

STYLE 6: STYLE 7: PIN 1. GATE 2. COLLECTOR STYLE 8: STYLE 9: STYLE 10: PIN 1. MT1 2. MT2 PIN 1. N/C 2. CATHODE 3. ANODE PIN 1. ANODE 2. CATHODE PIN 1. CATHODE 2. ANODE 3 CATHODE 3 FMITTER 3 RESISTOR ADJUST 3 GATE 4. COLLECTOR 4. CATHODE 4. ANODE CATHODE

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1	

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