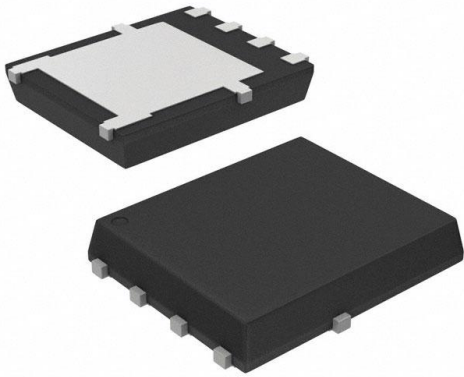


NVMFS3D0P04M8LT1G Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	NVMFS3D0P04M8LT1G-DG
Manufacturer	onsemi
Manufacturer Product Number	NVMFS3D0P04M8LT1G
Description	MV8 P INITIAL PROGRAM
Detailed Description	P-Channel 40 V 28A (Ta), 183A (Tc) 3.9W (Ta), 171W (Tc) Surface Mount 5-DFN (5x6) (8-SOFL)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

NVMFS3D0P04M8LT1G

Series:

-

FET Type:

P-Channel

Drain to Source Voltage (Vdss):

40 V

Drive Voltage (Max Rds On, Min Rds On):

4.5V, 10V

Vgs(th) (Max) @ Id:

2.4V @ 2mA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 175°C (Tj)

Qualification:

AEC-Q101

Supplier Device Package:

5-DFN (5x6) (8-SOFL)

Manufacturer:

onsemi

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

28A (Ta), 183A (Tc)

Rds On (Max) @ Id, Vgs:

2.7mOhm @ 30A,10V

Gate Charge (Qg) (Max) @ Vgs:

124 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

5827 pF @ 20 V

Power Dissipation (Max):

3.9W (Ta), 171W (Tc)

Grade:

Automotive

Mounting Type:

Surface Mount

Package / Case:

8-PowerTDFN, 5 Leads

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

MOSFET - Power, Single P-Channel

-40 V, 2.7 mΩ, -183 A

NVMFS3D0P04M8L

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- NVMFWS3D0P04M8L – Wettable Flanks Product
- NVM Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	-40	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D -183 A
		$T_C = 100^\circ\text{C}$	-129
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	Steady State	$T_C = 25^\circ\text{C}$	P_D 171 W
		$T_C = 100^\circ\text{C}$	86
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D -28 A
		$T_A = 100^\circ\text{C}$	-19
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D 3.9 W
		$T_A = 100^\circ\text{C}$	1.9
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM} -900	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	-143	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = -30 \text{ A}$)	E_{AS}	752	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

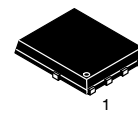
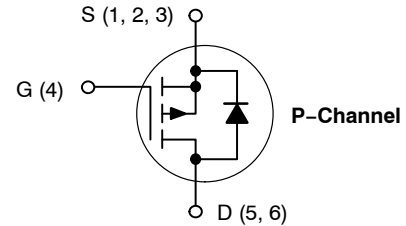
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

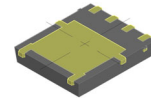
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain) (Note 2)	$R_{\theta JC}$	0.9	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	39	$^\circ\text{C}/\text{W}$

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-40 V	2.7 mΩ @ -10 V	-183 A
	4.2 mΩ @ -4.5 V	

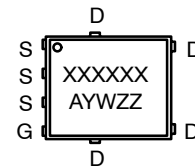


DFN5
(SO-8FL)
CASE 488AA
STYLE 1



DFNW5
(FULL-CUT
SO8FL WF)
CASE 507BA

MARKING DIAGRAM



XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFS3D0P04M8L

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			12		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -40\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 125^\circ\text{C}$		-100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -2\text{ mA}$	-1.0		-2.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-4.7		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -30\text{ A}$		2.1	2.7	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -15\text{ A}$		3.1	4.2	
Forward Transconductance	g_{FS}	$V_{DS} = -24\text{ V}, I_D = -50\text{ A}$		205		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -20\text{ V}$		5827		pF
Output Capacitance	C_{oss}			3225		
Reverse Transfer Capacitance	C_{rss}			85.8		
Total Gate Charge	$Q_G(\text{TOT})$	$V_{DS} = -20\text{ V}, I_D = -50\text{ A}$	$V_{GS} = -4.5\text{ V}$	58.7		nC
			$V_{GS} = -10\text{ V}$	124		
Threshold Gate Charge	$Q_G(\text{TH})$	$V_{GS} = -10\text{ V}, V_{DS} = -20\text{ V}, I_D = -50\text{ A}$		10.9		nC
Gate-to-Source Charge	Q_{GS}			21.6		
Gate-to-Drain Charge	Q_{GD}			17.3		
Plateau Voltage	V_{GP}			2.8		

SWITCHING CHARACTERISTICS (Notes 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -20\text{ V}, I_D = -50\text{ A}, R_G = 2.5\ \Omega$		15.8		ns
Rise Time	t_r			161		
Turn-Off Delay Time	$t_{d(off)}$			349		
Fall Time	t_f			256		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -15\text{ A}$	$T_J = 25^\circ\text{C}$	-0.75	-1.20	V
			$T_J = 125^\circ\text{C}$	-0.61		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = -50\text{ A}$		113		ns
Charge Time	t_a			59.4		
Discharge Time	t_b			53.1		
Reverse Recovery Charge	Q_{RR}			246		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

NVMFS3D0P04M8L

TYPICAL CHARACTERISTICS

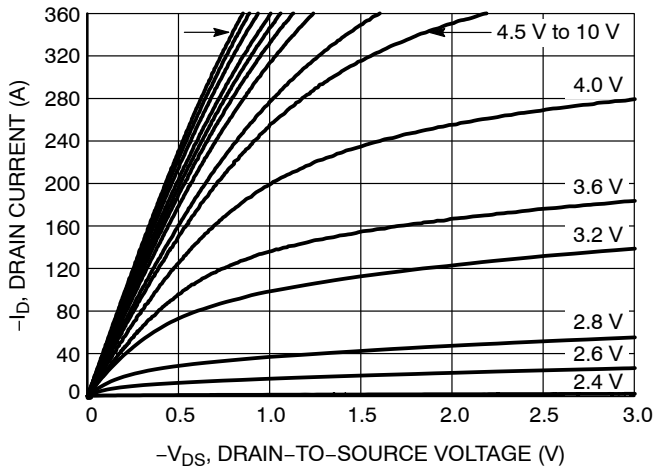


Figure 1. On-Region Characteristics

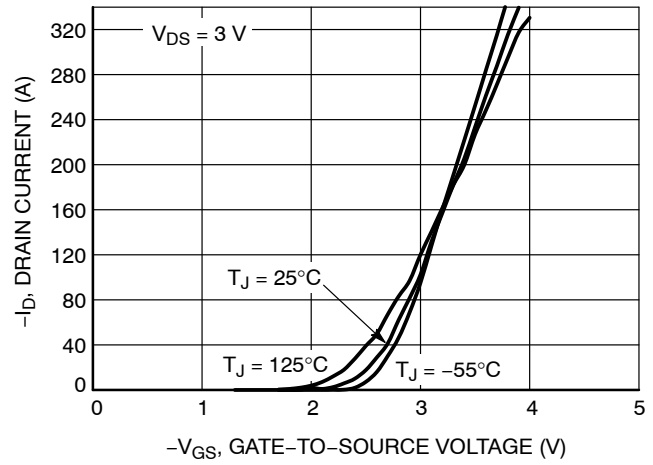


Figure 2. Transfer Characteristics

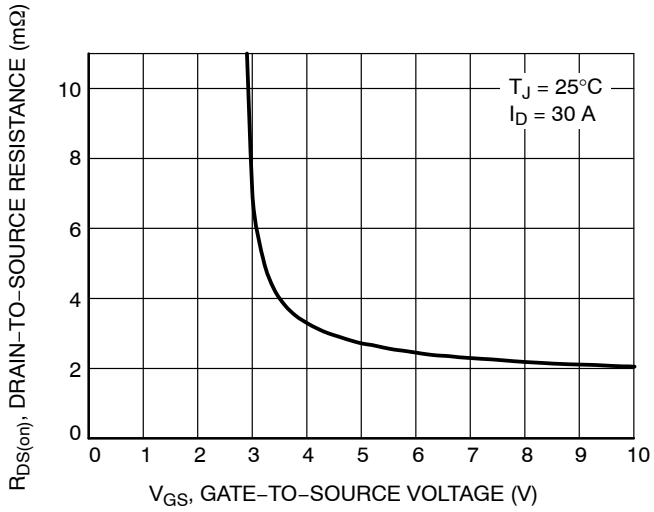


Figure 3. On-Resistance vs. Gate-to-Source Voltage

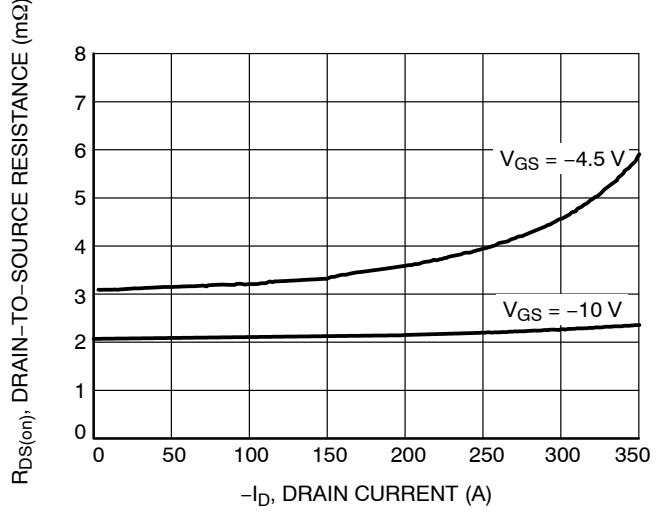


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

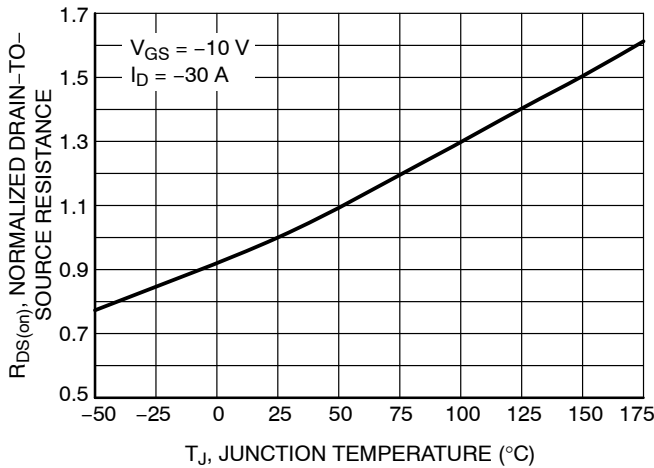


Figure 5. On-Resistance Variation with Temperature

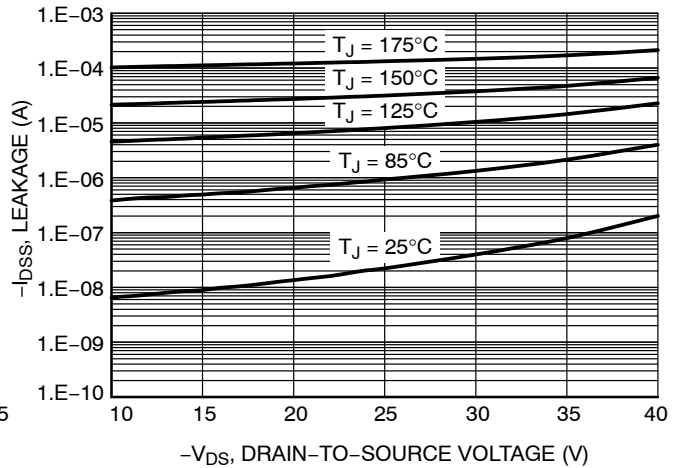


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVMFS3D0P04M8L

TYPICAL CHARACTERISTICS

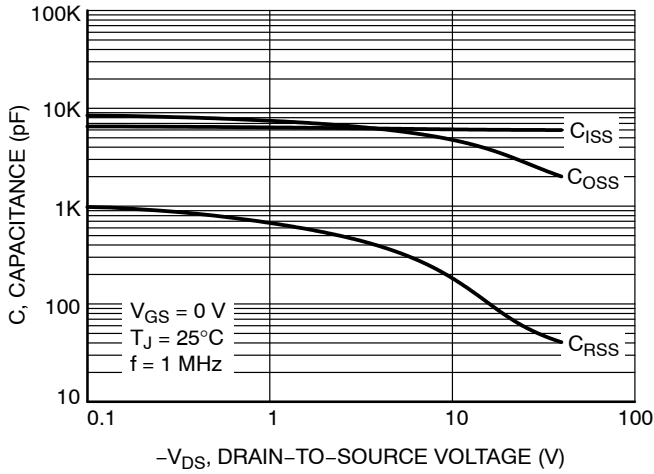


Figure 7. Capacitance Variation

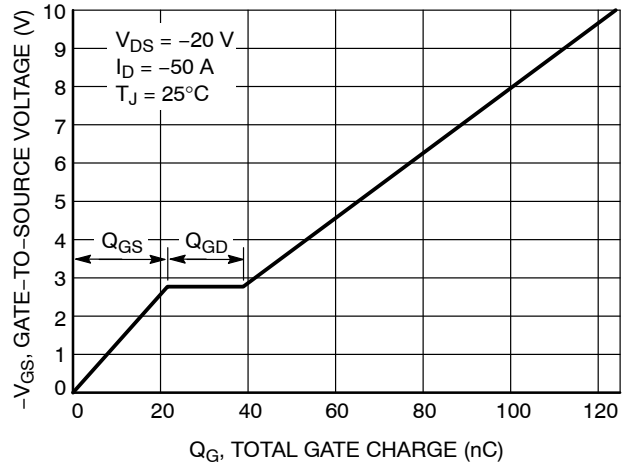


Figure 8. Gate-to-Source vs. Total Charge

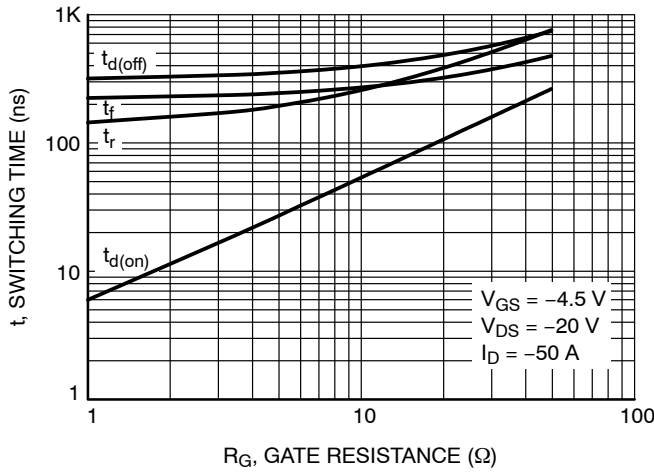


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

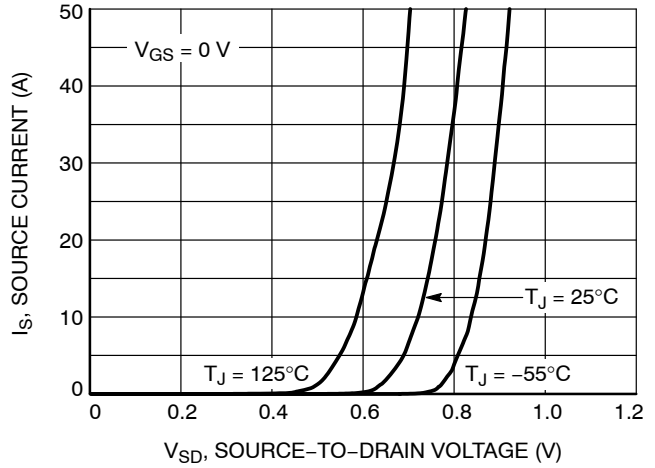


Figure 10. Diode Forward Voltage vs. Current

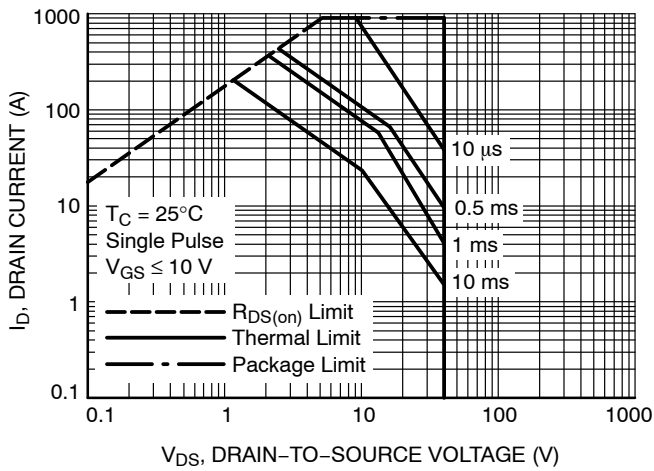


Figure 11. Maximum Rated Forward Biased Safe Operating Area

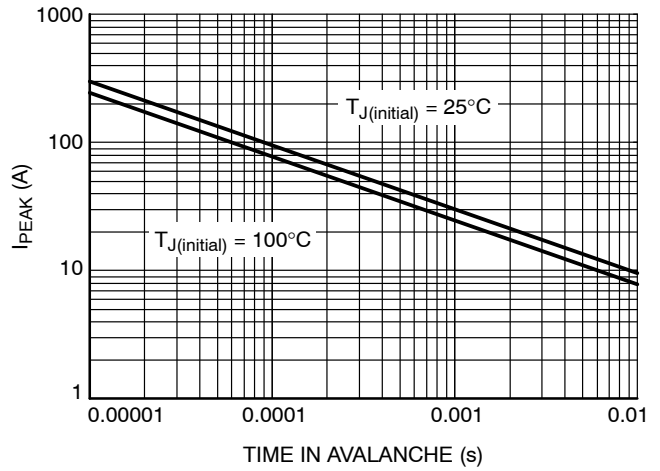


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVMFS3D0P04M8L

TYPICAL CHARACTERISTICS

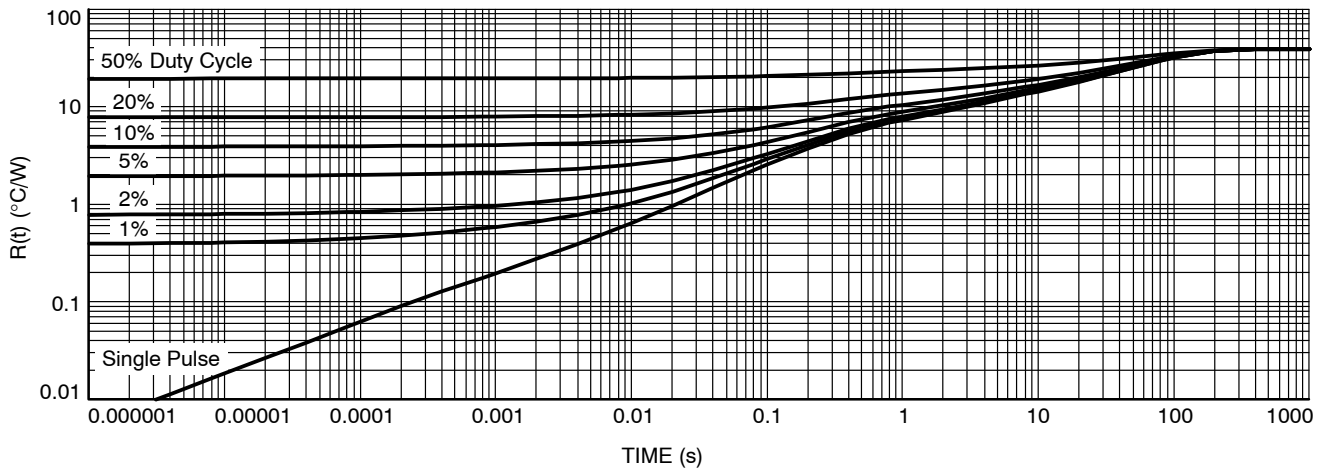


Figure 13. Thermal Response

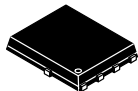
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS3D0P04M8LT1G	3D0P04	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFWS3D0P04M8LT1G	3D0P4W	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



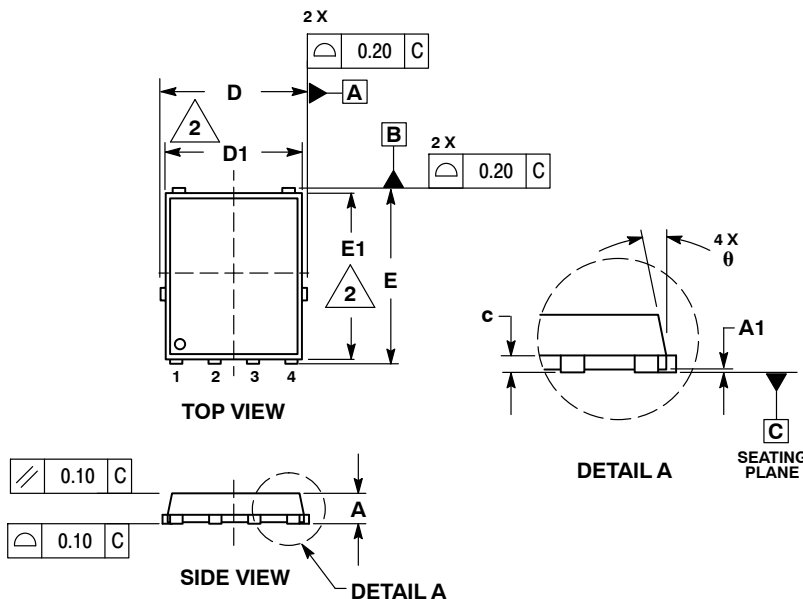
**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



1
SCALE 2:1

**DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N**

DATE 25 JUN 2018



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

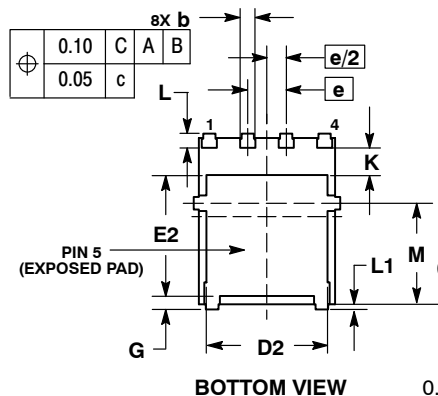
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

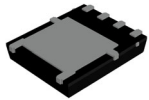
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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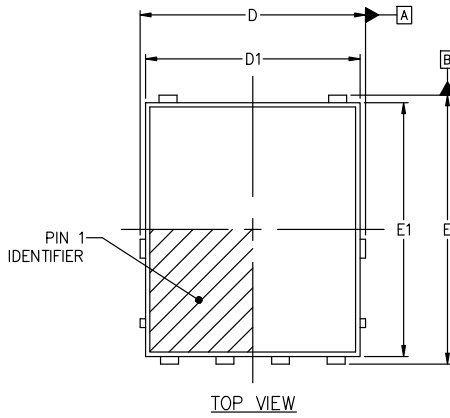


**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**

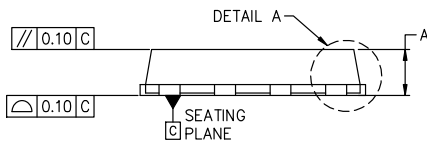


**DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C**

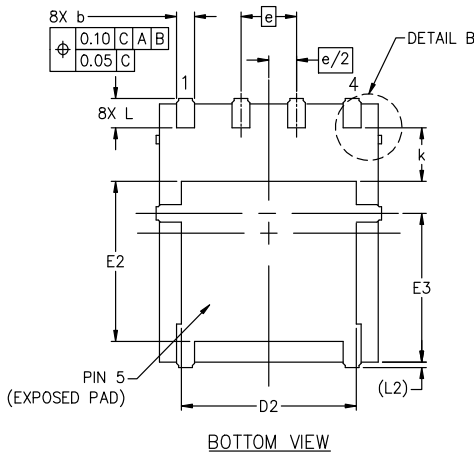
DATE 19 SEP 2024



TOP VIEW



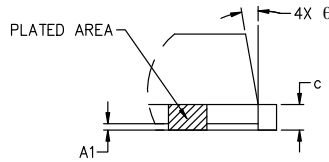
SIDE VIEW



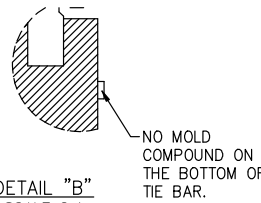
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

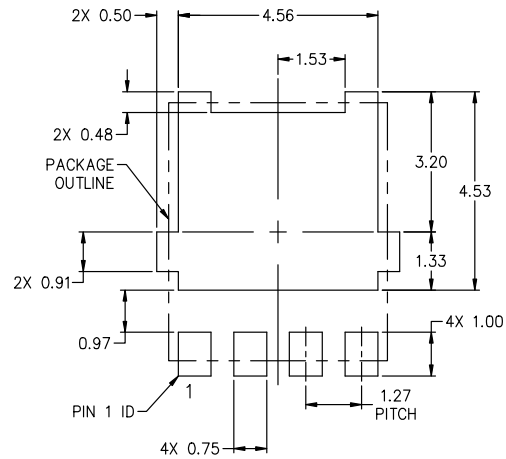


DETAIL "A"
SCALE 2:1



DETAIL "B"
SCALE 2:1

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
theta	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

OUR CERTIFICATE

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