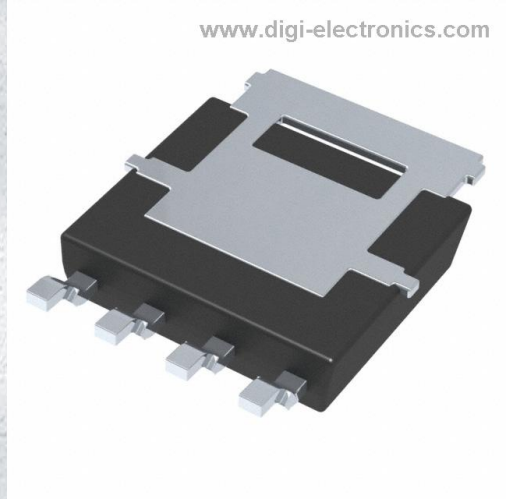
NVMYS2D2N06CLTWG Datasheet



DiGi Electronics Part Number	NVMYS2D2N06CLTWG-DG
Manufacturer	onsemi
Manufacturer Product Number	NVMYS2D2N06CLTWG
Description	MOSFET N-CH 60V 31A/185A LFPAK4
Detailed Description	N-Channel 60 V 31A (Ta), 185A (Tc) 3.9W (Ta), 134W (Tc) Surface Mount LFPAK4 (5x6)

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NVMYS2D2N06CLTWG	onsemi
Series:	Product Status:
-	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
60 V	31A (Ta), 185A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	1.9mOhm @ 50A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2V @ 180µA	69 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	4850 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	3.9W (Ta), 134W (Tc)
Operating Temperature:	Grade:
-55°C ~ 175°C (TJ)	Automotive
Qualification:	Mounting Type:
AEC-Q101	Surface Mount
Supplier Device Package:	Package / Case:
LFPAK4 (5x6)	SOT-1023, 4-LFPAK
Base Product Number:	
NVMYS2	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

NVMYS2D2N06CL

MOSFET – Power, Single N-Channel
60 V, 2.0 mΩ, 185 A

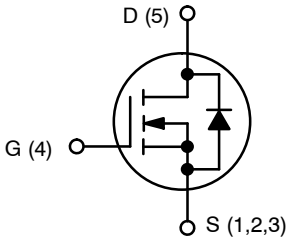
ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	2.0 mΩ @ 10 V	185 A
	2.7 mΩ @ 4.5 V	

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	T_C = 25°C	I_D	185	A
		T_C = 100°C		131	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25°C	P_D	134	W
		T_C = 100°C		67	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	31	A
		T_A = 100°C		22	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.9	W
		T_A = 100°C		1.9	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to + 175	°C
Source Current (Body Diode)			I_S	112	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 11.9 A)			E_{AS}	941	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

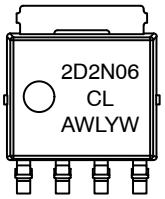
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	1.12	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



LFPAK4
CASE 760AB

2D6N06CL	= Specific Device Code
A	= Assembly Location
WL	=Wafer Lot
Y	= Year
W	= Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMYS2D2N06CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 180 μA		1.2		2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.3		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		1.6	1.9	mΩ
		V_{GS} = 4.5 V	I_D = 50 A		2.1	2.6	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 50 A			135		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			4850		pF
Output Capacitance	C_{OSS}				2450		
Reverse Transfer Capacitance	C_{RSS}				25		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V; I_D = 50 A			31		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 50 A			69		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 50 A			6.3		
Gate−to−Source Charge	Q_{GS}				11.5		
Gate−to−Drain Charge	Q_{GD}				7.6		
Plateau Voltage	V_{GP}				2.7		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 50 A, R_G = 2.5 Ω			13		ns
Rise Time	t_r				20		
Turn−Off Delay Time	$t_{d(OFF)}$				53		
Fall Time	t_f				9.4		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 20 A/μs, I_S = 50 A			64		ns
Charge Time	t_a				40		
Discharge Time	t_b				24		
Reverse Recovery Charge	Q_{RR}				84		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

NVMYS2D2N06CL

TYPICAL CHARACTERISTICS

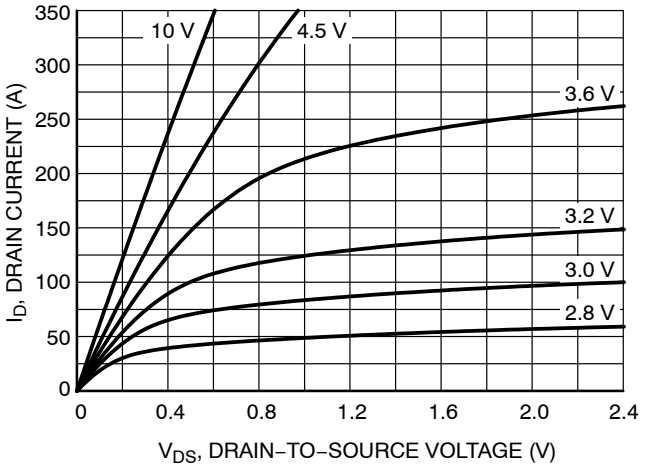


Figure 1. On−Region Characteristics

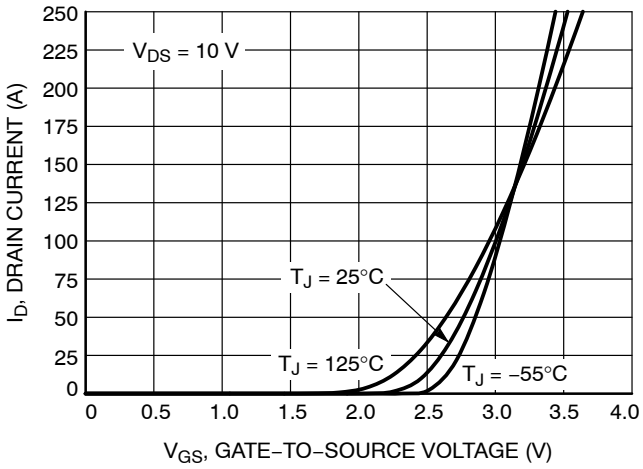


Figure 2. Transfer Characteristics

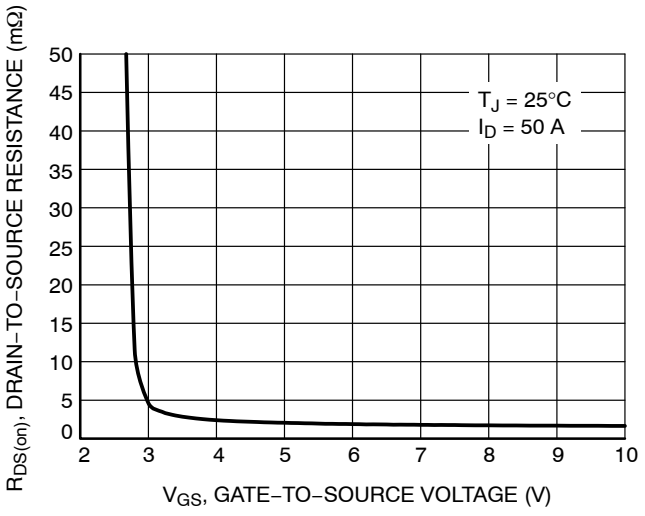


Figure 3. On−Resistance vs. Gate−to−Source Voltage

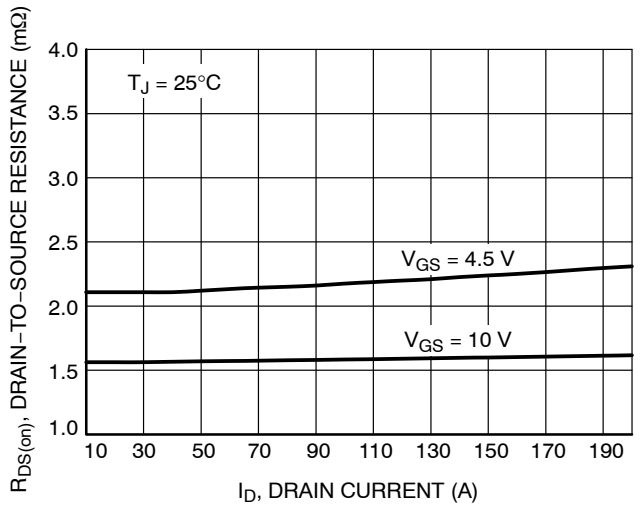


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

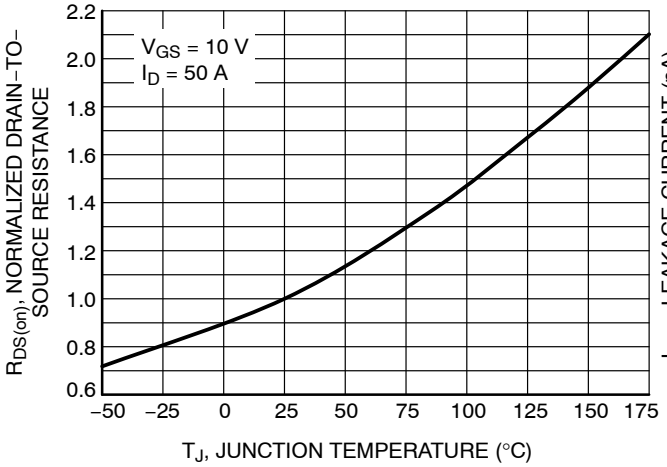


Figure 5. On−Resistance Variation with Temperature

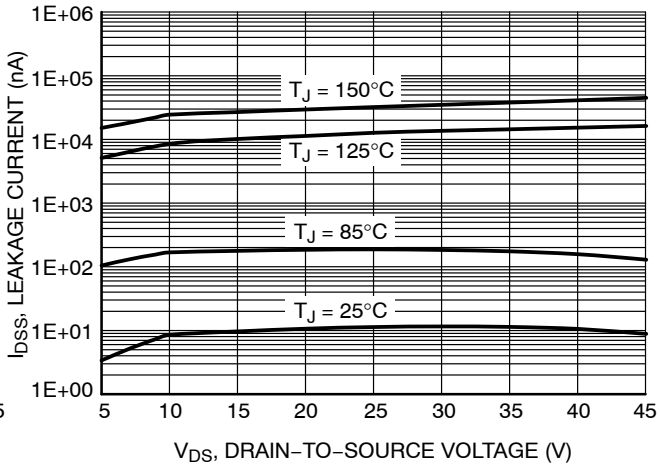


Figure 6. Drain−to−Source Leakage Current vs. Voltage

NVMYS2D2N06CL

TYPICAL CHARACTERISTICS

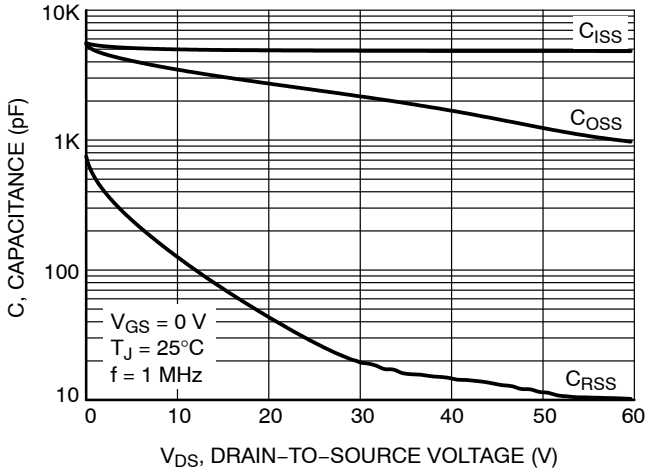


Figure 7. Capacitance Variation

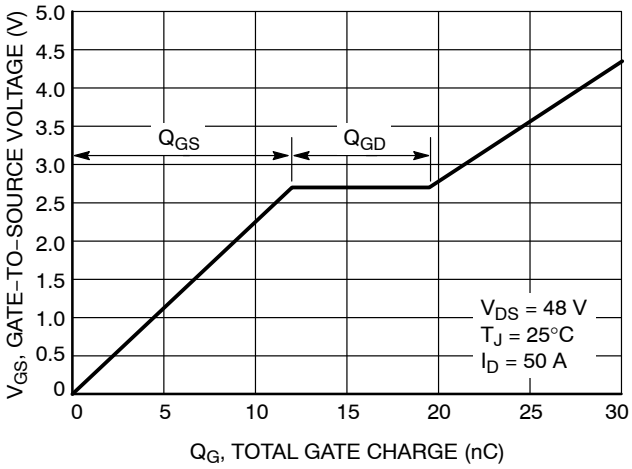


Figure 8. Gate−to−Source Voltage vs. Total Charge

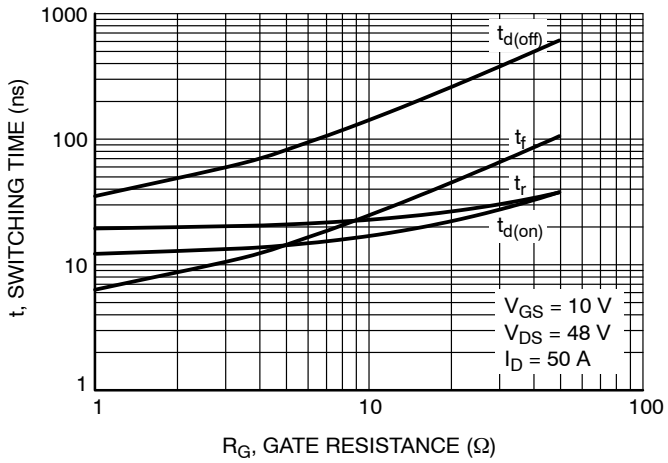


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

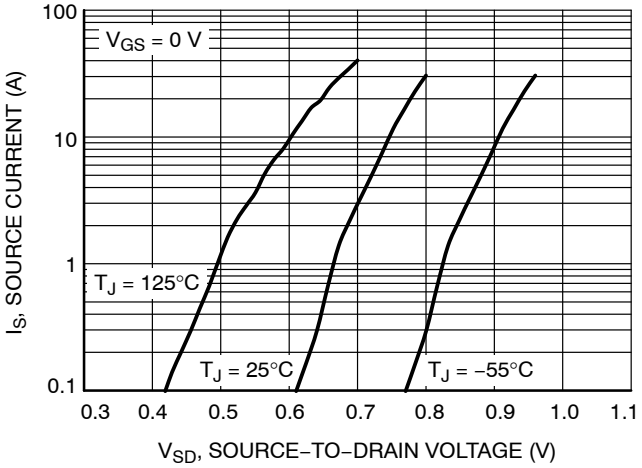


Figure 10. Diode Forward Voltage vs. Current

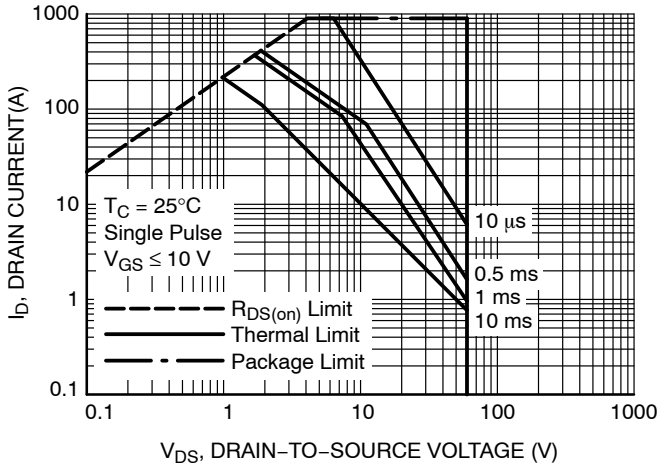


Figure 11. Maximum Rated Forward Biased Safe Operating Area

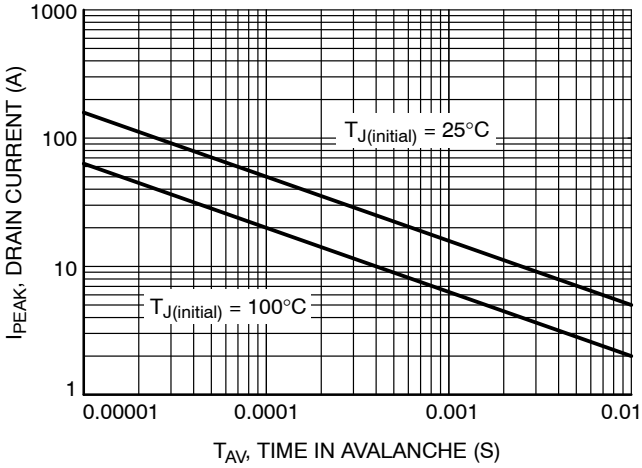


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVMYS2D2N06CL

TYPICAL CHARACTERISTICS

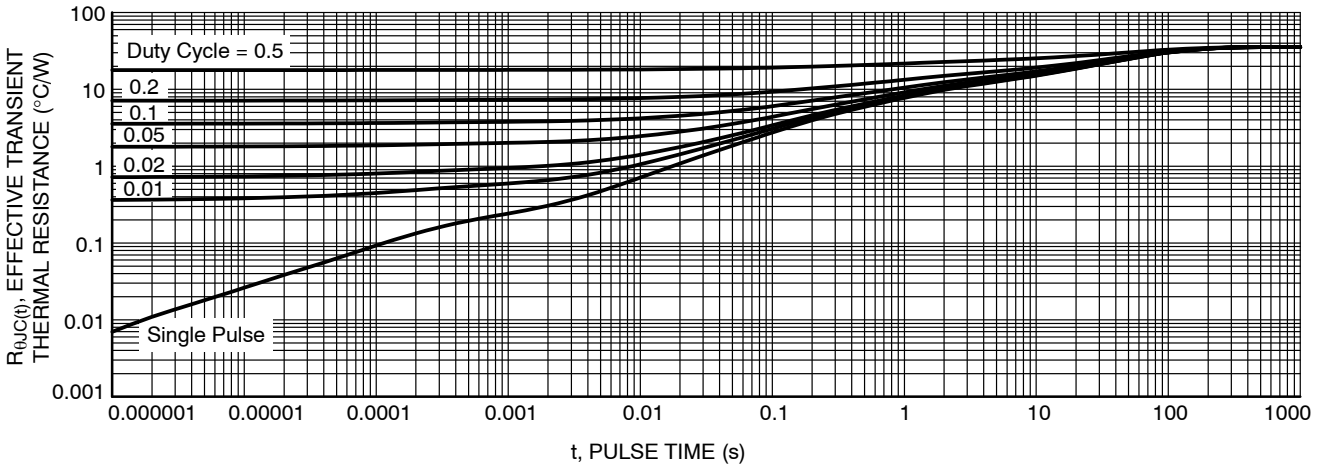


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

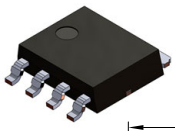
Device	Marking	Package	Shipping†
NVMYS2D2N06CLTWG	2D2N06CL	LFPAK4 (Pb−Free)	3000 / Tape & Reel

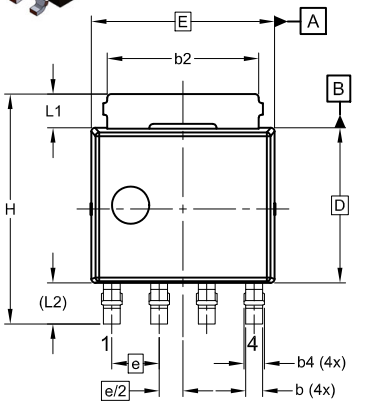
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

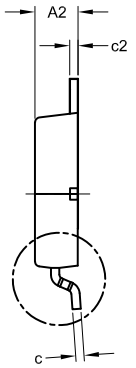
LFPAK4 4.90x4.15x1.15MM, 1.27P
CASE 760AB
ISSUE D

DATE 22 MAY 2024



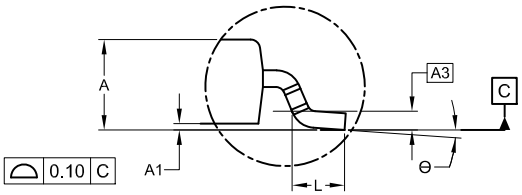


TOP VIEW

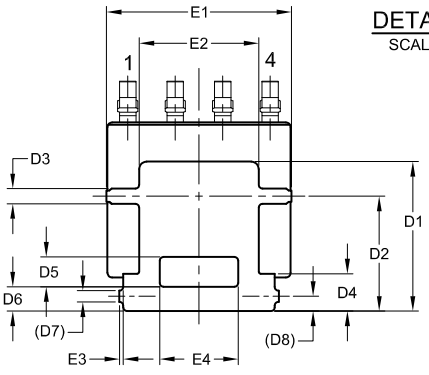


SIDE VIEW

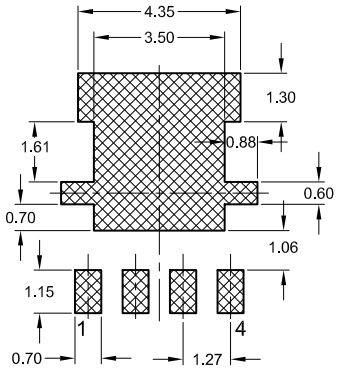
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.



DETAIL 'A'
SCALE: 2:1



BOTTOM VIEW

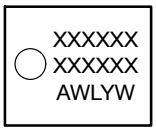


RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3		0.25 BSC	
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D		4.15 BSC	
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7		0.31 REF	
D8		0.40 REF	
E		4.90 BSC	
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e		1.27 BSC	
e/2		0.635 BSC	
e1		0.40 REF	
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2		1.10 REF	
Θ	0°	4°	8°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON82777G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**LFPAK4 4.90x4.15x1.15MM, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

OUR CERTIFICATE

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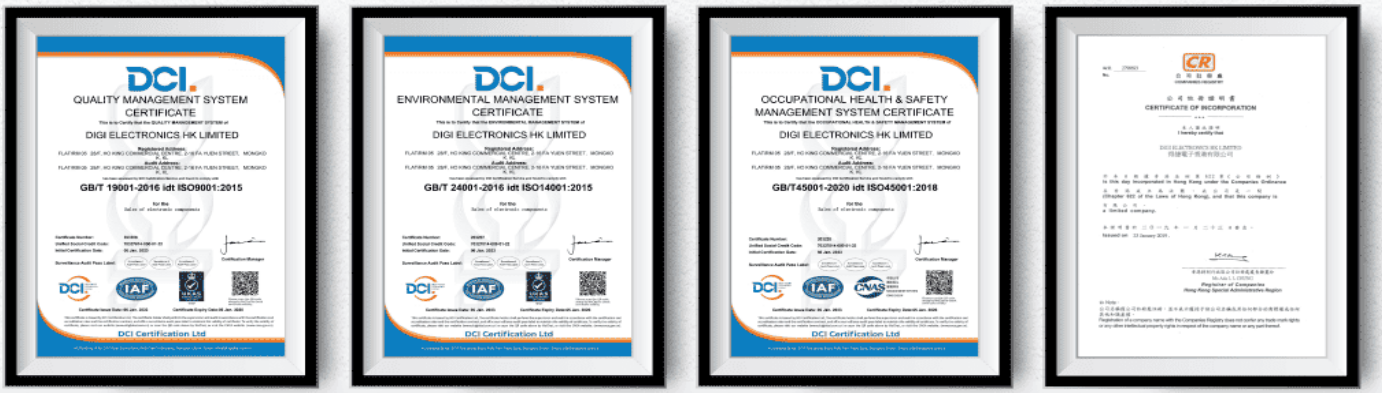

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