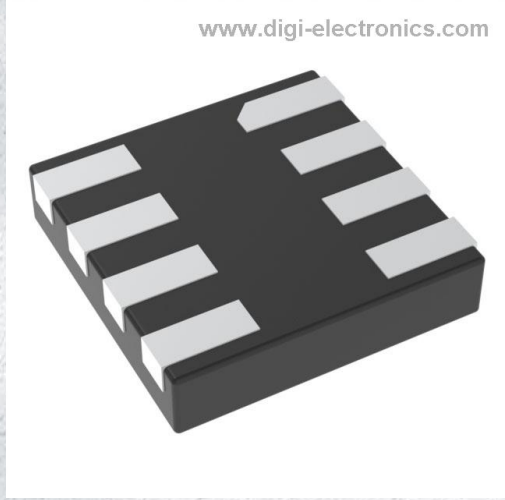
# P3P85R01AG-08CR Datasheet




| | |
|---|---|
| DiGi Electronics Part Number | P3P85R01AG-08CR-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | P3P85R01AG-08CR |
| Description | IC EMI REDUCTION TIME SAFE 8WDFN |
| Detailed Description | IC 200MHz 1 8-WFDFN |

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| P3P85R01AG-08CR | onsemi |
| Series: | Product Status: |
| Timing-Safe™ | Obsolete |
| DiGi-Electronics Programmable: | PLL: |
| Not Verified | Yes with Bypass |
| Input: | Output: |
| LVCMOS | Clock |
| Number of Circuits: | Ratio - Input:Output: |
| 1 | 1:1 |
| Differential - Input:Output: | Frequency - Max: |
| No/No | 200MHz |
| Divider/Multiplier: | Voltage - Supply: |
| No/Yes | 3V ~ 3.6V |
| Operating Temperature: | Mounting Type: |
| 0°C ~ 70°C | Surface Mount |
| Package / Case: | Supplier Device Package: |
| 8-WFDFN | 8-WDFN (2x2) |
| Base Product Number: | |
| P3P85R | |

## Environmental & Export classification

| Moisture Sensitivity Level (MSL): | REACH Status: |
| --- | --- |
| 1 (Unlimited) | REACH Unaffected |
| ECCN: | HTSUS: |
| EAR99 | 8542.39.0001 |

# P3P85R01A

# 3.3V, 75 MHz to 200 MHz LVCMOS TIMING SAFE™ Peak EMI Reduction Device

**ON Semiconductor®**

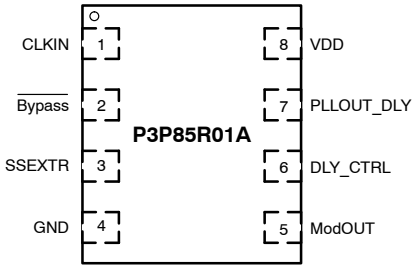
**http://onsemi.com**

**WDFN8**
**CASE 511AQ**

**MARKING DIAGRAMS**


DE = Specific Device Code
M = Date Code
▪ = Pb−Free Device
(Note: Microdot may be in either location)

**PIN CONFIGURATION**




**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

### Functional Description

P3P85R01A is a versatile, 3.3 V, LVCMOS, wide frequency range, TIMING SAFE Peak EMI reduction device. TIMING SAFE technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path. Refer to Figure 3.

P3P85R01A has an SSEXTR pin that selects different frequency deviations depending upon the value of the resistor connected between this pin and GND.

P3P85R01A has a DLY_CTRL pin used for adjusting the Input-Output clock delay, depending upon the value of capacitor connected at this pin to GND. The DLY_CTRL output phase is complementary to that of ModOUT clock. This signal enables better EMI management.

P3P85R01A has a $\overline{\text{Bypass}}$ pin to bypass PLL. The device works from 100 Hz to 200 MHz with a fixed input to output delay when in Bypass mode.

P3P85R01A has a PLLOUT_DLY for adjusting the PLL Output clock delay during power up time depending upon the value of capacitor connected at this pin to VDD. During power up time, ModOUT will be of the same frequency as CLKIN with a fixed input to output delay.

### General Features

- 1x, LVCMOS Peak EMI Reduction
- Input Frequency Range: 75 MHz – 200 MHz
- Output Frequency Range: 75 MHz – 200 MHz
- Analog Deviation Selection
- Analog Input−Output Delay Control
- Analog PLL Output Delay Control
- Low Cycle−to−Cycle Jitter
- Supply Voltage: 3.3 V ± 0.3 V
- 8 pin, WDFN, 2 mm x 2 mm (TDFN) Package
- Operating Temperature Range: 0°C to +70°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Application

- P3P85R01A is targeted for use in Displays, Giga LAN and SDRAM applications.

# P3P85R01A

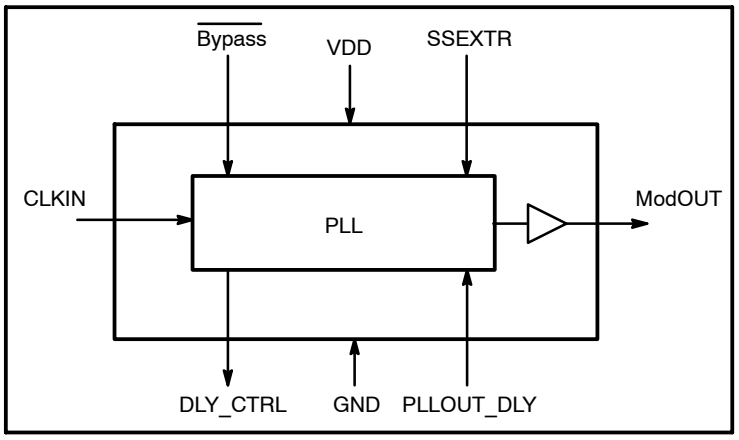



**Figure 1. Block Diagram**

**Table 1. PIN DESCRIPTION**

| Pin# | Pin Name | Type | Description |
|---|---|---|---|
| 1 | CLKIN | Input | External reference Clock Input |
| 2 | $\overline{\text{Bypass}}$ | Input | Bypass mode. When LOW device is in PLL Bypass mode.<br>When HIGH PLL, mode is enabled |
| 3 | SSEXTR | Input | Analog Deviation Selection through an external resistor to GND. |
| 4 | GND | Power | Ground |
| 5 | ModOUT | Output | Buffered Modulated Clock output |
| 6 | DLY_CTRL | Output | Analog Input−Output Delay Control through an external capacitor to GND. Output used for EMI management |
| 7 | PLLOUT_DLY | Input | Analog PLL output delay control during power−up time, through an external capacitor to VDD |
| 8 | VDD | Power | Supply Voltage |

**Table 2. OPERATING CONDITIONS**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 3.6 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| $C_{IN}$ | Input Capacitance | | 7 | pF |

**Table 3. ABSOLUTE MAXIMUM RATING**

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on any input pin with respect to Ground | −0.5 to +4.6 | V |
| $T_{STG}$ | Storage temperature | −65 to +125 | °C |
| $T_s$ | Max. Soldering Temperature (10 sec) | 260 | °C |
| $T_J$ | Junction Temperature | 150 | °C |
| $T_{DV}$ | Static Discharge Voltage (As per JEDEC STD22−A114−B) | 2 | kV |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. ELECTRICAL CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0 V | | | 50 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | | | 50 | μA |
| $V_{OL}$ | Output LOW Voltage (Note 1) | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage (Note 1) | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $I_{CC}$ | Static Supply Current | CLKIN pin pulled LOW | | | 100 | μA |
| $I_{DD}$ | Dynamic Supply Current | Unloaded output | | | 50 | mA |
| $C_L$ | Load Capacitance | @ 200 MHz | | 10 | | pF |
| $Z_o$ | Output Impedance | | | 27 | | Ω |

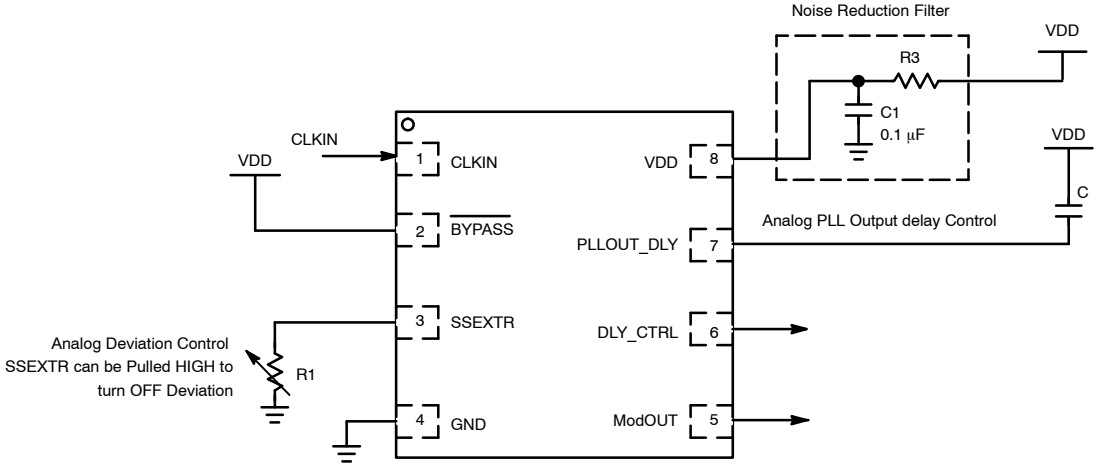
1. Parameter is guaranteed by design and characterization. Not tested in production

**Table 5. SWITCHING CHARACTERISTICS**

| Parameter | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Frequency | | | 75 | | 200 | MHz |
| Output Frequency | | | 75 | | 200 | MHz |
| Duty Cycle (Note 2) = ($t_2$ / $t_1$) * 100 | Measured at $V_{DD}$ / 2 | | 40 | 49 – 51 | 60 | % |
| Output Rise Time ($t_3$) (Notes 2 and 3) | Measured between 20% to 80% | | | | 2 | ns |
| Output Fall Time ($t_4$) (Notes 2 and 3) | Measured between 80% to 20% | | | | 1.8 | ns |
| Delay, CLKIN Rising Edge to ModOUT Rising Edge ($t_5$) (Notes 2 and 4) | @ 133 MHz, Variable Delay mode | | | −500 | | ps |
| | Fixed Delay mode | | | 1.4 | 1.7 | ns |
| Load line | Change in Input−Output delay, SSEXTR = OPEN | on DLY_CTRL | | −40 | | ps/pF |
| | | on ModOUT | | 40 | | |
| PLL OUT Delay Time (Note 5) | PLLOUT_DLY pin left OPEN | | | 1 | | ms |
| Cycle−to−cycle Jitter (Note 2) | Unloaded Outputs @ 133 MHz | | | ±100 | | ps |
| PLL Lock Time (Note 2) | Stable power supply, valid clock presented on CLKIN | | | | 1 | ms |
| Device−to−Device variation of Deviation and I/O delay | | | | ±20 | | % |

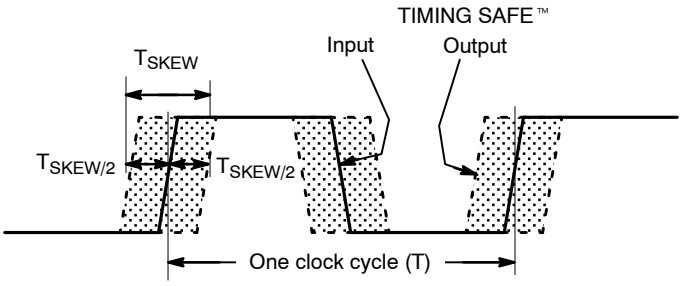
2. Parameter is guaranteed by design and characterization. Not tested in production
3. All parameters are specified with 10 pF − loaded outputs.
4. 10 pF load on ModOUT, DLY_CTRL and SSEXTR pins left OPEN.
5. Parameter is guaranteed by design.

# P3P85R01A

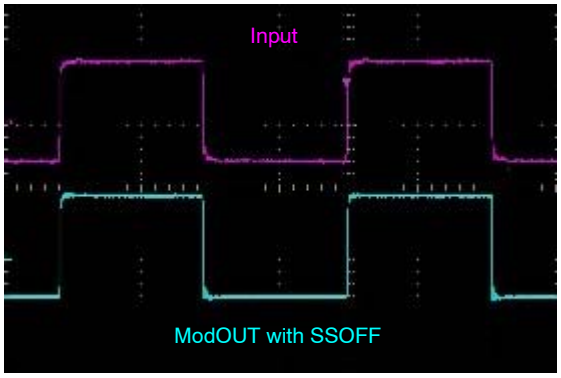



NOTES: Refer to Pin Description table for Functionality details.

**Figure 2. Application Schematic**




$T_{SKEW}$ represents input-output skew when spread spectrum is ON
For example, $T_{SKEW}/2$= 0.20 x T for an Input clock of 75 MHz,
translates into (1/75 MHz) x 0.20=2.66 nS



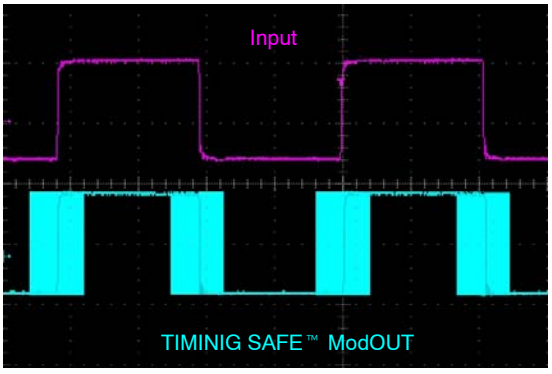




**Figure 3. Typical Example of TIMING SAFE Waveform**

## SWITCHING WAVEFORMS

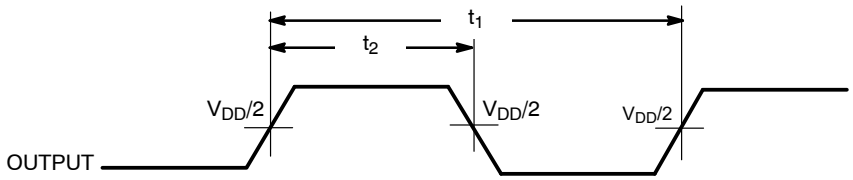



**Figure 4. Duty Cycle Timing**

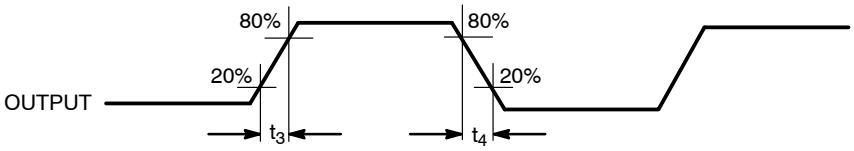



**Figure 5. Output Rise/Fall Time**

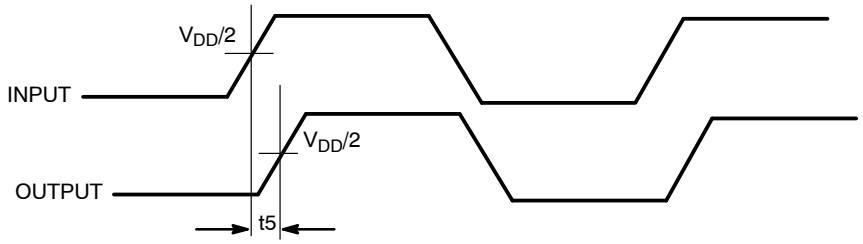



**Figure 6. Input − Output Propagation Delay**

# P3P85R01A

## CHARTS

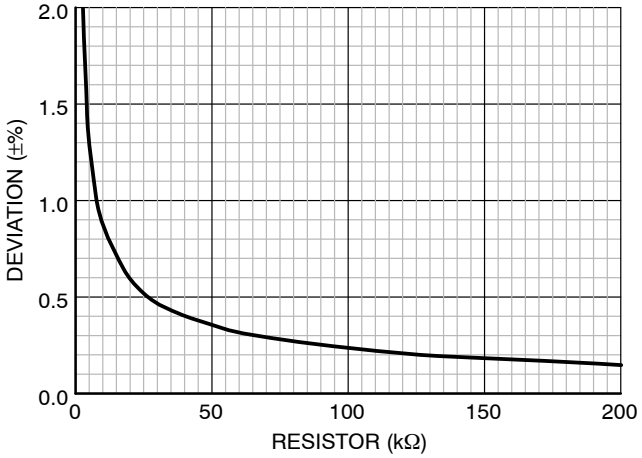



**Figure 7. Deviation vs. SSEXTR @ 106 MHz**

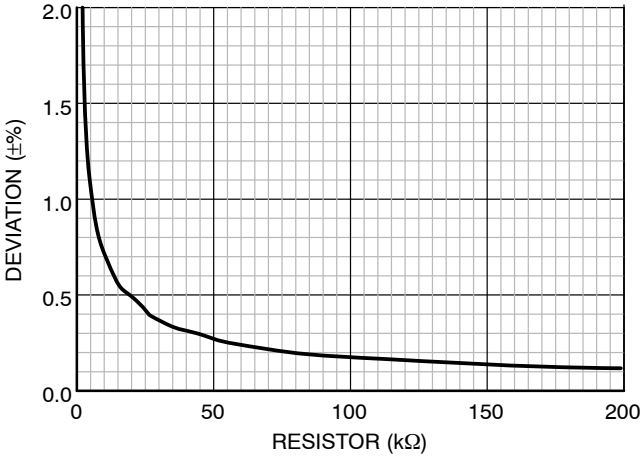



**Figure 8. Deviation vs. SSEXTR @ 125 MHz**

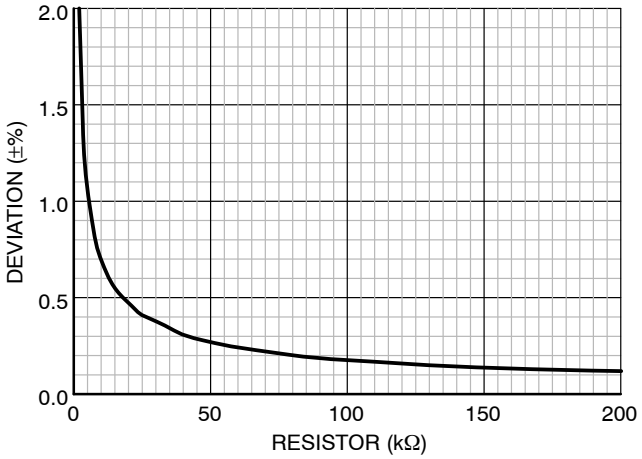



**Figure 9. Deviation vs. SSEXTR @ 133 MHz**

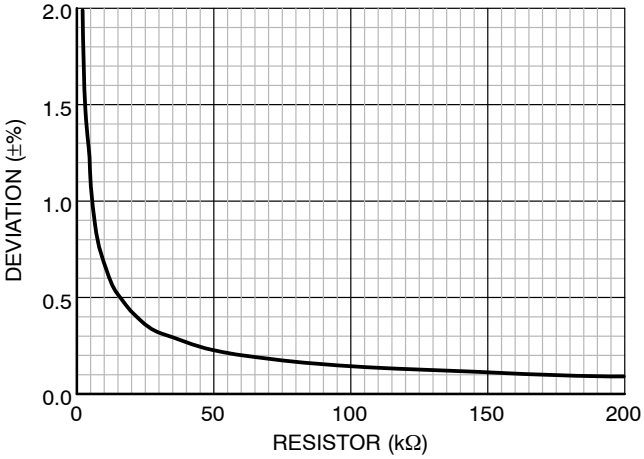



**Figure 10. Deviation vs. SSEXTR @ 145 MHz**

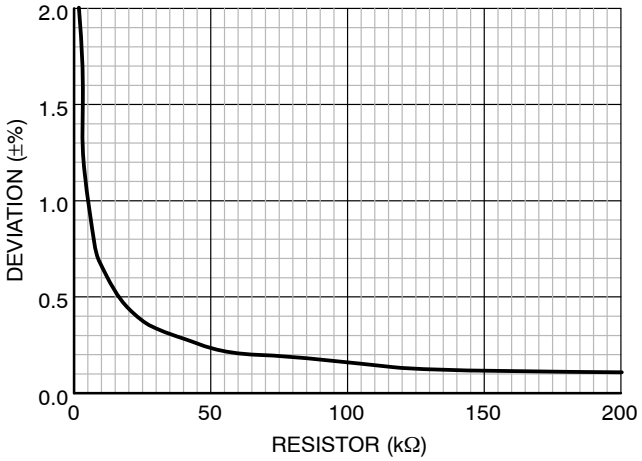



**Figure 11. Deviation vs. SSEXTR @ 156 MHz**

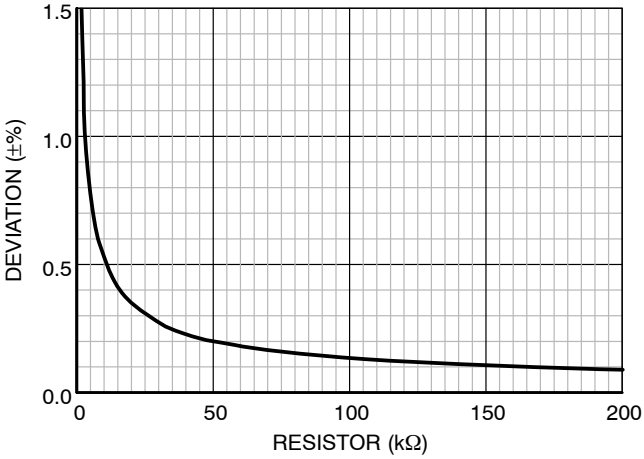



**Figure 12. Deviation vs. SSEXTR @ 166 MHz**

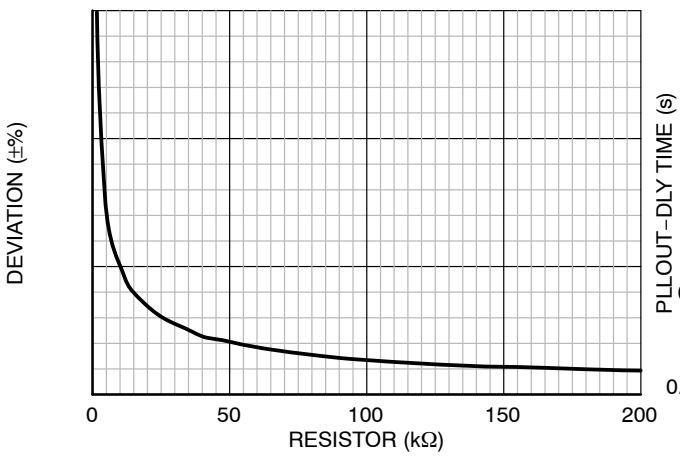



**Figure 13. Deviation vs. SSEXTR @ 175 MHz**

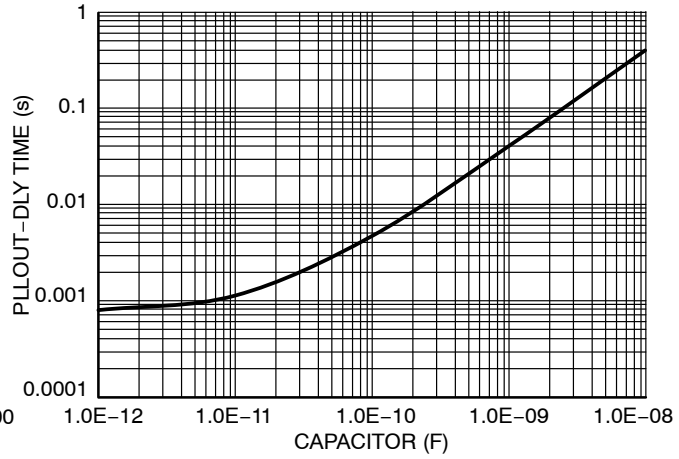



**Figure 14. PLLOUT−DLY Time vs. Capacitor**

## ORDERING INFORMATION

| Part Number | Top Marking | Temperature | Package Type | Shipping† |
|---|---|---|---|---|
| P3P85R01AG−08CR | DE | 0°C to +70°C | WDFN8 (2mm x 2mm) (Pb−Free) | 3000 / Tape & Reel |

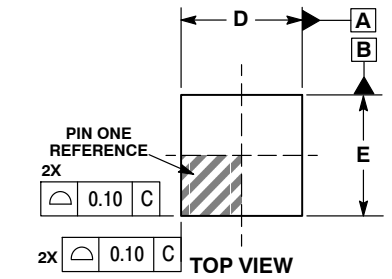
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

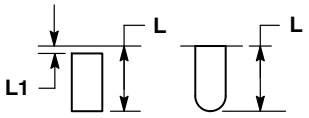
*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

# P3P85R01A

## PACKAGE DIMENSIONS

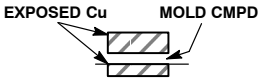
**WDFN8 2x2, 0.5P**
CASE 511AQ−01
ISSUE A



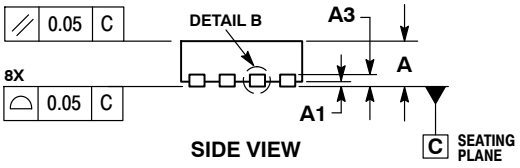




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

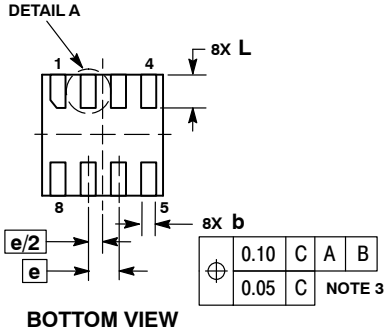
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| E | 2.00 BSC | |
| e | 0.50 BSC | |
| L | 0.50 | 0.60 |
| L1 | --- | 0.15 |




**DETAIL B**
**OPTIONAL CONSTRUCTION**

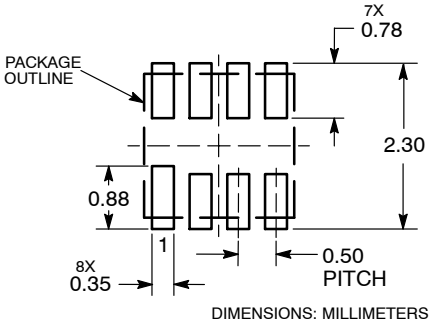



**SIDE VIEW**




**BOTTOM VIEW**

**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
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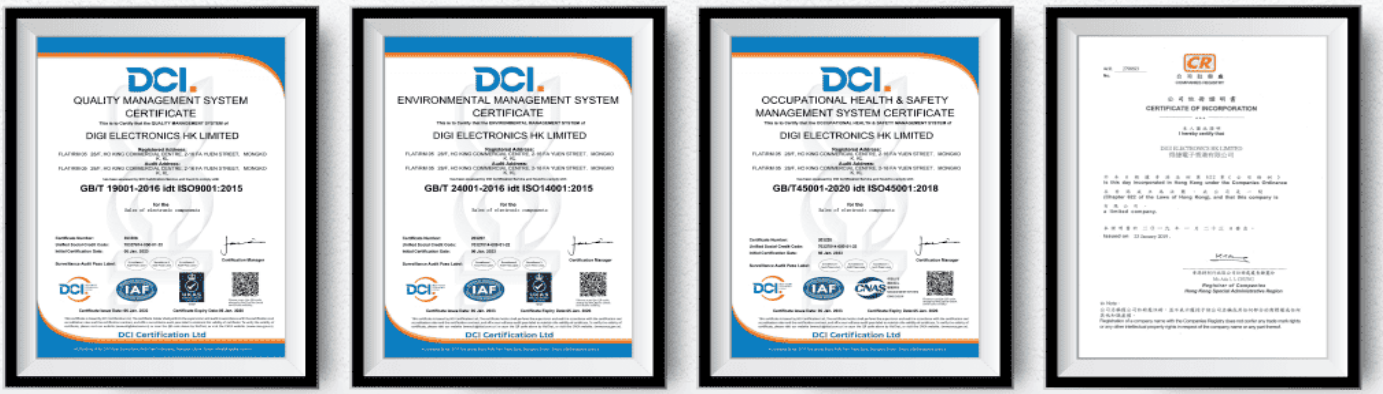



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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