

# MGM111A256V2R Datasheet

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DiGi Electronics Part Number	MGM111A256V2R-DG
Manufacturer	<a href="#">Silicon Labs</a>
Manufacturer Product Number	MGM111A256V2R
Description	RF TXRX MODULE 802.15.4 CHIP SMD
Detailed Description	802.15.4 Zigbee® Transceiver Module 2.4GHz Integrated, Chip Surface Mount

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## Purchase and inquiry

Manufacturer Product Number:

MGM111A256V2R

Series:

Mighty Gecko

DiGi-Electronics Programmable:

Not Verified

Protocol:

Zigbee®

Frequency:

2.4GHz

Power - Output:

10dBm

Serial Interfaces:

I2C, I2S, SPI, UART

Utilized IC / Part:

EFR32

Voltage - Supply:

1.85V ~ 3.8V

Current - Transmitting:

8.2mA

Operating Temperature:

-40°C ~ 85°C

Base Product Number:

MGM111

Manufacturer:

Silicon Labs

Product Status:

Not For New Designs

RF Family/Standard:

802.15.4

Modulation:

DSSS, O-QPSK

Data Rate:

250kbps

Sensitivity:

-99dBm

Antenna Type:

Integrated, Chip

Memory Size:

256kB Flash, 32kB RAM

Current - Receiving:

9.8mA

Mounting Type:

Surface Mount

Package / Case:

31-SMD Module

## Environmental & Export classification

RoHS Status:

RoHS Compliant

ECCN:

5A992C

Moisture Sensitivity Level (MSL):

3 (168 Hours)

HTSUS:

8517.62.0090



# MGM111 Mighty Gecko Mesh Networking Module Data Sheet

The Silicon Labs Mighty Gecko Module (MGM111) is a fully-integrated, pre-certified module, enabling rapid development of wireless mesh networking solutions.

Based on the Silicon Labs EFR32™ Mighty Gecko SoC, the MGM111 combines an energy-efficient, multi-protocol wireless SoC with a proven RF/antenna design and industry-leading wireless software stacks. This integration accelerates time-to-market and saves months of engineering effort and development costs.

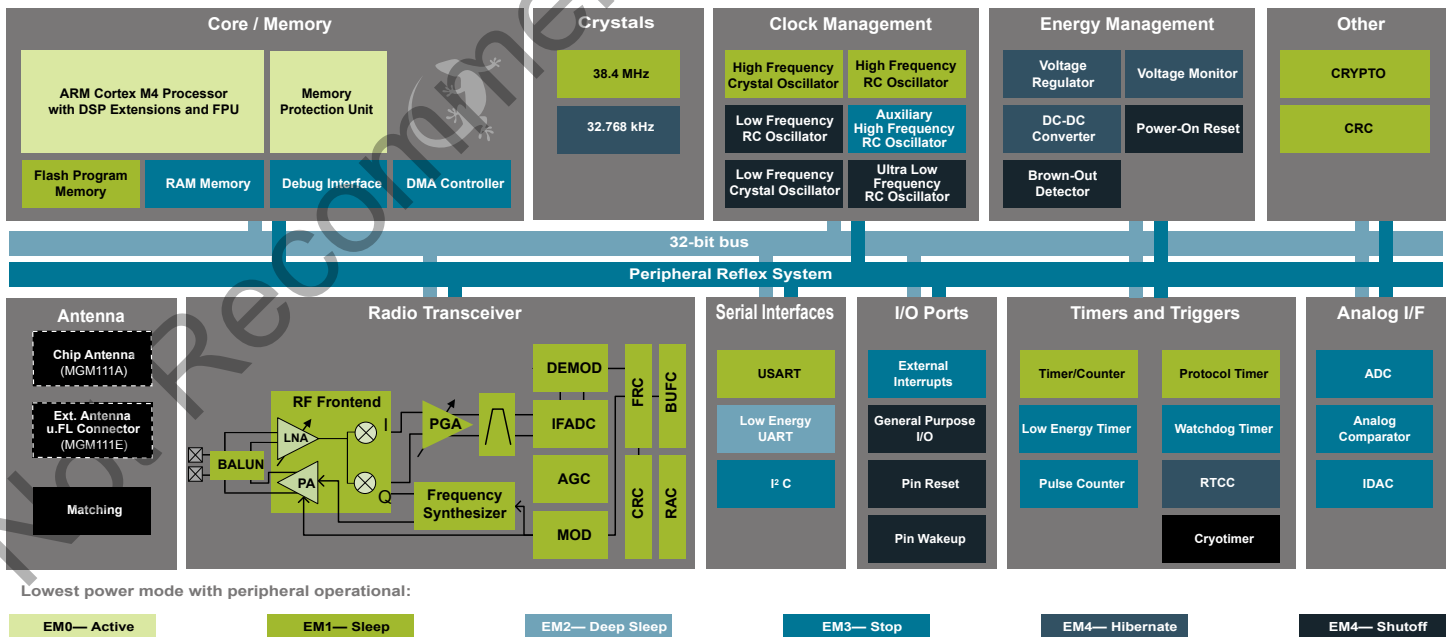
In addition, common software and development tools enable seamless migration from a module to discrete SoC-based design when the time is right.

MGM111 can be used in a wide variety of applications:

- Connected Home
- Building Automation
- Lighting
- Security and Monitoring
- Smart Grid / Metering
- Industrial Automation
- Others

## KEY FEATURES

- Industry-leading mesh networking (ZigBee/Thread) and Bluetooth Smart software and development tools
- Antenna: internal chip and U.FL variants
- TX power: up to +10 dBm
- RX sensitivity: down to -99 dBm
- 32-bit ARM® Cortex®-M4 at 40 MHz
- Flash memory: 256 kB
- RAM: 32 kB
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated DC-DC Converter



## 1. Feature List

### MCU Features

- ARM Cortex<sup>®</sup>-M4 + Floating Point Unit
- Up to 40 MHz Clock Speed
- Low Active Mode Current: 63  $\mu$ A/MHz
- 256 kB flash, 32 kB SRAM
- Advanced hardware cryptographic engine with support for AES-128/-256, ECC, SHA-1, SHA-256, and a Random Number Generator
- 8 Channel DMA Controller

### Digital Peripherals

- 2 x USART (UART, SPI, IrDA, I<sup>2</sup>S)
- Low Energy UART (LEUART<sup>™</sup>)
- I<sup>2</sup>C peripheral interface (address recognition down to EM3)
- Timers: RTCC, Low Energy Timer, Pulse Counter
- 12-channel Peripheral Reflex System (PRS)
- Up to 25 GPIO with interrupts

### Analog Peripherals

- ADC (12-bit, 1 Msps, 326  $\mu$ A)
- Current-mode Digital to Analog Converter (IDAC)
- 2 x Analog Comparator (ACMP)

### Energy Efficient Low Power Modes

- Energy Mode 2 (Deep Sleep) Current: 2.5  $\mu$ A  
(Full RAM retention and RTCC running from LXFO)
- Ultra-fast wake up: 3  $\mu$ S down to EM3
- Wide Supply Voltage range of 1.85 to 3.8 V

### Environmental & Regulatory

- Operating Temperature: -40 to +85°C

### Dimensions

- W x L x H: 12.9 x 15.0 x 2.2 mm

### Radio Features

- 2.4 GHz with integrated balun
- Support for wireless mesh networking (ZigBee/Thread)
- Integrated PA
- Packet Trace Interface (PTI) for non-intrusive packet trace with Simplicity Studio development tools
- Antenna interface: integrated high-performance chip antenna

### ZigBee and Thread Features

- IEEE 802.15.4
- Data Rate / Modulation: 250 kbps DSSS-OQPSK
- +10 dBm Programmable TX Power
- -99 dBm RX Sensitivity
- 9.8 mA RX current
- 8.2 mA TX current (at +0 dBm)
- Support for SoC and Network Co-Processor (NCP) architectures with SPI/UART host support
- Serial and Over-The-Air (OTA) bootloaders

## 2. Ordering Information

Ordering Code	Description	Max TX Power	Antenna	Packaging	Production Status
MGM111A256V1	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Cut Reel (100 pcs)	End of life
MGM111A256V1R	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Reel (1000 pcs)	End of life
MGM111E256V1	Mighty Gecko Module	+10 dBm	External (U.FL)	Cut Reel (100 pcs)	End of life
MGM111E256V1R	Mighty Gecko Module	+10 dBm	External (U.FL)	Reel (1000 pcs)	End of life
MGM111A256V2	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Cut Reel (100 pcs)	Not recommended for New Designs
MGM111A256V2R	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Reel (1000 pcs)	Not recommended for New Designs
MGM111E256V2	Mighty Gecko Module	+10 dBm	External (U.FL)	Cut Reel (100 pcs)	End of life
MGM111E256V2R	Mighty Gecko Module	+10 dBm	External (U.FL)	Reel (1000 pcs)	End of life
SLWRB4300B	MGM111A Radio Board Add-On for Mesh Networking Kit (SLWSTK6000A)	+10 dBm	Integrated chip antenna	Single unit	Not recommended for New Designs

**Note:**

1. IAR license required for ZigBee and Thread software development.

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### 3. System Overview

#### 3.1 Introduction

This section provides a brief overview of the MGM111 module architecture including both MCU and RF sub-systems. A detailed functional description of the Silicon Lab's EFR32MG1 SoC used inside the module is available in the *EFR32MG1 Mighty Gecko Datasheet* and *EFR32xG1 Wireless Gecko Reference Manual* and a block diagram of the EFR32MG1 SoC is shown in the figure below.

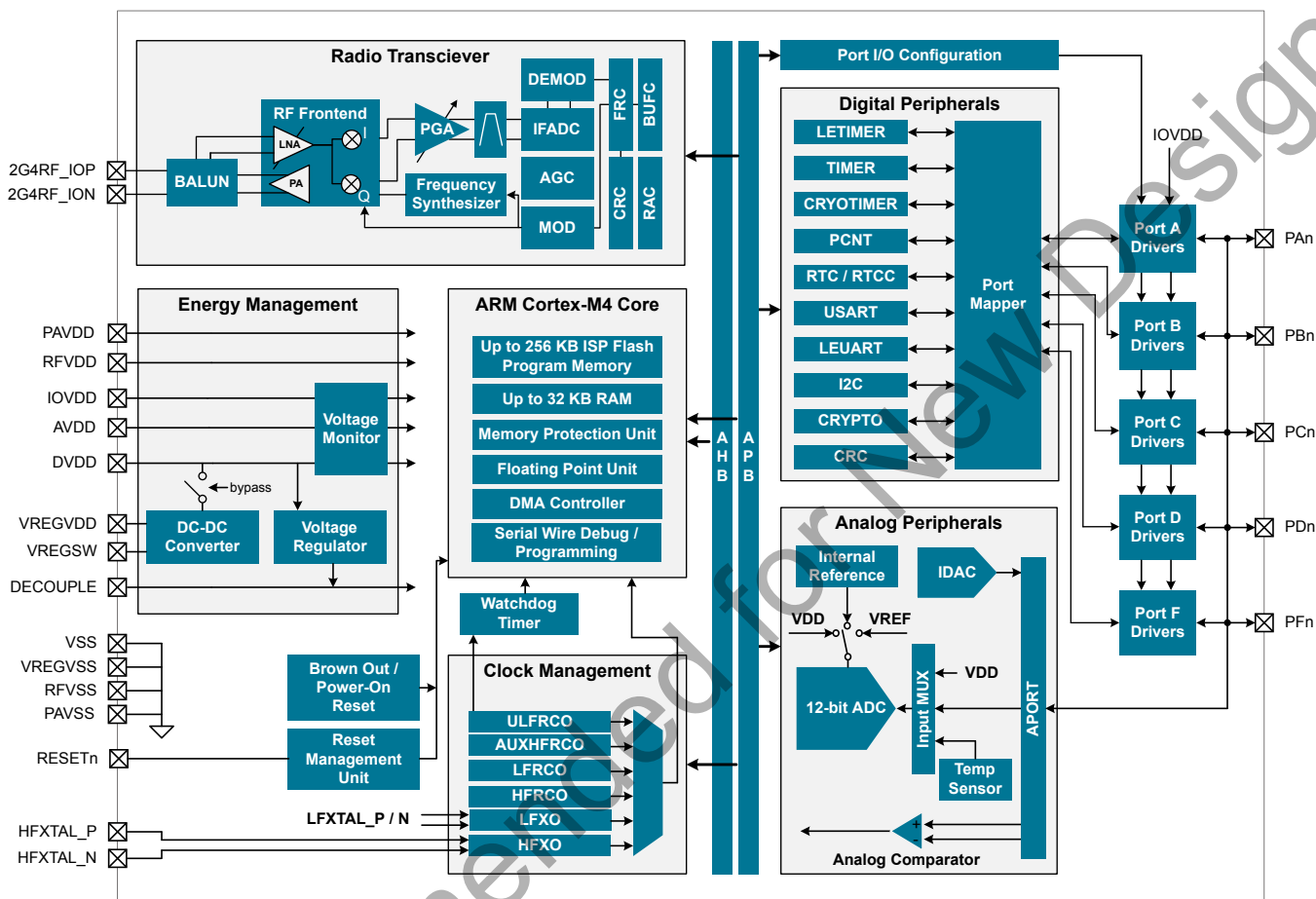


Figure 3.1. Detailed EFR32MG1 Block Diagram

#### 3.2 Radio

The MGM111 features a flexible, multi-protocol radio that supports wireless mesh networking (ZigBee® / Thread) and Bluetooth Smart protocols.

##### 3.2.1 Antenna Interface

The MGM111 module family includes options for either a high-performance, integrated chip-antenna (MGM111A) or external antenna (MGM111E) via a U.FL connector. The table below includes performance specifications for the integrated chip antenna.

Table 3.1. Antenna Efficiency and Peak Gain (MGM111A)

Parameter	With optimal layout	Note
Efficiency	-2 dB to -3 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Chapter 6. <a href="#">Layout Guidelines</a> for PCB layout and antenna integration guidelines for optimal performance.
Peak gain	1.0 dBi	

### 3.2.2 Packet and State Trace

The MGM111 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

### 3.2.3 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

Not Recommended for New Designs

### 3.3 Power

The MGM111 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

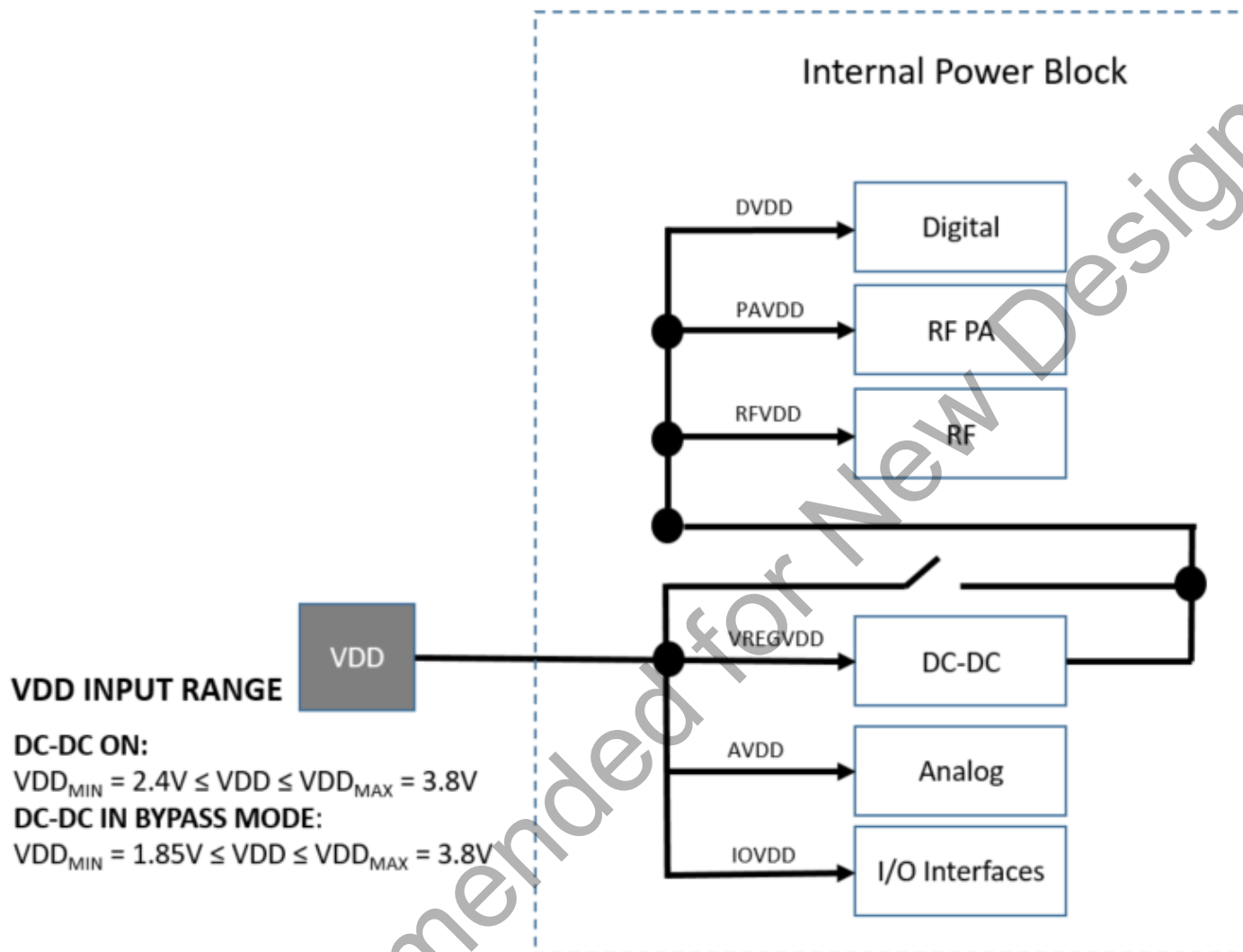


Figure 3.2. MGM111 Power Block

#### 3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

#### 3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2, and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

### 3.4 General Purpose Input/Output (GPIO)

MGM111 has 25 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

### 3.5 Clocking

#### 3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the MGM111. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

#### 3.5.2 Internal Oscillators

The MGM111 fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HF XO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LF XO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

### 3.6 Counters/Timers and PWM

#### 3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER\_0 only.

#### 3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

#### 3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

### 3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

### 3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn\_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

### 3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

## 3.7 Communications and Other Digital Peripherals

### 3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I<sup>2</sup>S

### 3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART<sup>TM</sup> provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

### 3.7.3 Inter-Integrated Circuit Interface (I<sup>2</sup>C)

The I<sup>2</sup>C module provides an interface between the MCU and a serial I<sup>2</sup>C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I<sup>2</sup>C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

### 3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

## 3.8 Security Features

### 3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

### 3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. It supports AES encryption and decryption with 128- or 256-bit keys and ECC over both GF(P) and GF(2<sup>m</sup>), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

## 3.9 Analog

### 3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

### 3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

### 3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05  $\mu$ A and 64  $\mu$ A with several ranges with various step sizes.

## 3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the MGM111. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

## 3.11 Core and Memory

### 3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 256 KB flash program memory
- 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

### 3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

Not Recommended for New Designs

### 3.12 Memory Map

The MGM111 memory map is shown in the figures below.

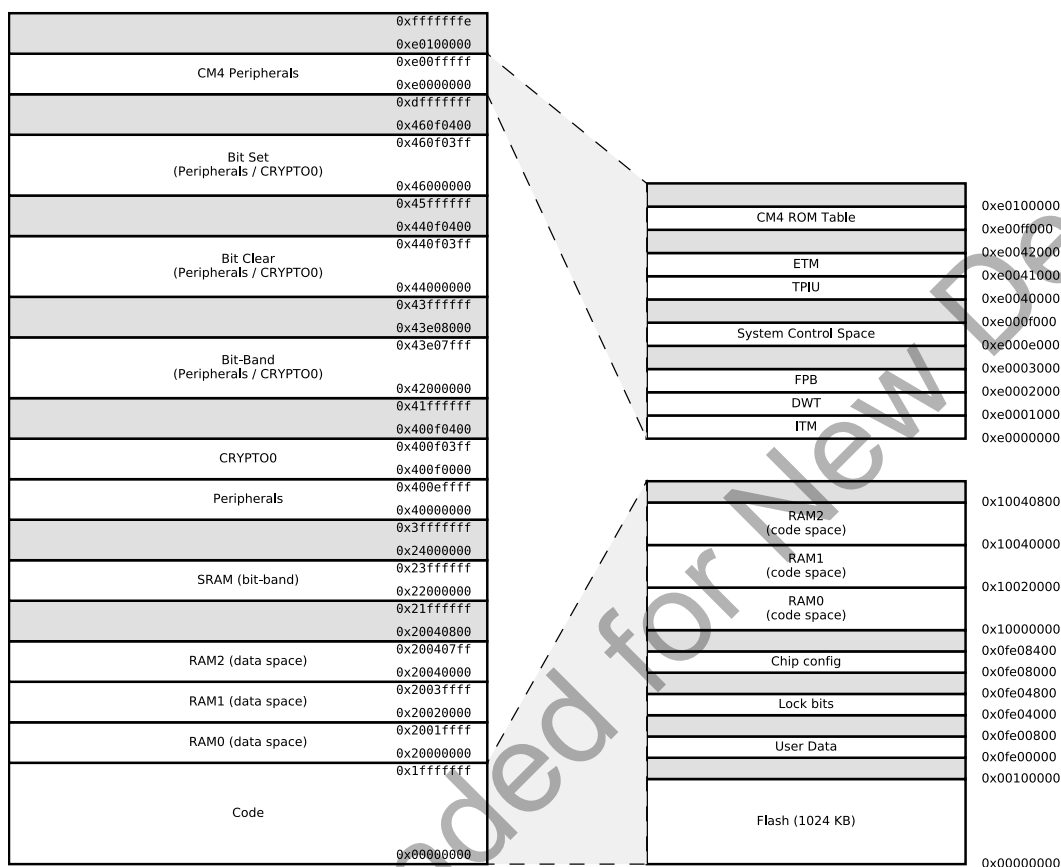


Figure 3.3. MGM111 Memory Map — Core Peripherals and Code Space

0x400e6000	PRS	0xffffffffe
0x400e5400	RMU	0xe0100000
0x400e5000		0xe00fffff
0x400e4400	CMU	CM4 Peripherals
0x400e4000		0xe0000000
0x400e3400	EMU	0xdfffffff
0x400e3000	LDMA	0x460f0400
0x400e2000		0x460f03ff
0x400e1400	EPOFF	
0x400e1000		
0x400e0800	MSC	
0x400e0000		
0x40088400	RFSENSE	Bit Set (Peripherals / CRYPTO0)
0x40087400	AGC	0x46000000
0x40087000		0x45ffffff
0x40086800	MODEM	0x440f0400
0x40086000	PROTIMER	0x440f03ff
0x40085400		
0x40085000	PROTIMER	
0x40084400	RAC	
0x40084000		
0x40083400	SYNTH	Bit Clear (Peripherals / CRYPTO0)
0x40083000		0x44000000
0x40082400	CRC	0x43ffffff
0x40081400	BUFC	0x43e00000
0x40081000		0x43e07fff
0x40080400	FRC	
0x40080000		
0x40054400	LESENSE	Bit-Band (Peripherals / CRYPTO0)
0x40052800	WDUG1	0x42000000
0x40052400	WDUG0	0x41ffffff
0x40052000		0x400f0400
0x4004ec00	PCNT2	0x400f03ff
0x4004e800	PCNT1	0x400f0000
0x4004e400	PCNT0	0x400effff
0x4004e000		0x40000000
0x4004a400	LEUART0	
0x4004a000		
0x40046400	LETIMER0	CRYPTO0
0x40046000		Peripherals
0x40042400	RTCC	0x40000000
0x40042000		0x3fffffff
0x40022400	SMU	0x24000000
0x40022000		0x23ffffff
0x4001f400	CSEN	0x22000000
0x4001f000		0x21ffffff
0x4001e400	CRYOTIMER	
0x4001e000		
0x4001d400	TRNG0	RAM2 (data space)
0x4001d000		0x20040800
0x4001c400	GPCRC	0x200407ff
0x4001c000		0x20040000
0x4001a800	WTIMER1	
0x4001a400	WTIMER0	
0x4001a000		
0x40018800	TIMER1	RAM1 (data space)
0x40018400	TIMER0	0x20020000
0x40018000		0x2001ffff
0x40011000	USART3	
0x40010c00	USART2	
0x40010800	USART1	
0x40010400	USART0	
0x40010000		
0x4000e800	RTC	RAM0 (data space)
0x4000c400	RTC	0x20000000
0x4000c000		0x1fffffff
0x4000b000		
0x4000a000	GPIO	
0x40008400	VDAC0	
0x40008000		
0x40006400	VDAC0	
0x40006000		
0x40004000	ADC0	
0x40002000		
0x40000800	ACMP1	
0x40000400	ACMP0	
0x40000000		0x00000000

Figure 3.4. MGM111 Memory Map — Peripherals

### 3.13 Configuration Summary

The features of the MGM111 are a subset of the feature set described in the *EFR32xG1 Wireless Gecko Reference Manual*. The Pin Definitions section describes device specific implementation of the features.

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on  $T_{AMB}=25\text{ }^{\circ}\text{C}$  and  $V_{DD}=3.3\text{ V}$ , by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a  $50\ \Omega$  antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation and operating temperature.

Refer to [Table 4.2 General Operating Conditions on page 17](#) for more details about operational supply and temperature limits.

#### 4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.1. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	$T_{STG}$		-40	—	+85	$^{\circ}\text{C}$
External main supply voltage	$V_{DDMAX}$		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / $\mu\text{s}$
Voltage on any 5V tolerant GPIO pin <sup>1</sup>	$V_{DIGPIN}$		-0.3	—	Min of 5.25 and VDD+2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	VDD+0.3	V
Input RF level	$P_{RFMAX2G4}$		—	—	10	dBm
Current per I/O pin (sink)	$I_{IOMAX}$		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA

**Note:**

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = VDD.

#### 4.1.2 General Operating Conditions

**Table 4.2. General Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T <sub>OP</sub>	Ambient Temperature	-40	25	85	°C
VDD supply voltage <sup>1</sup>	V <sub>VDD</sub>	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
VDD Current	I <sub>VDD</sub>	DCDC in bypass	—	—	200	mA
HFCLK frequency	f <sub>CORE</sub>	0 wait-states (MODE = WS0) <sup>2</sup>	—	—	26	MHz
		1 wait-states (MODE = WS1) <sup>2</sup>	—	38.4	40	MHz

**Note:**

- The minimum voltage required in bypass mode is calculated using R<sub>BYP</sub> from the DCDC specification table. Requirements for other loads can be calculated as  $V_{VDD\_min} + I_{LOAD} * R_{BYP\_max}$
- in MSC\_READCTRL register

Not Recommended for New Designs

### 4.1.3 DC-DC Converter

Test conditions:  $V_{DCDC\_I}=3.3$  V,  $V_{DCDC\_O}=1.8$  V,  $I_{DCDC\_LOAD}=50$  mA, Heavy Drive configuration,  $F_{DCDC\_LN}=7$  MHz, unless otherwise indicated.

**Table 4.3. DC-DC Converter**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	$V_{DCDC\_I}$	Bypass mode, $I_{DCDC\_LOAD} = 50$ mA	1.85	—	$V_{VDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, $I_{DCDC\_LOAD} = 100$ mA, or Low power (LP) mode, 1.8 V output, $I_{DCDC\_LOAD} = 10$ mA	2.4	—	$V_{VDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, $I_{DCDC\_LOAD} = 200$ mA	2.6	—	$V_{VDD\_MAX}$	V
Output voltage programmable range <sup>1</sup>	$V_{DCDC\_O}$		1.8	—	$V_{VREGVDD}$	V
Max load current	$I_{LOAD\_MAX}$	Low noise (LN) mode, Heavy Drive <sup>3</sup>	—	—	200	mA
		Low noise (LN) mode, Medium Drive <sup>3</sup>	—	—	100	mA
		Low noise (LN) mode, Light Drive <sup>3</sup>	—	—	50	mA
		Low power (LP) mode, $LPCMPBIAS^2 = 0$	—	—	75	$\mu$ A
		Low power (LP) mode, $LPCMPBIAS^2 = 3$	—	—	10	mA

**Note:**

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage,  $V_{VDD}$
2. In EMU\_DCDCMISCCTRL register
3. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

#### 4.1.4 Current Consumption

##### 4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3 V, DC-DC enabled. T<sub>OP</sub> = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.4. Current Consumption 3.3V with DC-DC**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>1</sup> .	I <sub>ACTIVE</sub>	38.4 MHz crystal, CPU running while loop from flash <sup>2</sup>	—	88	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	63	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	71	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	78	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	76	—	μA/MHz
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise CCM mode <sup>3</sup> .	I <sub>ACTIVE</sub>	38.4 MHz crystal, CPU running while loop from flash <sup>2</sup>	—	98	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	75	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	81	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	88	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	μA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>1</sup> .	I <sub>EM1</sub>	38.4 MHz crystal <sup>2</sup>	—	49	—	μA/MHz
		38 MHz HFRCO	—	32	—	μA/MHz
		26 MHz HFRCO	—	38	—	μA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise CCM mode <sup>3</sup> .	I <sub>EM1</sub>	38.4 MHz crystal <sup>2</sup>	—	61	—	μA/MHz
		38 MHz HFRCO	—	45	—	μA/MHz
		26 MHz HFRCO	—	58	—	μA/MHz
Current consumption in EM2 Deep Sleep mode. DCDC in Low Power mode <sup>4</sup> .	I <sub>EM2</sub>	Full RAM retention and RTCC running from LFXO	—	2.5	—	μA
		4 kB RAM retention and RTCC running from LFRCO	—	2.2	—	μA
Current consumption in EM3 Stop mode	I <sub>EM3</sub>	Full RAM retention and CRYO-TIMER running from ULFRCO	—	2.1	—	μA
Current consumption in EM4H Hibernate mode	I <sub>EM4</sub>	128 byte RAM retention, RTCC running from LFXO	—	0.86	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.58	—	μA
		128 byte RAM retention, no RTCC	—	0.58	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S Shutoff mode	$I_{EM4S}$	no RAM retention, no RTCC	—	0.04	—	$\mu\text{A}$

**Note:**

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DCDC voltage.
2. CMU\_HFXOCTRL\_LOWPOWER=0
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DCDC voltage.
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DCDC voltage.

#### 4.1.4.2 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T<sub>OP</sub> = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.5. Current Consumption 3.3 V with DC-DC**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	$I_{RX}$	1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	8.7	—	mA
		802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3	—	9.8	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	$I_{TX}$	F = 2.4 GHz, CW, 0 dBm, Radio clock prescaled by 3	—	8.2	—	mA
		F = 2.4 GHz, CW, 10.5 dBm	—	32.7	—	mA

#### 4.1.5 Wake up times

**Table 4.6. Wake up times**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up from EM2 Deep Sleep	$t_{EM2\_WU}$	Code execution from flash	—	10.7	—	$\mu\text{s}$
		Code execution from RAM	—	3	—	$\mu\text{s}$
Wakeup time from EM1 Sleep	$t_{EM1\_WU}$	Executing from flash	—	3	—	AHB Clocks
		Executing from RAM	—	3	—	AHB Clocks
Wake up from EM3 Stop	$t_{EM3\_WU}$	Executing from flash	—	10.7	—	$\mu\text{s}$
		Executing from RAM	—	3	—	$\mu\text{s}$
Wake up from EM4H Hibernate <sup>1</sup>	$t_{EM4H\_WU}$	Executing from flash	—	60	—	$\mu\text{s}$
Wake up from EM4S Shutoff <sup>1</sup>	$t_{EM4S\_WU}$		—	290	—	$\mu\text{s}$

**Note:**

1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.

#### 4.1.6 Brown Out Detector

For the table below, see [Figure 3.2 MGM111 Power Block on page 9](#) to see the internal connection and relation between DVDD and AVDD. The module itself has only one external power supply input (VDD).

**Table 4.7. Brown Out Detector**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AVDD BOD threshold	V <sub>AVDDBOD</sub>	AVDD rising	—	—	1.85	V
		AVDD falling	1.62	—	—	V
AVDD BOD hysteresis	V <sub>AVDDBOD_HYST</sub>		—	21	—	mV
AVDD response time	t <sub>AVDDBOD_DELAY</sub>	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	V <sub>EM4BOD</sub>	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V <sub>EM4BOD_HYST</sub>		—	46	—	mV
EM4 response time	t <sub>EM4BOD_DELAY</sub>	Supply drops at 0.1V/μs rate	—	300	—	μs

#### 4.1.7 Frequency Synthesizer Characteristics

**Table 4.8. Frequency Synthesizer Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	F <sub>RANGE_2400</sub>	2.4 GHz frequency range	2400	—	2483.5	MHz
LO tuning frequency resolution	F <sub>RES_2400</sub>	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation	ΔF <sub>MAX_2400</sub>		—	—	1677	kHz

#### 4.1.8 2.4 GHz RF Transceiver Characteristics

##### 4.1.8.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:  $T_{OP} = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ . RF center frequency 2.45 GHz. Measurements are conducted from the antenna feed point.

**Table 4.9. RF Transmitter General Characteristics for 2.4 GHz Band**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power	$POUT_{MAX}$		—	+10	—	dBm
Minimum active TX Power	$POUT_{MIN}$	CW		-30	—	dBm
Output power step size	$POUT_{STEP}$	-5 dBm < Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.85 V < $V_{VDD}$ < 3.3 V using DC-DC converter	—	2.2	—	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR\_T}$	From -40 to +85 °C, DCDC enabled	—	1.5	—	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR\_F}$	Over RF tuning frequency range	—	0.4	—	dB
RF tuning frequency range	$F_{RANGE}$		2400	—	2483.5	MHz

##### 4.1.8.2 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:  $T_{OP} = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ . RF center frequency 2.440 GHz. Measurements are conducted from the antenna feed point.

**Table 4.10. RF Receiver General Characteristics for 2.4 GHz Band**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	$F_{RANGE}$		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm

### 4.1.8.3 RF Receiver Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T=25 °C, VDD = 3.3 V. RF center frequency 2.445 GHz. Measurements are conducted from the antenna feed point.

**Table 4.11. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal <sup>1</sup> . Packet length is 20 octets.	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.	—	-99	—	dBm
		Signal is reference signal. Packet length is 20 octets. DC-DC converter in bypass mode.	—	-99	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 10 dB above sensitivity limit	—	-2.6	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>	ACR <sub>+1</sub>	Interferer is reference signal at +1 channel-spacing.	—	33.75	—	dB
		Interferer is filtered reference signal <sup>3</sup> at +1 channel-spacing.	—	52.2	—	dB
		Interferer is CW at +1 channel-spacing. <sup>4</sup>	—	58.6	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>	ACR <sub>-1</sub>	Interferer is reference signal at -1 channel-spacing.	—	35	—	dB
		Interferer is filtered reference signal <sup>3</sup> at -1 channel-spacing.	—	54.7	—	dB
		Interferer is CW at -1 channel-spacing.	—	60.1	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>	ACR <sub>2</sub>	Interferer is reference signal at ±2 channel-spacing	—	45.9	—	dB
		Interferer is filtered reference signal <sup>3</sup> at ±2 channel-spacing	—	56.8	—	dB
		Interferer is CW at ±2 channel-spacing	—	65.5	—	dB
Image rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>	IR	Interferer is CW in image band <sup>4</sup>	—	49.3	—	dB
Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup> . Interferer is reference signal.	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	57.2	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	57.9	—	dB
Blocking rejection of 802.11g signal centered at +12MHz or -13MHz	BLOCK <sub>80211G</sub>	Desired is reference signal at 6dB above reference sensitivity level <sup>2</sup>	—	51.6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	RSSI <sub>MAX</sub>		5	—	—	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI <sub>MIN</sub>		—	—	-98	dBm
RSSI resolution	RSSI <sub>RES</sub>	over RSSI <sub>MIN</sub> to RSSI <sub>MAX</sub>	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2003	RSSI <sub>LIN</sub>		—	±1	—	dB

**Note:**

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s
2. Reference sensitivity level is -85 dBm
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stop-band rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ±5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

Not Recommended for New Designs

## 4.1.9 Oscillators

### 4.1.9.1 LFXO

Table 4.12. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	$f_{LFXO}$		—	32.768	—	kHz
Crystal Frequency Tolerance			-100		+100	ppm

### 4.1.9.2 HFXO

Table 4.13. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	$f_{HFXO}$		—	38.4	—	MHz
Crystal Frequency Tolerance			-40		+40	ppm

### 4.1.9.3 LFRCO

Table 4.14. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	$f_{LFRCO}$	ENVREF = 1 in CMU_LFRCCOCTRL	30.474	32.768	34.243	kHz
		ENVREF = 0 in CMU_LFRCCOCTRL	30.474	32.768	33.915	kHz
Startup time	$t_{LFRCO}$		—	500	—	$\mu$ s
Current consumption <sup>1</sup>	$I_{LFRCO}$	ENVREF = 1 in CMU_LFRCCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCCOCTRL	—	494	—	nA

**Note:**

1. Block is supplied by VDD if ANASW = 0, or DCDC if ANASW=1 in EMU\_PWRCTRL register

#### 4.1.9.4 HFRCO and AUXHFRCO

**Table 4.15. HFRCO and AUXHFRCO**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	$f_{\text{HFRCO}}$	Any frequency band, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	$t_{\text{HFRCO}}$	$f_{\text{HFRCO}} \geq 19 \text{ MHz}$	—	300	—	ns
		$4 < f_{\text{HFRCO}} < 19 \text{ MHz}$	—	1	—	$\mu\text{s}$
		$f_{\text{HFRCO}} \leq 4 \text{ MHz}$	—	2.5	—	$\mu\text{s}$
Current consumption on all supplies	$I_{\text{HFRCO}}$	$f_{\text{HFRCO}} = 38 \text{ MHz}$	—	204	228	$\mu\text{A}$
		$f_{\text{HFRCO}} = 32 \text{ MHz}$	—	171	190	$\mu\text{A}$
		$f_{\text{HFRCO}} = 26 \text{ MHz}$	—	147	164	$\mu\text{A}$
		$f_{\text{HFRCO}} = 19 \text{ MHz}$	—	126	138	$\mu\text{A}$
		$f_{\text{HFRCO}} = 16 \text{ MHz}$	—	110	120	$\mu\text{A}$
		$f_{\text{HFRCO}} = 13 \text{ MHz}$	—	100	110	$\mu\text{A}$
		$f_{\text{HFRCO}} = 7 \text{ MHz}$	—	81	91	$\mu\text{A}$
		$f_{\text{HFRCO}} = 4 \text{ MHz}$	—	33	35	$\mu\text{A}$
		$f_{\text{HFRCO}} = 2 \text{ MHz}$	—	31	35	$\mu\text{A}$
		$f_{\text{HFRCO}} = 1 \text{ MHz}$	—	30	35	$\mu\text{A}$
Step size	$SS_{\text{HFRCO}}$	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	$PJ_{\text{HFRCO}}$		—	0.2	—	% RMS

#### 4.1.9.5 ULFRCO

**Table 4.16. ULFRCO**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	$f_{\text{ULFRCO}}$		0.95	1	1.07	kHz

#### 4.1.10 Flash Memory Characteristics

**Table 4.17. Flash Memory Characteristics<sup>1</sup>**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC <sub>FLASH</sub>		10000	—	—	cycles
Flash data retention	RET <sub>FLASH</sub>		10	—	—	years
Word (32-bit) programming time	t <sub>w_PROG</sub>		20	26	40	µs
Page erase time	t <sub>p_ERASE</sub>		20	27	40	ms
Mass erase time	t <sub>m_ERASE</sub>		20	27	40	ms
Device erase time <sup>2</sup>	t <sub>d_ERASE</sub>		—	60	74	ms
Page erase current <sup>3</sup>	I <sub>ERASE</sub>		—	—	3	mA
Mass or Device erase current <sup>3</sup>			—	—	5	mA
Write current <sup>3</sup>	I <sub>WRITE</sub>		—	—	3	mA

**Note:**

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)
- Measured at 25°C

#### 4.1.11 GPIO

Table 4.18. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	$V_{IOIL}$		—	—	$VDD \cdot 0.3$	V
Input high voltage	$V_{IOIH}$		$VDD \cdot 0.7$	—	—	V
Output high voltage relative to VDD	$V_{IOOH}$	Sourcing 3 mA, $VDD \geq 3$ V, DRIVESTRENGTH <sup>1</sup> = WEAK	$VDD \cdot 0.8$	—	—	V
		Sourcing 1.2 mA, $VDD \geq 1.62$ V DRIVESTRENGTH <sup>1</sup> = WEAK	$VDD \cdot 0.6$	—	—	V
		Sourcing 20 mA, $VDD \geq 3$ V, DRIVESTRENGTH <sup>1</sup> = STRONG	$VDD \cdot 0.8$	—	—	V
		Sourcing 8 mA, $VDD \geq 1.62$ V DRIVESTRENGTH <sup>1</sup> = STRONG	$VDD \cdot 0.6$	—	—	V
Output low voltage relative to VDD	$V_{IOOL}$	Sinking 3 mA, $VDD \geq 3$ V, DRIVESTRENGTH <sup>1</sup> = WEAK	—	—	$VDD \cdot 0.2$	V
		Sinking 1.2 mA, $VDD \geq 1.62$ V DRIVESTRENGTH <sup>1</sup> = WEAK	—	—	$VDD \cdot 0.4$	V
		Sinking 20 mA, $VDD \geq 3$ V, DRIVESTRENGTH <sup>1</sup> = STRONG	—	—	$VDD \cdot 0.2$	V
		Sinking 8 mA, $VDD \geq 1.62$ V DRIVESTRENGTH <sup>1</sup> = STRONG	—	—	$VDD \cdot 0.4$	V
Input leakage current	$I_{IOLEAK}$	All GPIO except LFXO pins, $GPIO \leq VDD$	—	0.1	30	nA
		LFXO Pins, $GPIO \leq VDD$	—	0.1	50	nA
Input leakage current on 5VTOL pads above VDD	$I_{5VTOLLEAK}$	$VDD < GPIO \leq VDD + 2$ V	—	3.3	15	$\mu$ A
I/O pin pull-up resistor	$R_{PU}$		30	43	65	k $\Omega$
I/O pin pull-down resistor	$R_{PD}$		30	43	65	k $\Omega$
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		20	25	35	ns
Output fall time, From 70% to 30% of $V_{IO}$	$t_{IOOF}$	$C_L = 50$ pF, DRIVESTRENGTH <sup>1</sup> = STRONG, SLEWRATE <sup>1</sup> = 0x6	—	1.8	—	ns
		$C_L = 50$ pF, DRIVESTRENGTH <sup>1</sup> = WEAK, SLEWRATE <sup>1</sup> = 0x6	—	4.5	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output rise time, From 30% to 70% of $V_{IO}$	$t_{IOOR}$	$C_L = 50$ pF, DRIVESTRENGTH <sup>1</sup> = STRONG, SLEWRATE = 0x6 <sup>1</sup>	—	2.2	—	ns
		$C_L = 50$ pF, DRIVESTRENGTH <sup>1</sup> = WEAK, SLEWRATE <sup>1</sup> = 0x6	—	7.4	—	ns
RESETn low time to ensure pin reset	$T_{RESET}$		100	—	—	ns
<b>Note:</b> 1. In GPIO_Pn_CTRL register						

#### 4.1.12 VMON

Table 4.19. VMON

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VMON Supply Current	$I_{VMON}$	In EM0 or EM1, 1 supply monitored	—	5.8	8.26	$\mu$ A
		In EM0 or EM1, 4 supplies monitored	—	11.8	16.8	$\mu$ A
		In EM2, EM3 or EM4, 1 supply monitored	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored	—	99	—	nA
VMON Loading of Monitored Supply	$I_{SENSE}$	In EM0 or EM1	—	2	—	$\mu$ A
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	$V_{VMON\_RANGE}$		1.62	—	3.4	V
Threshold step size	$N_{VMON\_STESP}$	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	$t_{VMON\_RES}$	Supply drops at 1V/ $\mu$ s rate	—	460	—	ns
Hysteresis	$V_{VMON\_HYST}$		—	26	—	mV

4.1.13 ADC

Table 4.20. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	V <sub>RESOLUTION</sub>		6	—	12	Bits
Input voltage range	V <sub>ADCIN</sub>	Single ended	0	—	2*V <sub>REF</sub>	V
		Differential	-V <sub>REF</sub>	—	V <sub>REF</sub>	V
Input range of external reference voltage, single ended and differential	V <sub>ADCREFIN_P</sub>		1	—	V <sub>AVDD</sub>	V
Power supply rejection <sup>1</sup>	PSRR <sub>ADC</sub>	At DC	—	80	—	dB
Analog input common mode rejection ratio	CMRR <sub>ADC</sub>	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE <sup>2</sup> = KEEPADC-WARM	I <sub>ADC_CONTINUOUS_LP</sub>	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sup>3</sup>	—	301	350	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 <sup>3</sup>	—	149	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 <sup>3</sup>	—	91	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE <sup>2</sup> = NORMAL	I <sub>ADC_NORMAL_LP</sub>	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sup>3</sup>	—	51	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 <sup>3</sup>	—	9	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE <sup>2</sup> = KEEPINSTANDBY or KEEPINSLOWACC	I <sub>ADC_STANDBY_LP</sub>	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sup>3</sup>	—	117	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sup>3</sup>	—	79	—	μA
Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE <sup>2</sup> = KEEPADC-WARM	I <sub>ADC_CONTINUOUS_HP</sub>	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 <sup>3</sup>	—	345	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 <sup>3</sup>	—	191	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 <sup>3</sup>	—	132	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE <sup>2</sup> = NORMAL	I <sub>ADC_NORMAL_HP</sub>	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>	—	102	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>	—	17	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE <sup>2</sup> = KEEPINSTANDBY or KEEPINSLOWACC	I <sub>ADC_STANDBY_HP</sub>	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>	—	162	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>	—	123	—	μA
Current from HFPERCLK	I <sub>ADC_CLK</sub>	HFPERCLK = 16 MHz	—	140	—	μA
ADC Clock Frequency	f <sub>ADCCLK</sub>		—	—	16	MHz
Throughput rate	f <sub>ADCRATE</sub>		—	—	1	MSPS
Conversion time <sup>4</sup>	t <sub>ADCCONV</sub>	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	t <sub>ADCSTART</sub>	WARMUPMODE <sup>2</sup> = NORMAL	—	—	5	μs
		WARMUPMODE <sup>2</sup> = KEEPINSTANDBY	—	—	2	μs
		WARMUPMODE <sup>2</sup> = KEEPINSLOWACC	—	—	1	μs
SNDR at 1MSPS and f <sub>in</sub> = 10kHz	SNDR <sub>ADC</sub>	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	58	67	—	dB
		v <sub>refp_in</sub> = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	SFDR <sub>ADC</sub>	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V <sub>REF_NOISE</sub>	Including quantization noise and distortion	—	380	—	μV
Offset Error	V <sub>ADCOFFSETERR</sub>		-3	0.25	3	LSB
Gain error in ADC	V <sub>ADC_GAIN</sub>	Using internal reference	—	-0.2	5	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL <sub>ADC</sub>	12 bit resolution	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL <sub>ADC</sub>	12 bit resolution	-6	—	6	LSB
Temperature Sensor Slope	V <sub>TS_SLOPE</sub>		—	-1.84	—	mV/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Note:</b>						
1. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL						
2. In ADCn_CNTL register						
3. In ADCn_BIASPROG register						
4. Derived from ADCCLK						

Not Recommended for New Designs

4.1.14 IDAC

Table 4.21. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of Ranges	N <sub>IDAC_RANGES</sub>		—	4	—	-
Output Current	I <sub>IDAC_OUT</sub>	RANGSEL <sup>1</sup> = RANGE0	0.05	—	1.6	μA
		RANGSEL <sup>1</sup> = RANGE1	1.6	—	4.7	μA
		RANGSEL <sup>1</sup> = RANGE2	0.5	—	16	μA
		RANGSEL <sup>1</sup> = RANGE3	2	—	64	μA
Linear steps within each range	N <sub>IDAC_STEPS</sub>		—	32	—	
Step size	SS <sub>IDAC</sub>	RANGSEL <sup>1</sup> = RANGE0	—	50	—	nA
		RANGSEL <sup>1</sup> = RANGE1	—	100	—	nA
		RANGSEL <sup>1</sup> = RANGE2	—	500	—	nA
		RANGSEL <sup>1</sup> = RANGE3	—	2	—	μA
Total Accuracy, STEPSEL <sup>1</sup> = 0x10	ACC <sub>IDAC</sub>	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-2	—	2	%
		EM0 or EM1	-18	—	22	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t <sub>IDAC_SU</sub>	Output within 1% of steady state value	—	5	—	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value)	$t_{IDAC\_SETTLE}$	Range setting is changed	—	5	—	$\mu s$
		Step value is changed	—	1	—	$\mu s$
Current consumption in EM0 or EM1 <sup>2</sup>	$I_{IDAC}$	Source mode, excluding output current	—	8.9	13	$\mu A$
		Sink mode, excluding output current	—	12	16	$\mu A$
Current consumption in EM2 or EM3 <sup>2</sup>	$I_{IDAC}$	Source mode, excluding output current, duty cycle mode, T = 25 °C	—	1.04	—	$\mu A$
		Sink mode, excluding output current, duty cycle mode, T = 25 °C	—	1.08	—	$\mu A$
		Source mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	8.9	—	$\mu A$
		Sink mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	12	—	$\mu A$
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	$I_{COMP\_SRC}$	RANGESEL1=0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.04	—	%
		RANGESEL1=1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.02	—	%
		RANGESEL1=2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$	—	0.02	—	%
		RANGESEL1=3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$	—	0.02	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	$I_{COMP\_SINK}$	RANGESEL1=0, output voltage = 100 mV	—	0.18	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.08	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.02	—	%

**Note:**

1. In IDAC\_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU\_PWRCTRL register and PWRSEL in the IDAC\_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

#### 4.1.15 Analog Comparator (ACMP)

Table 4.22. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	$V_{ACMPIN}$	CMPVDD = ACMPn_CTRL_PWRSEL <sup>1</sup>	0	—	CMPVDD	V
Supply Voltage	$V_{ACMPVDD}$	BIASPROG <sup>2</sup> ≤ 0x10 or FULL- BIAS <sup>2</sup> = 0	1.85	—	$V_{VDD\_MAX}$	V
		0x10 < BIASPROG <sup>2</sup> ≤ 0x20 and FULLBIAS <sup>2</sup> = 1	2.1	—	$V_{VDD\_MAX}$	V
Active current not including voltage reference	$I_{ACMP}$	BIASPROG <sup>2</sup> = 0x10, FULLBIAS <sup>2</sup> = 0	—	306	—	nA
		BIASPROG <sup>2</sup> = 0x20, FULLBIAS <sup>2</sup> = 1	—	74	95	μA
Current consumption of internal voltage reference	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1	—	2.4	—	μA
Hysteresis ( $V_{CM} = 1.25$ V, BIASPROG <sup>2</sup> = 0x10, FULL- BIAS <sup>2</sup> = 1)	$V_{ACMPHYST}$	HYSTSEL <sup>3</sup> = HYST0	-1.75	0	1.75	mV
		HYSTSEL <sup>3</sup> = HYST1	10	18	26	mV
		HYSTSEL <sup>3</sup> = HYST2	21	32	46	mV
		HYSTSEL <sup>3</sup> = HYST3	27	44	63	mV
		HYSTSEL <sup>3</sup> = HYST4	32	55	80	mV
		HYSTSEL <sup>3</sup> = HYST5	38	65	100	mV
		HYSTSEL <sup>3</sup> = HYST6	43	77	121	mV
		HYSTSEL <sup>3</sup> = HYST7	47	86	148	mV
		HYSTSEL <sup>3</sup> = HYST8	-4	0	4	mV
		HYSTSEL <sup>3</sup> = HYST9	-27	-18	-10	mV
		HYSTSEL <sup>3</sup> = HYST10	-47	-32	-18	mV
		HYSTSEL <sup>3</sup> = HYST11	-64	-43	-27	mV
		HYSTSEL <sup>3</sup> = HYST12	-78	-54	-32	mV
		HYSTSEL <sup>3</sup> = HYST13	-93	-64	-37	mV
		HYSTSEL <sup>3</sup> = HYST14	-113	-74	-42	mV
HYSTSEL <sup>3</sup> = HYST15	-135	-85	-47	mV		

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparator delay <sup>4</sup>	t <sub>ACMPDELAY</sub>	BIASPROG <sup>2</sup> = 0x10, FULLBIAS <sup>2</sup> = 0	—	3.7	—	μs
		BIASPROG <sup>2</sup> = 0x20, FULLBIAS <sup>2</sup> = 1	—	35	—	ns
Offset voltage	V <sub>ACMPOFFSET</sub>	BIASPROG <sup>2</sup> = 0x10, FULLBIAS <sup>2</sup> = 1	-35	—	35	mV
Reference Voltage	V <sub>ACMPREF</sub>	Internal 1.25 V reference	1	1.25	1.47	V
		Internal 2.5 V reference	2	2.5	2.8	V
Capacitive Sense Internal Resistance	R <sub>CSRES</sub>	CSRESSEL <sup>5</sup> = 0	—	inf	—	kΩ
		CSRESSEL <sup>5</sup> = 1	—	15	—	kΩ
		CSRESSEL <sup>5</sup> = 2	—	27	—	kΩ
		CSRESSEL <sup>5</sup> = 3	—	39	—	kΩ
		CSRESSEL <sup>5</sup> = 4	—	51	—	kΩ
		CSRESSEL <sup>5</sup> = 5	—	102	—	kΩ
		CSRESSEL <sup>5</sup> = 6	—	164	—	kΩ
		CSRESSEL <sup>5</sup> = 7	—	239	—	kΩ

**Note:**

1. CMPVDD is a supply chosen by the setting in ACMPn\_CTRL\_PWRSEL and may be VDD or DCDC.
2. In ACMPn\_CTRL register.
3. In ACMPn\_HYSTERESIS register.
4. ±100 mV differential drive.
5. In ACMPn\_INPUTSEL register.

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

I<sub>ACMPREF</sub> is zero if an external voltage reference is used.

4.1.16 I2C

I2C Standard-mode (Sm)

Table 4.23. I2C Standard-mode (Sm)<sup>1</sup>

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency <sup>2</sup>	f <sub>SCL</sub>		0	—	100	kHz
SCL clock low time	t <sub>LOW</sub>		4.7	—	—	μs
SCL clock high time	t <sub>HIGH</sub>		4	—	—	μs
SDA set-up time	t <sub>SU,DAT</sub>		250	—	—	ns
SDA hold time <sup>3</sup>	t <sub>HD,DAT</sub>		100	—	3450	ns
Repeated START condition set-up time	t <sub>SU,STA</sub>		4.7	—	—	μs
(Repeated) START condition hold time	t <sub>HD,STA</sub>		4	—	—	μs
STOP condition set-up time	t <sub>SU,STO</sub>		4	—	—	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>		4.7	—	—	μs

**Note:**

1. For CLHR set to 0 in the I2Cn\_CTRL register
2. For the minimum HPPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time (t<sub>HD,DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>)

**I2C Fast-mode (Fm)**

**Table 4.24. I2C Fast-mode (Fm)<sup>1</sup>**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency <sup>2</sup>	f <sub>SCL</sub>		0	—	400	kHz
SCL clock low time	t <sub>LOW</sub>		1.3	—	—	μs
SCL clock high time	t <sub>HIGH</sub>		0.6	—	—	μs
SDA set-up time	t <sub>SU,DAT</sub>		100	—	—	ns
SDA hold time <sup>3</sup>	t <sub>HD,DAT</sub>		100	—	900	ns
Repeated START condition set-up time	t <sub>SU,STA</sub>		0.6	—	—	μs
(Repeated) START condition hold time	t <sub>HD,STA</sub>		0.6	—	—	μs
STOP condition set-up time	t <sub>SU,STO</sub>		0.6	—	—	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>		1.3	—	—	μs

**Note:**

1. For CLHR set to 1 in the I2Cn\_CTRL register
2. For the minimum HPPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time (t<sub>HD,DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>)

**I2C Fast-mode Plus (Fm+)**

**Table 4.25. I2C Fast-mode Plus (Fm+)<sup>1</sup>**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency <sup>2</sup>	f <sub>SCL</sub>		0	—	1000	kHz
SCL clock low time	t <sub>LOW</sub>		0.5	—	—	μs
SCL clock high time	t <sub>HIGH</sub>		0.26	—	—	μs
SDA set-up time	t <sub>SU,DAT</sub>		50	—	—	ns
SDA hold time	t <sub>HD,DAT</sub>		100	—	—	ns
Repeated START condition set-up time	t <sub>SU,STA</sub>		0.26	—	—	μs
(Repeated) START condition hold time	t <sub>HD,STA</sub>		0.26	—	—	μs
STOP condition set-up time	t <sub>SU,STO</sub>		0.26	—	—	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>		0.5	—	—	μs

**Note:**

1. For CLHR set to 0 or 1 in the I2Cn\_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual

4.1.17 USART SPI

SPI Master Timing

Table 4.26. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period <sup>1 2</sup>	$t_{SCLK}$		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI <sup>1 2</sup>	$t_{CS\_MO}$		0	—	8	ns
SCLK to MOSI <sup>1 2</sup>	$t_{SCLK\_MO}$		3	—	20	ns
MISO setup time <sup>1 2</sup>	$t_{SU\_MI}$	VDD = 3.0 V	37	—	—	ns
MISO hold time <sup>1 2</sup>	$t_{H\_MI}$		6	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V<sub>DD</sub> (figure shows 50% of V<sub>DD</sub>)

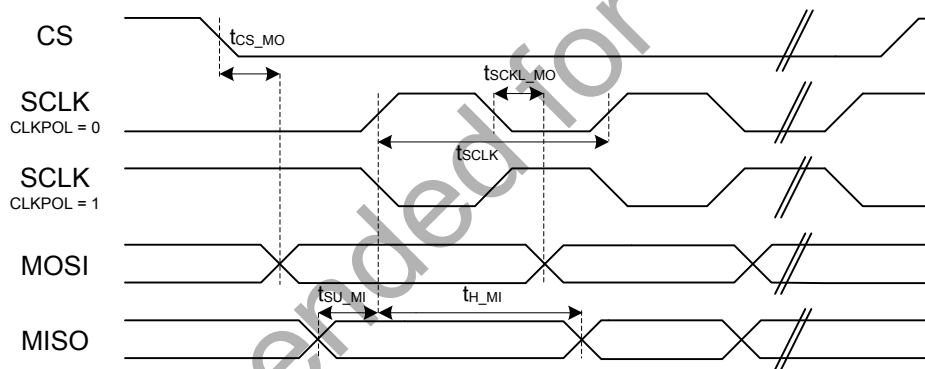


Figure 4.1. SPI Master Timing Diagram (SMSDELAY = 0)

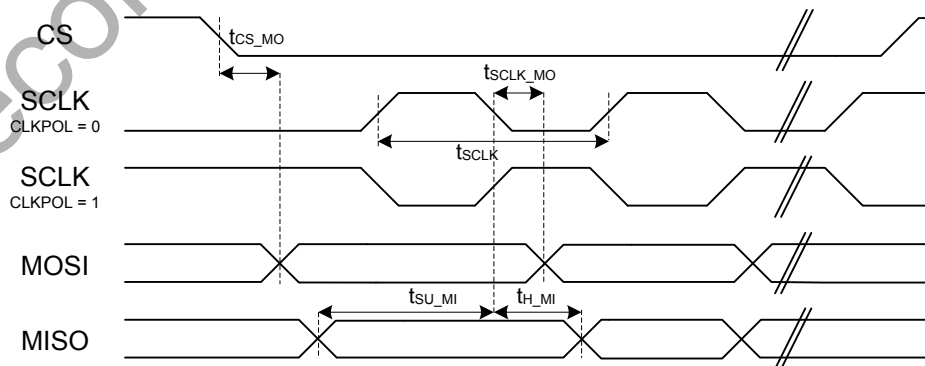


Figure 4.2. SPI Master Timing Diagram (SMSDELAY = 1)

SPI Slave Timing

Table 4.27. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCKL period <sup>1 2</sup>	$t_{SCLK\_sl}$		2 *	—	—	ns
SCLK high period <sup>1 2</sup>	$t_{SCLK\_hi}$		3 *	—	—	ns
SCLK low period <sup>1 2</sup>	$t_{SCLK\_lo}$		3 *	—	—	ns
CS active to MISO <sup>1 2</sup>	$t_{CS\_ACT\_MI}$		4	—	50	ns
CS disable to MISO <sup>1 2</sup>	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time <sup>1 2</sup>	$t_{SU\_MO}$		4	—	—	ns
MOSI hold time <sup>1 2</sup>	$t_{H\_MO}$		3 + 2 *	—	—	ns
SCLK to MISO <sup>1 2</sup>	$t_{SCLK\_MI}$		16 +	—	66 + 2 *	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of  $V_{DD}$  (figure shows 50% of  $V_{DD}$ )

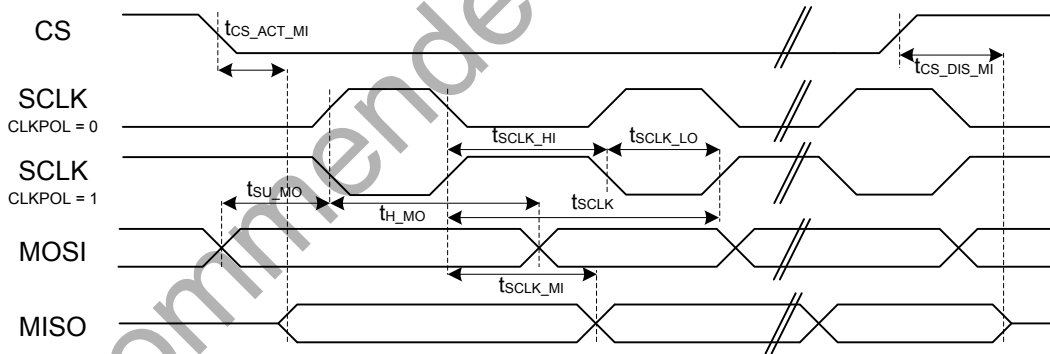


Figure 4.3. SPI Slave Timing Diagram

## 5. Typical Connection Diagrams

### 5.1 Network Co-Processor (NCP) Application with UART Host

The MGM111 can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug, and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

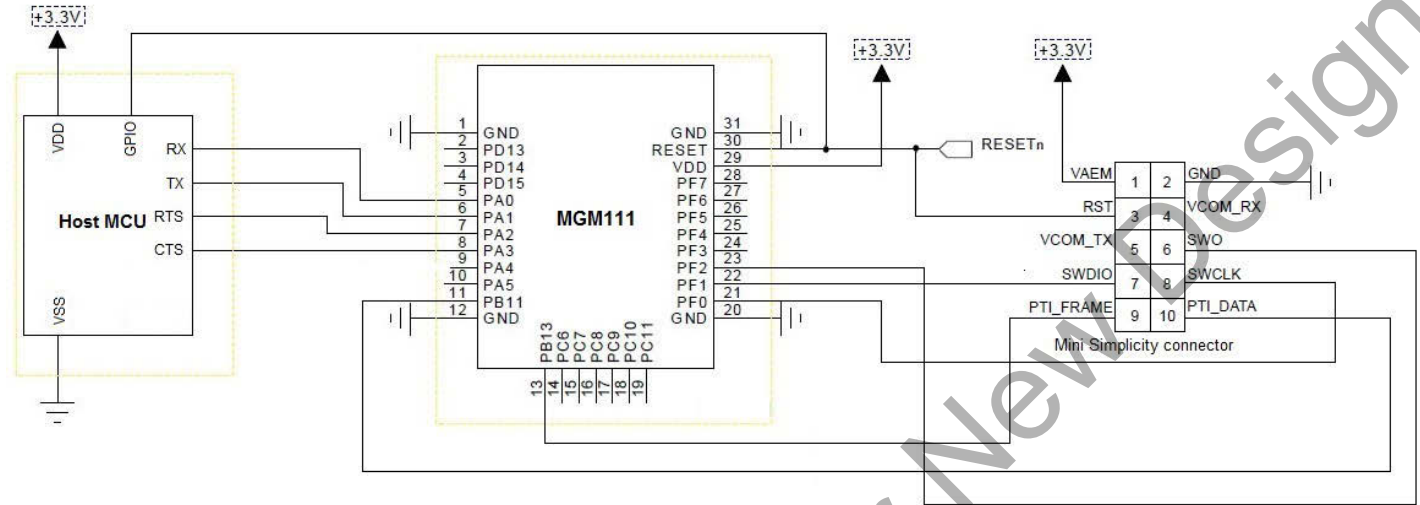


Figure 5.1. Connection Diagram: UART NCP Configuration

### 5.2 Network Co-Processor (NCP) Application with SPI Host

The MGM111 can be controlled over the SPI interface as a peripheral to an external host processor. Typical power supply, programming/debug and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

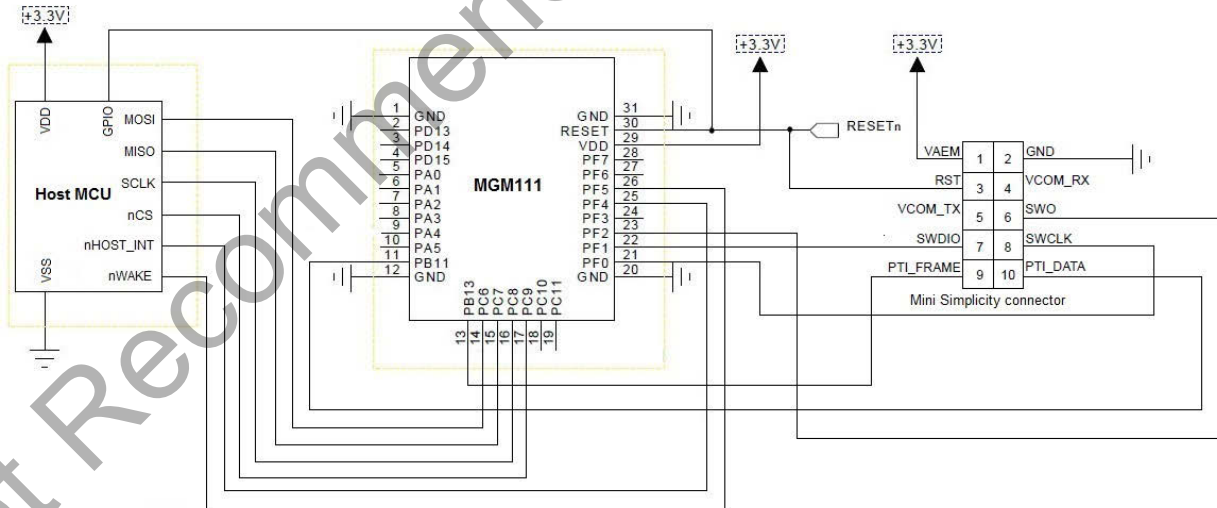


Figure 5.2. Connection Diagram: SPI NCP Configuration

### 5.3 SoC Application

The MGM111 can be used in a standalone SoC configuration with no external host processor. Typical power supply and programming/debug connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details. Refer to *AN772: Using the Application Bootloader* for recommendations on supported serial flash ICs (optional).

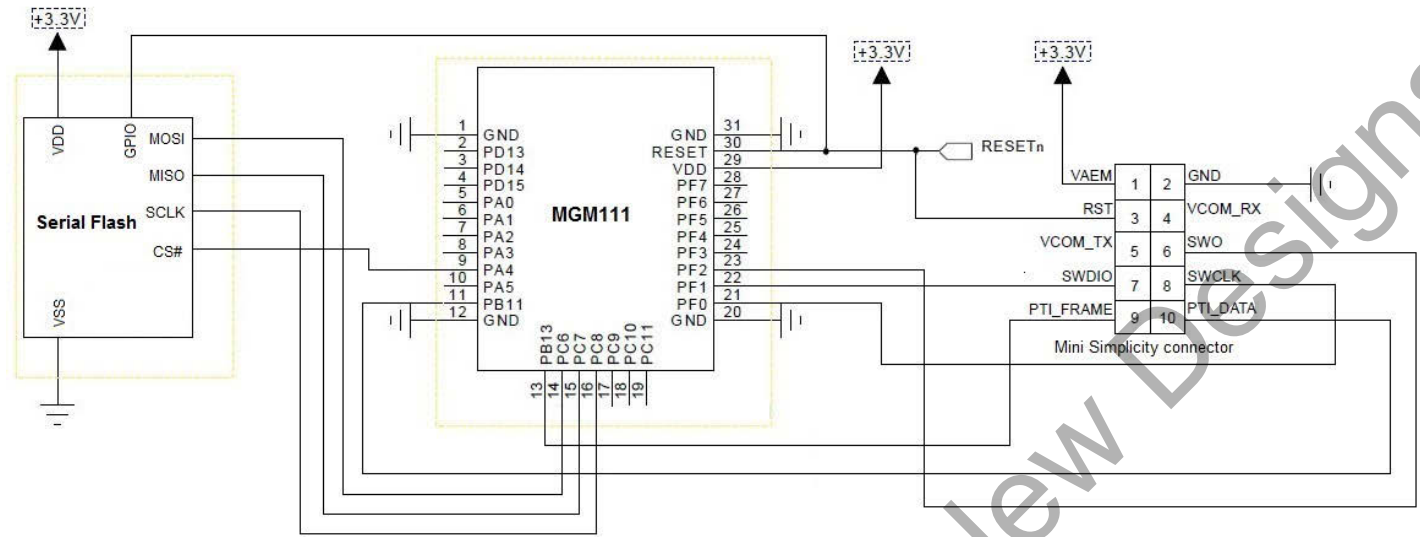


Figure 5.3. Connection Diagram: SoC Configuration

## 6. Layout Guidelines

For optimal performance of the MGM111A (with intergrated antenna), please follow the PCB layout guidelines and ground plane recommendations indicated in this section.

### 6.1 Module Placement and Application PCB Layout Guidelines

- Place the module at the edge of the PCB, as shown in the figure below.
- Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna (shown in the figure below).
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Do not place plastic or any other dielectric material in touch with the antenna.

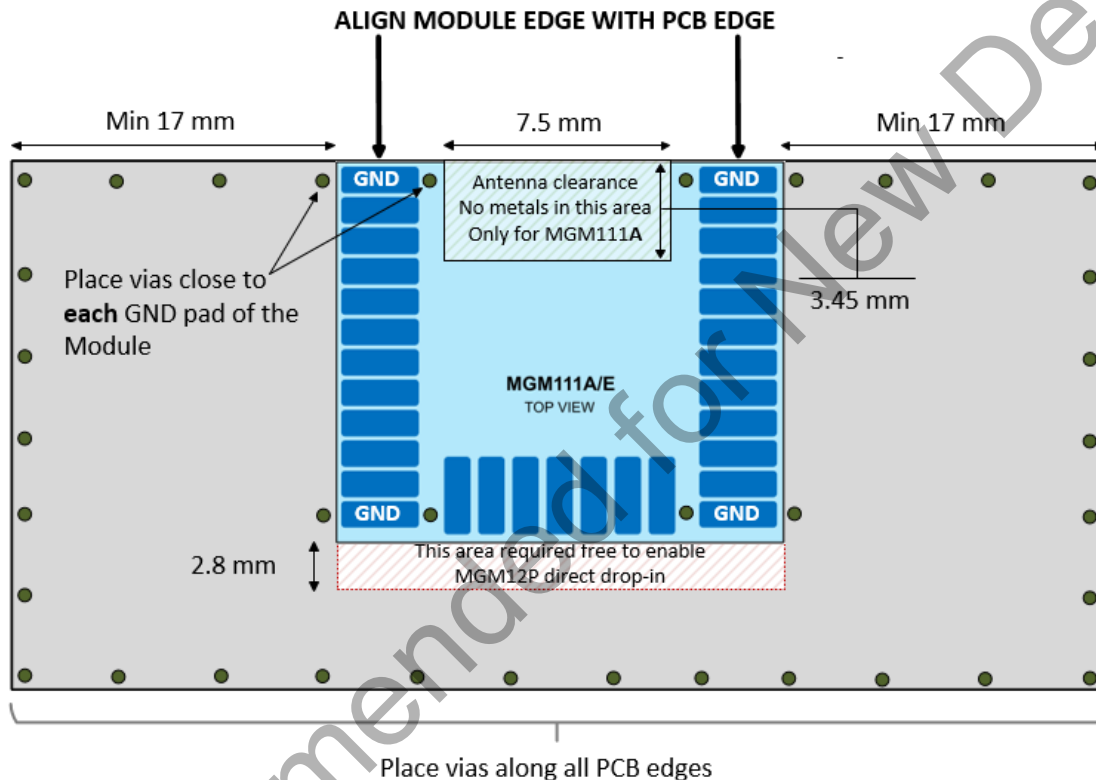
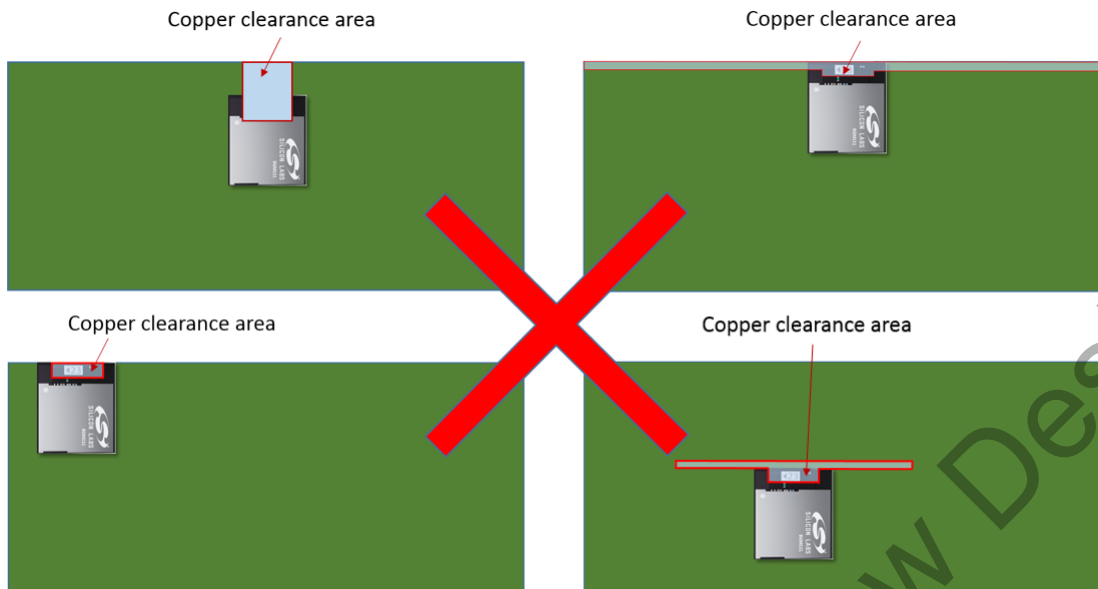
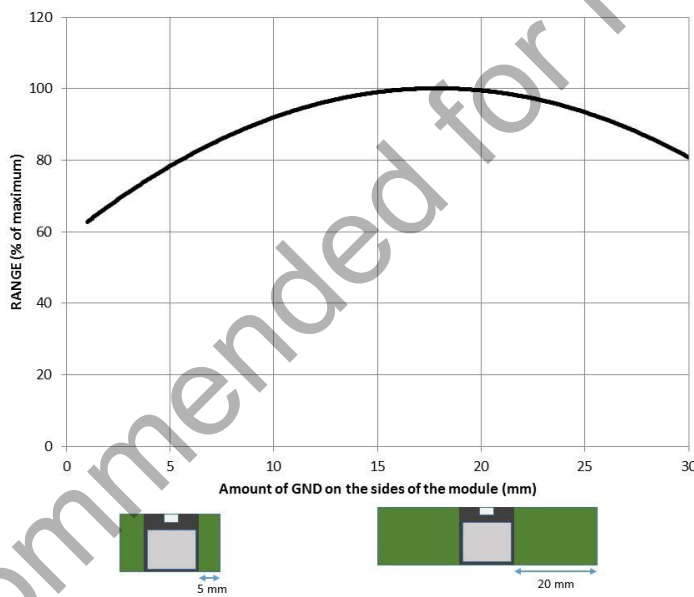


Figure 6.1. Recommended Application PCB Layout for MGM111A

The layouts in the next figure will result in severely degraded RF-performance.



**Figure 6.2. Non-optimal Module Placements for MGM111A**



**Figure 6.3. Impact of GND Plane Size vs. Range for MGM111A**

### 6.2 Effect of Plastic and Metal Materials

Do not place plastic or any other dielectric material in close proximity to the antenna.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

### 6.3 Locating the Module Close to Human Body

Placing the module in touch or very close to the human body will negatively impact antenna efficiency and reduce range.

## 6.4 2D Radiation Pattern Plots

### 2D pattern, front view

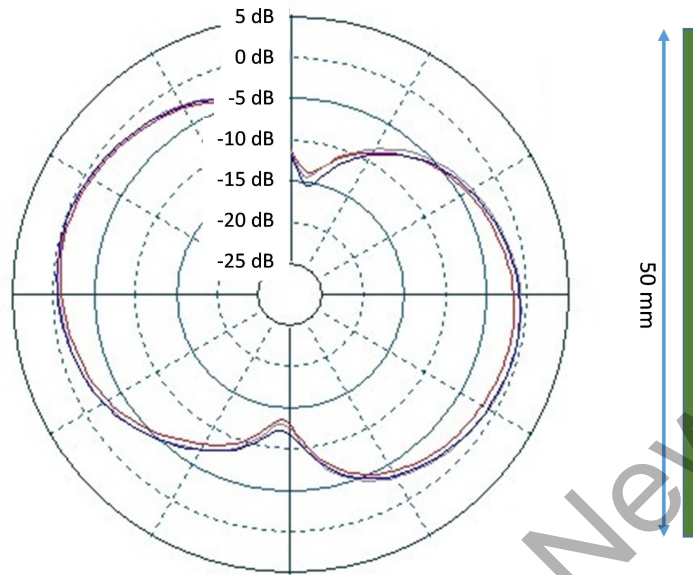


Figure 6.4. Typical 2D Radiation Pattern – Front View

### 2D pattern, side view

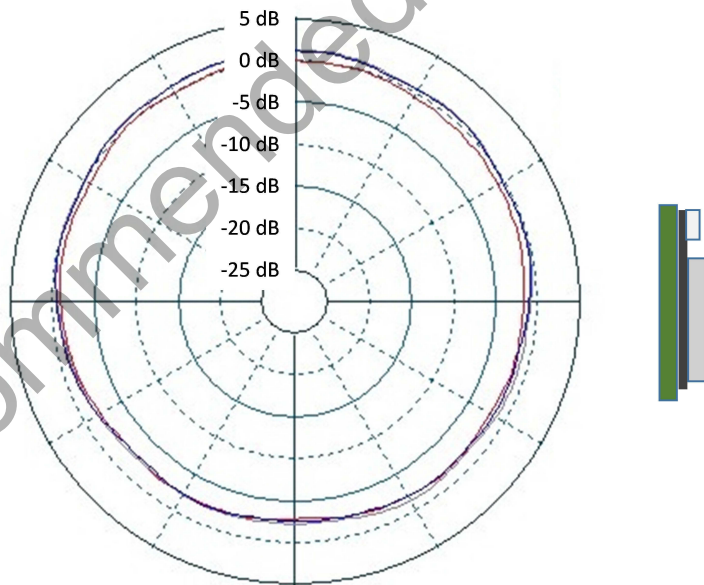


Figure 6.5. Typical 2D Radiation Pattern – Side View

### 2D pattern, top view

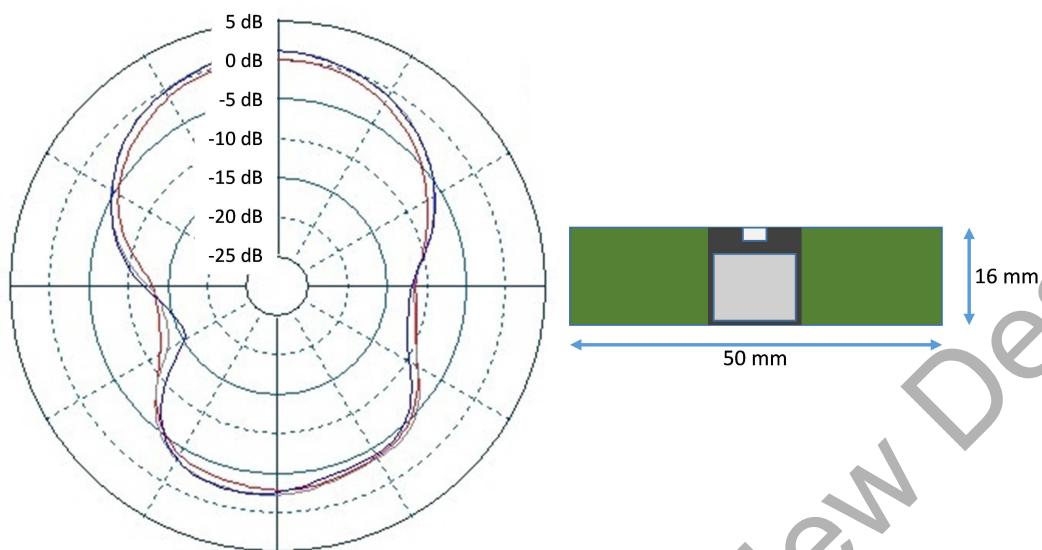


Figure 6.6. Typical 2D Radiation Pattern – Top View

Not Recommended for New Designs

## 7. Hardware Design Guidelines

The MGM111 is an easy-to-use module with regard to hardware application design but certain design guidelines must be followed to guarantee optimal performance. These guidelines are listed in the next sub-sections.

### 7.1 Power Supply Requirements

Coin cell batteries cannot withstand high peak currents (e.g. higher than 15 mA). If the peak current exceeds 15 mA it's recommended to place 47 - 100  $\mu$ F capacitor in parallel with the coin cell battery to improve the battery life time. Notice that the total current consumption of your application is a combination of the radio, peripherals and MCU current consumption so you must take all of these into account. MGM111 should be powered by a unipolar supply voltage with nominal value of 3.3 V.

### 7.2 Reset Functions

The MGM111 can be reset by three different methods: by pulling the RESET line low, by the internal watchdog timer or software command. The reset state in MGM111 does not provide any power saving functionality and thus is not recommended as a means to conserve power. MGM111 has an internal system power-up reset function. The RESET pin includes an on-chip pull-up resistor and can therefore be left unconnected if no external reset switch or source is needed.

### 7.3 Debug and Firmware Updates

This section contains information on debug and firmware update methods. For additional information, refer to the following application note: [AN958: Debugging and Programming Interfaces for Custom Designs](#).

#### 7.3.1 JTAG

It is recommended to expose the JTAG debug pins in your own hardware design for firmware update and debug purposes. The following table lists the required pins for JTAG connection.

The debug pins have pull-down and pull-up enabled by default, so leaving them enabled may increase current consumption if left connected to supply or ground. If enabling the JTAG pins the module must be power cycled to enable a SWD debug session.

Table 7.1. JTAG Pads

PAD NAME	PAD NUMBER	JTAG SIGNAL NAME	COMMENTS
PF3	24	TDI	This pin is disabled after reset. Once enabled the pin has a built-in pull-up.
PF2	23	TDO	This pin is disabled after reset
PF1	22	TMS	Pin is enabled after reset and has a built-in pull-up
PF0	21	TCK	Pin is enabled after reset and has a built-in pull-down

#### 7.3.2 Packet Trace Interface (PTI)

The MGM111 integrates a true PHY-level PTI with the MAC, allowing complete, non-intrusive capture of all packets to and from the EFR32 Wireless STK development tools.

## 8. Pin Definitions

### 8.1 Pin Definitions

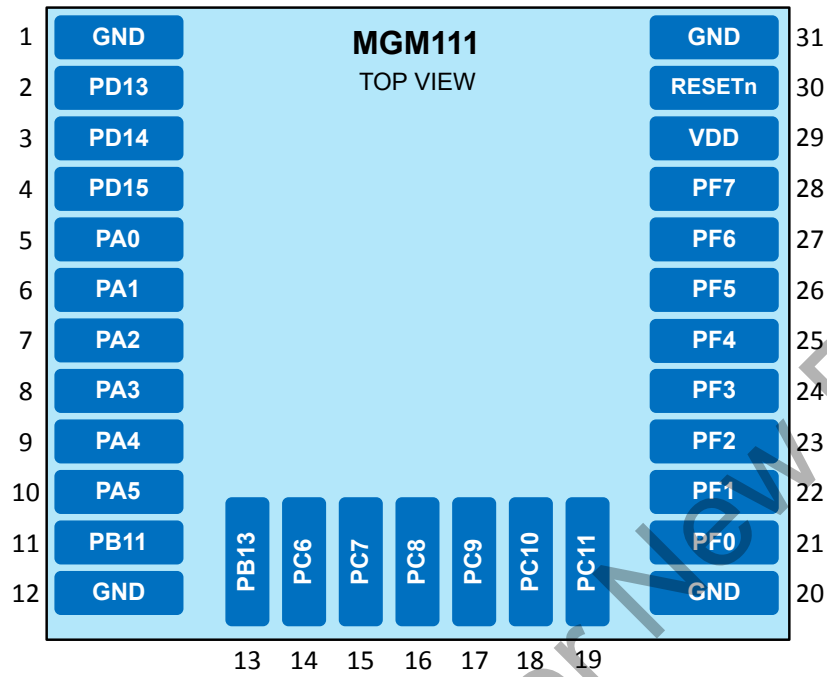


Figure 8.1. MGM111 Pinout

**Table 8.1. Device Pinout**

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
1	GND	Ground				
2	PD13	BUSCY [ADC0: APORT3YCH5 ACMP0: APORT3YCH5 ACMP1: APORT3YCH5 IDAC0: APORT1YCH5]  BUSDX [ADC0: APORT4XCH5 ACMP0: APORT4XCH5 ACMP1: APORT4XCH5]	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MO- DEM_DOUT #19 MODEM_ANT0 #18 MO- DEM_ANT1 #17	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
3	PD14	BUSCX [ADC0: APORT3XCH6 ACMP0: APORT3XCH6 ACMP1: APORT3XCH6 IDAC0: APORT1XCH6]  BUSDY [ADC0: APORT4YCH6 ACMP0: APORT4YCH6 ACMP1: APORT4YCH6]	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MO- DEM_DOUT #20 MODEM_ANT0 #19 MO- DEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4
4	PD15	BUSCY [ADC0: APORT3YCH7 ACMP0: APORT3YCH7 ACMP1: APORT3YCH7 IDAC0: APORT1YCH7]  BUSDX [ADC0: APORT4XCH7 ACMP0: APORT4XCH7 ACMP1: APORT4XCH7]	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE- TIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MO- DEM_DOUT #21 MODEM_ANT0 #20 MO- DEM_ANT1 #19	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
5	PA0	ADC0_EXTN BUSCX [ADC0: APORT3XCH8 ACMP0: APORT3XCH8 ACMP1: APORT3XCH8 IDAC0: APORT1XCH8]  BUSDY [ADC0: APORT4YCH8 ACMP0: APORT4YCH8 ACMP1: APORT4YCH8]	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MO- DEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
6	PA1	ADC0_EXTP BUSCY [ADC0: APORT3YCH9 ACMP0: APORT3YCH9 ACMP1: APORT3YCH9 IDAC0: APORT1YCH9]  BUSDX [ADC0: APORT4XCH9 ACMP0: APORT4XCH9 ACMP1: APORT4XCH9]	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MO- DEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1
7	PA2	BUSCX [ADC0: APORT3XCH10 ACMP0: APORT3XCH10 ACMP1: APORT3XCH10 IDAC0: APORT1XCH10]  BUSDY [ADC0: APORT4YCH10 ACMP0: APORT4YCH10 ACMP1: APORT4YCH10]	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 LE- TIM0_OUT0 #2 LE- TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0 MODEM_ANT0 #31 MO- DEM_ANT1 #30	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
8	PA3	BUSCY [ADC0: APORT3YCH11 ACMP0: APORT3YCH11 ACMP1: APORT3YCH11 IDAC0: APORT1YCH11]  BUSDX [ADC0: APORT4XCH11 ACMP0: APORT4XCH11 ACMP1: APORT4XCH11]	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1 MODEM_ANT0 #0 MODEM_ANT1 #31	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 GPIO_EM4WU8
9	PA4	BUSCX [ADC0: APORT3XCH12 ACMP0: APORT3XCH12 ACMP1: APORT3XCH12 IDAC0: APORT1XCH12]  BUSDY [ADC0: APORT4YCH12 ACMP0: APORT4YCH12 ACMP1: APORT4YCH12]	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 LE- TIM0_OUT0 #4 LE- TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2 MODEM_ANT0 #1 MODEM_ANT1 #0	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4
10	PA5	BUSCY [ADC0: APORT3YCH13 ACMP0: APORT3YCH13 ACMP1: APORT3YCH13 IDAC0: APORT1YCH13]  BUSDX [ADC0: APORT4XCH13 ACMP0: APORT4XCH13 ACMP1: APORT4XCH13]	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 LE- TIM0_OUT0 #5 LE- TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3 MODEM_ANT0 #2 MODEM_ANT1 #1	PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
11	PB11	BUSCY [ADC0: APORT3YCH27 ACMP0: APORT3YCH27 ACMP1: APORT3YCH27 IDAC0: APORT1YCH27]  BUSDX [ADC0: APORT4XCH27 ACMP0: APORT4XCH27 ACMP1: APORT4XCH27]	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
12	GND	Ground				
13	PB13	BUSCY [ADC0: APORT3YCH29 ACMP0: APORT3YCH29 ACMP1: APORT3YCH29 IDAC0: APORT1YCH29]  BUSDX [ADC0: APORT4XCH29 ACMP0: APORT4XCH29 ACMP1: APORT4XCH29]	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
14	PC6	BUSAX [ADC0: APORT1XCH6 ACMP0: APORT1XCH6 ACMP1: APORT1XCH6]  BUSBY [ADC0: APORT2YCH6 ACMP0: APORT2YCH6 ACMP1: APORT2YCH6]	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE- TIM0_OUT0 #11 LETIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MO- DEM_DOUT #9 MODEM_ANT0 #8 MODEM_ANT1 #7	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
15	PC7	BUSAY [ADC0: APORT1YCH7 ACMP0: APORT1YCH7 ACMP1: APORT1YCH7] BUSBX [ADC0: APORT2XCH7 ACMP0: APORT2XCH7 ACMP1: APORT2XCH7]	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE- TIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MO- DEM_DOUT #10 MODEM_ANT0 #9 MODEM_ANT1 #8	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12
16	PC8	BUSAX [ADC0: APORT1XCH8 ACMP0: APORT1XCH8 ACMP1: APORT1XCH8] BUSBY [ADC0: APORT2YCH8 ACMP0: APORT2YCH8 ACMP1: APORT2YCH8]	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE- TIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MO- DEM_DOUT #11 MODEM_ANT0 #10 MO- DEM_ANT1 #9	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13
17	PC9	BUSAY [ADC0: APORT1YCH9 ACMP0: APORT1YCH9 ACMP1: APORT1YCH9] BUSBX [ADC0: APORT2XCH9 ACMP0: APORT2XCH9 ACMP1: APORT2XCH9]	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIM0_OUT0 #14 LETIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MO- DEM_DOUT #12 MODEM_ANT0 #11 MO- DEM_ANT1 #10	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
18	PC10	BUSAX [ADC0: APORT1XCH10 ACMP0: APORT1XCH10 ACMP1: APORT1XCH10]  BUSBY [ADC0: APORT2YCH10 ACMP0: APORT2YCH10 ACMP1: APORT2YCH10]	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDT10 #12 TIM0_CDT11 #11 TIM0_CDT12 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MO- DEM_DOUT #13 MODEM_ANT0 #12 MO- DEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
19	PC11	BUSAY [ADC0: APORT1YCH11 ACMP0: APORT1YCH11 ACMP1: APORT1YCH11]  BUSBX [ADC0: APORT2XCH11 ACMP0: APORT2XCH11 ACMP1: APORT2XCH11]	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDT10 #13 TIM0_CDT11 #12 TIM0_CDT12 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MO- DEM_DOUT #14 MODEM_ANT0 #13 MO- DEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3
20	GND	Ground				
21	PF0	BUSAX [ADC0: APORT1XCH16 ACMP0: APORT1XCH16 ACMP1: APORT1XCH16]  BUSBY [ADC0: APORT2YCH16 ACMP0: APORT2YCH16 ACMP1: APORT2YCH16]	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDT10 #21 TIM0_CDT11 #20 TIM0_CDT12 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MO- DEM_DOUT #22 MODEM_ANT0 #21 MO- DEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
22	PF1	BUSAY [ADC0: APORT1YCH17 ACMP0: APORT1YCH17 ACMP1: APORT1YCH17]  BUSBX [ADC0: APORT2XCH17 ACMP0: APORT2XCH17 ACMP1: APORT2XCH17]	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MO- DEM_DOUT #23 MODEM_ANT0 #22 MO- DEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0
23	PF2	BUSAX [ADC0: APORT1XCH18 ACMP0: APORT1XCH18 ACMP1: APORT1XCH18]  BUSBY [ADC0: APORT2YCH18 ACMP0: APORT2YCH18 ACMP1: APORT2YCH18]	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MO- DEM_DOUT #24 MODEM_ANT0 #23 MO- DEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0
24	PF3	BUSAY [ADC0: APORT1YCH19 ACMP0: APORT1YCH19 ACMP1: APORT1YCH19]  BUSBX [ADC0: APORT2XCH19 ACMP0: APORT2XCH19 ACMP1: APORT2XCH19]	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MO- DEM_DOUT #25 MODEM_ANT0 #24 MO- DEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
25	PF4	BUSAX [ADC0: APORT1XCH20 ACMP0: APORT1XCH20 ACMP1: APORT1XCH20]  BUSBY [ADC0: APORT2YCH20 ACMP0: APORT2YCH20 ACMP1: APORT2YCH20]	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDT10 #25 TIM0_CDT11 #24 TIM0_CDT12 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LETIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MO- DEM_DOUT #26 MODEM_ANT0 #25 MO- DEM_ANT1 #24	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
26	PF5	BUSAY [ADC0: APORT1YCH21 ACMP0: APORT1YCH21 ACMP1: APORT1YCH21]  BUSBX [ADC0: APORT2XCH21 ACMP0: APORT2XCH21 ACMP1: APORT2XCH21]	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDT10 #26 TIM0_CDT11 #25 TIM0_CDT12 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE- TIM0_OUT0 #29 LETIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MO- DEM_DOUT #27 MODEM_ANT0 #26 MO- DEM_ANT1 #25	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29
27	PF6	BUSAX [ADC0: APORT1XCH22 ACMP0: APORT1XCH22 ACMP1: APORT1XCH22]  BUSBY [ADC0: APORT2YCH22 ACMP0: APORT2YCH22 ACMP1: APORT2YCH22]	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDT10 #27 TIM0_CDT11 #26 TIM0_CDT12 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE- TIM0_OUT0 #30 LETIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	FRC_DCLK #30 FRC_DOUT #29 FRC_DFRAME #28 MODEM_DCLK #30 MODEM_DIN #29 MO- DEM_DOUT #28 MODEM_ANT0 #27 MO- DEM_ANT1 #26	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30

MGM111		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
28	PF7	BUSAY [ADC0: APORT1YCH23 ACMP0: APORT1YCH23 ACMP1: APORT1YCH23]  BUSBX [ADC0: APORT2XCH23 ACMP0: APORT2XCH23 ACMP1: APORT2XCH23]	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDT10 #28 TIM0_CDT11 #27 TIM0_CDT12 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE- TIM0_OUT0 #31 LETIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MO- DEM_DOUT #29 MODEM_ANT0 #28 MO- DEM_ANT1 #27	CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
29	VDD	Module power supply				
30	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
31	GND	Ground				

### 8.1.1 GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port are indicated by a number from 15 down to 0.

Table 8.2. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	PA5 (5V)	PA4	PA3	PA2	PA1	PA0
Port B			PB13		PB11	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	-	-	-	-	-	-
Port D	PD15	PD14	PD13				-	-	-	-	-	-	-	-	-	-
Port E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	PF7 (5V)	PF6 (5V)	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

## 8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 8.3. Alternate Functionality Overview**

Alternate Functionality	LOCATION								Description
	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital out- put.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital out- put.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 ex- ternal reference in- put negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 ex- ternal reference in- put positive pin
CMU_CLK0	0: PA1 2: PC6 3: PC11	5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 2: PC7 3: PC10	5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock.  Note that this func- tion is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data in- put / output and JTAG Test Mode Select.  Note that this func- tion is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output.  Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In.  Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out.  Note that this function is enabled to pin out of reset.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
MODEM_ANT0	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	MODEM antenna control output 0, used for antenna diversity.
MODEM_ANT1	0: PA4 1: PA5 2: PB11	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	MODEM antenna control output 1, used for antenna diversity.
MODEM_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	MODEM data clock out.
MODEM_DIN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	MODEM data in.
MODEM_DOUT	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	MODEM data out.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11  7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2		12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4		4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.
PRS_CH5		4: PD14 5: PD15							Peripheral Reflex System PRS, channel 5.
	3: PD13								
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13	15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11  7: PB13	10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11  6: PB13	9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDT10	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDT11	0: PA4 1: PA5 2: PB11	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDT12	0: PA5 1: PB11 3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US0_CTS	0: PA4 1: PA5 2: PB11	4: PB13  7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11  3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11  7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive.  USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication.  USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11  6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11	4: PB13  7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PA5 1: PB11  3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11  7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive.  USART1 Synchronous mode Master Input / Slave Output (MISO).

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13  11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.  USART1 Synchronous mode Master Output / Slave Input (MOSI).

Not Recommended for New Designs

### 8.3 Analog Port (APORT)

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, and DACs. The APORT consists of wires, switches, and control needed to configurably implement the routes. Please see the device Reference Manual for a complete description.

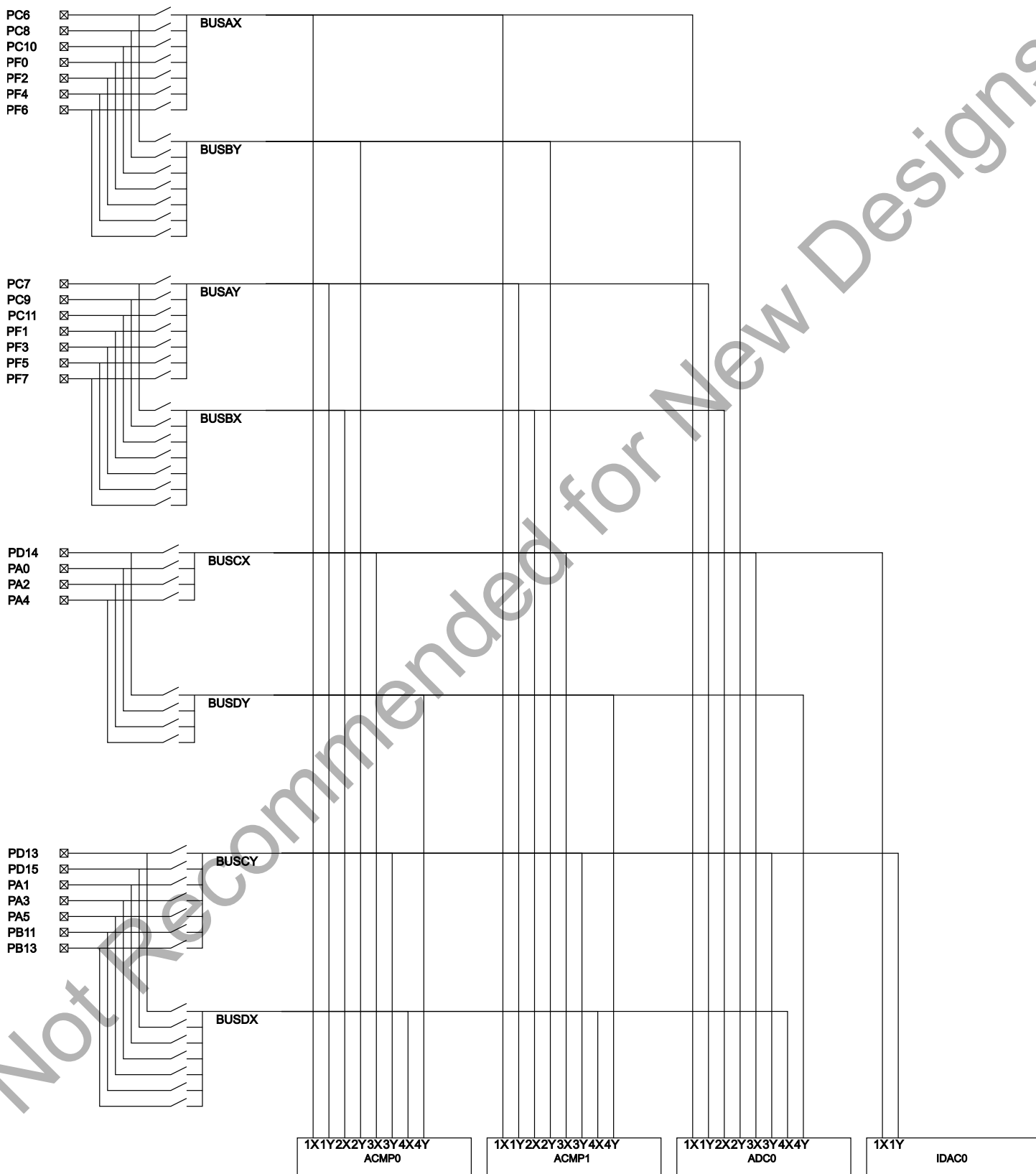


Figure 8.2. MGM111 APORT

**Table 8.4. APORT Client Map**

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP0	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6
ACMP0	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
ACMP0	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
ACMP0	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP0	APORT3XCH2	BUSCX	
	APORT3XCH4		
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		
	APORT3XCH30		
ACMP0	APORT3YCH3	BUSCY	
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		PA3
	APORT3YCH13		PA5
	APORT3YCH27		PB11
	APORT3YCH29		PB13
ACMP0	APORT4XCH3	BUSDX	
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		PA3
	APORT4XCH13		PA5
	APORT4XCH27		PB11
	APORT4XCH29		PB13
ACMP0	APORT4YCH2	BUSDY	
	APORT4YCH4		
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		PA2
	APORT4YCH12		PA4
	APORT4YCH28		
	APORT4YCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP1	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6
ACMP1	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
ACMP1	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
ACMP1	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6
ACMP1	APORT3XCH2	BUSCX	
	APORT3XCH4		
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		
	APORT3XCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP1	APORT3YCH3	BUSCY	
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		PA3
	APORT3YCH13		PA5
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		
ACMP1	APORT4XCH3	BUSDX	
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		PA3
	APORT4XCH13		PA5
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		
ACMP1	APORT4YCH2	BUSDY	
	APORT4YCH4		
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		PA2
	APORT4YCH12		PA4
	APORT4YCH28		
	APORT4YCH30		
ADC0	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6

Analog Module	Analog Module Channel	Shared Bus	Pin
ADC0	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
ADC0	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
ADC0	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6
ADC0	APORT3XCH2	BUSCX	
	APORT3XCH4		
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		
	APORT3XCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
ADC0	APORT3YCH3	BUSCY	
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		PA3
	APORT3YCH13		PA5
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		
ADC0	APORT4XCH3	BUSDX	
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		PA3
	APORT4XCH13		PA5
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		
ADC0	APORT4YCH2	BUSDY	
	APORT4YCH4		
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		PA2
	APORT4YCH12		PA4
	APORT4YCH28		
	APORT4YCH30		
IDAC0	APORT1XCH2	BUSCX	
	APORT1XCH4		
	APORT1XCH6		PD14
	APORT1XCH8		PA0
	APORT1XCH10		PA2
	APORT1XCH12		PA4
	APORT1XCH28		
	APORT1XCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
IDAC0	APORT1YCH3	BUSCY	
	APORT1YCH5		PD13
	APORT1YCH7		PD15
	APORT1YCH9		PA1
	APORT1YCH11		PA3
	APORT1YCH13		PA5
	APORT1YCH27		PB11
	APORT1YCH29		PB13
	APORT1YCH31		

Not Recommended for New Designs

## 9. Package Specifications

### 9.1 MGM111 Dimensions

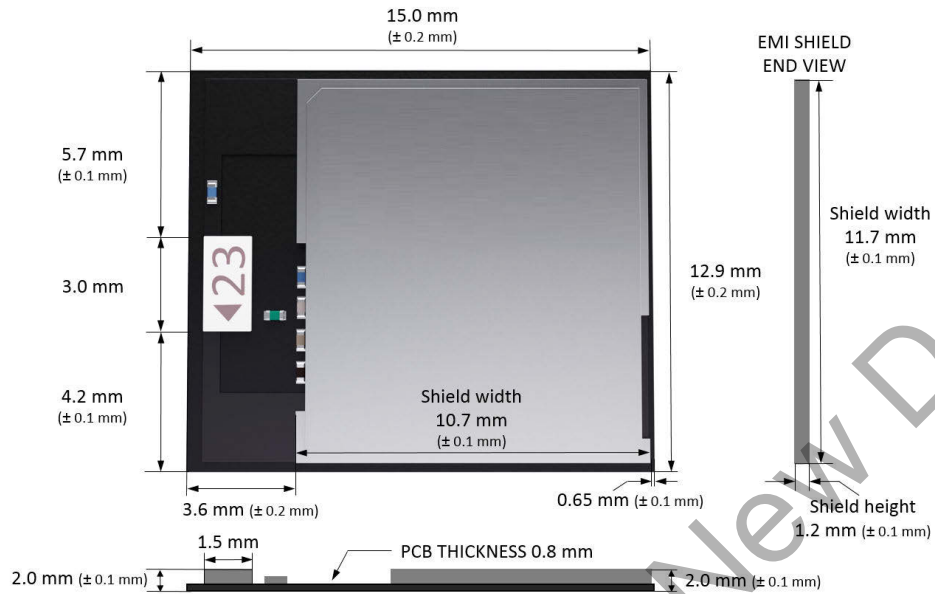


Figure 9.1. MGM111A Package Dimensions

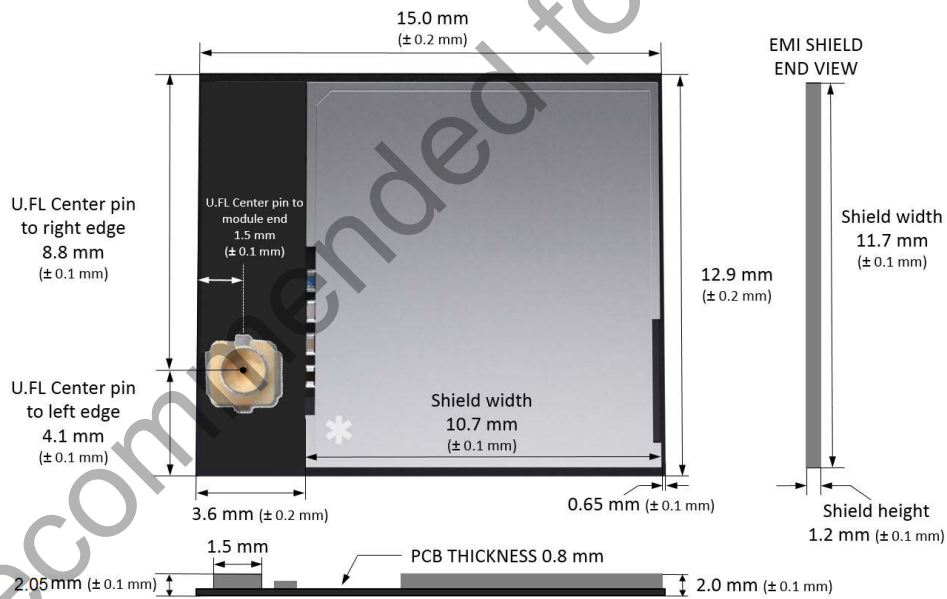


Figure 9.2. MGM111E Package Dimensions

### 9.2 MGM111 Module Footprint

The figure below shows the Module footprint and PCB dimensions.

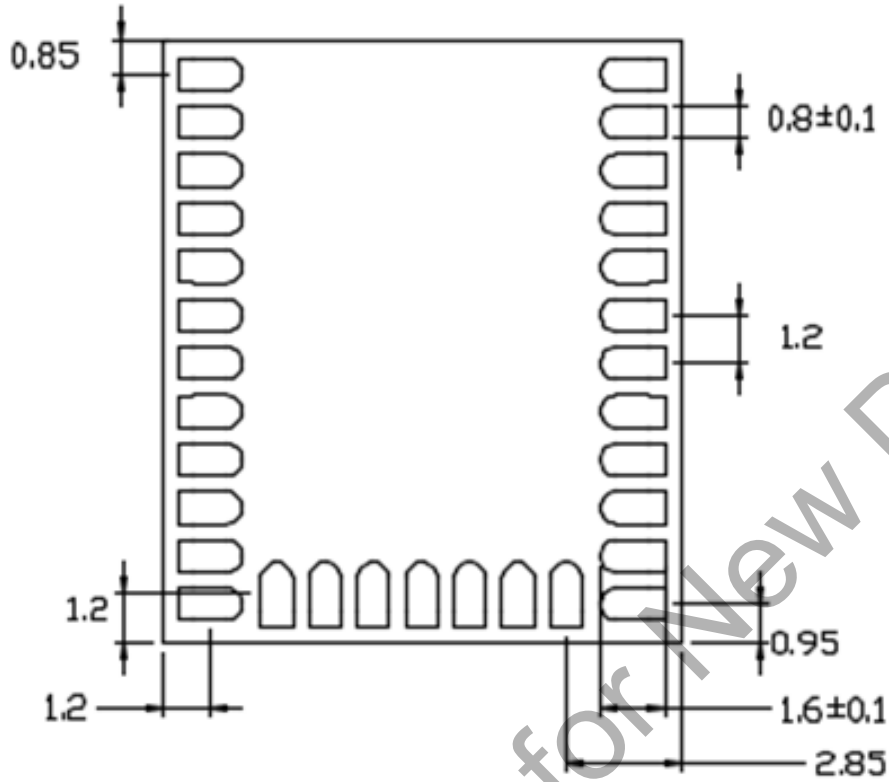


Figure 9.3. MGM111 Footprint

### 9.3 MGM111 Recommended PCB Land Pattern

The figure below shows the recommended land pattern. The antenna clearance section is not required for the MGM111E module.

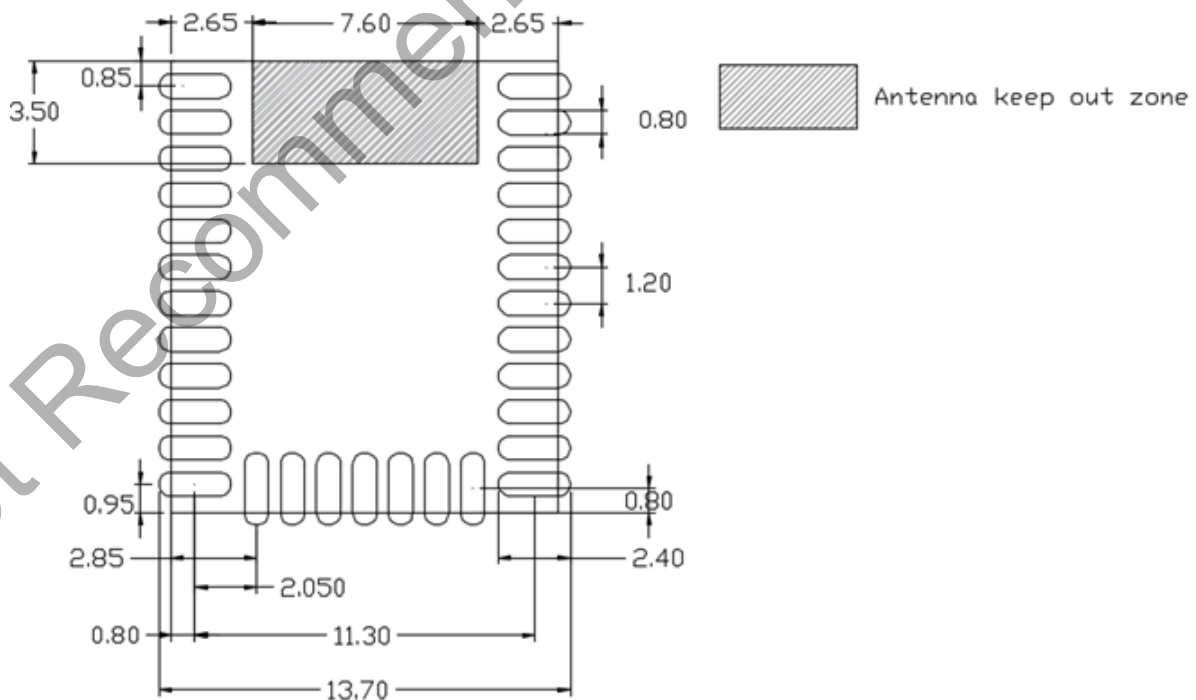


Figure 9.4. MGM111 Recommended PCB Land Pattern

## 9.4 MGM111 Package Marking

The figure below shows the Module markings printed on the RF-shield.



Figure 9.5. MGM111A Package Marking

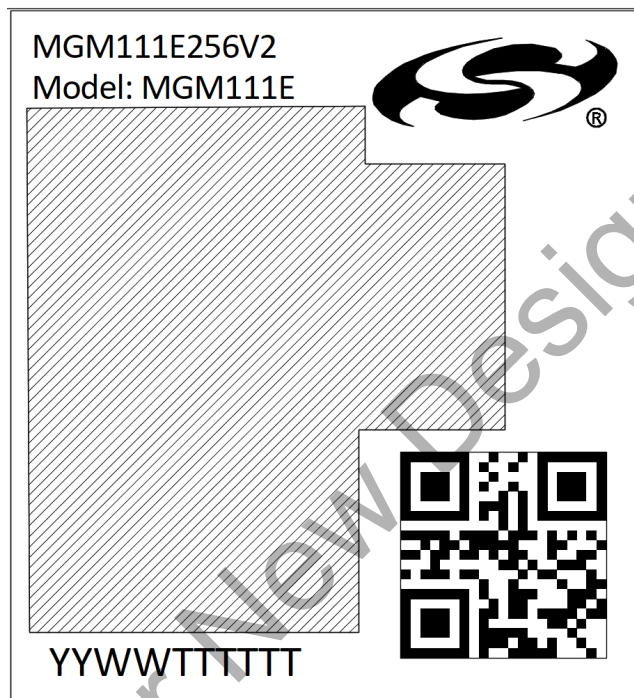


Figure 9.6. MGM111E Package Marking

### Mark Description

The package marking consists of:

- MGM111A256V2 - Part number designation
- Model: MGM111A – Model number designation
- MGM111E256V2 - Part number designation
- Model: MGM111E – Model number designation
- QR Code: YYWMMABCDE
  - YY – The last 2 digits of the assembly year
  - WW – The 2 digit work week when the device was assembled
  - MMABCDE – Silicon Labs unit code
- Trace Code: YYWWTTTTTT
  - YY – The last 2 digits of the assembly year
  - WW – The 2 digit work week when the device was assembled
  - TTTTTT – A trace or manufacturing code. The first letter is the device revision
- Certification-related information (such as the CE Mark, FCC and IC IDs, etc.) is being engraved on the grayed out area, and/or printed on the back side of the module (silkscreen), in accordance with the requirements by regulatory bodies.

## 10. Tape and Reel Specifications

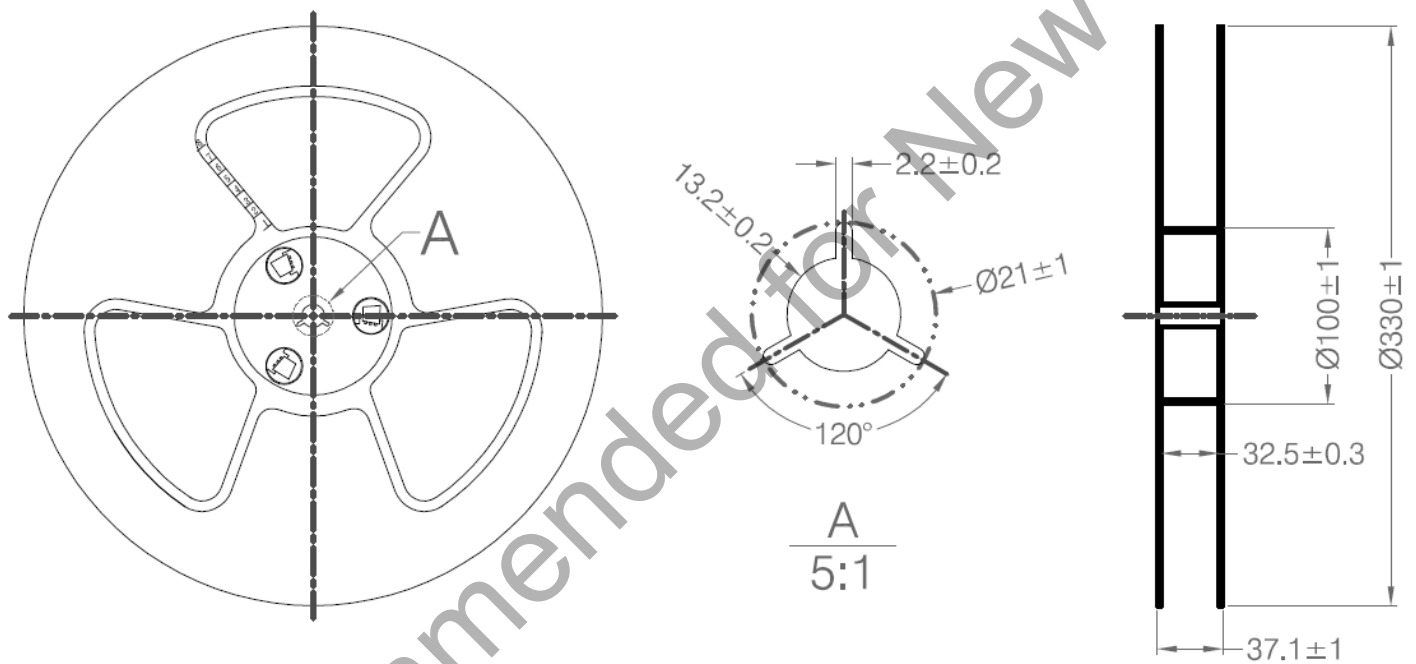
### 10.1 Tape and Reel Packaging

This section contains information regarding the tape and reel packaging for the MGM111 Mighty Gecko Module.

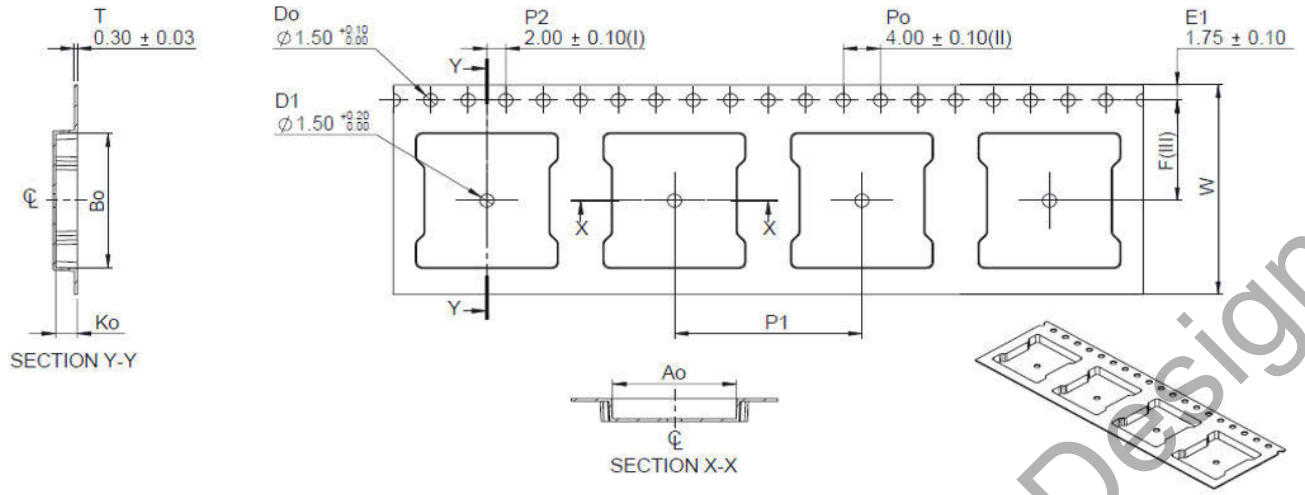
### 10.2 Reel Material and Dimensions

- Reel material: Polystyrene (PS)
- Reel diameter: 13 inches (330 mm)
- Number of modules per reel: 1000 pcs
- Disk deformation, folding whitening and mold imperfections: Not allowed
- Disk set: consists of two 13 inch (330 mm) rotary round disks and one central axis (100 mm)
- Antistatic treatment: Required
- Surface resistivity:  $10^4 - 10^9 \Omega/\text{sq}$ .

Figure 10.1. Reel Dimensions - Side View



Symbol	Dimensions [mm]
W0	$32.5 \pm 0.3$
W1	$37.1 \pm 1.0$



Ao	13.20	+/- 0.10
Bo	15.30	+/- 0.10
Ko	2.30	+/- 0.10
F	11.50	+/- 0.10
P1	20.00	+/- 0.10
W	24.00	+0.30 / -0.10

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other materials available.
- (V) Dimension with ( ) is used for design reference purposes no measurement required.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 10.2. Tape Information

### 10.3 Module Orientation and Tape Feed

The user direction of feed, start and end of tape on reel and orientation of the Modules on the tape are shown in the figures below.

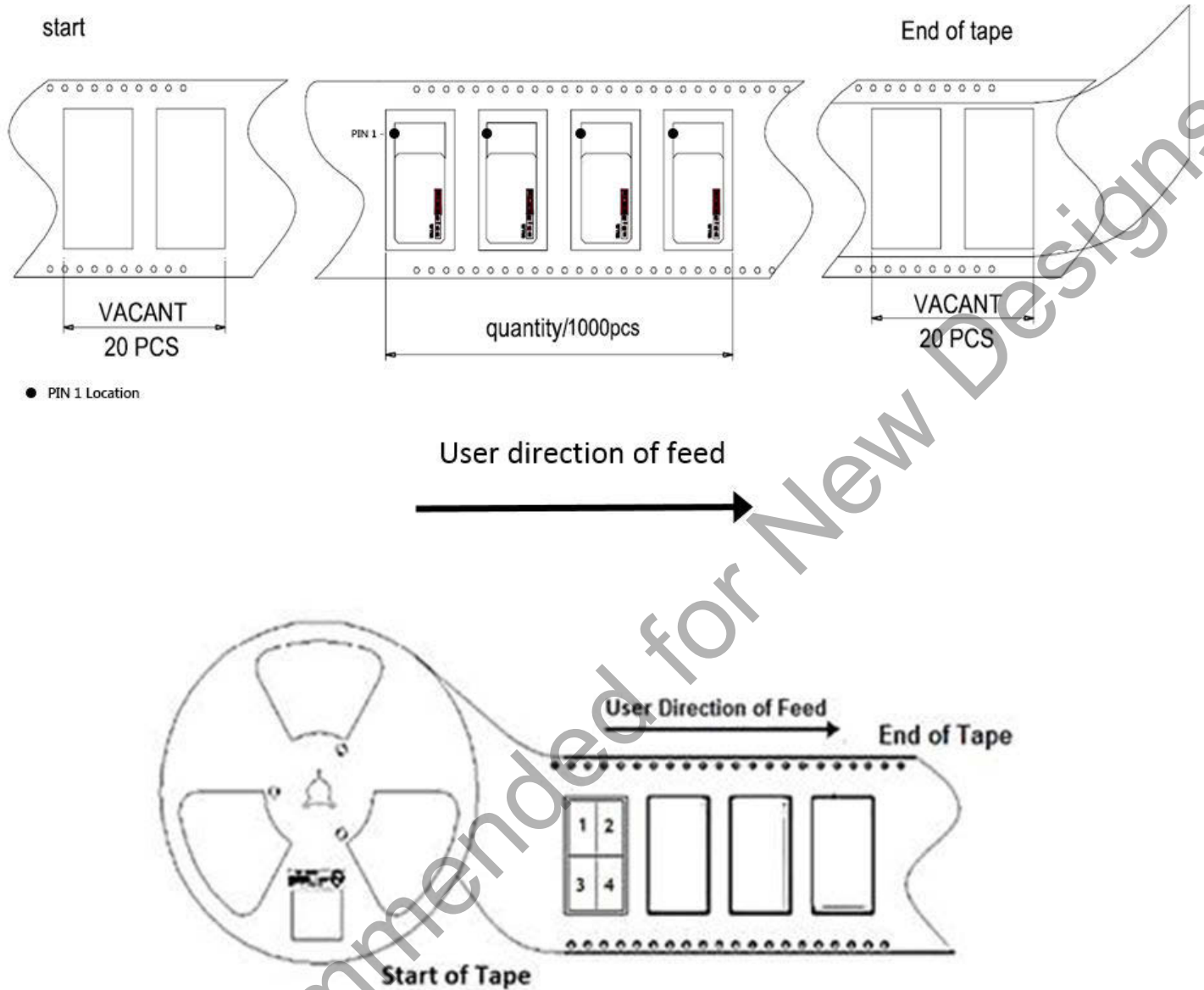
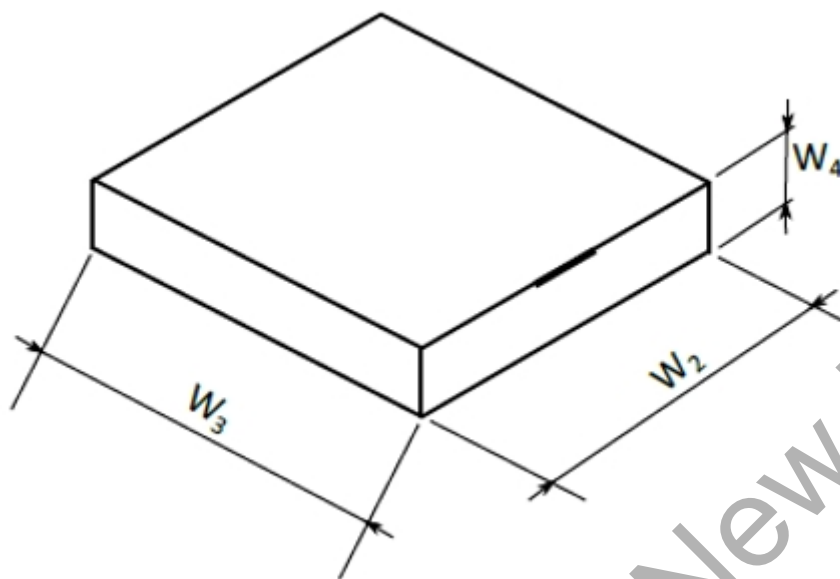


Figure 10.3. Module Orientation and Feed Direction

### 10.4 Tape and Reel Box Dimensions

Figure 10.4. Tape and Reel Box Dimensions



Symbol	Dimensions [mm]
$W_2$	368
$W_3$	338
$W_4$	72

### 10.5 Moisture Sensitivity Level

Reels are delivered in packing which conforms to MSL3 (Moisture Sensitivity Level 3) requirements.

## 11. Certificates

### 11.1 Approved Antenna Types

MGM111E is approved with a standard 2.14 dBi dipole antenna. Any antenna of the same type, similar in-band out of band characteristics and with the same or less gain can be used without reassessment. In case using antenna of a different type and/or higher gain reassessments and notification to the particular certification authority is required.

### 11.2 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

#### FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures. As long as the condition above is met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

#### OEM Responsibilities to comply with FCC Regulations

The MGM111 Module has been certified for integration into products only by OEM integrators under the following condition:

- The antenna(s) must be installed such that a minimum separation distance of 10.5 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

As long as the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**Note:** In the event that this condition cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

#### End Product Labeling

The MGM111 Module is labeled with its own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**"Contains Transmitter Module FCC ID: QOQMGM111"**

or

**"Contains FCC ID: QOQMGM111"**

The OEM integrator must not provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

### 11.3 IC

#### IC (English)

This radio transmitter has been approved by Industry Canada to operate with the embedded chip antenna. Other antenna types are strictly prohibited for use with this device.

This device complies with Industry Canada's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

#### RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5. MGM111 meets the given requirements when the minimum separation distance to human body 15 mm. RF exposure or SAR evaluation is not required when the separation distance is 15 mm or more. If the separation distance is less than 15 mm the OEM integrator is responsible for evaluating the SAR.

#### OEM Responsibilities to comply with IC Regulations

The MGM111 Module has been certified for integration into products only by OEM integrators under the following conditions:

- The antenna(s) must be installed such that a minimum separation distance of 15 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**Note:** In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the IC authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate IC authorization.

#### End Product Labeling

The MGM111 module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**"Contains Transmitter Module IC: 5123A-MGM111"**

or

**"Contains IC: 5123A-MGM111"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

## IC (Français)

Cet émetteur radio (IC : 5123A-MGM111) a reçu l'approbation d'Industrie Canada pour une exploitation avec l'antenne puce incorporée. Il est strictement interdit d'utiliser d'autres types d'antenne avec cet appareil.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage; et
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible de provoquer un fonctionnement non désiré de l'appareil.

## Déclaration relative à l'exposition aux radiofréquences (RF)

Les limites applicables à l'exemption de l'évaluation courante du DAS sont énoncées dans le CNR 102, 5e édition. Le module Bluetooth MGM111 répond aux exigences données quand la distance de séparation minimum par rapport au corps humain est de 15 mm. L'évaluation de l'exposition aux RF ou du DAS n'est pas requise quand la distance de séparation est de 15 mm ou plus. Si la distance de séparation est inférieure à 15 mm, il incombe à l'intégrateur FEO d'évaluer le DAS.

## Responsabilités du FEO ayant trait à la conformité avec les règlements IC

Le Module Bluetooth MGM111 a été certifié pour une intégration dans des produits uniquement par les intégrateurs FEO dans les conditions suivantes:

- La ou les antennes doivent être installées de telle façon qu'une distance de séparation minimum de 15 mm soit maintenue entre le radiateur (antenne) et toute personne à tout moment.
- Le module émetteur ne doit pas être installé au même endroit ou fonctionner conjointement avec toute autre antenne ou émetteur.

Dès lors que les deux conditions ci-dessus sont respectées, aucun test supplémentaire de l'émetteur n'est obligatoire. Cependant, il incombe toujours à l'intégrateur FEO de tester la conformité de son produit final vis-à-vis de toute exigence supplémentaire requise avec ce module installé (par exemple, émissions de dispositifs numériques, exigences relatives aux matériels périphériques PC, etc).

**Note:** S'il s'avère que ces conditions ne peuvent être respectées (pour certaines configurations ou la colocation avec un autre émetteur), alors l'autorisation IC n'est plus considérée comme valide et l'identifiant IC ne peut plus être employé sur le produit final. Dans ces circonstances, l'intégrateur FEO aura la responsabilité de réévaluer le produit final (y compris l'émetteur) et d'obtenir une autorisation IC distincte.

## Étiquetage du produit final

L'étiquette du Module MGM111 porte son propre identifiant IC. Si l'identifiant IC n'est pas visible quand le module est installé à l'intérieur d'un autre appareil, alors l'extérieur de l'appareil dans lequel le module est installé doit aussi porter une étiquette faisant référence au module qu'il contient. Dans ce cas, une étiquette comportant les informations suivantes doit être apposée sur une partie visible du produit final.

**"Contient le module émetteur IC: 5123A-MGM111"**

ou

**"Contient IC : 5123A-MGM111"**

L'intégrateur FEO doit être conscient de ne pas fournir d'informations à l'utilisateur final permettant d'installer ou de retirer ce module RF ou de changer les paramètres liés aux RF dans le mode d'emploi du produit final.

## 11.4 CE and UKCA - EU and UK

The MGM111 modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating a MGM111 module will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their end-products as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

The modules are entitled to carry the CE and UKCA Marks, and a formal Declaration of Conformity (DoC) is available at the product web page which is reachable starting from <https://www.silabs.com/>.

### 11.5 KC (South-Korea)

MGM111 Mighty Gecko Mesh Networking Module has certification in South-Korea.

Certification number for MGM111A: MSIP-CRM-BGT-MGM111A

Certification number for MGM111E: MSIP-CRM-BGT-MGM111E

### 11.6 AU/NZ

The MGM111 has been certified to be used in Australia and New Zealand. In order to have a RCM mark on an end product integrating MGM111, a company must comply with a or b below.

- have a company presence in Australia
- have a company/distributor/agent in Australia that will sponsor the importing of the end product

Not Recommended for New Designs

## 12. Revision History

### Revision 1.3

March, 2025

- Updated [10.2 Reel Material and Dimensions](#).

### Revision 1.2

December, 2023

- Updated [2. Ordering Information](#).

### Revision 1.1

October, 2022

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated [3.6.3 Low Energy Timer \(LETIMER\)](#) lowest energy mode.
- Removed BIASPROG = 1, FULLBIAS = 0 specifications from [4.1.15 Analog Comparator \(ACMP\)](#).
- Added timing specifications for RESETn low time in [Table 4.18 GPIO on page 28](#).
- Added [Figure 4.2 SPI Master Timing Diagram \(SMSDELAY = 1\)](#) on page 40.
- Updated [Figure 9.3 MGM111 Footprint on page 75](#).
- Updated [Figure 9.4 MGM111 Recommended PCB Land Pattern on page 75](#).
- Added two figures to [9.4 MGM111 Package Marking](#) and updated Mark Description.
- Updated [11.4 CE and UKCA - EU and UK](#).
- Removed all references to RFSENSE.

### Revision 1.0

- Full Production

### Revision 0.5

- Initial Publication

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