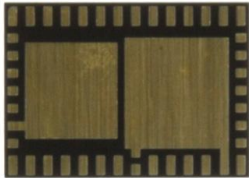


# SI32176-C-FM1 Datasheet

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|                              |  |
|------------------------------|--|
| DiGi Electronics Part Number | SI32176-C-FM1-DG   |
| Manufacturer                 | <a href="#">Skyworks Solutions Inc.</a>                                  |
| Manufacturer Product Number  | SI32176-C-FM1  |
| Description                  | IC TELECOM INTERFACE 42QFN   |
| Detailed Description         | Telecom IC Subscriber Line Interface Concept (SLIC ), CODEC 42-QFN (5x7) |

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## Purchase and inquiry

Manufacturer Product Number:

SI32176-C-FM1

Series:

ProSLIC®

Function:

Subscriber Line Interface Concept (SLIC), CODEC

Number of Circuits:

1

Current - Supply:

-

Mounting Type:

Surface Mount

Supplier Device Package:

42-QFN (5x7)

Manufacturer:

Skyworks Solutions Inc.

Product Status:

Active

Interface:

GCI, PCM, SPI

Voltage - Supply:

3.3V

Operating Temperature:

0°C ~ 70°C

Package / Case:

42-WFQFN Exposed Pad

Base Product Number:

SI32176

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

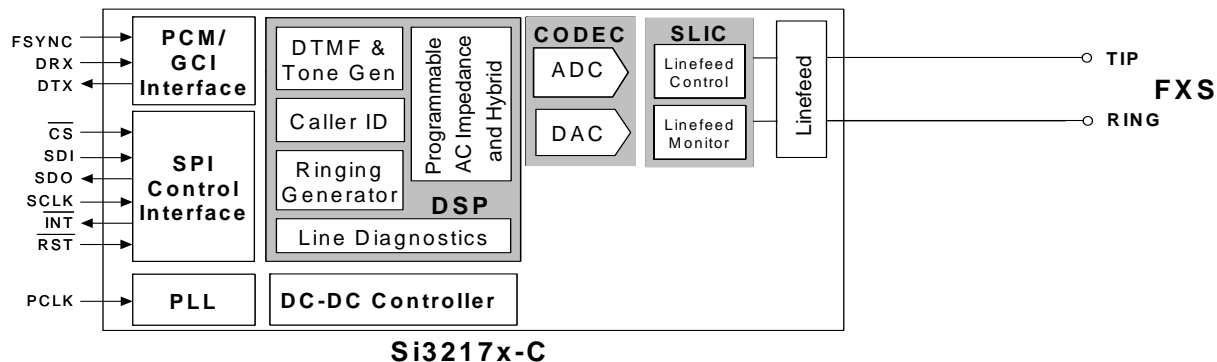
ECCN:

EAR99



# Si3217x-C

## Functional Block Diagram



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# Si3217x-C

## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions<sup>1</sup>**

| Parameter                                 | Symbol            | Test Condition | Min* | Typ  | Max* | Unit |
|---|-------------------|----------------|------|------|------|------|
| Ambient Temperature                       | T <sub>A</sub>    | F-grade        | 0    | 25   | 70   | °C   |
|   |                   | G-grade        | -40  | 25   | 85   | °C   |
| Silicon Junction Temperature, QFN-42      | T <sub>JHV</sub>  | Linefeed Die   | —    | —    | 145  | °C   |
| Supply Voltage, Si3217x-C                 | V <sub>DD</sub>   |                | 3.13 | 3.3  | 3.47 | V    |
| Battery Voltage, Si32171/4/6 <sup>2</sup> | V <sub>BAT</sub>  |                | -110 | -95  | -15  | V    |
| Battery Voltage, Si32170/7 <sup>2</sup>   | V <sub>BAT</sub>  |                | -140 | -130 | -15  | V    |
| IO Supply Voltage, Si3217x-C              | V <sub>DDIO</sub> |                | 1.71 | —    | 3.47 | V    |

**Notes:**

1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Operation at minimum voltage dependent upon loop conditions and dc-dc converter configuration.

Table 2. Power Supply Characteristics for Si3217x-C

| Parameter   | Symbol     | Test Condition   | Min | Typ  | Max | Unit |
|---|------------|--|-----|------|-----|------|
| Supply Currents:<br>Reset                               | $I_{DD}$   | $V_T$ and $V_R = \text{Hi-Z}$ , $R_{ST} = 0$   | —   | 6.3  | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 0    | —   | mA   |
| Supply Currents:<br>High Impedance,<br>Open             | $I_{DD}$   | $V_T$ and $V_R = \text{Hi-Z}$  | —   | 20.8 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 0.6  | —   | mA   |
| Supply Currents:<br>Forward/Reverse,<br>On-hook         | $I_{DD}$   | $V_{TR} = -48 \text{ V}$ ,<br>Automatic Power Save Mode Enabled  | —   | 10.8 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 0.6  | —   | mA   |
| Supply Currents:<br>Forward/Reverse,<br>On-hook         | $I_{DD}$   | $V_{TR} = -48 \text{ V}$ ,<br>Automatic Power Save Mode Disabled   | —   | 31.2 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 2.1  | —   | mA   |
| Supply Currents:<br>Tip/Ring Open,<br>On-hook           | $I_{DD}$   | $V_T$ or $V_R = -48 \text{ V}$<br>$V_R$ or $V_T = \text{Hi-Z}$ ,<br>Automatic Power Save Mode Enabled                  | —   | 10.9 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 0.4  | —   | mA   |
| Supply Currents:<br>Tip/Ring Open,<br>On-hook           | $I_{DD}$   | $V_T$ or $V_R = -48 \text{ V}$<br>$V_R$ or $V_T = \text{Hi-Z}$ ,<br>Automatic Power Save Mode Disabled                 | —   | 30.6 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 1.3  | —   | mA   |
| Supply Currents:<br>Forward/Reverse OHT,<br>On-hook     | $I_{DD}$   | $V_{TR} = 48 \text{ V}$  | —   | 43.8 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 2.9  | —   | mA   |
| Supply Currents:<br>Forward/Reverse Active,<br>Off-hook | $I_{DD}$   | $I_{LOOP} = 20 \text{ mA}$ , $R_{LOAD} = 200 \Omega$   | —   | 44.6 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 21.3 | —   | mA   |
| Supply Currents:<br>Ringing                             | $I_{DD}$   | $V_{TR} = 55 V_{RMS} + 0 V_{DC}$ ,<br>balanced, sinusoidal, $f = 20 \text{ Hz}$<br>$R_{LOAD} = 5 R_{EN} = 1400 \Omega$ | —   | 35.8 | —   | mA   |
|   | $I_{VBAT}$ |  | —   | 37.5 | —   | mA   |

**Notes:**

- All specifications are for a single channel of Si3217x with a tracking flyback dc-dc converter
- $I_{DD}$  includes  $I_{DDIO}$ .

# Si3217x-C

**Table 3. AC Characteristics for FXS**

| Parameter  | Test Condition  | Min                  | Typ | Max  | Unit            |
|--|---|----------------------|-----|------|-----------------|
| <b>TX/RX Performance</b>   |   |                      |     |      |                 |
| Overload Level   |   | 2.5                  | —   | —    | V <sub>PK</sub> |
| Overload Compression   | 2-Wire – PCM  | Figure 4             | —   | —    |                 |
| Single Frequency Distortion <sup>1</sup>   | 2-Wire – PCM or PCM – 2-Wire:<br>200 Hz to 3.4 kHz                                    | —                    | —   | –40  | dB              |
|  | PCM – 2-Wire – PCM:<br>200 Hz – 3.4 kHz,<br>16-bit Linear mode                        | —                    | —   | –63  | dB              |
| Signal-to-(Noise + Distortion) Ratio <sup>2</sup>  | 200 Hz to 3.4 kHz<br>D/A or A/D 8-bit<br>Active off-hook, and OHT, any Z <sub>T</sub> | Figure 3             | —   | —    |                 |
| Audio Tone Generator Signal-to-Distortion Ratio <sup>2</sup>   | 0 dBm <sub>0</sub> , Active off-hook, and OHT,<br>any Z <sub>T</sub>                  | 46                   | —   | —    | dB              |
| Intermodulation Distortion   |   | —                    | —   | –41  | dB              |
| Gain Accuracy <sup>2</sup>   | 2-Wire to PCM or PCM to 2-Wire<br>1014 Hz, Any gain setting                           | –0.2                 | —   | 0.2  | dB              |
| Attenuation Distortion vs. Frequency   | 0 dBm 0 <sup>6</sup>  | See Figure 16 and 17 |     |      |                 |
| Group Delay vs. Frequency  |   | See Figure 18 and 19 |     |      |                 |
| Gain Tracking <sup>3</sup>   | 1014 Hz sine wave,<br>reference level –10 dBm<br>Signal level:                        | —                    | —   | —    | —               |
|  | 3 dB to –37 dB  | —                    | —   | 0.25 | dB              |
|  | –37 dB to –50 dB  | —                    | —   | 0.5  | dB              |
|  | –50 dB to –60 dB  | —                    | —   | 1.0  | dB              |
| Round-Trip Group Delay   | 1014 Hz, Within same time-slot  | —                    | 450 | 500  | μs              |
| 2-Wire Return Loss <sup>4</sup>  | 200 Hz to 3.4 kHz   | 26                   | 30  | —    | dB              |
| Transhybrid Balance <sup>4</sup>   | 300 Hz to 3.4 kHz   | 26                   | 30  | —    | dB              |
| <b>Notes:</b>  |   |                      |     |      |                 |
| 1. The input signal level should be 0 dBm <sub>0</sub> for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm <sub>0</sub> . The output signal magnitude at any other frequency is smaller than the maximum value specified. |   |                      |     |      |                 |
| 2. Analog signal measured as V <sub>TIP</sub> – V <sub>RING</sub> . Assumes ideal line impedance matching.   |   |                      |     |      |                 |
| 3. The quantization errors inherent in the μ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.              |   |                      |     |      |                 |
| 4. V <sub>DD</sub> , V <sub>DDIO</sub> = 3.3 V, V <sub>BAT</sub> = –52 V, no fuse resistors; R <sub>L</sub> = 600 Ω, Z <sub>S</sub> = 600 Ω synthesized using RS register coefficients.  |   |                      |     |      |                 |
| 5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.   |   |                      |     |      |                 |
| 6. 0 dBm 0 is equal to 0 dBm into 600 Ω.   |   |                      |     |      |                 |

Table 3. AC Characteristics for FXS (Continued)

| Parameter  | Test Condition                         | Min | Typ | Max | Unit     |
|--|--|-----|-----|-----|----------|
| <b>Noise Performance</b>   |  |     |     |     |          |
| Idle Channel Noise <sup>5</sup>  | C-Message weighted                     | —   | 8   | 12  | dBrnC    |
|  | Psophometric weighted                  | —   | -82 | -78 | dBmP     |
| PSRR from $V_{DD}$ , $V_{DDIO}$ @ 3.3 V  | RX and TX, 200 Hz to 3.4 kHz           | —   | 55  | —   | dB       |
| <b>Longitudinal Performance</b>  |  |     |     |     |          |
| Longitudinal to Metallic/PCM Balance (forward or reverse)  | 200 Hz to 1 kHz                        | 58  | 60  | —   | dB       |
|  | 1 kHz to 3.4 kHz                       | 53  | 58  | —   | dB       |
| Metallic/PCM to Longitudinal Balance   | 200 Hz to 3.4 kHz                      | 40  | —   | —   | dB       |
| Longitudinal Impedance   | 200 Hz to 3.4 kHz at TIP or RING       | —   | 50  | —   | $\Omega$ |
| Longitudinal Current Capability  | Active off-hook 60 Hz<br>Reg 73 = 0x0B | —   | 25  | —   | mA       |
| <b>Notes:</b>  |  |     |     |     |          |
| 1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be -10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.                  |  |     |     |     |          |
| 2. Analog signal measured as $V_{TIP} - V_{RING}$ . Assumes ideal line impedance matching.   |  |     |     |     |          |
| 3. The quantization errors inherent in the $\mu/A$ -law companding process can generate slightly worse gain tracking performance in the signal range of 3 to -37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate. |  |     |     |     |          |
| 4. $V_{DD}$ , $V_{DDIO}$ = 3.3 V, $V_{BAT}$ = -52 V, no fuse resistors; $R_L$ = 600 $\Omega$ , $Z_S$ = 600 $\Omega$ synthesized using RS register coefficients.  |  |     |     |     |          |
| 5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed -55 dBm.   |  |     |     |     |          |
| 6. 0 dBm 0 is equal to 0 dBm into 600 $\Omega$ .   |  |     |     |     |          |

# Si3217x-C

**Table 4. Linefeed Characteristics for FXS**

| Parameter                                    | Symbol        | Test Condition   | Min | Typ | Max  | Unit       |
|--|---------------|--|-----|-----|------|------------|
| Maximum Loop Resistance                      | $R_{LOOP}$    | $R_{DC,MAX} = 430 \Omega$<br>$I_{LOOP} = 18 \text{ mA}$ , $V_{BAT} = -52 \text{ V}$ ,<br>$R_{PROT} = 0 \Omega$ | —   | —   | 2000 | $\Omega$   |
| DC Feed Current                              |               | Differential   | —   | —   | 45   | mA         |
|  |               | Common Mode  | —   | —   | 30   | mA         |
|  |               | Differential + Common Mode   | —   | —   | 45   | mA         |
| DC Loop Current Accuracy                     |               | $I_{LIM} = 18 \text{ mA}$  | —   | —   | 10   | %          |
| DC Open Circuit Voltage Accuracy             |               | Active Mode; $V_{OC} = 48 \text{ V}$ ,<br>$V_{TIP} - V_{RING}$   | —   | —   | 4    | V          |
| DC Differential Output Resistance            | $R_{DO}$      | $I_{LOOP} < I_{LIM}$   | 160 | —   | 640  | $\Omega$   |
| DC On-Hook Voltage Accuracy—Ground Start     | $V_{OHTO}$    | $I_{RING} < I_{LIM}$ ; $V_{RING}$ wrt ground,<br>$V_{RING} = -51 \text{ V}$                                    | —   | —   | 4    | V          |
| DC Output Resistance—Ground Start            | $R_{ROTO}$    | $I_{RING} < I_{LIM}$ ; RING to ground  | 160 | —   | 640  | $\Omega$   |
| DC Output Resistance—Ground Start            | $R_{TOTO}$    | TIP to ground  | 400 | —   | —    | k $\Omega$ |
| Loop Closure Detect Threshold Accuracy       |               | $I_{THR} = 13 \text{ mA}$  | —   | —   | 10   | %          |
| Ground Key Detect Threshold Accuracy         |               | $I_{THR} = 13 \text{ mA}$  | —   | —   | 10   | %          |
| Ring Trip Threshold Accuracy                 |               | AC detection,<br>$V_{RING} = 70 \text{ Vpk}$ , no offset,<br>$I_{TH} = 80 \text{ mA}$                          | —   | —   | 4    | mA         |
|  |               | DC detection,<br>20 V dc offset, $I_{TH} = 13 \text{ mA}$  | —   | —   | 1    | mA         |
|  |               | DC Detection,<br>48 V DC offset, $R_{loop} = 1500 \Omega$  | —   | —   | 3    | mA         |
| Ringing Amplitude*                           | $V_{RINGING}$ | Si32171/4/6 Open circuit, $V_{BAT} = -110 \text{ V}$   | 108 | —   | —    | $V_{PK}$   |
|  |               | Si32170/7 Open circuit,<br>$V_{BAT} = -140 \text{ V}$  | 132 | —   | —    | $V_{PK}$   |
| Sinusoidal Ringing Total Harmonic Distortion | $R_{THD}$     | Si32171/4/6 : $60 V_{RMS}$ ,<br>15 $V_{OFFSET}$ , 0–5 REN  | —   | 1   | —    | %          |
|  |               | Si32170/7 : $55 V_{RMS}$ , 48 $V_{OFFSET}$ ,<br>0–5 REN  | —   | —   | —    | —          |
| Ringing Frequency Accuracy                   |               | $f = 16 \text{ Hz to } 60 \text{ Hz}$  | —   | —   | 1    | %          |
| Ringing Cadence Accuracy                     |               | Accuracy of ON/OFF times   | —   | —   | 50   | ms         |
| Loop Voltage Sense Accuracy                  |               | $V_{TIP} - V_{RING} = 48 \text{ V}$  | —   | 2   | 4    | %          |
| Loop Current Sense Accuracy                  |               | $I_{LOOP} = 18 \text{ mA}$   | —   | 7   | 10   | %          |
| Power Alarm Threshold Accuracy               |               | Power Threshold = 1.0 W<br>$V_{BAT} = -56 \text{ V}$ , $I_{LDDD} = 40 \text{ mA}$ ,<br>$R_{LOAD} = 600 \Omega$ | —   | 15  | —    | %          |
| Test Load Impedance                          | $R_{TL}$      | HVIC_STATE_SPARE[23] = 1   | 1.0 | —   | 3.0  | k $\Omega$ |

**Table 4. Linefeed Characteristics for FXS (Continued)**

| Parameter         | Symbol   | Test Condition           | Min     | Typ | Max      | Unit |
|-------------------|----------|--------------------------|---------|-----|----------|------|
| Test Load Voltage | $V_{TL}$ | HVIC_STATE_SPARE[23] = 1 | $\pm 5$ |     | $\pm 50$ | V    |

**\*Note:** Ringing amplitude is set for 108 or 128 V peak and measured at TIP-RING using no series protection resistance.

# Si3217x-C

**Table 5. Digital I/O Characteristics**

| Parameter   | Symbol   | Test Condition       | Min                   | Typ | Max                   | Unit          |
|---|----------|----------------------|-----------------------|-----|-----------------------|---------------|
| High Level Input Voltage                                    | $V_{IH}$ |                      | $0.7 \times V_{DDIO}$ | —   | $V_{DDIO}$            | V             |
| Low Level Input Voltage                                     | $V_{IL}$ |                      | —                     | —   | $0.3 \times V_{DDIO}$ | V             |
| High Level Output Voltage*                                  | $V_{OH}$ |                      | $V_{DDIO} - 0.6$      | —   | —                     | V             |
| Low Level Output Voltage*                                   | $V_{OL}$ | $I_O = 4 \text{ mA}$ | —                     | —   | 0.4                   | V             |
| SDITHRU and $\overline{\text{RST}}$ Internal Pullup Current |          |                      | 33                    | 42  | 65                    | $\mu\text{A}$ |
| Input Leakage Current                                       | $I_L$    |                      | —                     | —   | 10                    | $\mu\text{A}$ |

**Table 6. Charge Pump Characteristics**

| Parameter                    | Symbol   | Test Condition | Min                   | Typ | Max               | Unit |
|------------------------------|----------|----------------|-----------------------|-----|-------------------|------|
| Output Voltage (DCDRV, DCFF) | $V_{CP}$ |                | $2 \times V_{DD} - 1$ | —   | $2 \times V_{DD}$ | V    |
| Output Current               | $I_{CP}$ |                | —                     | —   | 3*                | mA   |

**\*Note:** Peak drive current capability is > 60 mA.

**Table 7. Switching Characteristics—General Inputs**

| Parameter                           | Symbol   | Min     | Typ | Max | Unit          |
|-------------------------------------|----------|---------|-----|-----|---------------|
| $\overline{\text{RST}}$ Pulse Width | $t_{rl}$ | 33/PCLK | —   | —   | $\mu\text{s}$ |

**Note:** All timing is referenced to the 50% level of the waveform. Input test levels are  $V_{IH} = V_{DD} - 0.4 \text{ V}$ ,  $V_{IL} = 0.4 \text{ V}$ . Rise and Fall times are referenced to the 20% and 80% levels of the waveform.

Table 8. Switching Characteristics—SPI

| Parameter   | Symbol    | Test Condition | Min | Typ | Max | Unit |
|---|-----------|----------------|-----|-----|-----|------|
| Cycle Time SCLK                                   | $t_c$     |                | 62  | —   | —   | ns   |
| Rise Time, SCLK                                   | $t_r$     |                | —   | —   | 25  | ns   |
| Fall Time, SCLK                                   | $t_f$     |                | —   | —   | 25  | ns   |
| Delay Time, SCLK Fall to SDO Active               | $t_{d1}$  |                | —   | —   | 20  | ns   |
| Delay Time, SCLK Fall to SDO Transition           | $t_{d2}$  |                | —   | —   | 20  | ns   |
| Delay Time, $\overline{CS}$ Rise to SDO Tri-state | $t_{d3}$  |                | —   | —   | 20  | ns   |
| Setup Time, $\overline{CS}$ to SCLK Fall          | $t_{su1}$ |                | 25  | —   | —   | ns   |
| Hold Time, $\overline{CS}$ to SCLK Rise           | $t_{h1}$  |                | 20  | —   | —   | ns   |
| Setup Time, SDI to SCLK Rise                      | $t_{su2}$ |                | 25  | —   | —   | ns   |
| Hold Time, SDI to SCLK Rise                       | $t_{h2}$  |                | 20  | —   | —   | ns   |
| Delay Time between Chip Selects                   | $t_{cs}$  |                | 220 | —   | —   | ns   |
| SDI to SDITHRU Propagation Delay                  | $t_{d4}$  |                | —   | 4   | 10  | ns   |

**Notes:**

- All timing is referenced to the 50% level of the waveform. Input test levels are  $V_{IH} = V_{DDIO} - 0.4$  V,  $V_{IL} = 0.4$  V.
- Characteristics for outputs specified with  $C_L = 20$  pF.

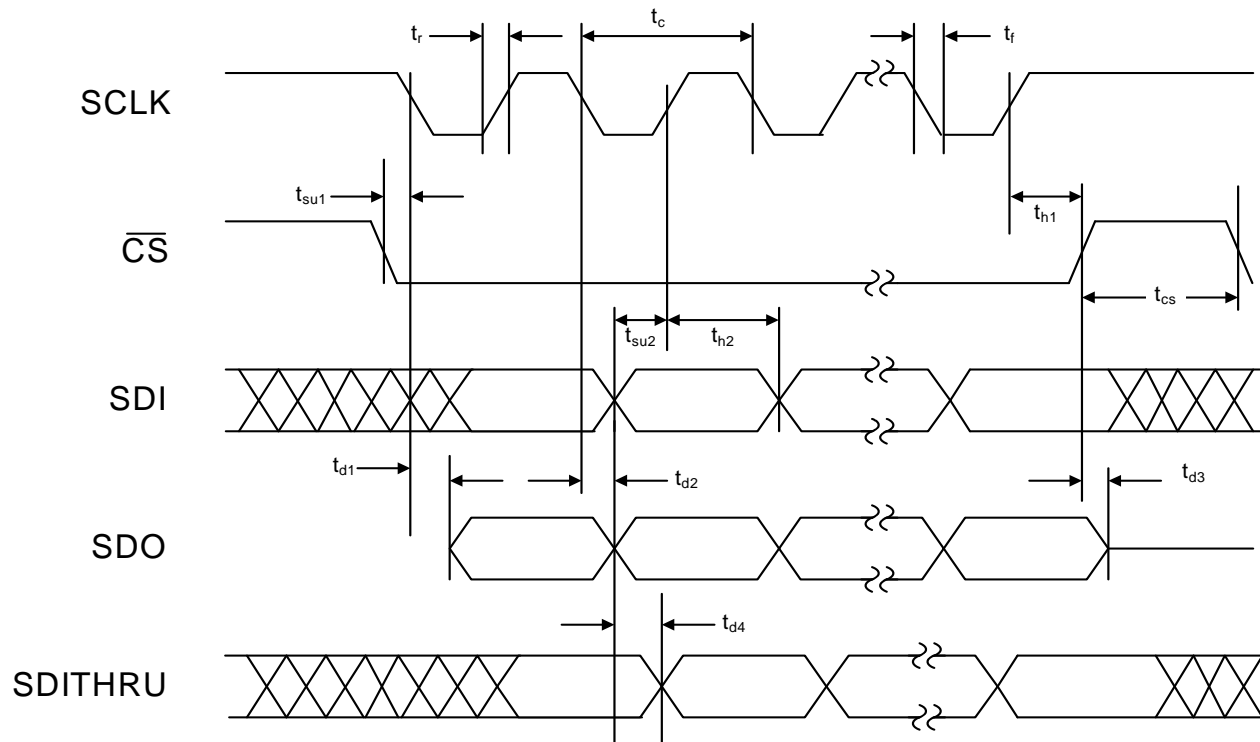


Figure 1. SPI Timing Diagram

# Si3217x-C

**Table 9. Switching Characteristics—PCM Highway Interface**

| Parameter  | Symbol                   | Test Condition | Min <sup>1</sup> | Typ <sup>1</sup> | Max <sup>1</sup>        | Unit              |
|--|--------------------------|----------------|------------------|------------------|-------------------------|-------------------|
| PCLK Period  | $t_p$                    |                | 122              | —                | 1953                    | ns                |
| PCLK Jitter Tolerance                              | $t_{\text{jitter(FXS)}}$ |                | —                | —                | 8                       | ns <sub>RMS</sub> |
| Valid PCLK Inputs <sup>2</sup>                     |                          |                | —                | 256              | —                       | kHz               |
|  |                          |                | —                | 512              | —                       | kHz               |
|  |                          |                | —                | 768              | —                       | kHz               |
|  |                          |                | —                | 1.024            | —                       | MHz               |
|  |                          |                | —                | 1.536            | —                       | MHz               |
|  |                          |                | —                | 1.544            | —                       | MHz               |
|  |                          |                | —                | 2.048            | —                       | MHz               |
|  |                          |                | —                | 4.096            | —                       | MHz               |
|  |                          |                | 8.192            | —                | MHz                     |                   |
| FSYNC Period <sup>3</sup>                          | $t_{fs}$                 |                | —                | 125              | —                       | μs                |
| PCLK Duty Cycle Tolerance                          | $t_{dty}$                |                | 40               | 50               | 60                      | %                 |
| FSYNC Jitter Tolerance <sup>4</sup>                | $t_{\text{jitter}}$      |                | —                | —                | ±120                    | ns                |
| Rise Time, PCLK                                    | $t_r$                    |                | —                | —                | 25                      | ns                |
| Fall Time, PCLK                                    | $t_f$                    |                | —                | —                | 25                      | ns                |
| Delay Time, PCLK Rise to DTX Active                | $t_{d1}$                 |                | —                | —                | 20                      | ns                |
| Delay Time, PCLK Rise to DTX Transition            | $t_{d2}$                 |                | —                | —                | 20                      | ns                |
| Delay Time, PCLK Rise to DTX Tristate <sup>6</sup> | $t_{d3}$                 |                | —                | —                | 20                      | ns                |
| Setup Time, FSYNC to PCLK Fall                     | $t_{su1}$                |                | 25               | —                | —                       | ns                |
| Hold Time, FSYNC to PCLK Fall                      | $t_{h1}$                 |                | 20               | —                | —                       | ns                |
| Setup Time, DRX to PCLK Fall                       | $t_{su2}$                |                | 25               | —                | —                       | ns                |
| Hold Time, DRX to PCLK Fall                        | $t_{h2}$                 |                | 20               | —                | —                       | ns                |
| FSYNC Pulse Width                                  | $t_{wfs}$                |                | $t_p$            | —                | $125 \mu\text{s} - t_p$ |                   |

**Notes:**

1. All timing is referenced to the 50% level of the waveform. Input test levels are  $V_{IH} - V_{IO} - 0.4 \text{ V}$ ,  $V_{IL} = 0.4 \text{ V}$ .
2. A constant PCLK and FSYNC are required.
3. FSYNC source is assumed to be 8 kHz under all operating conditions.
4. FSYNC Jitter Tolerance relative to PCLK.
5. Characteristics for outputs specified with  $C_L = 20 \text{ pF}$ .
6. Specification applies to PCLK fall to DTX tristate when that mode is selected.

Table 10. Thermal Conditions

| Parameter  | Symbol        | Test Condition       | Value      | Unit |
|--|---------------|----------------------|------------|------|
| Storage Temperature Range                                | $T_{STG}$     |                      | -55 to 150 | °C   |
| Thermal Resistance, Typical <sup>1</sup><br>QFN-42       | $\theta_{JA}$ |                      | 53         | °C/W |
|  | $\theta_{JB}$ |                      | 33         |      |
|  | $\theta_{JC}$ |                      | 39         |      |
| Continuous Power Dissipation <sup>2,3</sup><br>QFN-42    | $P_D$         | $T_A = 85\text{ °C}$ | 0.75       | W    |
| Maximum Junction Temperature,<br>QFN-42 (Linefeed Die)   | $T_{JHV}$     | Continuous           | 145        | °C   |
| Maximum Junction Temperature<br>QFN-42 (Low Voltage Die) | $T_{JLV}$     |                      | 125        | °C   |

**Notes:**

1. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane. Thermal resistance values are empirical measurements taken from Skyworks Solutions EVBs.
2. Operation of the Si3217x above 125 °C junction temperature may degrade device reliability.
3. Si3217x linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold should normally be set to 145 °C; when in the ringing state with cadence the thermal shutdown may be set to 200 °C. For optimal reliability long term operation of the Si3217x linefeed above 150 °C junction temperature should be avoided.

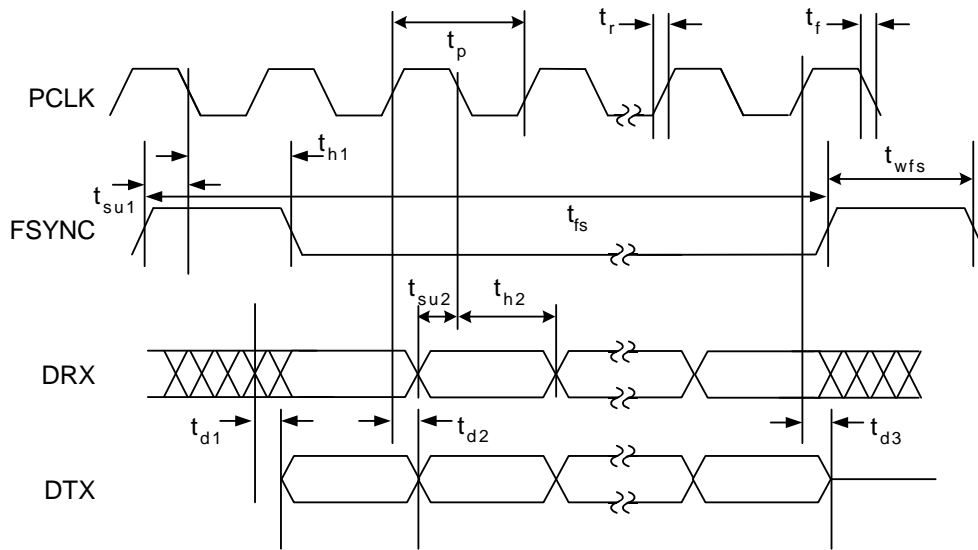
Table 11. Absolute Maximum Ratings<sup>1</sup>

| Parameter   | Symbol              | Test Condition | Value        | Unit |
|---|---------------------|----------------|--------------|------|
| Supply Voltage                                    | $V_{DD}, V_{DDIO}$  |                | -0.5 to 4.0  | V    |
| Digital Input Voltage                             | $V_{IND}$           |                | -0.3 to 3.6  | V    |
| Battery Supply Voltage <sup>2</sup> , Si32171/4/6 | $V_{BAT}$           |                | +0.4 to -115 | V    |
| Battery Supply Voltage <sup>2</sup> , Si32170/7   | $V_{BAT}$           |                | +0.4 to -142 | V    |
| Tip or Ring Voltage, Si32171/4/6 <sup>3</sup>     | $V_{TIP}, V_{RING}$ |                | -130         | V    |
| Tip or Ring Voltage, Si32170/7 <sup>3</sup>       | $V_{TIP}, V_{RING}$ |                | -142         | V    |
| TIP, RING Current                                 | $I_{TIP}, I_{RING}$ |                | ±100         | mA   |

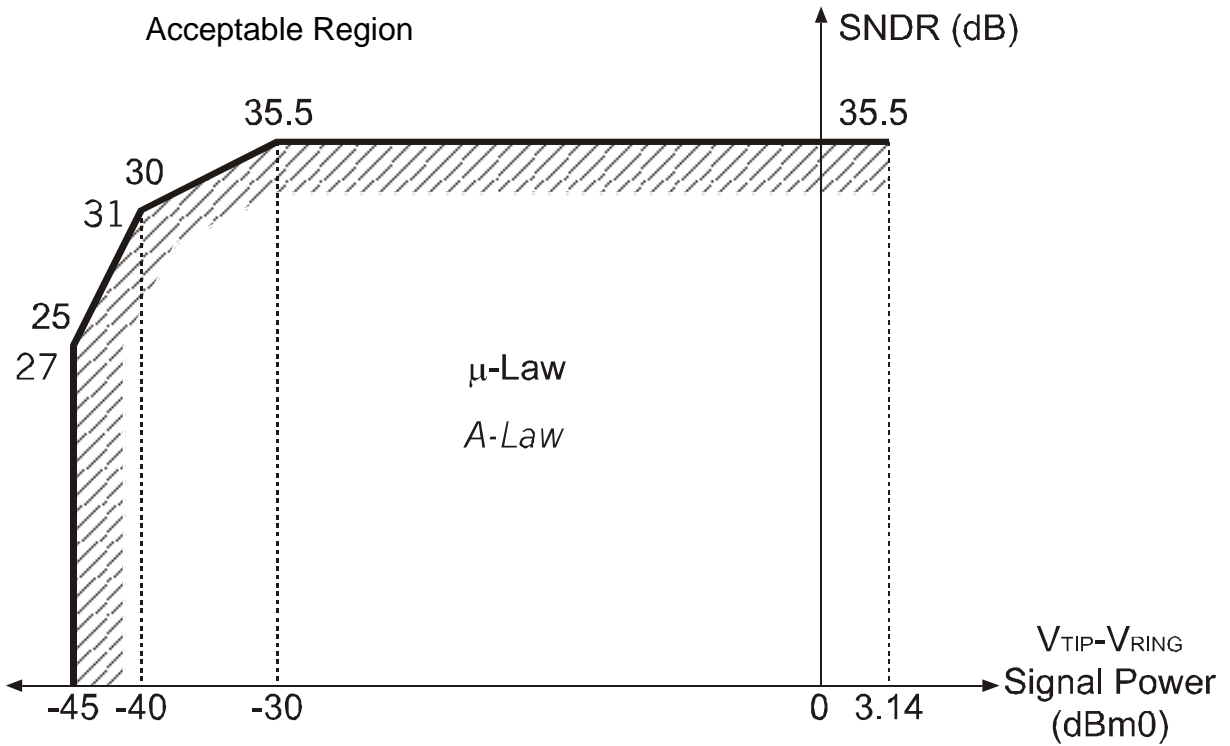
**Notes:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. The dv/dt of the voltage applied to the VBAT pins must be limited to 10 V/μs.
3. Specification requires circuit for surge event as shown in typical application circuit. VTIP or VRING must not be more than 14 V more negative than VBAT if a fixed protection device is used.

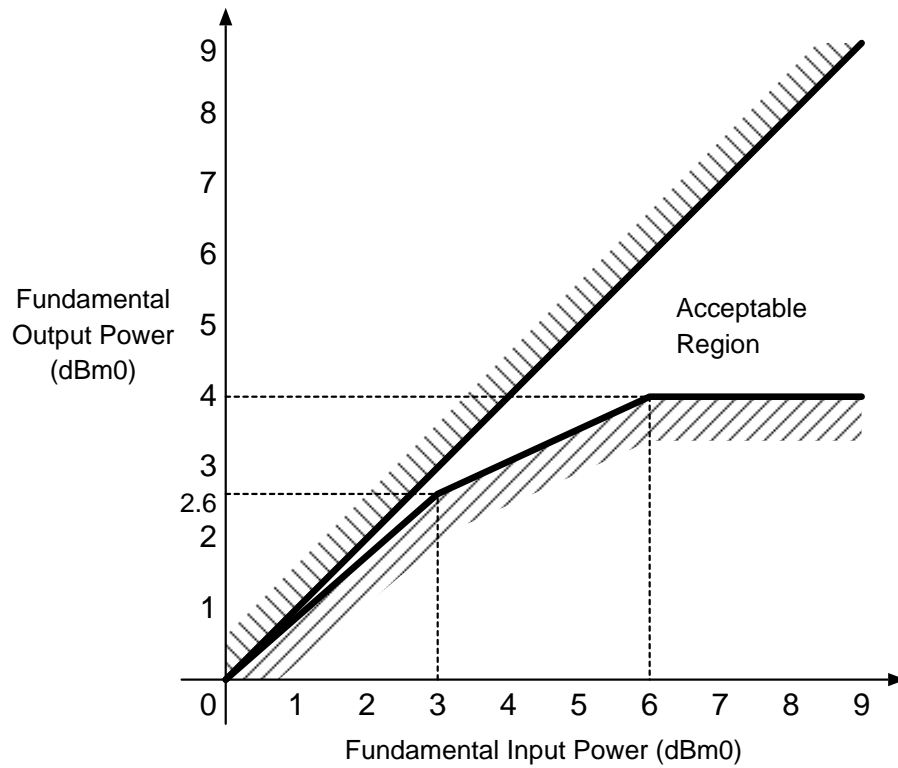
# Si3217x-C



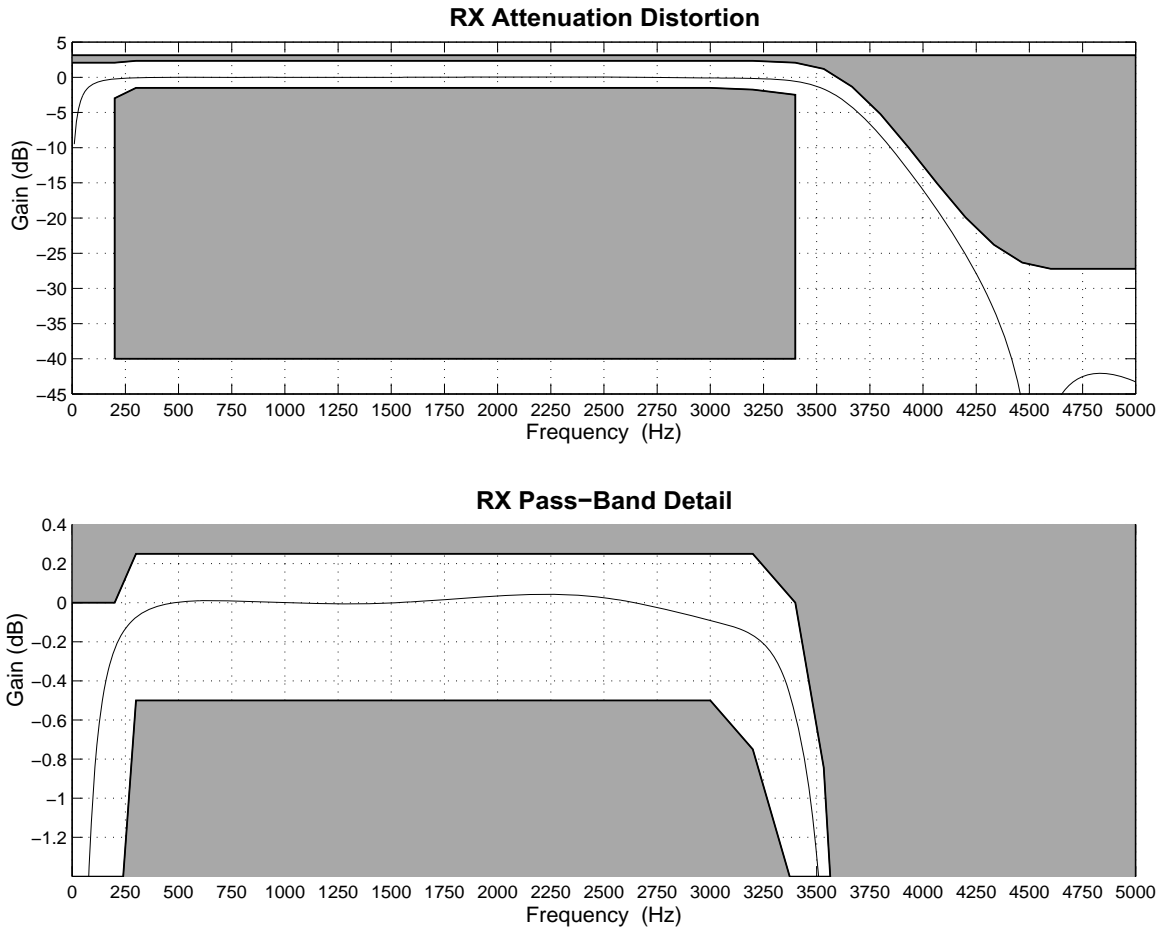
**Figure 2. PCM Highway Interface Timing Diagram**



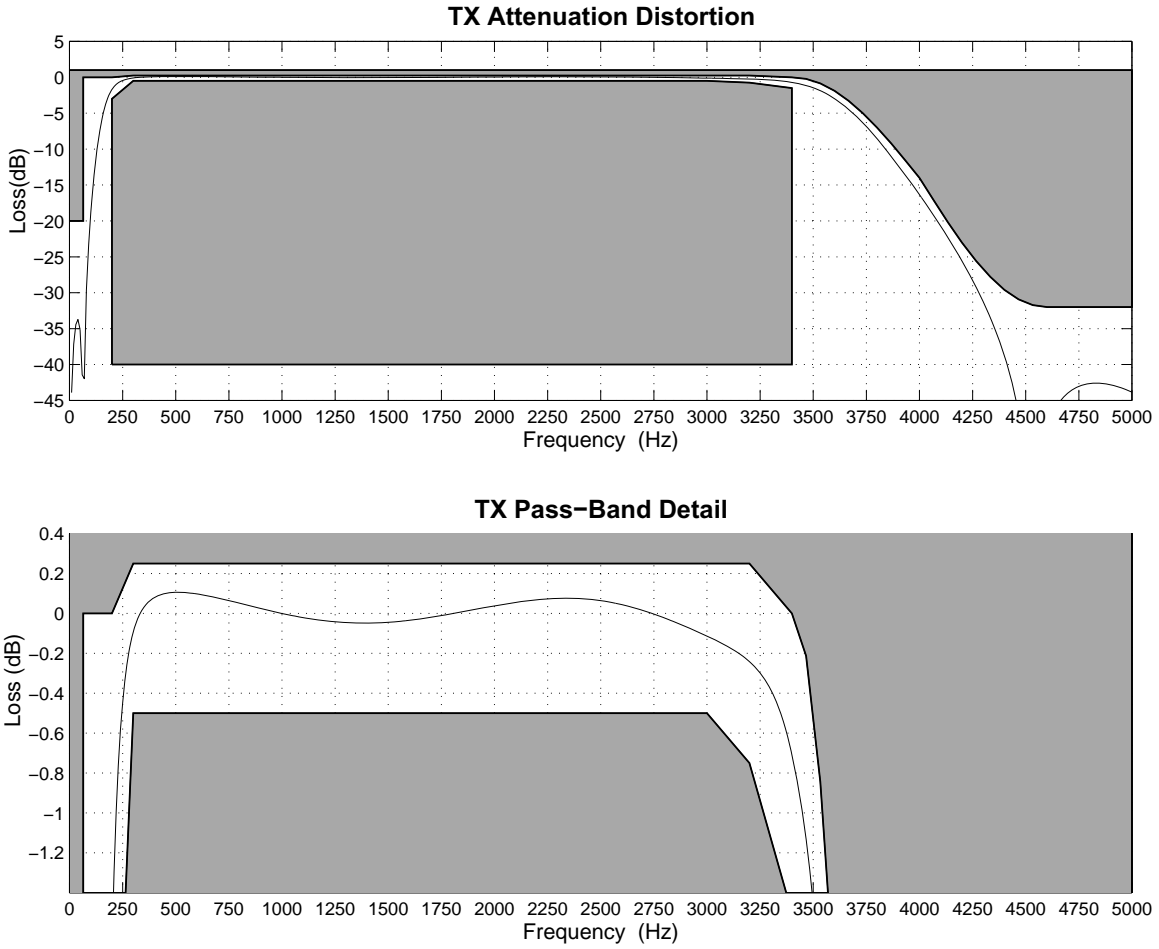
**Figure 3. Transmit and Receive Path SNDR**

**Figure 4. Overload Compression Performance**

# Si3217x-C

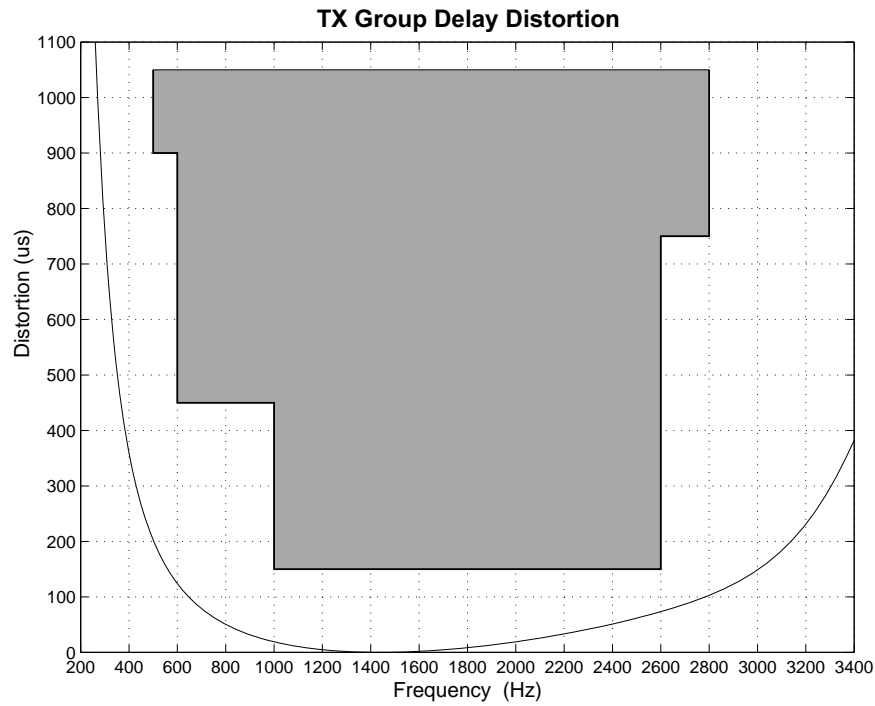


**Figure 5. Receive Path Frequency Response**

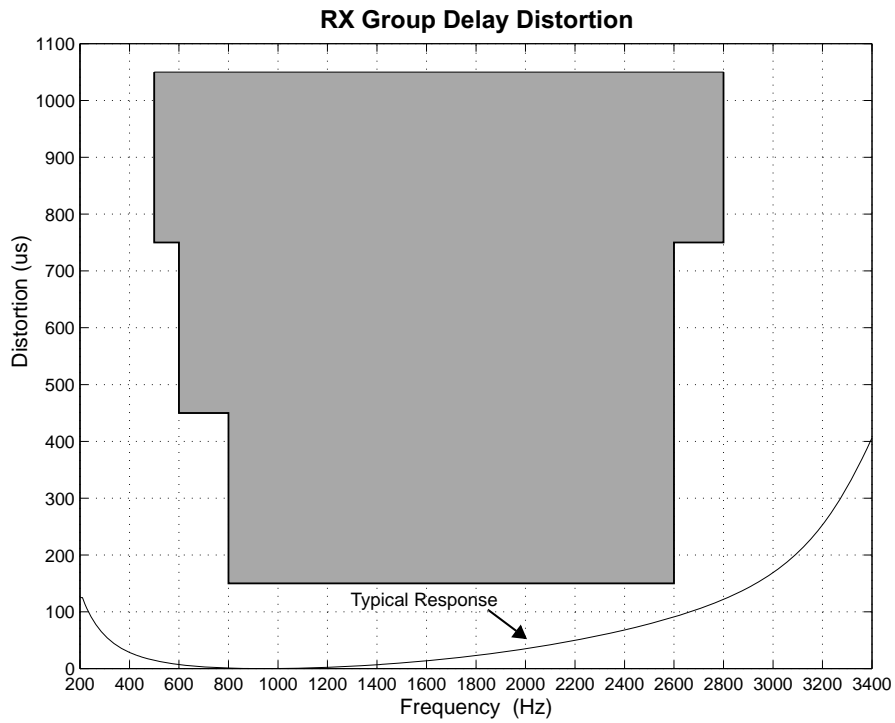


**Figure 6. Transmit Path Frequency Response**

# Si3217x-C

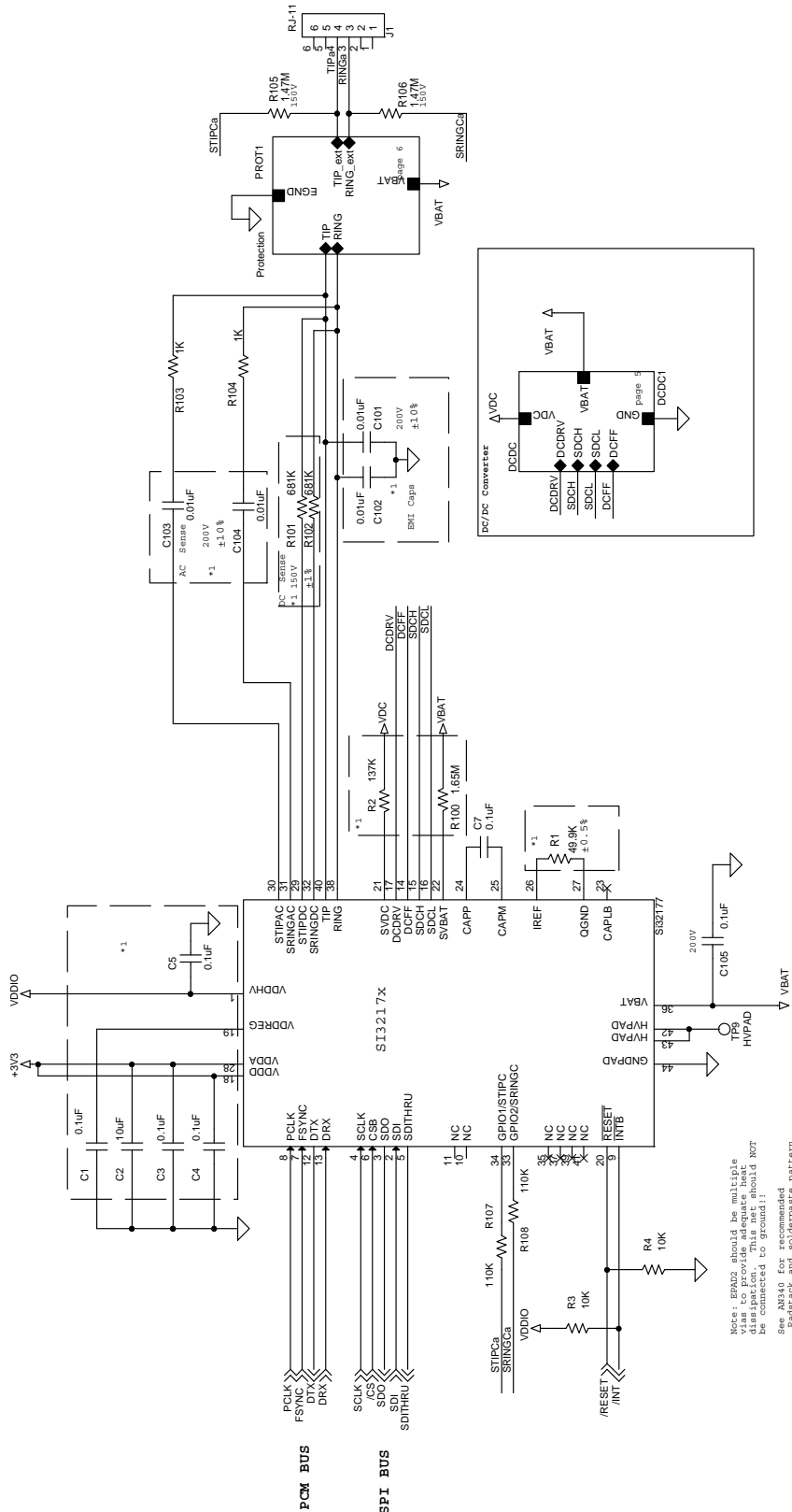


**Figure 7. Transmit Group Delay Distortion**



**Figure 8. Receive Group Delay Distortion**

2. Schematics



\*1: Place near 3217x Pin

Note: EPR20 should be multiple connected to ground for heat dissipation. This net should NOT be connected to ground!  
See AH40 for recommended Padstack and solderpaste pattern

Figure 9. Top Level Schematic



This design is optimized for VDC=8V-16V

Commercial Temp Only 0C-70C

VBAT < 95V

Ring Tracking not supported by this design

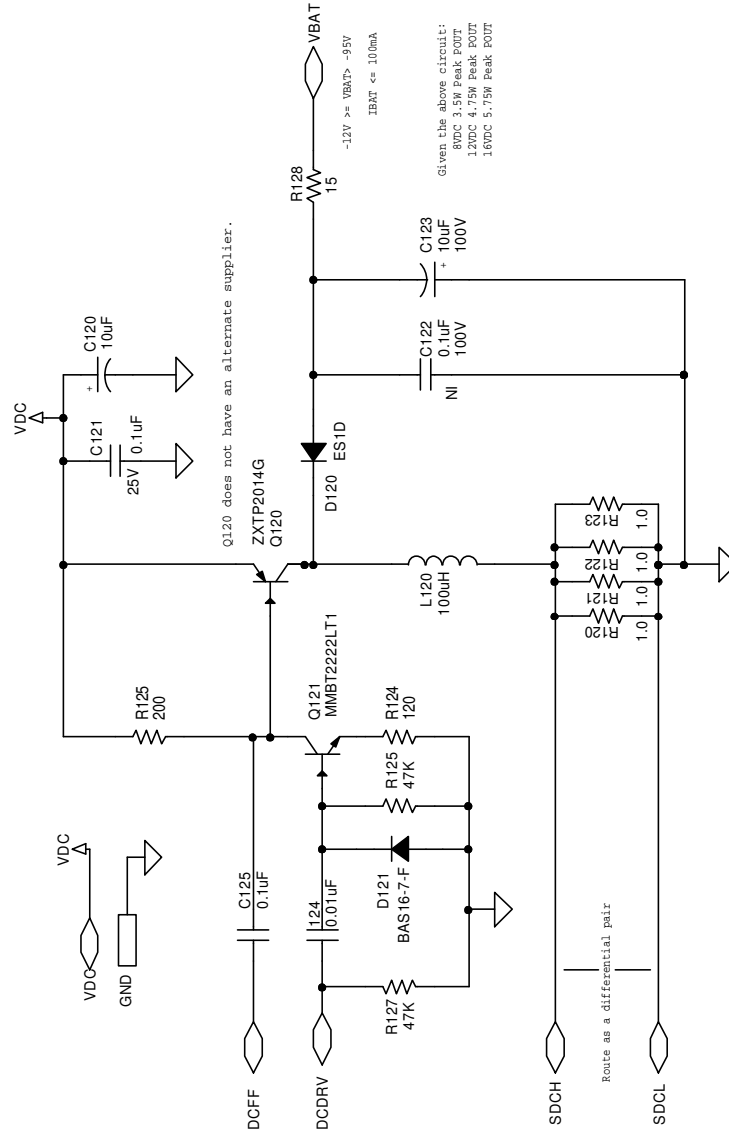


Figure 11. BJT Buck Boost DC-DC Option

# Si3217x-C

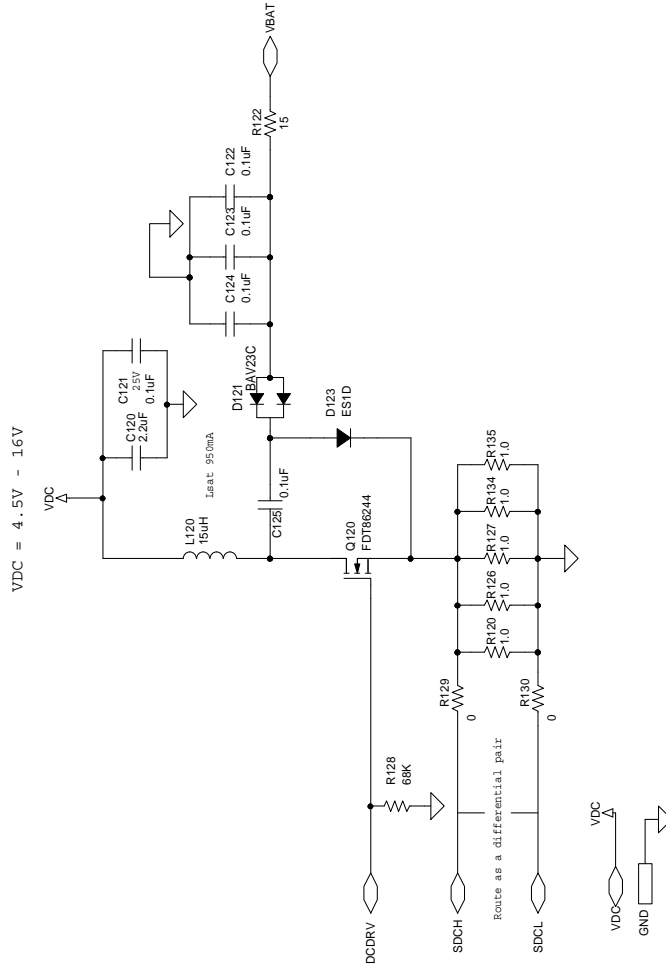


Figure 12. Si3217x-C Low Cost Quasi-Cuk DC-DC Schematic

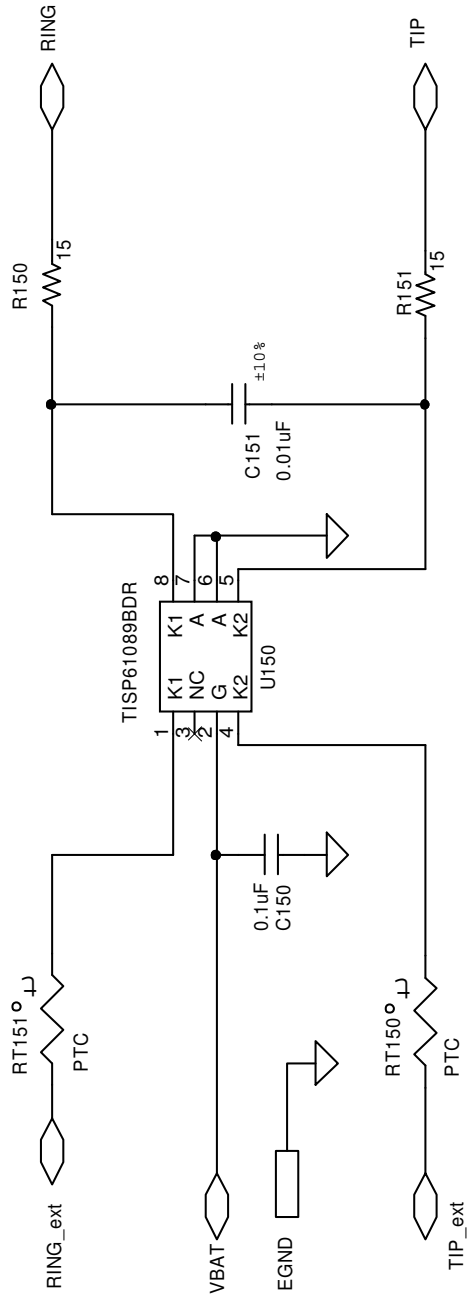


Figure 13. Protection

# Si3217x-C

## 3. Bill of Materials

**Table 12. Si3217x-C Top Level Bill of Materials**

| Reference           | Value        | Rating | Voltage | Tol        | Type      | PCB Footprint  | Mfr Part Number  | Mfr      |
|---------------------|--------------|--------|---------|------------|-----------|----------------|------------------|----------|
| C1 C3 C4 C5 C7      | 0.1 $\mu$ F  |        | 10V     | $\pm$ 10%  | X7R       | C0402          | C0402X7R100-104K | Venkel   |
| C2                  | 10 $\mu$ F   |        | 6.3V    | $\pm$ 20%  | X5R       | C0603          | C0603X5R6R3-106M | Venkel   |
| C101 C102 C103 C104 | 0.01 $\mu$ F |        | 200V    | $\pm$ 10%  | X7R       | C0805          | C0805X7R201-103K | Venkel   |
| C105                | 0.1 $\mu$ F  |        | 200V    | $\pm$ 20%  | X7R       | C1206          | C1206X7R201-104M | Venkel   |
| R1                  | 49.9K        | 1/16W  |         | $\pm$ 0.5% | ThickFilm | R0603          | CR0603-16W-4992D | Venkel   |
| R2                  | 137K         | 1/16W  |         | $\pm$ 1%   | ThickFilm | R0402          | CR0402-16W-2673F | Venkel   |
| R3 R4               | 10K          | 1/16W  |         | $\pm$ 5%   | ThickFilm | R0402          | CR0402-16W-103J  | Venkel   |
| R100                | 1.65M        | 1/10W  |         | $\pm$ 1%   | ThickFilm | R0805          | CR0805-10W-1654F | Venkel   |
| R101 R102           | 681K         | 1/10W  |         | $\pm$ 1%   | ThickFilm | R0805          | CR0805-10W-6813F | Venkel   |
| R103 R104           | 1K           | 1/16W  |         | $\pm$ 1%   | ThickFilm | R0402          | CR0402-16W-1001F | Venkel   |
| R105 R106           | 1.47M        | 1/8W   |         | $\pm$ 1%   | ThickFilm | R1206          | CR1206-8W-1474F  | Venkel   |
| R107 R108           | 110K         | 1/16W  |         | $\pm$ 1%   | ThickFilm | R0402          | CR0402-16W-1103F | Venkel   |
| U1                  | Si32170/7    |        | 140V    |            | MCM       | LGA42M5X7 P0.5 | Si32170/7-C-GM1  | Skyworks |

**Table 13. Si3217x-C Flyback Bill of Materials**

| Reference               | Value       | Rating | Volt | Tol       | Type      | PCB Footprint | Mfr Part Number  | Mfr       |
|-------------------------|-------------|--------|------|-----------|-----------|---------------|------------------|-----------|
| C120<br>(Not Installed) | 10 $\mu$ F  |        | 25   | $\pm$ 20% | X7R       | C1210         | C1210X7R250-106M | Venkel    |
| C122<br>(Not Installed) | 470 pF      |        | 100  | $\pm$ 10% | X7R       | C0603         | C0603X7R101-471K | Venkel    |
| D121<br>(Not Installed) | 75 V        | 200mW  | 75   |           | Zener     | SOD-323       | BZX384C75-V      | Vishay    |
| D122<br>(Not Installed) | BAS16X      | 200mA  | 75   |           | Switch    | SOD-523       | BAS16XV2T1G      | On Semi   |
| R125<br>(Not Installed) | 15          | 1/2W   |      | $\pm$ 5%  | ThickFilm | R1210         | CR1210-2W-150J   | Venkel    |
| C121                    | 0.1 $\mu$ F |        | 50   | $\pm$ 10% | X7R       | C0603         | C0603X7R500-104K | Venkel    |
| C123                    | 0.1 $\mu$ F |        | 10   | $\pm$ 10% | X7R       | C0402         | C0402X7R100-104K | Venkel    |
| C124 C125<br>C126       | 0.1 $\mu$ F |        | 200  | $\pm$ 20% | X7R       | C1206         | C1206X7R201-104M | Venkel    |
| D123                    | ES1F        | 1.0A   | 300  |           | Fast      | DO-214AC      | ES1F             | Fairchild |
| Q120                    | FQT7N10L    | 1.7A   | 100  |           | N-CHNL    | SOT223-GDS    | FQT7N10L         | Fairchild |
| R120                    | 0.1         | 1/2W   |      | $\pm$ 1%  | ThickFilm | R1210         | LCR1210-R100F    | Venkel    |

**Table 13. Si3217x-C Flyback Bill of Materials**

|           |           |       |  |     |           |                    |                  |        |
|-----------|-----------|-------|--|-----|-----------|--------------------|------------------|--------|
| R121 R122 | 0         | 1A    |  |     | ThickFilm | R0402              | CR0402-16W-000   | Venkel |
| R123      | 15        | 1/16W |  | ±1% | ThickFilm | R0402              | CR0402-16W-15R0F | Venkel |
| R124      | 68K       | 1/16W |  | ±5% | ThickFilm | R0402              | CR0402-16W-683J  | Venkel |
| R126      | 15        | 1/2W  |  | ±5% | ThickFilm | R1210              | CR1210-2W-150J   | Venkel |
| T120      | 8 $\mu$ H | 4A    |  |     |           | XFMR-<br>UTB01701s | UTB01890s        | UMEC   |

# Si3217x-C

**Table 14. Si3217x-C BJT Buck Boost Bill of Materials**

| Reference              | Value       | Rating | Volt | Tol  | Type      | PCB Footprint | Mfr Part Number  | Mfr               |
|------------------------|-------------|--------|------|------|-----------|---------------|------------------|-------------------|
| C122                   | 0.1 uF      |        | 100  | ±20% | X7R       | C0603         | C0603X7R101-104M | Venkel            |
| C120 C123              | 10 uF       |        | 100  | ±20% | Alum_Elec | C2X5MM-RAD    | ECA2AM100        | Panasonic         |
| C121 C125              | 0.1 uF      |        | 25   | ±20% | X7R       | C0603         | C0603X7R250-104M | Venkel            |
| D120                   | ES1D        | 1.0A   | 200  |      | Single    | DO-214AC      | ES1D             | Diodes Inc.       |
| D121                   | BAS16-7-F   | 300mA  | 75   |      | Single    | SOT23-AXK     | BAS16-7-F        | Diodes Inc.       |
| L120                   | 100 uH      | 3.64A  |      | ±20% | Shielded  | IND-SPD       | DR127-101-R      | Cooper<br>Bussman |
| Q120                   | ZXTP2014G   | 4A     | 140  |      | PNP       | SOT223-BCE    | ZXTP2014G        | Zetex             |
| Q121                   | MMBT2222LT1 | 600mA  | 30   |      | NPN       | SOT23-BEC     | MMBT2222LT1      | On Semi           |
| R120 R121<br>R122 R123 | 1           | 1/16W  |      | ±1%  | ThickFilm | R0402         | CR0402-16W-1R00F | Venkel            |
| R124                   | 120         | 1/10W  |      | ±1%  | ThickFilm | R0603         | CR0603-10W-1200F | Venkel            |
| R125 R127              | 47K         | 1/16W  |      | ±1%  | ThickFilm | R0402         | CR0402-16W-4702F | Venkel            |
| R125                   | 200         | 1/10W  |      | ±1%  | ThickFilm | R0603         | CR0603-10W-2000F | Venkel            |
| R128                   | 15          | 1/10W  |      | ±1%  | ThickFilm | R0805         | CR0805-10W-15R0F | Venkel            |
| C124                   | 0.01 µF     |        | 10   | ±20% | X7R       | C0402         | C0402X7R100-103M | Venkel            |

**Si3217x-C****Table 15. Si3217x-C Low Cost Quasi-Ćuk DC-DC BOM**

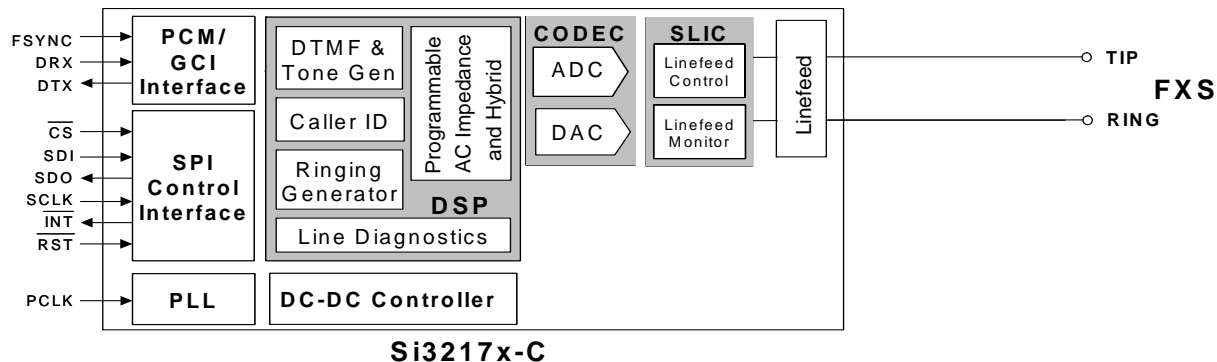
| Reference                           | Value       | Rating | Volt | Tol       | Type                          | PCB_Footprint | Mfr Part Number  | Mfr                  |
|-------------------------------------|-------------|--------|------|-----------|-------------------------------|---------------|------------------|----------------------|
| C102 C104<br>C107 C110<br>C117 C118 | 0.1 $\mu$ F |        | 10   | $\pm$ 10% | X7R                           | C0402 C0402L  | C0402X7R100-104K | Venkel               |
| C106                                | 10 $\mu$ F  |        | 6.3  | $\pm$ 20% | X5R                           | C0603 C0603L  | C0603X5R6R3-106M | Venkel               |
| C120                                | 2.2 $\mu$ F |        | 16   | $\pm$ 20% | X7R                           | C0805         | C0805X7R160-225M | Venkel               |
| C121                                | 0.1 $\mu$ F |        | 25   | $\pm$ 20% | X7R                           | C0603         | C0603X7R250-104M | Venkel               |
| C122 C123<br>C124 C125              | 0.1 $\mu$ F |        | 250  | $\pm$ 10% | X7T                           | C0805         | C2012X7T2E104K   | TDK Corpora-<br>tion |
| D121                                | BAV23C      | 400mA  | 200  |           | Dual Com-<br>mon Cath-<br>ode | SOT23-AAK     | BAV23C           | Diodes Inc.          |
| D123                                | ES1D        | 1.0A   | 200  |           | Fast                          | DO-214AC      | ES1D             | Diodes Inc.          |
| L120                                | 15 $\mu$ FH | 1.6A   |      | $\pm$ 20% | Shielded                      | IND-NR6028    | NR 6028T 150M    | Taiyo Yuden          |
| Q120                                | FDT86244    | 2.8A   | 150  |           | N-CHNL                        | SOT223-GDS4   | FDT86244         | Fairchild            |
| R120 R126<br>R127 R134<br>R135      | 1.0         | 1/16W  |      | $\pm$ 1%  | ThickFilm                     | R0402         | CR0402-16W-1R00F | Venkel               |
| R128                                | 68K         | 1/16W  |      | $\pm$ 5%  | ThickFilm                     | R0402         | CR0402-16W-683J  | Venkel               |
| R129 R130                           | 0           | 1A     |      |           | ThickFilm                     | R0402 R0402L  | CR0402-16W-000   | Venkel               |

**Table 16. Si3217x-C Protection Bill of Materials**

| Reference      | Value        | Rating | Volt | Tol       | Type      | PCB Footprint     | Mfr Part Number  | Mfr    |
|----------------|--------------|--------|------|-----------|-----------|-------------------|------------------|--------|
| C150           | 0.1 $\mu$ F  |        | 200  | $\pm$ 20% | X7R       | C1206             | C1206X7R201-104M | Venkel |
| C151           | 0.01 $\mu$ F |        | 200  | $\pm$ 10% | X7R       | C0805             | C0805X7R201-103K | Venkel |
| RT150<br>RT151 | PTC          | 3A     | 250  |           | TelCom    | PTC-MF-SM013/250V | MF-SM013/250V    | Bourns |
| R150 R151      | 15           | 1/10W  |      | $\pm$ 1%  | ThickFilm | R0805             | CR0805-10W-15R0F | Venkel |
| U150           | TISP61089BDR |        | -150 |           | SLIC      | SO8N6.0P1.27      | TISP61089BDR     | Bourns |

# Si3217x-C

## 4. Functional Description



**Figure 14. Si3217x-C Functional Block Diagram**

The Si3217x series provides all SLIC, codec, DTMF detection, and signal generation functions needed for one complete analog telephone interface. The Si3217x performs all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions; it also supports extensive metallic loop testing capabilities.

The Si3217x provides a standard voice-band (200 Hz– 3.4 kHz) audio codec and, optionally, an audio codec with both wideband (50 Hz–7 kHz) and standard voice-band modes. The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio bandwidth. The Si3217x incorporates a programmable dc-dc converter controller that reacts to line conditions to provide the optimal battery voltage required for each line-state. Si3217x-C ICs are available with voltage ratings of –110 V or –140 V to support a wide range of ringing voltages; see "9. Ordering Guide," on page 39 for the voltage rating of each Si3217x-C version.

Programmable on-hook voltage, programmable off-hook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC.

The Si3217x supports balanced 5 REN ringing with or without a programmable dc offset. The available voltage offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

## 5. FXS Features

### 5.1. DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in Figure 15. The constant-voltage region has a low resistance, typically  $160\ \Omega$ . The constant-current region approximates infinite resistance.

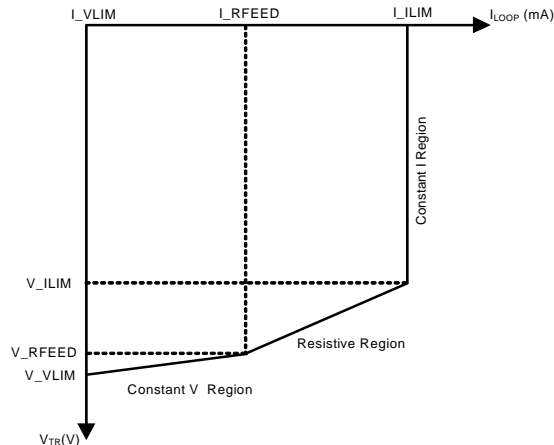


Figure 15. Dual ProSLIC DC Feed Characteristics

### 5.2. Linefeed Operating States

The linefeed interface includes eight different register-programmable operating states as listed in Table 17. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

### 5.3. Line Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip ADC and stores the resulting values in individual RAM locations. Additionally, the loop voltage ( $V_{TIP} - V_{RING}$ ), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

# Si3217x-C

## 6. Power Monitoring and Power Fault Detection

The Si3217x line monitoring functions are used to continuously protect against excessive power conditions. The Si3217x contains an on-chip, analog sensing diode that provides real-time temperature data and turns off the device when a preset threshold is exceeded.

If the Si3217x detects a fault condition or overpower condition, it automatically sets that device to the open state and generates a "power alarm" interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended since it is used to protect the Si3217x HVIC under excessive power conditions. The various power alarms and linefeed faults supporting automatic intervention are described below.

1. Total power exceeded.
2. Excessive foreign current or voltage on TIP and/or RING.
3. Thermal shutdown event.

### 6.1. Thermal Overload Shutdown

If the die temperature exceeds the maximum junction temperature threshold,  $T_{Jmax}$ , of 145 °C or 200 °C, the device has the ability to shut itself down to a low-power state without user intervention. The thermal shutdown circuit contains a sufficient amount of hysteresis and/or turn-on delay time so as to remain shut down during a power cross event, where 50 Hz or 60 Hz, 600 V, is connected to TIP and/or RING.

**Table 17. Linefeed Operating States**

| Linefeed State                   | Description   |
|----------------------------------|---|
| Open                             | Output is high-impedance, and all line supervision functions are powered down. Audio is powered down. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state. |
| Forward Active<br>Reverse Active | Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead. Loop closure and ground key detect circuitry are active.   |
| Forward OHT<br>Reverse OHT       | Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.  |
| TIP Open                         | Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 k $\Omega$ ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.  |
| RING Open                        | Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 k $\Omega$ ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.  |
| Ringing                          | Drives programmable ringing signal onto TIP and RING leads with or without dc offset.   |
| Line Diagnostics                 | The channel is put into diagnostic mode. In this mode, the channel has special diagnostic resources available.  |

## 6.2. Loop Closure Detection

The Si3217x provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

## 6.3. Ground Key Detection

The Si3217x provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

## 6.4. Ringing Generation

The Si3217x provides the ability to generate a programmable sinusoidal or trapezoidal ringing waveform, with or without dc offset. The ringing frequency, wave shape, cadence, and offset are all register-programmable. Three ringing modes are supported: balanced, unbalanced, and low-power ringing (LPR). Figure 16 illustrates the fundamental differences between the three ringing modes.

## 6.5. Polarity Reversal

The Si3217x supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

## 6.6. Two-Wire Impedance Synthesis

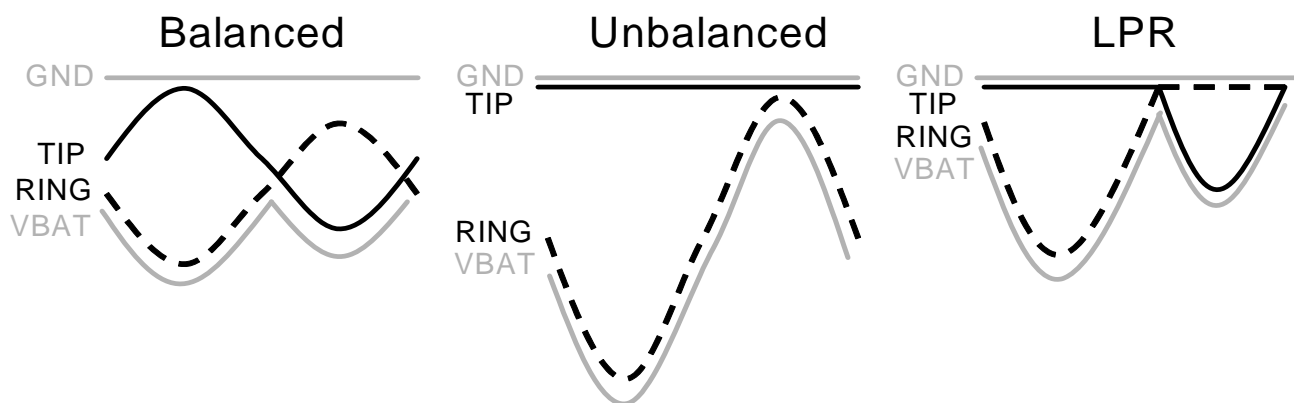
The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si3217x to the reference impedance. Most real or complex two-wire impedances can be generated with appropriate register coefficients.

## 6.7. Transhybrid Balance Filter

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path.

## 6.8. Tone Generators

The Si3217x includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.



**Figure 16. Ringing Modes**

# Si3217x-C

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## 6.9. DTMF Detection (Si32170/1/4 Only)

In DTMF, two tones generate a DTMF digit. One tone is chosen from four possible row tones, and one tone is chosen from four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits.

## 6.10. Pulse Metering (Si32170/1 Only)

The pulse metering system for the Si32170/1 is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of  $0.5 V_{RMS}$  at TIP and RING into a  $200 \Omega$  ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thus creating a trapezoidal envelope.

The amplitude is controlled by an automatic gain control circuit (AGC). While the tone is ramping up, the AGC takes the feedback audio and applies it to a band pass filter, which is programmed for the 12 or 16 kHz frequency of interest. When the peak is detected, the ramp is stopped.

See AN340 section 2.3.9 for additional details and considerations on Pulse Metering.

## 6.11. DC-DC Controller

The Si3217x-C devices integrate a dc-dc controller to control an external tracking dc-dc converter which generates the high voltage supply (VBAT) to the SLIC. The tracking VBAT voltage generated from a single positive dc input is optimized to minimize power consumption by closely tracking the SLIC state, even tracking the ringing waveforms.

The dc-dc controller output DCDRV is driven by an internal charge pump which allows it to connect directly to the gate of the MOSFET switch of the dc-dc converter. This eliminates the need for the MOSFET predrive circuit that is typically required when other SLICs are used with a MOSFET with  $V_{TH}$  greater than  $V_{DD}$ . See Table 7.

## 6.12. Wideband Audio

The Si32174/6/7 ICs support a software-selectable wideband (50 Hz–7 kHz) and narrowband (200 Hz–3.4 kHz) audio codec. The wideband mode provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. Wideband audio samples are transmitted and received on the PCM interface using two consecutive 8 kHz frames.

### 6.13. In-Circuit and Metallic Loop Testing (MLT)

A rich set of features is provided for in-circuit testing of the FXS system and the connected telephone line (MLT):

- Tone generators
- Audio diagnostic filters
- Digital and analog loop-back modes
- Internal test load
- Monitor ADC
- DSP algorithms

Using these facilities, it is possible to test the Si3217x's dc-dc converter, codec, line-feed, PCM bus interface, DSP, SPI bus interface, and call progress state-machine as well as testing the connected telephone line and external protection circuitry.

The audio diagnostic filters on the FXS are intended to provide programmable filtering of the TX digital audio signal and calculate the peak and/or average signal power of the filters' outputs. The signal powers are then compared to programmable thresholds. The programmable filters can be used to band-pass filter a certain tone or notch out certain tones, so that the signal power measurements are frequency selective. This filtering is useful in a telephony system because it can measure harmonic distortion, intermodulation, noise, etc.

The Si3217x incorporates an internal test load resistor that can be connected across Tip/Ring (Figure 17). The audio diagnostics system and built-in test load can be used to test the FXS interface (Si3217x) itself without requiring an external load, a connected line, or any relays. This facility can be used for production and in-service testing of such things as:

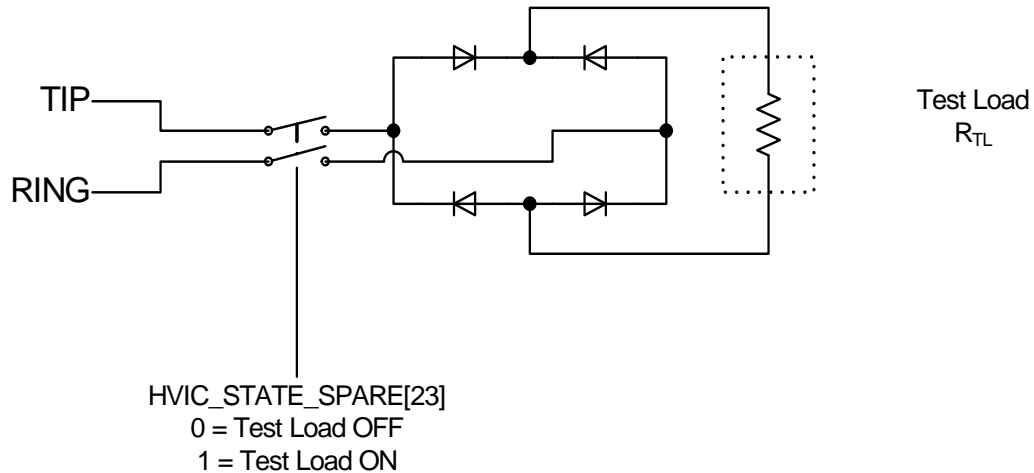
- Dial tone draw/break
- Audio quality measurements
- Pulse digit detection
- DC feed
- Ringtrip
- Polarity reversal
- Transmission loss

MLT, e.g., GR-909, is facilitated by the built-in DSP, monitor ADC, and test load. They provide the ability to detect multiple fault conditions within the CPE as well as on the Tip/Ring pair (T-R). Thirteen different measured and/or calculated parameters are reported by the Monitor ADC. Host software for use in conjunction with the ProSLIC API is available from Skyworks Solutions. Typical MLT tests include:

- Hazardous Potential Test – This checks for ac voltage  $> 50 V_{RMS}$  or dc voltage  $> 135 V$  between Tip and Ground (T-G) or Ring and Ground (R-G).
- Foreign Electromotive Force Test – Checks T-G or R-G for ac voltage  $> 10 V_{RMS}$  or dc voltage  $> 6 V$ . Uses same threshold as for hazardous voltage test.
- Resistive Faults Test – Checks for dc resistance from T-R, T-G or R-G. Any measurement  $< 150 k\Omega$  is considered a resistive fault.
- Receiver-Off-Hook Test – Distinguishes between a T-R resistive fault and an off-hook condition.
- Ringers Test – Measures the magnitude of the connected ring load (REN) across T-R. Results are  $> 0.175 REN$  and  $< 5 REN$  for a valid load
- AC Line Impedance (line length) – T-R, T-G, and R-G. Generates a tone at several specific frequencies (audio band) and measures the reflected signal amplitude (complex spectrum) that comes back (with transhybrid balance filter disabled). The reflected signal is then used to calculate the line impedance based on certain assumptions of wire gauge, etc.
- Line Capacitance – T-R, T-G, R-G. Generates a linear ramp function with polarity reversal, and measures the time constant.

## Si3217x-C

Diagnostic information is available even in the presence of fault conditions that cause the system's protection devices (fuses, PTCs, etc.) to open. A high-impedance sensing path (pins SRINGC and STIPC) can be used to measure the conditions on Tip/Ring even when the FXS system is effectively disconnected from the line. No relay is required and this sensing path inherently meets Dielectric Withstand per GR-49 (> 1000 V).



**Figure 17. Si3217x Internal Test Load Circuit**

## 7. System Interfaces

### 7.1. SPI Control Interface

The controller interface to the Si3217x is a 4-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CS), serial data input (SDI), and serial data output (SDO). In addition, the ProSLIC devices feature a serial data through output (SDITHRU) to support operation of up to 16 channels using a single chip select line. The FXS port occupies one SPI channel. The device operates with both 8-bit and 16-bit SPI controllers.

### 7.2. PCM Interface and Companding

The Si3217x contains a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM Mode Select, PCM Transmit Start, and PCM Receive Start settings.

The interface can be configured to support from 4 to 128 8-bit time slots in each 125  $\mu$ s frame, corresponding to a PCM clock (PCLK) frequency range of 256 kHz to 8.192 MHz. 1.544 MHz is also supported.

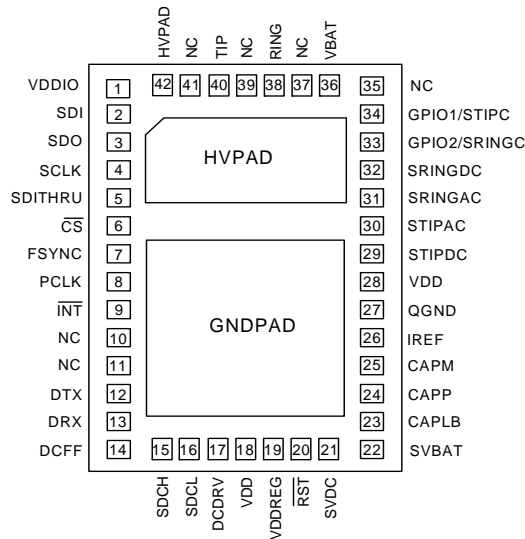
The Si3217x supports both  $\mu$ -255 Law ( $\mu$ -Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

### 7.3. Input/Output Voltage Selection

Revision C devices have the ability to gluelessly interface directly to 1.8 V devices via the PCM, SPI, Interrupt and RESET pins (SCLK, CS, SDI, SDO, SDITHRU, PCLK, FSYNC, DTX, DRX, INT, RST). The I/O voltage selection is made by attaching the desired voltage (3.3 V or 1.8 V) to the VDDIO pin (pin 1).

# Si3217x-C

## 8. Pin Descriptions: Si3217x-C



| Pin # | Pin Name                | Description  |
|-------|-------------------------|--|
| 1     | VDDIO                   | <b>IO Voltage Supply (3.3 V or 1.8 V).</b>   |
| 2     | SDI                     | <b>Serial Port Data Input.</b><br>Serial port control data input.  |
| 3     | SDO                     | <b>Serial Port Data Output.</b><br>Serial port control data output.  |
| 4     | SCLK                    | <b>Serial Port Bit Clock Input.</b><br>Serial port clock input. Controls the serial data on SDO and latches the data on SDI.                             |
| 5     | SDITHRU                 | <b>SDI Passthrough.</b><br>Cascaded SDI output signal for daisy-chain mode.  |
| 6     | $\overline{\text{CS}}$  | <b>Chip Select Input.</b><br>Active low. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, the serial port is operational. |
| 7     | FSYNC                   | <b>Frame Sync Clock Input.</b><br>8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.                                 |
| 8     | PCLK                    | <b>PCM Bus Clock Input.</b><br>Clock input for PCM bus timing.   |
| 9     | $\overline{\text{INT}}$ | <b>Interrupt Output.</b><br>Maskable interrupt output. Open drain output for wire-ORed operation.  |
| 10    | NC                      | No connection.   |
| 11    | NC                      | No connection.   |
| 12    | DTX                     | <b>Transmit PCM Data Output.</b><br>Output data to PCM bus.  |

| Pin # | Pin Name                | Description  |
|-------|-------------------------|--|
| 13    | DRX                     | <b>Transmit PCM Data Input.</b><br>Input data from PCM bus.  |
| 14    | DCFF                    | <b>DC Feed-Forward/High Current General Purpose Output</b><br>Feed-forward drive of external bipolar transistors to improve dc-dc converter efficiency |
| 15    | SDCH                    | <b>DC Monitor.</b><br>DC-DC converter monitor input used to detect overcurrent situations in the converter   |
| 16    | SDCL                    | <b>DC Monitor.</b><br>DC-DC converter monitor input used to detect overcurrent situations in the converter.  |
| 17    | DCDRV                   | <b>DC Drive/Battery Switch.</b><br>DC-DC converter control signal output which drives external bipolar transistor.                                     |
| 18    | VDD                     | <b>IC Voltage Supply.</b><br>3.3 V supply for internal circuitry.  |
| 19    | VDDREG                  | <b>1.8 V Regulated Core Power Supply.</b>  |
| 20    | $\overline{\text{RST}}$ | <b>Reset Input.</b><br>Active low input. Hardware reset used to place all control registers in the default state.                                      |
| 21    | SVDC                    | <b>DC-DC Input Voltage Sensor.</b><br>Senses $V_{DC}$ input to dc-dc converter.  |
| 22    | SVBAT                   | <b>VBAT Sense.</b><br>Analog current input used to sense voltage on dc-dc converter output voltage lead.   |
| 23    | CAPLB                   | <b>Calibration Capacitor.</b>  |
| 24    | CAPP                    | <b>SLIC Stabilization Capacitor.</b><br>Capacitor used in low pass filter to stabilize SLIC feedback loops.  |
| 25    | CAPM                    | <b>SLIC Stabilization Capacitor.</b><br>Capacitor used in low pass filter to stabilize SLIC feedback loops.  |
| 26    | IREF                    | <b>Current Reference Input.</b><br>Connects to an external resistor used to provide a high accuracy reference current.                                 |
| 27    | QGND                    | <b>Quiet Ground Reference Input.</b>   |
| 28    | VDD                     | <b>IC Voltage Supply.</b><br>3.3 V supply for internal circuitry.  |
| 29    | STIPDC                  | <b>TIP DC Sense.</b><br>Analog current input used to sense voltage on the TIP lead.  |
| 30    | STIPAC                  | <b>TIP AC Sense Input.</b><br>Analog ac input used to detect voltage on the TIP lead.  |

# Si3217x-C

| Pin # | Pin Name        | Description   |
|-------|-----------------|---|
| 31    | SRINGAC         | <b>RING AC Sense Input.</b><br>Analog ac input used to detect voltage on the RING lead  |
| 32    | SRINGDC         | <b>RING DC Sense Input.</b><br>Analog current input used to sense voltage on the RING lead.   |
| 33    | GPIO2<br>SRINGC | <b>General Purpose I/O.</b><br>RING Coarse Sense Input.<br>Voltage sensing outside protection circuit.  |
| 34    | GPIO1<br>STIPC  | <b>General Purpose I/O.</b><br>TIP Coarse Sense Input.<br>Voltage sensing outside protection circuit.   |
| 35    | NC              | <b>No Connect.</b><br>This pin should be left unbiased.   |
| 36    | VBAT            | <b>Battery Voltage Supply.</b><br>Connect to battery supply from dc-dc converter.   |
| 37    | NC              | <b>No Connect.</b><br>This pin should be left unbiased.   |
| 38    | RING            | <b>RING Terminal.</b><br>Connect to the RING lead of the subscriber loop.   |
| 39    | NC              | <b>No Connect.</b><br>This pin should be left unbiased.   |
| 40    | TIP             | <b>TIP Terminal.</b><br>Connect to the TIP lead of the subscriber loop.   |
| 41    | NC              | <b>No Connect.</b><br>This pin should be left unbiased.   |
| 42    | NC              | <b>No Connect.</b><br>This pin is internally connected to HVPAD and should be left unbiased.  |
| 43    | HVPAD           | <b>Exposed Paddle.</b><br>Connect to electrically-isolated low thermal impedance inner layer and/or backside thermal plane using multiple thermal vias. |
| 44    | GNDPAD          | <b>Exposed Paddle.</b><br>Connect to ground.  |

## 9. Ordering Guide

**Table 18. Si3217x Revision C Ordering Guide**

| P/N <sup>1</sup> | Description   | Package Type     | Max V <sub>BAT</sub> | Temperature  |
|------------------|---|------------------|----------------------|--------------|
| Si32170-C-FM1    | Narrowband FXS, PCM Interface, DTMF detection, pulse metering | LGA <sup>2</sup> | -140 V               | 0 to 70 °C   |
| Si32170-C-GM1    | Narrowband FXS, PCM Interface, DTMF detection, pulse metering | LGA <sup>2</sup> | -140 V               | -40 to 85 °C |
| Si32171-C-FM1    | Narrowband FXS, PCM Interface, DTMF detection, pulse metering | LGA <sup>2</sup> | -110 V               | 0 to 70 °C   |
| Si32171-C-GM1    | Narrowband FXS, PCM Interface, DTMF detection, pulse metering | LGA <sup>2</sup> | -110 V               | -40 to 85 °C |
| Si32174-C-FM1    | Wideband capable FXS, PCM Interface, DTMF detection           | LGA <sup>2</sup> | -110 V               | 0 to 70 °C   |
| Si32174-C-GM1    | Wideband capable FXS, PCM Interface, DTMF detection           | LGA <sup>2</sup> | -110 V               | -40 to 85 °C |
| Si32176-C-FM1    | Wideband capable FXS, PCM Interface                           | LGA <sup>2</sup> | -110 V               | 0 to 70 °C   |
| Si32176-C-GM1    | Wideband capable FXS, PCM Interface                           | LGA <sup>2</sup> | -110 V               | -40 to 85 °C |
| Si32177-C-FM1    | Wideband capable FXS, PCM Interface                           | LGA <sup>2</sup> | -140 V               | 0 to 70 °C   |
| Si32177-C-GM1    | Wideband capable FXS, PCM Interface                           | LGA <sup>2</sup> | -140 V               | -40 to 85 °C |

**Notes:**

1. Adding the suffix "R" to the part number (e.g. Si32176-C-FM1R) denotes tape and reel.
2. LGA - Land Grid Array.

# Si3217x-C

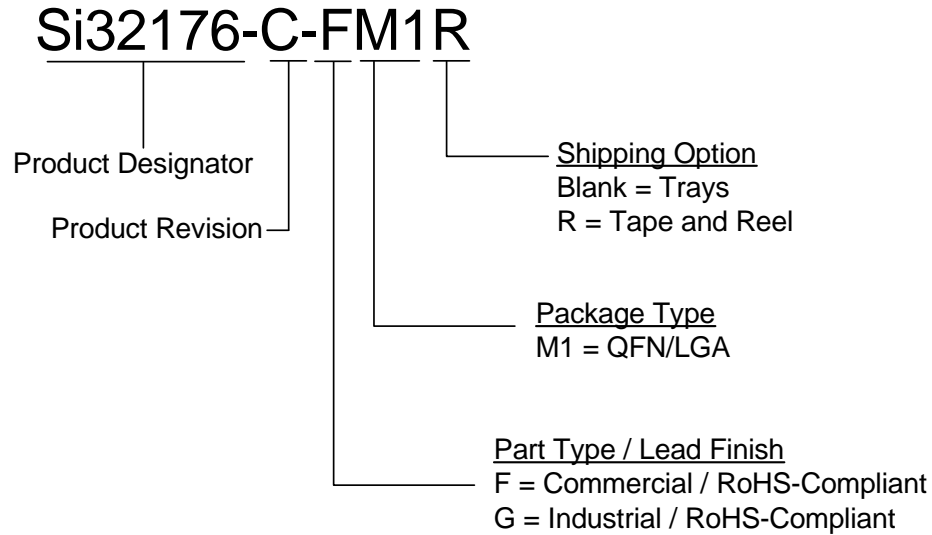
**Table 19. Ordering Guide—Si3217x Revision C Evaluation Kits**

| Part Number        | Description   | V <sub>BAT</sub> Max |
|--------------------|---|----------------------|
| Si32171CFB10SL0EVB | Narrowband FXS with DTMF detection and pulse metering, 110 V Flyback dc-dc converter (MOSFET and transformer based) EVB | -110 V               |
| Si32174CQC10SL0EVB | Wideband FXS with DTMF detection, 100 V low cost quasi-Cuk dc-dc converter (NMOS FET and inductor based) EVB            | -100 V               |
| Si32176CBB10SL0EVB | Wideband FXS, 100 V buck-boost dc-dc converter (BJT and inductor based) EVB   | -100 V               |
| Si32177CFB10SL0EVB | Wideband FXS, 138 V flyback dc-dc converter (MOSFET and transformer based) EVB  | -138 V               |

## 10. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



# Si3217x-C

## 11. Package Outline

### 11.1. 42-Pin QFN/LGA

Figure 18 illustrates the package details for the Si3217x. Table 20 lists the values for the dimensions shown in the illustration.

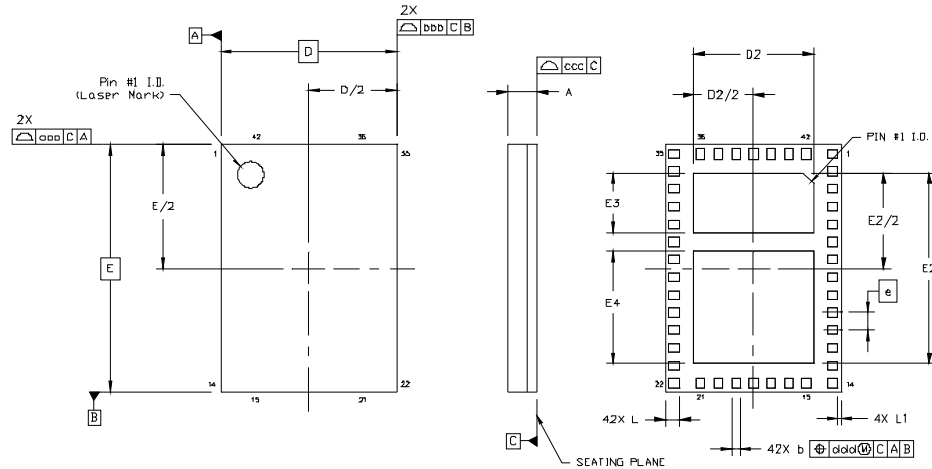


Figure 18. 42-Pin QFN/LGA Package

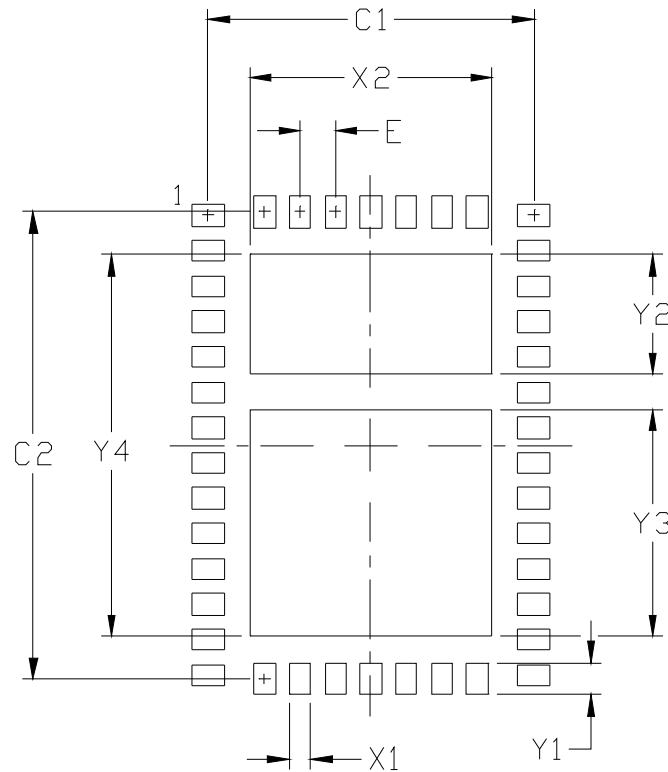
Table 20. 42-Pin QFN/LGA Package Diagram Dimensions

| Dimension | Min      | Nom  | Max  |
|-----------|----------|------|------|
| A         | 0.80     | 0.85 | 0.90 |
| b         | 0.20     | 0.25 | 0.30 |
| D         | 5.00 BSC |      |      |
| D2        | 3.35     | 3.40 | 3.45 |
| e         | 0.50 BSC |      |      |
| E         | 7.00 BSC |      |      |
| E2        | 5.35     | 5.40 | 5.45 |
| E3        | 1.65     | 1.70 | 1.75 |
| E4        | 3.15     | 3.20 | 3.25 |
| L         | 0.35     | 0.40 | 0.45 |
| L1        | 0.05     | 0.10 | 0.15 |
| aaa       | —        | —    | 0.10 |
| bbb       | —        | —    | 0.10 |
| ccc       | —        | —    | 0.08 |
| ddd       | —        | —    | 0.10 |

**Notes:**

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- Dimensioning and Tolerancing per ANSI Y14.5M-1994.
- Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 12. PCB Land Pattern Si3217x QFN



**Table 21. PCB Land Pattern**

| Dimension | mm   |
|-----------|------|
| C1        | 4.60 |
| C2        | 6.60 |
| E         | 0.50 |
| X1        | 0.30 |
| X2        | 3.45 |
| Y1        | 0.45 |
| Y2        | 1.75 |
| Y3        | 3.25 |
| Y4        | 5.45 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

# Si3217x-C

## 12.1. QFN PCB Design

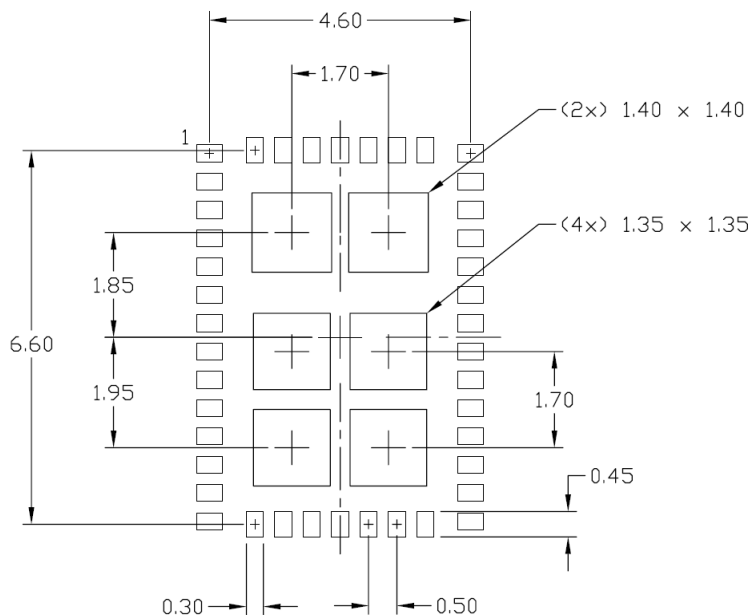
1. PCB design must ensure sufficient thermal relief for high power operation of the device. See layout guidelines in application note AN340 for further details.
2. A minimum of four vias are required under each E-Pad. Eight or more vias are recommended.
3. Via diameter should be between 0.20 and 0.31 mm.
4. Vias should either be filled or tented on the top side of the board to prevent solder thieving under the device.

## 12.2. QFN Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

## 12.3. QFN Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 1x2 array of 1.40 mm square openings on 1.7 mm pitch should be used for the top center pad and a 2x2 array of 1.35 mm square openings on 1.7 mm pitch should be used for the bottom center pad (as shown below).

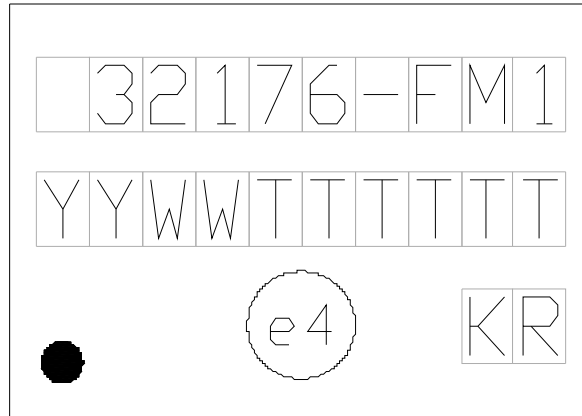


## 12.4. QFN Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

### 13. Top Markings

#### 13.1. Si3217x-C Package Top Marking



#### 13.2. Si3217x-C LGA Package Top Marking Explanation

|                        |  |  |
|------------------------|--|--|
| <b>Line 1 Marking:</b> | <b>Device Part Number</b>                        | <b>e.g., 32176-FM1</b>   |
| <b>Line 2 Marking:</b> | YY = Year<br>WW = Work Week                      | Assigned by the Assembly House. Corresponds to the year and work week of the assembly release. |
|                        | TTTTTT = Mfg Code                                | Manufacturing Code from the Assembly Purchase Order form.                                      |
| <b>Line 3 Marking:</b> | Circle = 0.5 mm Diameter<br>Lower Left-Justified | Pin 1 Identifier   |
|                        | Circle = 1.3 mm Diameter<br>Center-Justified     | "e4" Pb-Free Symbol  |
|                        | Country of Origin<br>ISO Code Abbreviation       | e.g., KR   |

# Si3217x-C

## DOCUMENT CHANGE LIST

### Revision 0.1 (Revision B to Revision C)

- First version of Si3217x revision C data sheet, based on Si3217x-Si3291x data sheet version 1.3
- Removed all references to Si32178 and Si3291x. DAA functionality for FXO support is not included in revision C devices. Refer to the most recent revision B data sheet for more information on these devices.
- Table 2 power supply characteristics changed to TBD pending characterization of revision C silicon
- Added support for 1.8 V I/O. Pin 1 changes from VDDHV to VDDIO (no impact to 3.3 V designs)
- Changed names of VDDA and VDDD pins to VDD.
- Added charge pump on DCDRV output to enable direct connection to dc-dc converter MOSFETs, see Table 12. Charge Pump Characteristics
- Si32171 pulse metering amplitude reduced to 0.5 VRMS
- Added new PMOS buck boost dc-dc converter schematics and EVBs
- Increased maximum VBAT of Si32177 to -140 V

### Revision 0.1 to Revision 1.0

- Added new part number Si32170
- Corrected formatting
- Added additional thermal resistance values  $\theta_{JB}$  and  $\theta_{JC}$
- Added supply current measurements to Table 2
- Changed test load resistor value to 2.2 k $\Omega$  (typical), was 5.3 k $\Omega$  in rev B
- Updated EVB ordering guide with new part numbers for revision C evaluation boards
- Corrected single frequency distortion (8-bit) values in Table 3 to show a maximum of -40 dB
- Deleted Table 5 (Monitor ADC Characteristics for FXS) to be consistent with Si3226x data sheets

### Revision 1.0 to Revision 1.1

- Added new part number Si32174 (wideband with DTMF detection)
- Renamed EPADs to use more descriptive names, HVPAD and GNDPAD
- Updated EVB part numbers
- Changed  $R_{TL}$  specification in Table 4 to replace typical value with a range from minimum to maximum
- Added support for 256 kHz PCLK over full temperature range.
- Removed notes specifying voltage and temperature conditions for Tables 2 through 9.
- Replaced PMOS buck boost DC-DC converter reference schematic with a quasi-Ćuk type design



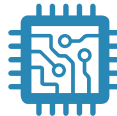
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