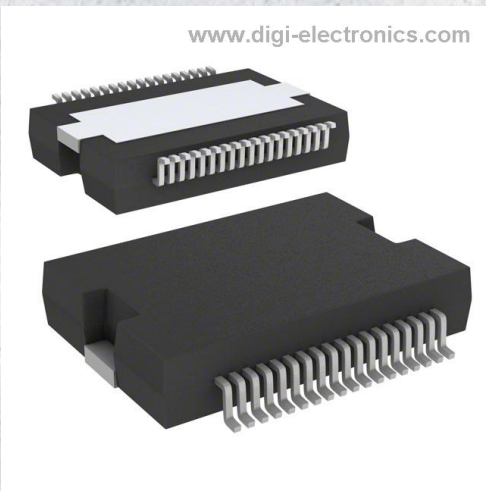
L6230PD Datasheet



DiGi Electronics Part Number	L6230PD-DG
Manufacturer	STMicroelectronics
Manufacturer Product Number	L6230PD
Description	IC MOTOR DRIVER 8V-52V 36POWERSO
Detailed Description	Motor Driver DMOS Parallel PowerSO-36

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Manufacturer Product Number:	Manufacturer:
L6230PD	STMicroelectronics
Series:	Product Status:
STSPIN L62	Active
Motor Type - Stepper:	Motor Type - AC, DC:
-	Brushless DC (BLDC)
Function:	Output Configuration:
Driver - Fully Integrated, Control and Power Stage	Half Bridge (3)
Interface:	Technology:
Parallel	DMOS
Step Resolution:	Applications:
-	General Purpose
Current - Output:	Voltage - Supply:
1.4A	8V ~ 52V
Voltage - Load:	Operating Temperature:
8V ~ 52V	-25°C ~ 125°C (TJ)
Mounting Type:	Package / Case:
Surface Mount	36-BSSOP (0.433", 11.00mm Width) Exposed Pad
Supplier Device Package:	Base Product Number:
PowerSO-36	L6230

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

life.augmented

L6230

Datasheet

DMOS driver for three-phase brushless DC motor

PowerS036

VFQFPN32

Features

- Operating supply voltage from 8 to 52 V
- 2.8 A output peak current (1.4 A RMS)
- $R_{DS(ON)}$ 0.73 Ω typ. value at T_J = 25 °C
- Integrated fast freewheeling diodes
- Operating frequency up to 100 kHz
- Non-dissipative overcurrent detection and protection
- Cross conduction protection
- Diagnostic output
- Uncommited comparator
- Thermal shutdown
- Undervoltage lockout

Applications

- BLDC motor driving
- Sinusoidal / six-step driving
- Field oriented control driving system

Description

The L6230 is a DMOS fully integrated 3-phase motor driver with overcurrent protection optimized for FOC application thanks to the independent current senses.

Realized in BCD technology, the device combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip.

An uncommitted comparator with open-drain output is available.

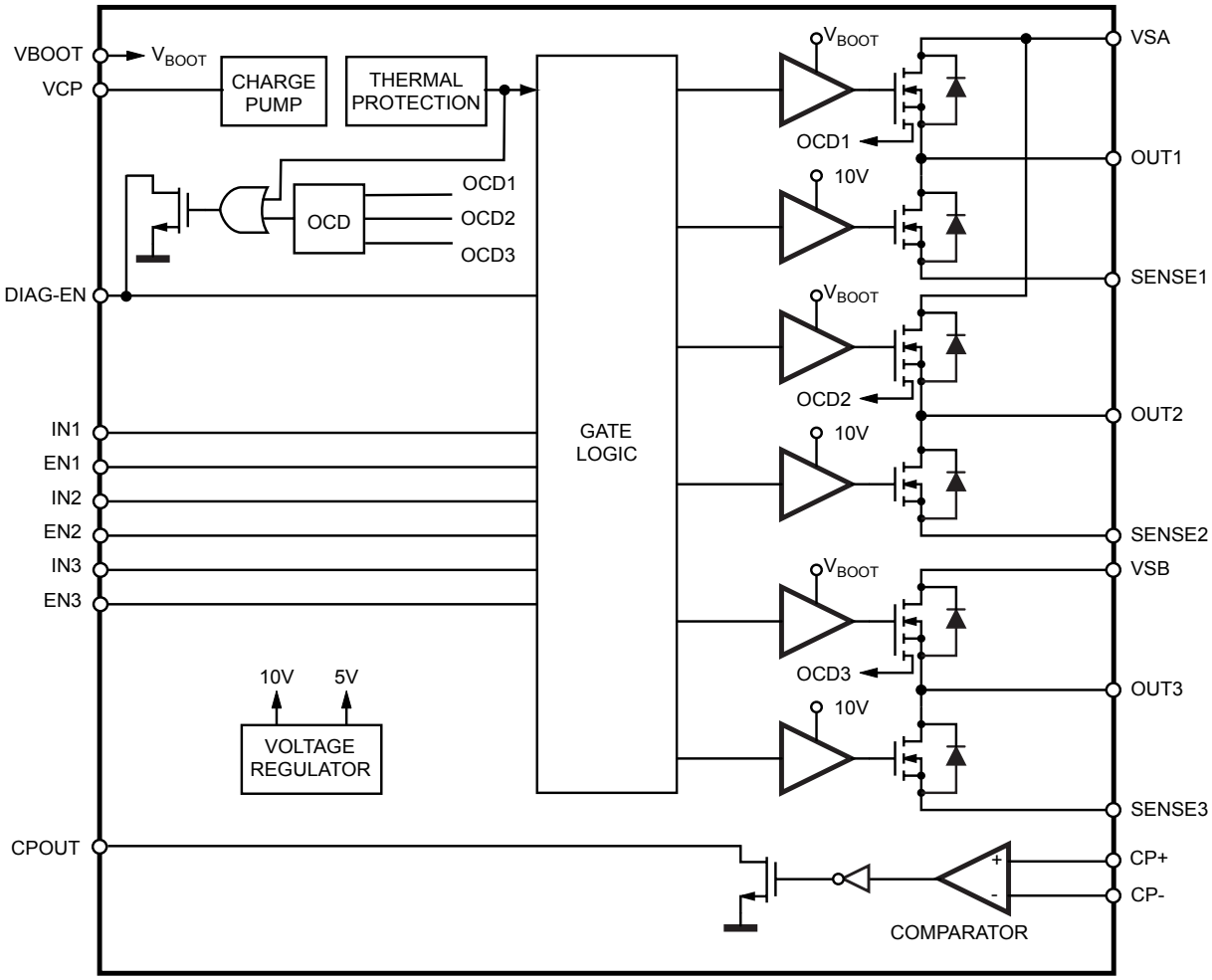
Available in Power SO36 and VFQFPN32 packages, the L6230 features a non-dissipative overcurrent protection on the high-side power MOSFET and thermal shutdown.

Product status link
L6230

Product label
SUSTAINABLE TECHNOLOGY

1 Block diagram

Figure 1. **Block diagram**



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply voltage	VSA = VSB = V_S	60	V
V_{OD}	Differential voltage between: VSA, OUT1, OUT2, SENSE1, SENSE2 and VSB, OUT3, SENSE3	VSA = VSB = V_S = 60 V V_{SENSEx} = GND	60	V
V_{BOOT}	Bootstrap peak voltage	VSA = VSB = V_S	V_S + 10	V
V_{IN}, V_{EN}	Logic inputs voltage range	-	-0.3 to 7	V
V_{CP-}, V_{CP+}	Voltage range at CP- and CP+ pins	-	-0.3 to 7	V
V_{SENSE}	Voltage range at SENSEx pins	-	-1 to 4	V
$I_{S(peak)}$	Pulsed supply current (for each VS pin)	VSA = VSB = V_S t_{PULSE} < 1 ms	3.55	A
I_S	RMS supply current (for each VS pin)	VSA = VSB = V_S	1.4	A
T_{stg}, T_{OP}	Storage and operating temperature range	-	-40 to 150	°C

2.2 Recommended operating condition

Table 2. Recommended operating condition

Symbol	Parameter	Test conditions	Min.	Max.	Unit
V_S	Supply voltage	VSA = VSB = V_S	8	52	V
V_{OD}	Differential voltage between: VSA, OUT1, OUT2, SENSE1, SENSE2 and VSB, OUT3, SENSE3	VSA = VSB = V_S V_{SENSE1} = V_{SENSE2} = V_{SENSE3}	-	52	V
V_{CP-}, V_{CP+}	Voltage range at pin VREF	-	-0.1	5	V
V_{CPM}	Common mode voltage at the comparator inputs	-	0	3	V
V_{SENSE}	Voltage range at SENSEx pins	pulsed t_W < t_{rr}	-6	6	V
		DC	-1	1	V
I_{OUT}	RMS output current	-	-	1.4	A
f_{SW}	Switching frequency	-	-	100	kHz
T_J	Operating junction temperature	-	-25	125	°C

2.3 Thermal data

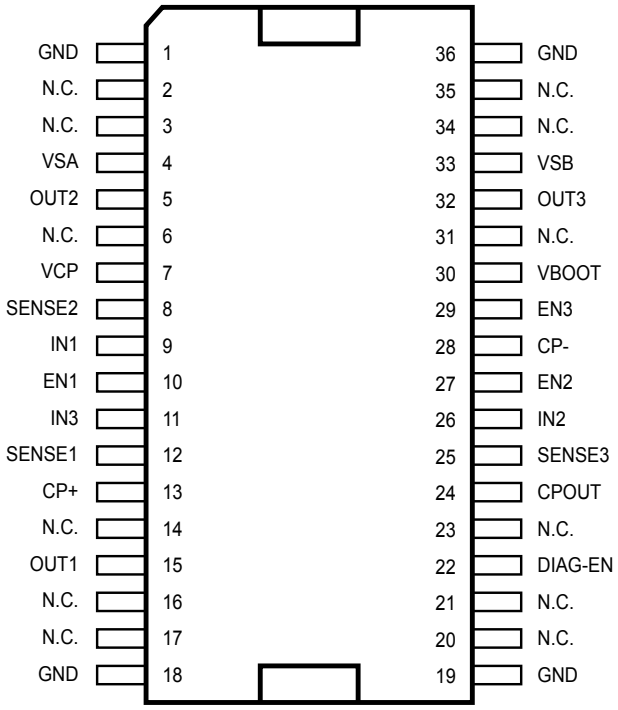
Table 3. Thermal data

Symbol	Description	Value		Unit
		PowerSO36	VFQFPN32	
$R_{th(j\text{-}amb)1}$	Maximum thermal resistance junction ambient (1)	36	-	°C/W
$R_{th(j\text{-}amb)1}$	Maximum thermal resistance junction ambient (2)	16	-	°C/W
$R_{th(j\text{-}amb)2}$	Maximum thermal resistance junction ambient (3)	63	-	°C/W
$R_{th(j\text{-}amb)3}$	Maximum thermal resistance junction ambient (4)	-	42	°C/W

1. *Mounted on a multilayer FR4 PCB with a dissipating copper surface on the bottom side of 6 cm^2 (with a thickness of 35 µm).*
2. *Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer.*
3. *Mounted on a multilayer FR4 PCB without any heat-sinking surface on the board.*
4. *Mounted on a double-layer FR4 PCB with a dissipating copper surface of 0.5 cm^2 on the top side plus 6 cm^2 ground layer connected through 18 via holes (9 below the IC).*

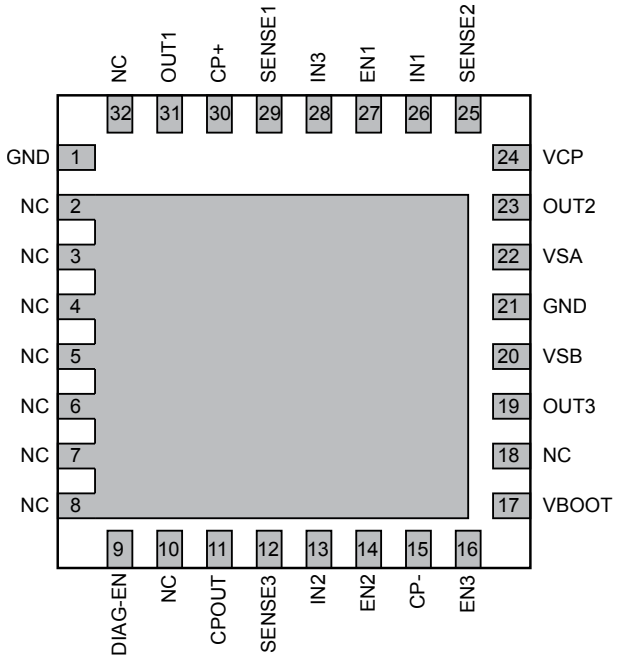
3 Pin connections

Figure 2. **Pin connection PowerSO36 (top view)**



Note: The slug is internally connected to pins 1, 18, 19, and 36 (GND pins).

Figure 3. **Pin connection VFQFPN32 (top view)**



Note: The pins 2 to 8 are connected to the die PAD.
The die PAD must be connected to the GND pin.

Table 4. Pin description

PowerSO36	VFQFPN32	Pin name	Type	Function
30	17	VBOOT	Power supply	Bootstrap voltage needed for driving the upper power MOSFETs.
7	24	VCP	Output	Charge pump oscillator output.
22	9	DIAG-EN	Logic output/ input	Double function: chip Enable as input and overcurrent/ overtemperature indication as output. LOW logic level switches OFF all power MOSFETs, putting the power stages in high impedance status. An internal open-drain transistor pulls to GND the pin when an overcurrent on one of the high-side MOSFETs is detected or during thermal protection.
9	26	IN1	Logic input	Driving input half-bridge 1.
10	27	EN1	Logic input	Enable input half-bridge 1.
26	13	IN2	Logic input	Driving input half-bridge 2.
27	14	EN2	Logic input	Enable input half-bridge 2.
11	28	IN3	Logic input	Driving input half-bridge 3.
29	16	EN3	Logic input	Enable input half-bridge 3.
28	15	CP-	Analog input	Inverting input of internal comparator.
13	30	CP+	Analog input	Non-inverting input of internal comparator.
24	11	CPOUT	Output	Open-drain output of internal comparator.
25	12	SENSE3	Power supply	Half-bridge 3 source pin. This pin must be connected to power ground through a sensing power resistor.
32	19	OUT3	Power output	Output half-bridge 3.
33	20	VSB	Power supply	Half-bridge 3 power supply voltage. It must be connected to the supply voltage together with pin VSA.
8	25	SENSE2	Power supply	Half-bridge 2 source pin. This pin must be connected to power ground through a sensing power resistor.
5	23	OUT2	Power output	Output half-bridge 2.
12	29	SENSE1	Power supply	Half-bridge 1 source pin. This pin must be connected to power ground through a sensing power resistor.
15	31	OUT1	Power output	Output half-bridge 1.
4	22	VSA	Power supply	Half-bridge 1 and half-bridge 2 power supply voltage. It must be connected to the supply voltage together with pin VSB.
1, 18, 19, 36	1	GND	Ground	Ground terminal.
-	2, 3, 4, 5, 6, 7, 8	NC	-	These pins are connected to the die PAD. The die PAD must be connected to the GND pin.
2, 3, 6, 14, 16, 17, 20, 21, 23, 31, 34, 35	10, 18, 32	NC	-	Not connected.

4 Electrical characteristics

Test conditions: V_S = 48 V, T_{amb} = 25 °C , unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{Sth(ON)}$	Turn ON threshold		5.8	6.3	6.8	V
$V_{Sth(OFF)}$	Turn OFF threshold		5	5.5	6	V
I_S	Quiescent supply current	All bridges OFF; T_J = -25 to 125 °C (1)	-	5	10	mA
$T_{J(OFF)}$	Thermal shutdown temperature		-	165	-	°C
Output DMOS transistors						
$R_{DS(ON)}$	High-side / low-side switch ON resistance	T_J = 25 °C	-	0.73	0.85	Ω
		T_J = 125 °C (1)	-	1.18	1.35	Ω
I_{DSS}	Leakage current	DIAG-EN = LOW; OUT = V_S	-	-	2	mA
		DIAG-EN = LOW; OUT = GND	-0.3	-	-	mA
Source drain diodes						
V_{SD}	Forward ON voltage	I_{SD} = 1.4 A, DIAG-EN = LOW	-	1.15	1.3	V
t_{rr}	Reverse recovery time	I_f = 1.4 A	-	300	-	ns
t_{fr}	Forward recovery time		-	200	-	ns
Logic input (INx, ENx, DIAG-EN)						
V_{IL}	Low level logic input voltage		-	-	0.8	V
V_{IH}	High level logic input voltage		2	-	-	V
I_{IL}	Low level logic input current	0 V logic input voltage	-10	-	-	µA
I_{IH}	High level logic input current	7 V logic input voltage	-	-	10	µA
Switching characteristics						
$t_{D(ON)EN}$	Enable to out turn-on delay time (2)	I_{LOAD} = 1.4 A, resistive load	500	650	800	ns
$t_{D(OFF)EN}$	Enable to out turn-off delay time(2)		500	-	1000	ns
$t_{D(ON)IN}$	Other logic inputs to output turn-on delay time		-	1.6	-	µs
$t_{D(OFF)IN}$	Other logic inputs to out turn-off delay time		-	800	-	ns
t_{RISE}	Output rise time (2)		40	-	250	ns
t_{FALL}	Output fall time (2)		40	-	250	ns
t_{DT}	Dead time		0.5	1	-	µs
f_{CP}	Charge pump frequency	T_J = -25 to 125 °C(1)	-	0.6	1	MHz
Comparator						
V_{OFFSET}	Offset voltage	V_{CP-} = 0.5 V	-14	-	+14	mV
t_{prop}	Turn OFF propagation delay	(3)	-	500	-	ns
I_{BIAS}	Input bias current		-	-	10	µA
R_{CPOUT}	Open-drain ON resistance		-	40	60	Ω

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Overcurrent detection and protection						
I_{SOVER}	Supply overcurrent protection threshold	T_J = -25 to 125 °C(1)	2	2.8	3.55	A
R_{DIAG}	Open drain ON resistance	I_{DIAG} = 4 mA	-	40	60	Ω
$t_{OCD(ON)}$	OCD turn-ON delay time(4)	I_{DIAG} = 4mA; C_{DIAG} < 100 pF	-	200	-	ns
$t_{OCD(OFF)}$	OCD turn-OFF delay time(4)	I_{DIAG} = 4mA; C_{DIAG} < 100 pF	-	100	-	ns

1. *Tested at 25 °C in a restricted range and guaranteed by characterization.*
2. *See Figure 4: Switching characteristic definition.*
3. *Measured applying a voltage of 1 V to pin CP- and a voltage drop from 2 V to 0 V to pin CP+.*
4. *See Figure 5.*

Figure 4. Switching characteristic definition

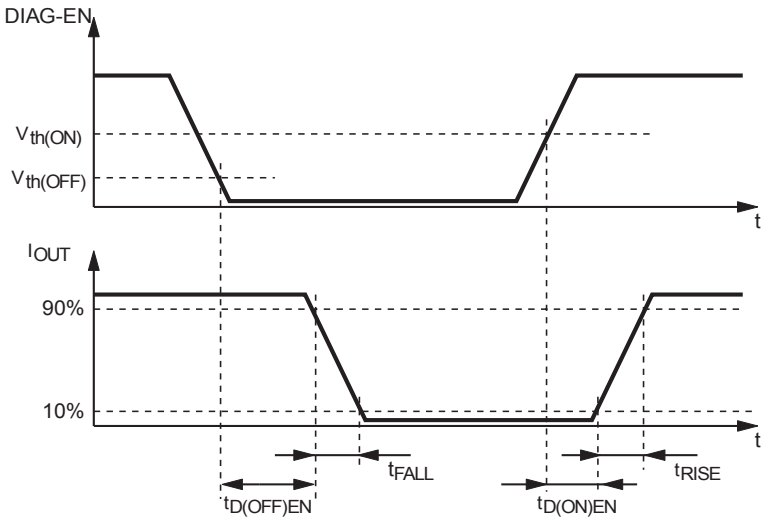
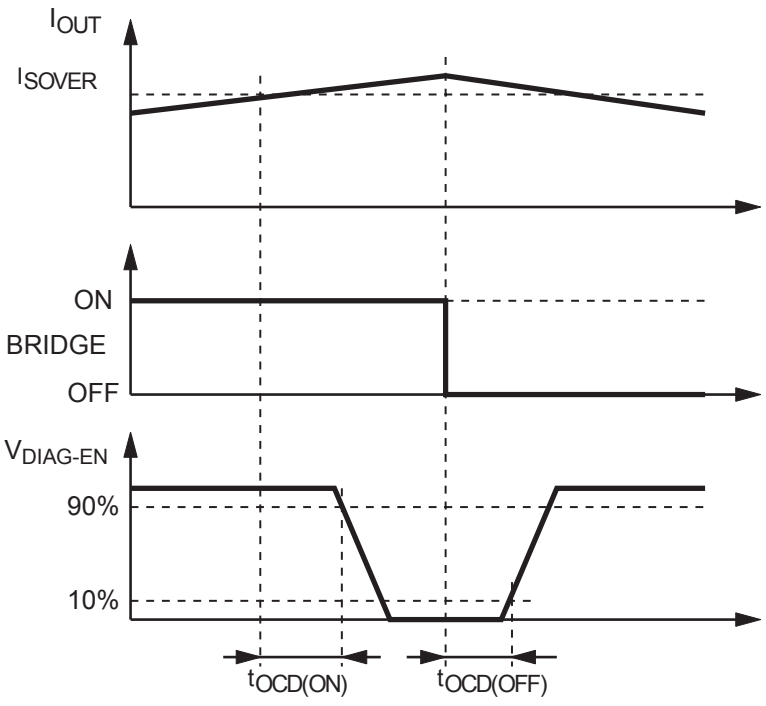


Figure 5. Overcurrent detection timing definition



5 Circuit description

5.1 Power stages and charge pump

The L6230 device integrates a triple half-bridge bridge, which consists of 6 power MOSFETs connected as shown in the block diagram (see Figure 1), each power MOSFET has an $R_{DS(ON)}$ = 0.73 Ω (typical value at 25 °C) with intrinsic fast free-wheeling diode. Cross conduction protection is implemented by using a deadtime (t_{DT} = 1 µs typical value) set by internal timing circuit between the turn off and turn on of two power MOSFETs in one leg of a bridge.

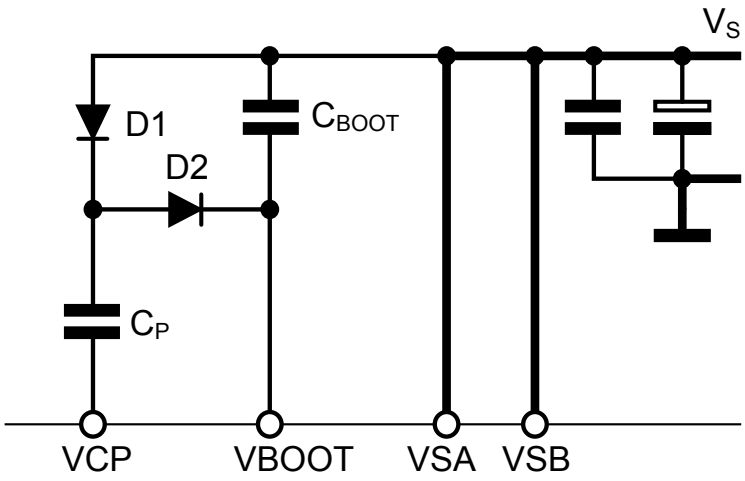
Pins VSA and VSB must be connected together to the supply voltage (V_S).

Using N-channel power MOSFET for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped supply (V_{BOOT}) is obtained through an internal oscillator and few external components to realize a charge pump circuit as shown in Figure 6. The oscillator output (pin VCP) is a square wave at 600 kHz (typically) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table 6.

Table 6. Charge pump external component values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
D_1	1N4148
D_2	1N4148

Figure 6. Charge pump circuit



5.2 Logic inputs

Pins INx and ENx are TTL/CMOS and microcontroller compatible logic inputs. The internal structure is shown in Figure 7. Typical value for turn-ON and turn-OFF thresholds are respectively $V_{th(ON)}$ = 1.8 V and $V_{th(OFF)}$ = 1.3 V.

The pin DIAG-EN has identical input structure with the exception that the drain of the overcurrent and thermal protection MOSFET is also connected to this pin. Due to this connection some care needs to be taken in driving this pin. The EN input may be driven in one of two configurations as shown in Figure 8 or Figure 9. If driven by an open-drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in Figure 8. If the driver is a standard push-pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in Figure 9.

The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF. More information for selecting the values can be found in Section 5.3.

Figure 7. Logic input internal structure

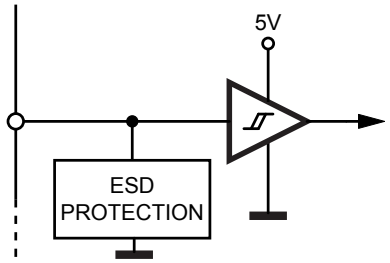


Figure 8. Pin DIAG-EN open collector driving

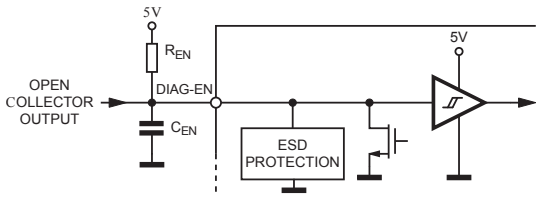


Figure 9. Pin DIAG-EN push-pull driving

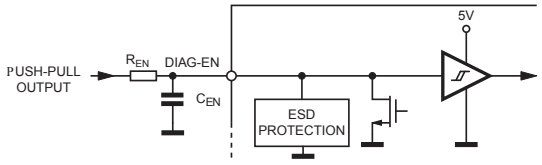


Table 7. Truth table

Inputs			Outputs
DIAG-EN	ENx	INx	OUTx
L	X (1)	X (1)	High-Z (2) (3)
H	L	X (1)	High-Z (2)
H	H	L	Low-side MOSFET on
H	H	H	High-side MOSFET on

1. *X: don't care.*
2. *High impedance output (both high-side and low-side MOSFETs off).*
3. *All half-bridges disabled.*

5.3 Non-dissipative overcurrent detection and protection

The L6230 device integrates an “Overcurrent Detection” circuit (OCD) for full protection. This circuit provides output to output and output to ground short-circuit protection as well.

With this internal overcurrent detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Figure 10 shows a simplified schematic for the overcurrent detection circuit.

To implement the overcurrent detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high-side power MOSFET. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold (typically I_{SOVER} = 2.8 A) the OCD comparator signals a fault condition. When a fault condition is detected, an internal open-drain MOSFET with a pull down capability of 4 mA connected to pin DIAG is turned on.

The pin DIAG-EN can be used to signal the fault condition to a microcontroller or to shut down the 3-phase bridge simply by connecting it to pin EN and adding an external R-C (see R_{EN}, C_{EN}).

Figure 10. Overcurrent protection simplified schematic

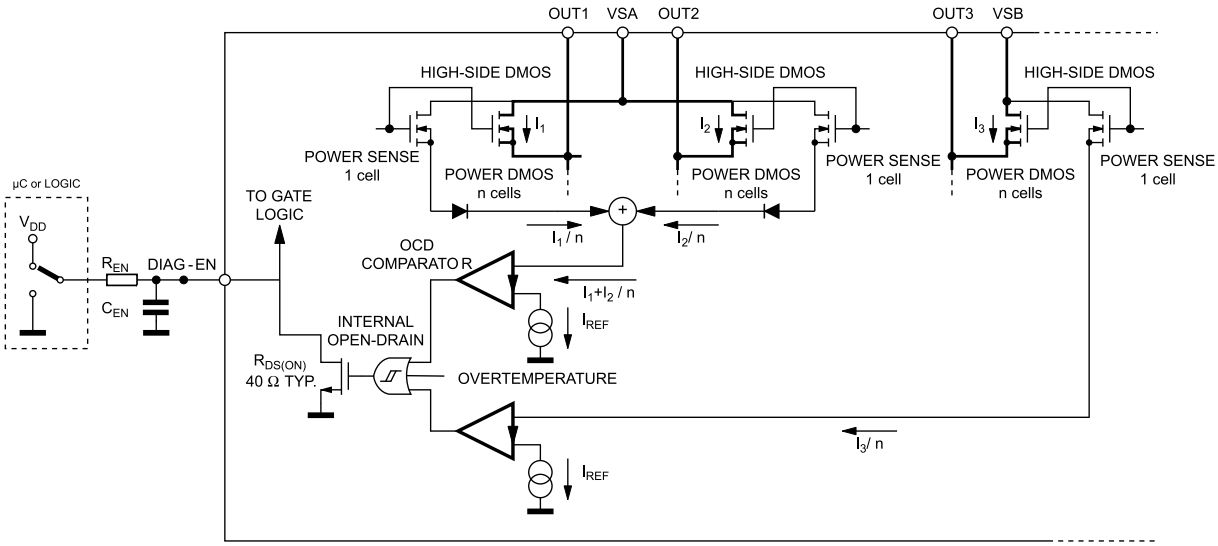


Figure 11 shows the overcurrent detection operation. The disable time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in Figure 12. The delay time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in Figure 13.

The C_{EN} is also used for providing immunity to pin DIAG-EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF that allow obtaining 200 µs disable time.

Figure 11. **Overcurrent protection waveforms**

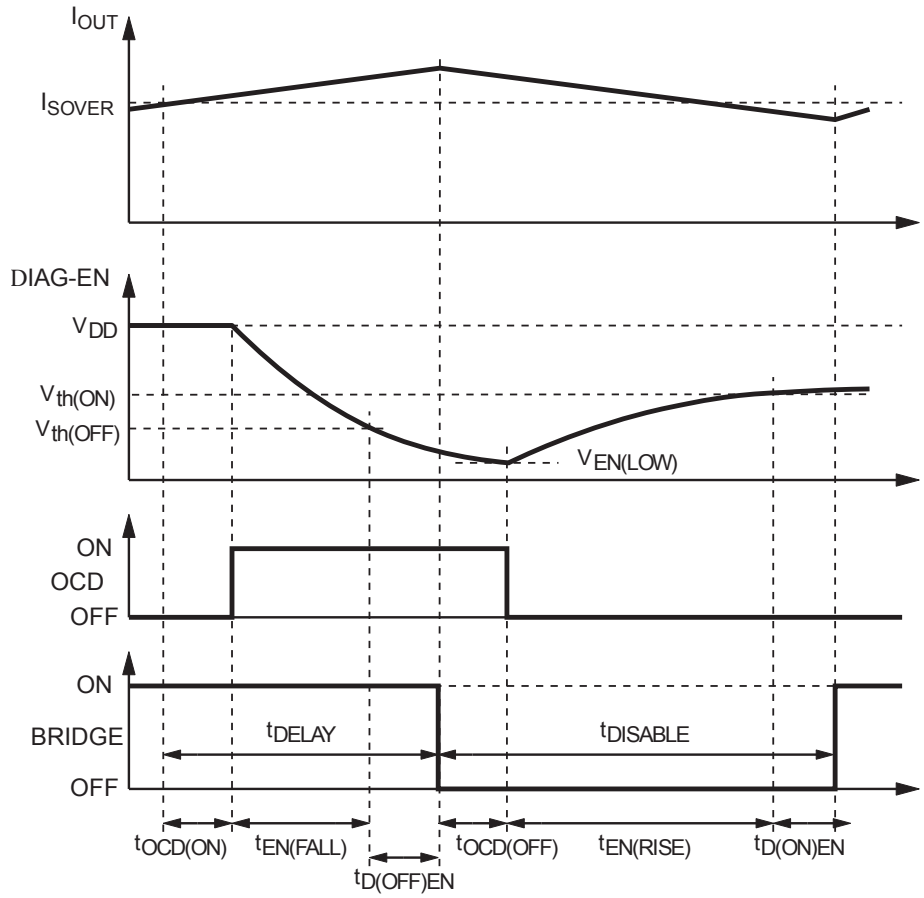


Figure 12. **$t_{DISABLE}$ versus C_{EN} and R_{EN}**

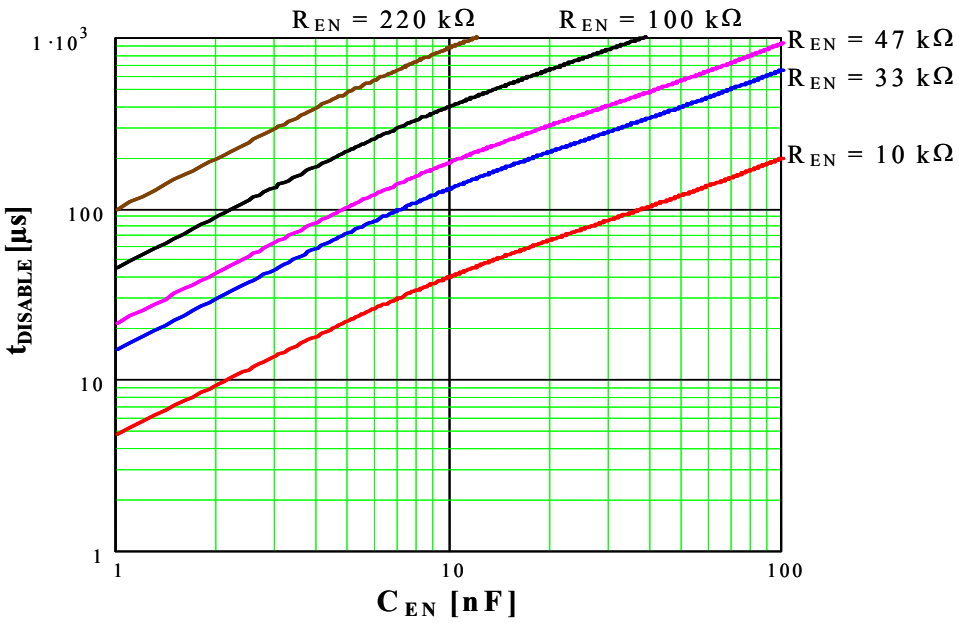
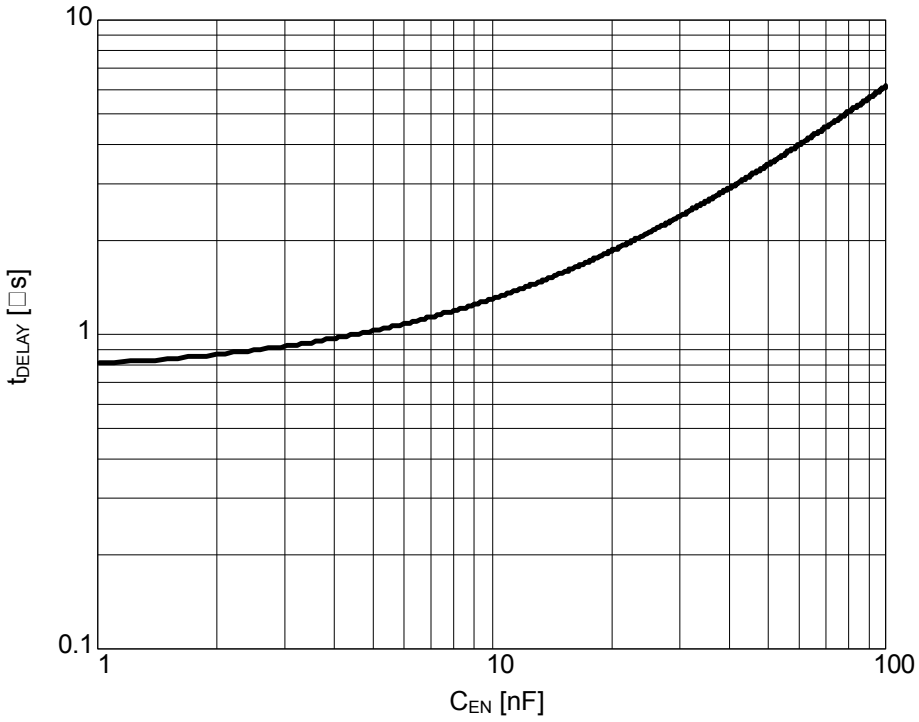


Figure 13. t_{DELAY} versus C_{EN}



6 Application information

A typical application using the L6230 device is shown in this section.

A high quality ceramic capacitor (C_2) in the range of 100 nF to 200 nF should be placed between the power pins VSA and VSB and ground near the L6230 device to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching.

The capacitor (C_{EN}) connected from the DIAG-EN input to ground sets the shutdown time when an overcurrent is detected (see Section 5.3).

The current sensing inputs (SENSEx) should be connected to the sensing resistor R_{SENSE} with a trace length as short as possible in the layout. The sense resistor should be non-inductive resistor to minimize the dI/dt transients across the resistor. To increase noise immunity, unused logic pins are best connected to 5 V (high logic level) or GND (low logic level), see Table 4. It is recommended to keep power ground and signal ground separated on PCB.

Table 8. Component values for typical application

Component	Value
C_1	100 µF
C_2	100 nF
C_{BOOT}	220 nF
C_{EN}	5.6 nF
C_P	10 nF
D_1	1N4148
D_2	1N4148
R_{EN}	100 kΩ

The examples reported describe some typical application to drive a 3-phase BLDC motor using the L6230 device.

In the first example is shown a field oriented control (FOC) system, with this method it is possible to provide smooth and precise motor control of BLDC motors.

A six-step driving method with current control is reported in the second example, the inputs sequence is generated by an external controller and the L6230 comparator is used to obtain the information for the peak current control.

Finally, the third example shows how to implement a sensorless motor control system, the information on the rotor position is achieved by BEMF zero-crossing detection.

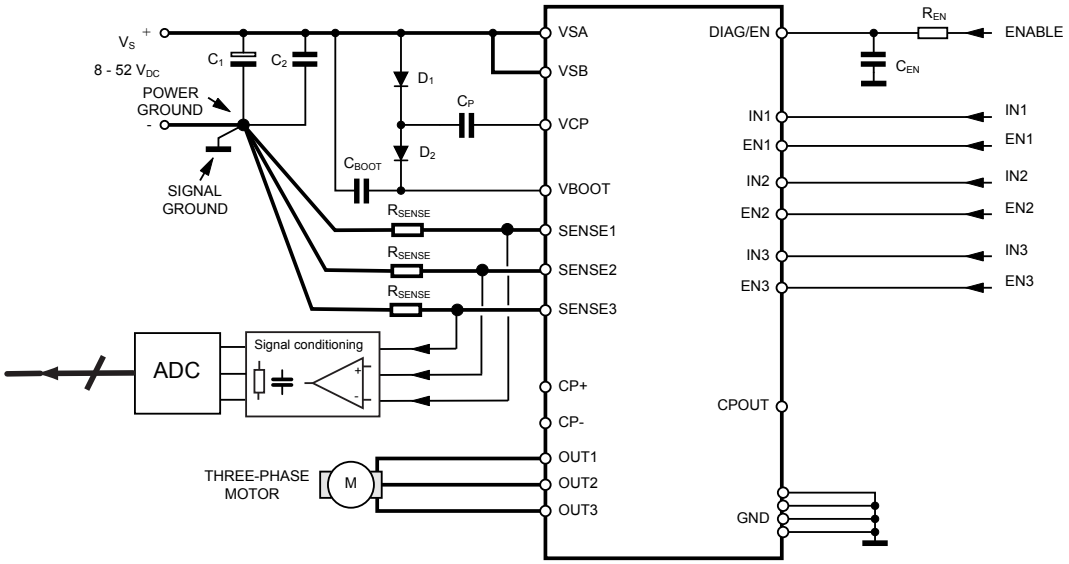
6.1 Field oriented control driving method

In this configuration (see Figure 14) three sensing resistors are required, one for each channel. The sensing signals coming from the output power stage are conditioned by external operational amplifiers which provide the proper feedback signals to the AtoD converter and the system controller. According to the feedback signals the six input lines are generated by the controller.

Note that some filtering and level shifting RC networks should be added between the sense resistor and the correspondent op-amp input.

The uncommitted internal comparator with open-drain output is available.

Figure 14. F.O.C. typical application



6.2 Six-step driving method with current control

In this configuration only one sense resistor is needed, the three OUT pins are connected together to the R_{SENSE} (see Figure 15).

The inverting input comparator CP- monitors the voltage drop across the external sense resistor connected between the source of the three lower power MOSFET transistors and ground.

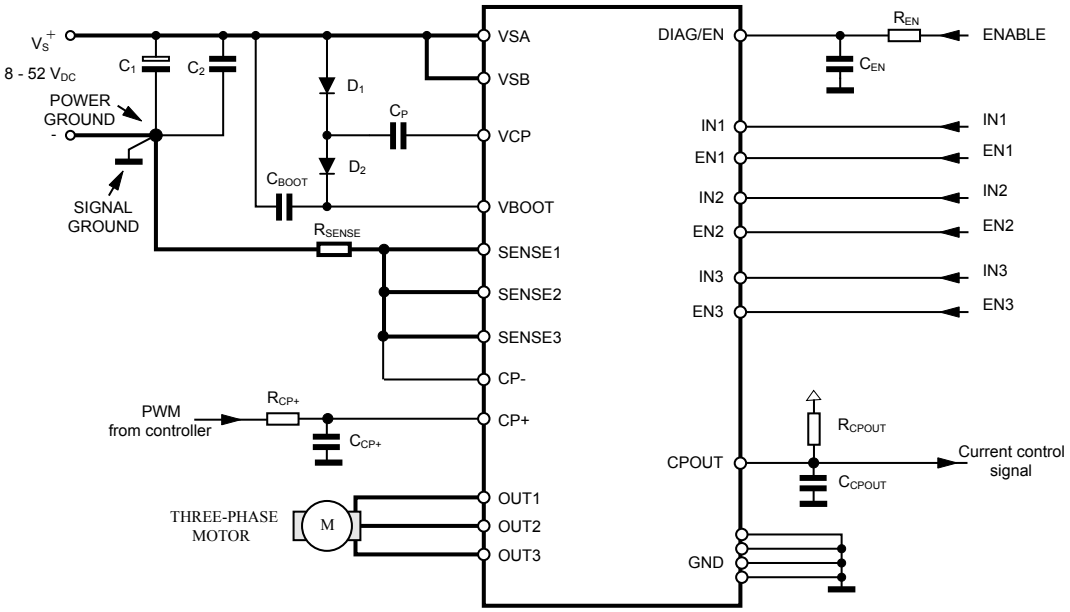
As the current in the motor increases the voltage across the R_{SENSE} increases proportionally. When the voltage drop across the sense resistor becomes greater than the reference voltage applied at non-inverting input CP+ the internal open-drain is switched on pulling down the CPOUT pin.

This signal could be managed by the controller to generate the proper input sequence for the six-step driving method with current control and select what current decay method to implement.

When the sense voltage decreases below the CP+ voltage, the internal open-drain is switched off and the voltage at the CPOUT pin starts to increase charging the capacitor C_{CPOUT}.

The reference voltage at the pin CP+ will be set according to the sense resistor value and the desired regulated current ($V_{CP+} \approx R_{SENSE} \cdot I_{TARGET}$). A very simple way to obtain variable voltage is the low-pass filtering of the PWM signal coming from a controller.

Figure 15. Six-step with current control typical application



6.3 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat-sinking can be achieved using copper on the PCB with a proper area and thickness.

For instance, using a VFQFPN32L 5x5 mm package the typical $R_{th(JA)}$ is about 42 °C/W when mounted on a double-layer FR4 PCB with a dissipating copper area of 0.5 cm^2 on the top side plus the 6 cm^2 ground layer connected through 18 via holes (9 below the IC).

Otherwise, using a PowerSO package with a copper slug soldered on a 1.5 mm copper thickness FR4 board with a 6 cm^2 dissipating footprint (copper thickness of 35 µm), the $R_{th(jA)}$ is about 35 °C/W. Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15 °C/W.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 VFQFPN32 package information

Figure 16. VFQFPN 5x5x1.0 mm, 32 lead, pitch 0.50 package outline

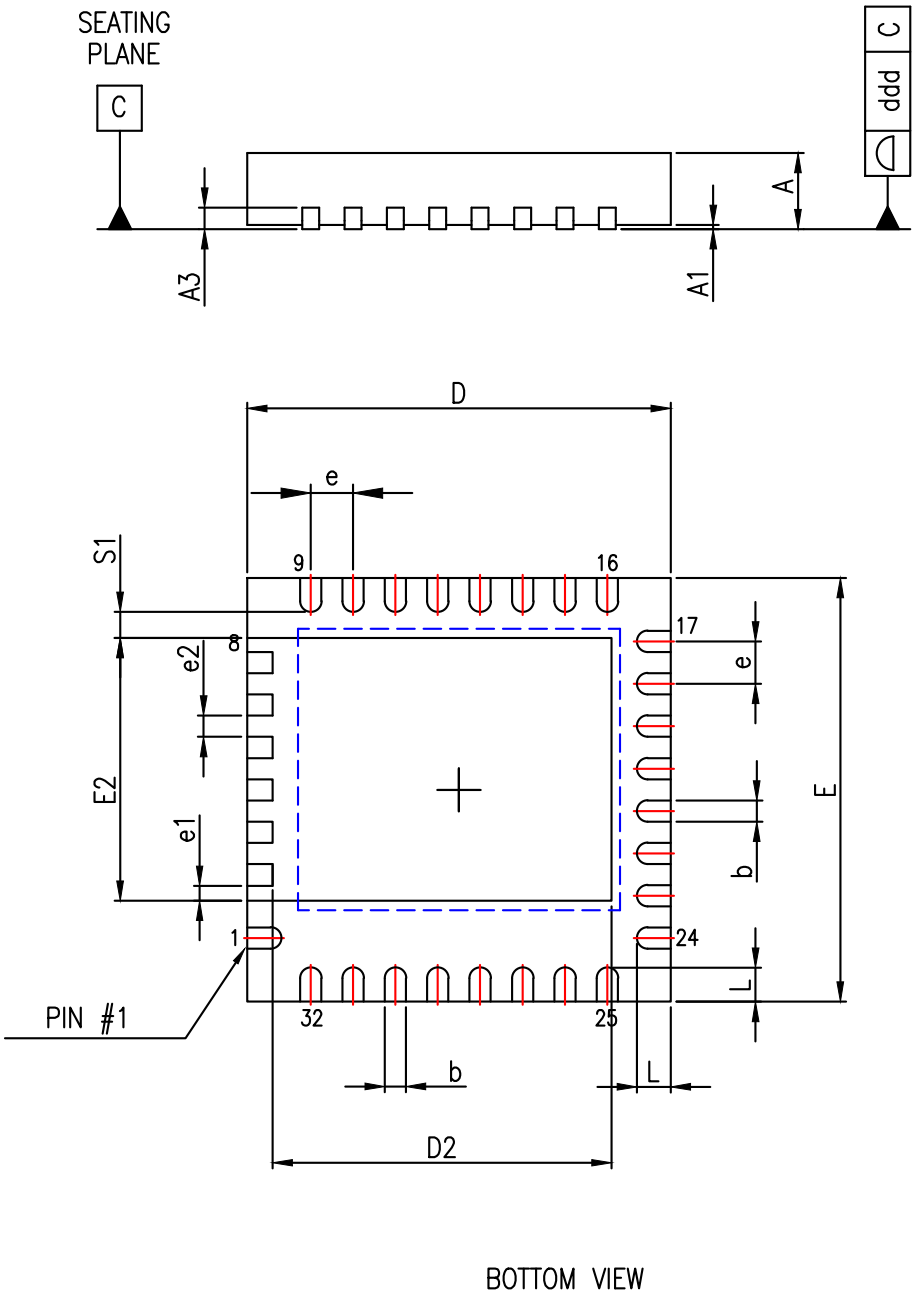


Table 9. **VFQFPN 5x5x1.0 mm, 32 lead, pitch 0.50 mechanical data**

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0	-	0.05
A3	-	0.20	-
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.90	4.00	4.10
E	4.90	5.00	5.10
E2	3.00	3.10	3.20
e	-	0.50	-
L	0.30	0.40	0.50
e1	-	0.175	-
e2	-	0.250	-
S1	-	0.31 Ref	-
ddd	-	-	0.08

7.2 PowerSO36 package information

Figure 17. **PowerSO36 package outline**

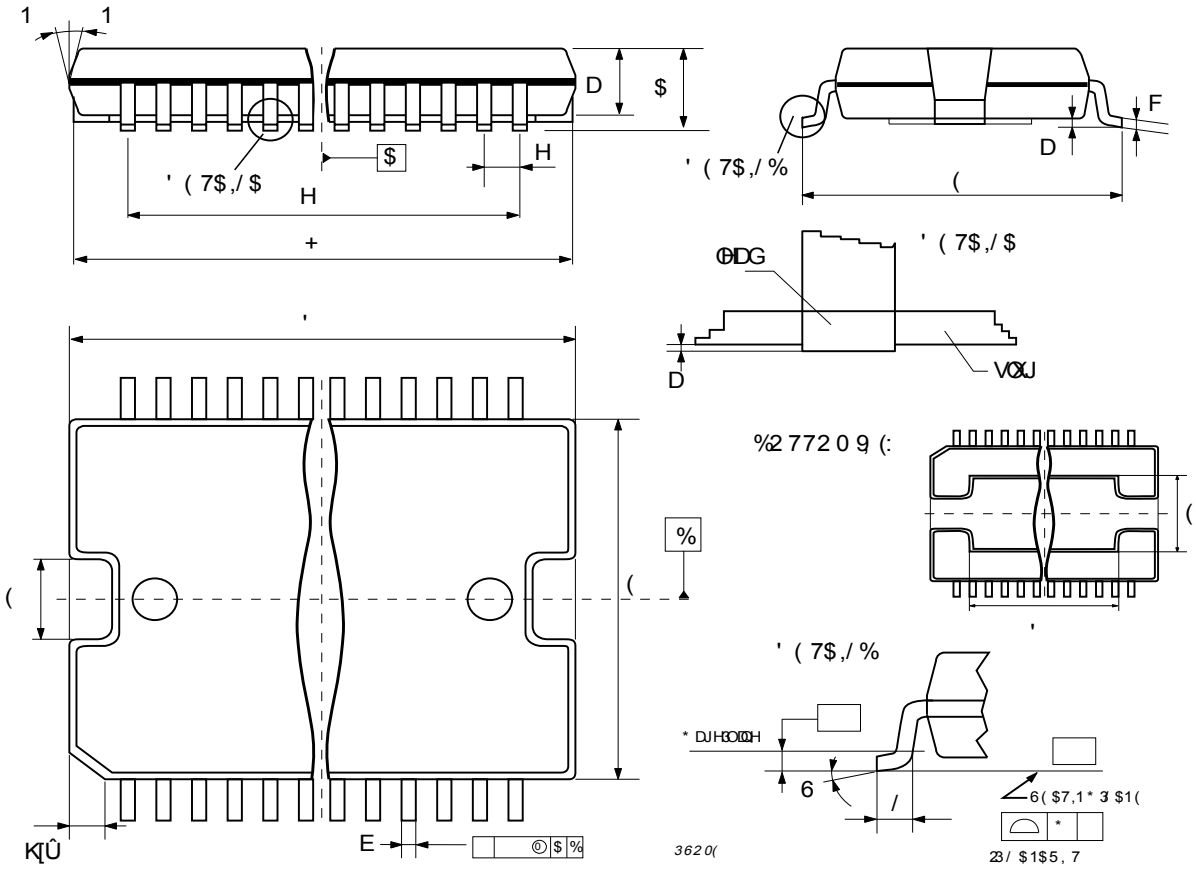


Table 10. PowerSO36 package mechanical data

Symbol	Dimensions		
	mm		
	Min.	Typ.	Max.
A	-	-	3.60
a1	0.10	-	0.30
a2	-	-	3.30
a3	0	-	0.10
b	0.22	-	0.38
c	0.23	-	0.32
D (1)	15.80	-	16.00
D1	9.40	-	9.80
E	13.90	-	14.50
e	-	0.65	-
e3	-	11.05	-
E1 (1)	10.90	-	11.10
E2	-	-	2.90
E3	5.80	-	6.20
E4	2.90	-	3.20
G	0	-	0.10
H	15.50	-	15.90
h	-	-	1.10
L	0.80	-	1.10
N	10° (max.)		
S	8° (max.)		

1. *“D” and “E1” do not include mold flash or protrusions.*
   - *- Mold flash or protrusions shall not exceed 0.15 mm (0.006 inch)*
   - *- Critical dimensions are “a3”, “E” and “G”.*

8 Ordering information

Table 11. **Order code**

Order Code	Package	Package marking	Packing
L6230PD	PowerSO36	L6230PD	Tube
L6230PDTR	PowerSO36	L6230PD	Tape and reel
L6230Q	VFQFPN32	L6230Q	Tube
L6230QTR	VFQFPN32	L6230Q	Tape and reel

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
14-Oct-2010	1	First release.
07-Jun-2011	2	Updated maturity status from preliminary data to final datasheet.
01-Aug-2016	3	Updated Figure 1. Updated Table 1 and Table 2 (corrected SENSE pin labels). Updated Figure 2, Figure 3, Figure 10, Section 5.3, and Figure 14 to Figure 1 (replaced “DIAG/EN” by “DIAG-EN”). Added cross-reference to Table 4in Section 6, to Section 5.3 in Section 5.2 and in Section 6. Updated Section 6.2 (several updates). Replaced “DIAG/EN” by “DIAG-EN” in whole document. Minor modifications throughout document.
15-Nov-2024	4	Updated Table 2, Table 4, and Table 5. Added Table 7. Updated Section 5.1, Section 5.3, and Section 7.1. Removed 'Six-step driving method with BEMF zero-crossing detection' section.

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