

# ST10R272LT1 Datasheet

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|------------------------------|--|
| DiGi Electronics Part Number | ST10R272LT1-DG   |
| Manufacturer                 | <a href="#">STMicroelectronics</a>                                 |
| Manufacturer Product Number  | ST10R272LT1  |
| Description                  | IC MCU 16BIT ROMLESS 100TQFP                                       |
| Detailed Description         | ST10 ST10 Microcontroller IC 16-Bit 50MHz ROMless 100-TQFP (14x14) |

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## Purchase and inquiry

Manufacturer Product Number:

ST10R272LT1

Series:

ST10

DiGi-Electronics Programmable:

Not Verified

Core Size:

16-Bit

Connectivity:

EBI/EMI, SSP, UART/USART

Number of I/O:

77

Program Memory Type:

ROMless

RAM Size:

1K x 8

Data Converters:

-

Operating Temperature:

0°C ~ 70°C (TA)

Supplier Device Package:

100-TQFP (14x14)

Base Product Number:

ST10R

Manufacturer:

STMicroelectronics

Product Status:

Obsolete

Core Processor:

ST10

Speed:

50MHz

Peripherals:

POR, PWM, WDT

Program Memory Size:

-

EEPROM Size:

-

Voltage - Supply (Vcc/Vdd):

3V ~ 3.6V

Oscillator Type:

Internal

Mounting Type:

Surface Mount

Package / Case:

100-LQFP

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.31.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991A2



# ST10R272L

## 16-BIT LOW VOLTAGE ROMLESS MCU WITH MAC

### DATASHEET

#### ■ High Performance 16-bit CPU

- CPU Frequency: 0 to 50 MHz
- 40ns instruction cycle time at 50-MHz CPU clock
- Multiply-Accumulate unit (MAC)
- 4-stage pipeline
- Register-based design with multiple variable register banks
- Enhanced boolean bit manipulation facilities
- Additional instructions to support HLL and operating systems
- Single-cycle context switching support
- 1024 bytes on-Chip special function register area

#### ■ Memory Organisation

- 1KByte on-chip RAM
- Up to 16 MBytes linear address space for code and data (1 MByte with SSP used)

#### ■ External Memory Interface

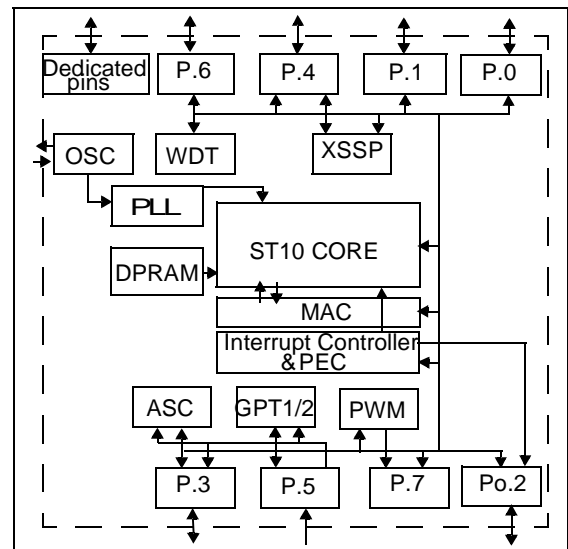
- Programmable external bus characteristics for different address ranges
- 8-bit or 16-bit external data bus
- Multiplexed or demultiplexed external address/data buses
- Five programmable chip-select signals
- Hold and hold-acknowledge bus arbitration support

#### ■ One Channel PWM Unit

- Fail Safe Protection
- Programmable watchdog timer
- Oscillator Watchdog

#### ■ Interrupt

- 8-channel interrupt-driven single-cycle data transfer facilities via peripheral event controller (PEC)
- 16-priority-level interrupt system with 17 sources, sample-rate down to 40 ns



#### ■ Timers

- Two multi-functional general purpose timer units with 5 timers
- Clock Generation via on-chip PLL, or via direct or prescaled clock input

#### ■ Serial Channels

- Synchronous/asynchronous
- High-speed-synchronous serial port SSP

#### ■ Up to 77 general purpose I/O lines

#### ■ No bootstrap loader

#### ■ Electrical Characteristics

- 5V Tolerant I/Os
- 5V Fail-Safe Inputs (Port 5)
- Power: 3.3 Volt +/-0.3V
- Idle and power down modes

#### ■ Support

- C-compilers, macro-assembler packages, emulators, evaluation boards, HLL-debuggers, simulators, logic analyser disassemblers, programming boards

#### ■ Package

- 100-Pin Thin Quad Flat Pack (TQFP)

Rev. 1.3

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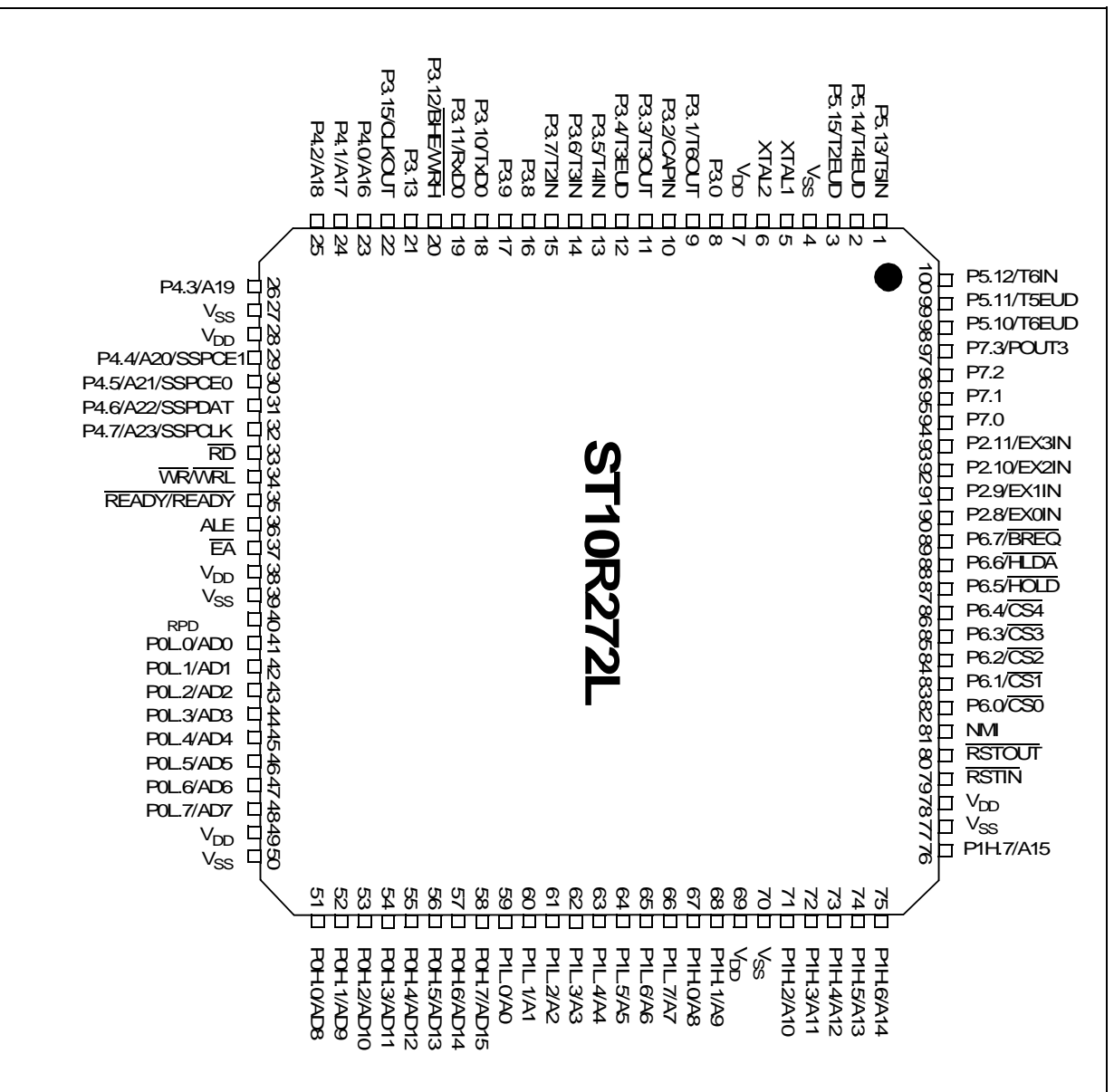
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**ST10R272L - PIN DESCRIPTION**

**1 PIN DESCRIPTION**



**Figure 1 TQFP-100 pin configuration (top view)**

## ST10R272L - PIN DESCRIPTION

| Symbol          | Pin Number (TQFP)                                | Input (I)<br>Output (O)         | Kind <sup>(1)</sup>                    | Function  |
|-----------------|--|---------------------------------|--|---|
| P5.10<br>-P5.15 | 98-100<br>1- 3<br>98<br>99<br>100<br>1<br>2<br>3 | I<br>I<br>I<br>I<br>I<br>I<br>I | 5S<br>5S<br>5S<br>5S<br>5S<br>5S<br>5S | 6-bit input-only port with Schmitt-Trigger characteristics. Port 5 pins also serve as timer inputs:<br><br>P5.10    T6EUD    GPT2 Timer T6 Ext.Up/Down Ctrl.Input<br><br>P5.11    T5EUD    GPT2 Timer T5 Ext.Up/Down Ctrl.Input<br><br>P5.12    T6IN      GPT2 Timer T6 Count Input<br><br>P5.13    T5IN      GPT2 Timer T5 Count Input<br><br>P5.14    T4EUD    GPT1 Timer T4 Ext.Up/Down Ctrl.Input<br><br>P5.15    T2EUD    GPT1 Timer T2 Ext.Up/Down Ctrl.Input |
| XTAL1           | 5  | I                               | 3T                                     | XTAL1: Input to the oscillator amplifier and internal clock generator   |
| XTAL2           | 6  | O                               | 3T                                     | XTAL2: Output of the oscillator amplifier circuit.<br><br>To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Observe minimum and maximum high/low and rise/fall times specified in the AC Characteristics.  |

Table 1 Pin definitions

## ST10R272L - PIN DESCRIPTION

| Symbol          | Pin Number (TQFP) | Input (I)<br>Output (O) | Kind <sup>(1)</sup> | Function   |   |
|-----------------|-------------------|-------------------------|---------------------|--|---|
| P3.0 –<br>P3.13 | 8-21              | I/O                     | 5T                  | A 15-bit (P3.14 is missing) bidirectional I/O port. Port 3 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The following pins have alternate functions: |   |
| P3.15           | 22                | I/O                     | 5T                  |  |   |
|                 | 9                 | O                       | 5T                  |  | P3.1 T6OUT GPT2 Timer T6 toggle latch output                      |
|                 | 10                | I                       | 5T                  |  | P3.2 CAPIN GPT2 Register CAPREL capture input                     |
|                 | 11                | O                       | 5T                  |  | P3.3 T3OUT GPT1 Timer T3 toggle latch output                      |
|                 | 12                | I                       | 5T                  |  | P3.4 T3EUD GPT1 Timer T3 ext.up/down ctrl.input                   |
|                 | 13                | I                       | 5T                  |  | P3.5 T4IN GPT1 Timer T4 input for count/gate/reload/capture       |
|                 | 14                | I                       | 5T                  |  | P3.6 T3IN GPT1 Timer T3 count/gate input                          |
|                 | 15                | I                       | 5T                  |  | P3.7 T2IN GPT1 Timer T2 input for count/gate/reload/capture       |
|                 | 18                | O                       | 5T                  |  | P3.10 TxD0 ASC0 clock/data output (asyn./syn.)                    |
|                 | 19                | I/O                     | 5T                  |  | P3.11 RxD0 ASC0 data input (asyn.) or I/O (syn.)                  |
|                 | 20                | O                       | 5T                  |  | P3.12 $\overline{\text{BHE}}$ Ext. Memory High Byte Enable Signal |
|                 |                   | O                       | 5T                  |  | $\overline{\text{WRH}}$ Ext. Memory High Byte Write Strobe        |
|                 | 22                | O                       | 5T                  | P3.15 CLKOUT System clock output (=CPU clock)  |   |

Table 1 Pin definitions

## ST10R272L - PIN DESCRIPTION

| Symbol                                    | Pin Number (TQFP) | Input (I)<br>Output (O) | Kind <sup>(1)</sup> | Function   |
|---|-------------------|-------------------------|---------------------|--|
| P4.0–<br>P4.7                             | 23-26<br>29-32-   | I/O                     | 5T                  | An 8-bit bidirectional I/O port. Port 8 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines for external bus configuration.               |
|   | 23                | O                       | 5T                  | P4.0 A16 Least Significant Segment Addr. Line  |
|   | ...               | ...                     | ...                 | ...  |
|   | 26                | O                       | 5T                  | P4.3 A19 Segment Address Line  |
|   | 29                | O                       | 5T                  | P4.4 A20 Segment Address Line  |
|   |                   | O                       | 5T                  | SSPCE1 Chip Enable Line 1  |
|   | 30                | O                       | 5T                  | P4.5 A21 Segment Address Line  |
|   |                   | O                       | 5T                  | SSPCE0 SSPChip Enable Line 0   |
|   | 31                | O                       | 5T                  | P4.6 A22 Segment Address Line  |
|   |                   | I/O                     | 5T                  | SSPDAT SSP Data Input/Output Line  |
|   | 32                | O                       | 5T                  | P4.7 A23 Most Significant Segment Addr. Line   |
|   |                   | O                       | 5T                  | SSPCLK SSP Clock Output Line   |
| $\overline{RD}$                           | 33                | O                       | 5T                  | External Memory Read Strobe. RD is activated for every external instruction or data read access.   |
| $\overline{WR}/$<br>$\overline{WRL}$      | 34                | O                       | 5T                  | External Memory Write Strobe. In WR-mode, this pin is activated for every external data write access. In WRL-mode, this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection. |
| $\overline{READY}/$<br>$\overline{READY}$ | 35                | I                       | 5T                  | Ready Input. Active level is programmable. When the Ready function is enabled, the selected inactive level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to the selected active level. Polarity is programmable.   |

Table 1 Pin definitions

## ST10R272L - PIN DESCRIPTION

| Symbol   | Pin Number (TQFP)             | Input (I)<br>Output (O) | Kind <sup>(1)</sup> | Function  |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
|--|-------------------------------|-------------------------|---------------------|---|------------------|-------|--------|----------------|---------|---------|----------------|-----|----------|------------------|-------|--------|----------------|-----------|-----------|----------------|----------|------------|
| ALE  | 36                            | O                       | 5T                  | Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.  |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| $\overline{EA}$                                | 37                            | I                       | 5T                  | External Access Enable pin. Low level at this pin during and after reset forces the ST10R272L to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. The ST10R272L must have this pin tied to '0'.   |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| PORT0:<br>POL.0–<br>POL.7,<br>POH.0 -<br>POH.7 | 41 - 48<br><br>51 - 58        | I/O                     | 5T                  | <p>PORT0 has two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>For external bus configuration, PORT0 acts as address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.</p> <p><b>Demultiplexed bus modes</b></p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>D0 – D7</td> <td>D0 - D7</td> </tr> <tr> <td>P0H.0 – P0H.7:</td> <td>I/O</td> <td>D8 - D15</td> </tr> </table> <p><b>Multiplexed bus modes</b></p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>AD0 – AD7</td> <td>AD0 - AD7</td> </tr> <tr> <td>P0H.0 – P0H.7:</td> <td>A8 – A15</td> <td>AD8 – AD15</td> </tr> </table> | Data Path Width: | 8-bit | 16-bit | P0L.0 – P0L.7: | D0 – D7 | D0 - D7 | P0H.0 – P0H.7: | I/O | D8 - D15 | Data Path Width: | 8-bit | 16-bit | P0L.0 – P0L.7: | AD0 – AD7 | AD0 - AD7 | P0H.0 – P0H.7: | A8 – A15 | AD8 – AD15 |
| Data Path Width:                               | 8-bit                         | 16-bit                  |                     |   |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| P0L.0 – P0L.7:                                 | D0 – D7                       | D0 - D7                 |                     |   |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| P0H.0 – P0H.7:                                 | I/O                           | D8 - D15                |                     |   |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| Data Path Width:                               | 8-bit                         | 16-bit                  |                     |   |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| P0L.0 – P0L.7:                                 | AD0 – AD7                     | AD0 - AD7               |                     |   |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| P0H.0 – P0H.7:                                 | A8 – A15                      | AD8 – AD15              |                     |   |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |
| PORT1:<br>P1L.0–<br>P1L.7,<br>P1H.0 -<br>P1H.7 | 59- 66<br><br>67, 68<br>71-76 | I/O                     | 5T                  | <p>PORT1 has two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 acts as a 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.</p>  |                  |       |        |                |         |         |                |     |          |                  |       |        |                |           |           |                |          |            |

Table 1 Pin definitions

## ST10R272L - PIN DESCRIPTION

| Symbol                     | Pin Number (TQFP) | Input (I)<br>Output (O) | Kind <sup>(1)</sup> | Function  |
|----------------------------|-------------------|-------------------------|---------------------|---|
| $\overline{\text{RSTIN}}$  | 79                | I                       | 5T                  | Reset Input with Schmitt-Trigger characteristics. Resets the device when a low level is applied for a specified duration while the oscillator is running. An internal pullup resistor enables power-on reset using <u>only</u> a capacitor connected to $V_{SS}$ . With a bonding option, the $\overline{\text{RSTIN}}$ pin can also be pulled-down for 512 internal clock cycles for hardware, software or watchdog timer triggered resets |
| $\overline{\text{RSTOUT}}$ | 80                | O                       | 5T                  | Internal Reset Indication Output. This pin is set to a low level when the part is executes hardware-, software- or watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.  |
| $\overline{\text{NMI}}$    | 81                | I                       | 5S                  | Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If it is not used, $\overline{\text{NMI}}$ should be pulled high externally.   |
| P6.0-<br>P6.7              | 82-89             | I/O                     | 5T                  | An 8-bit bidirectional I/O port. Port 6 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers.<br><br>The following Port 6 pins have alternate functions:   |
|                            | 82                | O                       | 5T                  | P6.0 $\overline{\text{CS0}}$ Chip Select 0 Output   |
|                            | ...               | ...                     | ...                 | ...      ...      ...   |
|                            | 86                | O                       | 5T                  | P6.4 $\overline{\text{CS4}}$ Chip Select 4 Output   |
|                            | 87                | I                       | 5T                  | P6.5 $\overline{\text{HOLD}}$ External Master Hold Request Input<br>(Master mode: O, Slave mode: I)   |
|                            | 88                | I/O                     | 5T                  | P6.6 $\overline{\text{HLDA}}$ Hold Acknowledge Output   |
|                            | 89                | O                       | 5T                  | P6.7 $\overline{\text{BREQ}}$ Bus Request Output  |

Table 1 Pin definitions

## ST10R272L - PIN DESCRIPTION

| Symbol          | Pin Number (TQFP)           | Input (I)<br>Output (O) | Kind <sup>1)</sup> | Function   |
|-----------------|-----------------------------|-------------------------|--------------------|--|
| P2.8 –<br>P2.11 | 90 - 93                     | I/O                     | 5T                 | Port 2 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers.<br><br>The following Port 2 pins have alternate functions: |
|                 | 90                          | I                       | 5T                 | P2.8      EX0IN      Fast External Interrupt 0 Input   |
|                 | ...                         | ...                     | ...                | ...      ...      ...  |
|                 | 93                          | I                       | 5T                 | P2.11      EX3IN      Fast External Interrupt 3 Input  |
| P7.0 –<br>P7.3  | 94 - 97                     | I/O                     | 5T                 | Port 7 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers.<br><br>The following Port 7 pins have alternate functions: |
|                 | 97                          | O                       | 5T                 | P7.3      POUT3      PWM (Channel 3) Output  |
| RPD             | 40                          | I/O                     | 5T                 | Input timing pin for the return from powerdown circuit and power-up asynchronous reset.  |
| V <sub>DD</sub> | 7, 28,<br>38, 49,<br>69, 78 | -                       | PO                 | Digital supply voltage.  |
| V <sub>SS</sub> | 4, 27,<br>39, 50,<br>70, 77 | -                       | PO                 | Digital ground.  |

Table 1 Pin definitions

- 1) The following I/O kinds are used. Refer to *ELECTRICAL CHARACTERISTICS* on page 40 for a detailed description.

PO: Power pin

3T: 3 V tolerant pin (voltage max. respect to V<sub>SS</sub> is -0.5 to V<sub>DD</sub> + 0.5)

5V: 5 V tolerant pin (voltage max. respect to V<sub>SS</sub> is -0.5 to 5.5 only if chip is powered)

5S: 5 V tolerant and fail-safe pin (-0.5-5.5 max. voltage w.r.t. V<sub>SS</sub> even if chip is not powered).

## ST10R272L - FUNCTIONAL DESCRIPTION

## 2 FUNCTIONAL DESCRIPTION

ST10R272L architecture combines the advantages of both RISC and CISC processors with an advanced peripheral subsystem. The following block diagram overviews the different on-chip components and the internal bus structure.

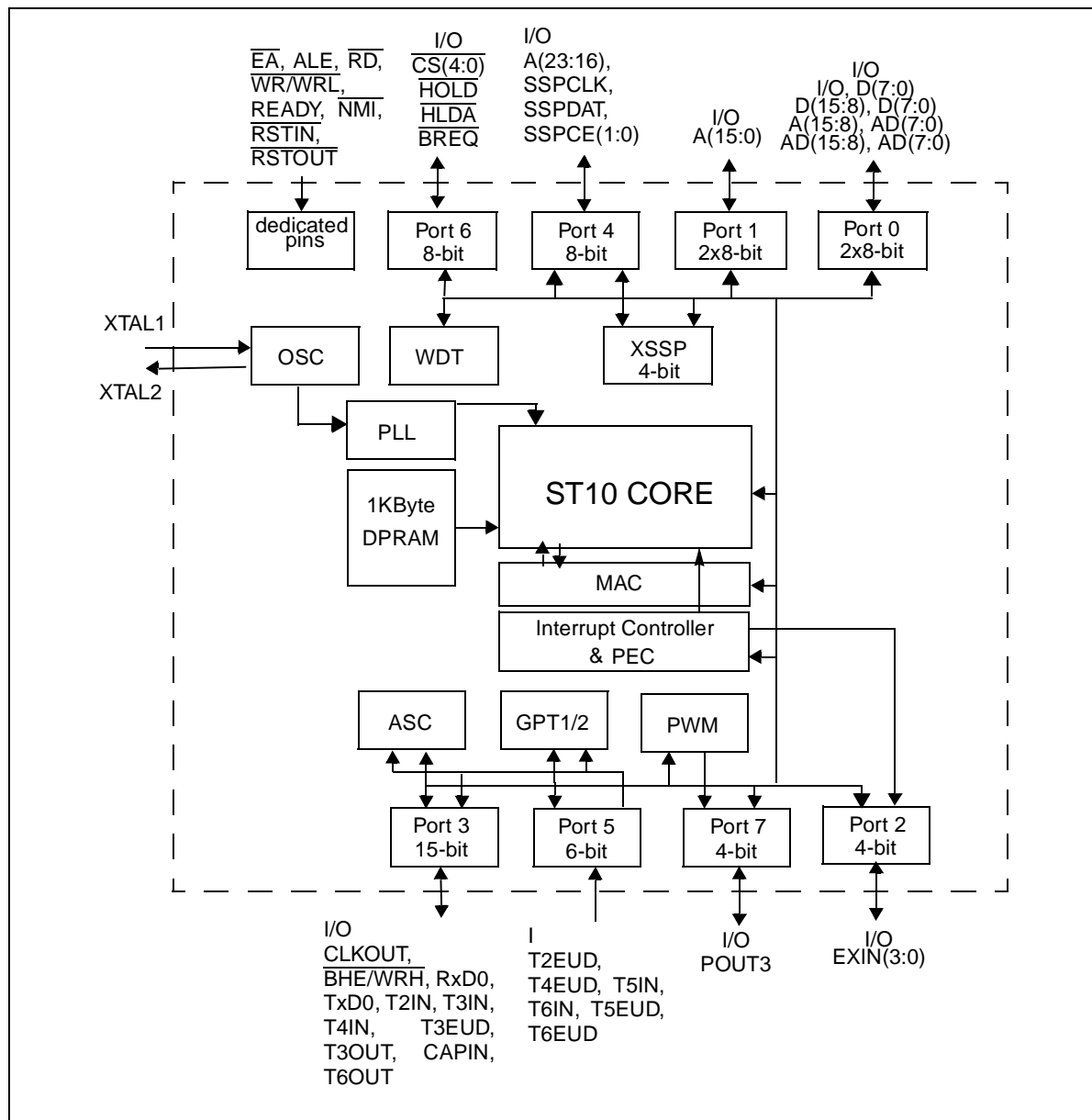


Figure 2 Block diagram

## ST10R272L - MEMORY MAPPING

### 3 MEMORY MAPPING

The ST10R272L is a ROMless device, the internal RAM space is 1 KByte. The RAM address space is used for variables, register banks, the system stack, the PEC pointers (in 00'FCE0h - 00'FCFFh) and the bit-addressable space (in 00'FD00h - 00'FDFFh).

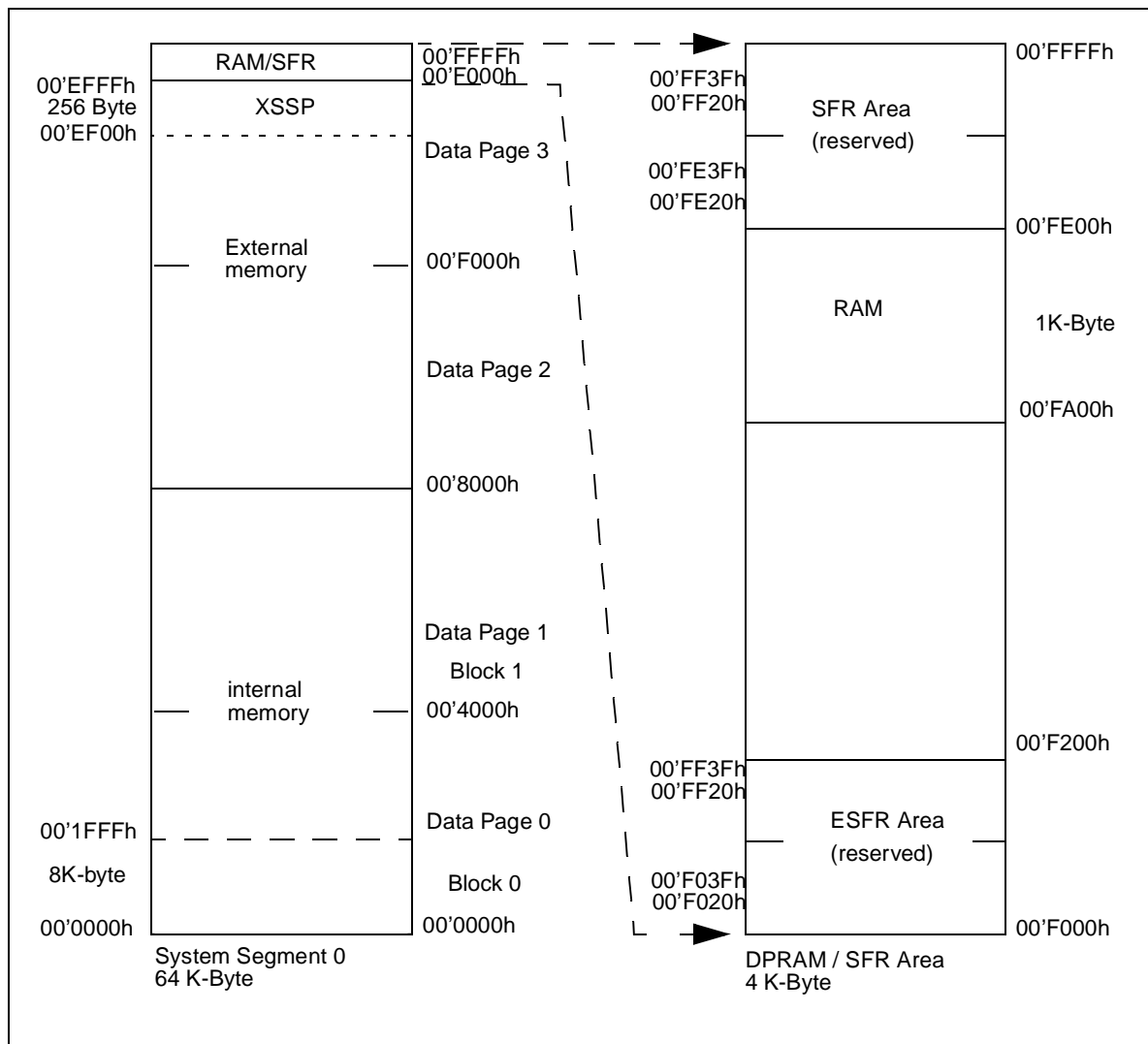


Figure 3 Memory map

## ST10R272L - CENTRAL PROCESSING UNIT

### 4 CENTRAL PROCESSING UNIT

The main core of the CPU contains a 4-stage instruction pipeline, a MAC multiply-accumulation unit, a separate multiply and divide unit, a bit-mask generator and a barrel shifter. Most instructions can be executed in one machine cycle requiring 40ns at 50MHz CPU clock.

The CPU includes an actual register context consisting of 16 wordwide GPRs physically located in the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, one register bank may overlap others.

A system stack of up to 1024 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are compared against the stack pointer value during each stack access to detect stack overflow or underflow.

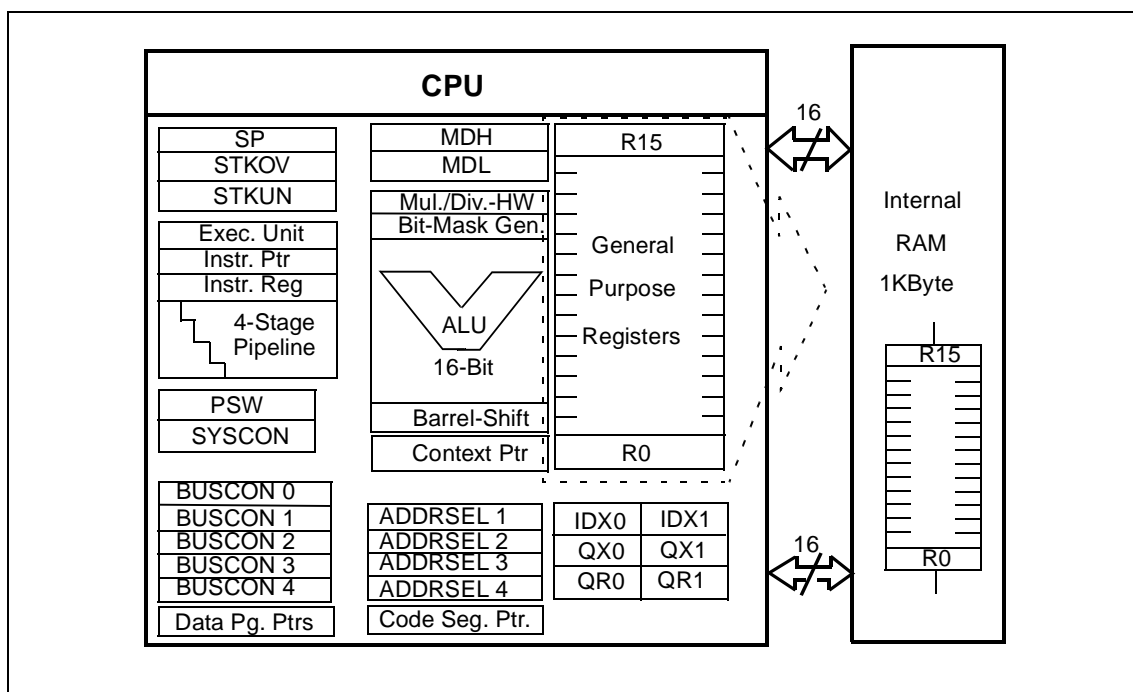


Figure 4 CPU block diagram

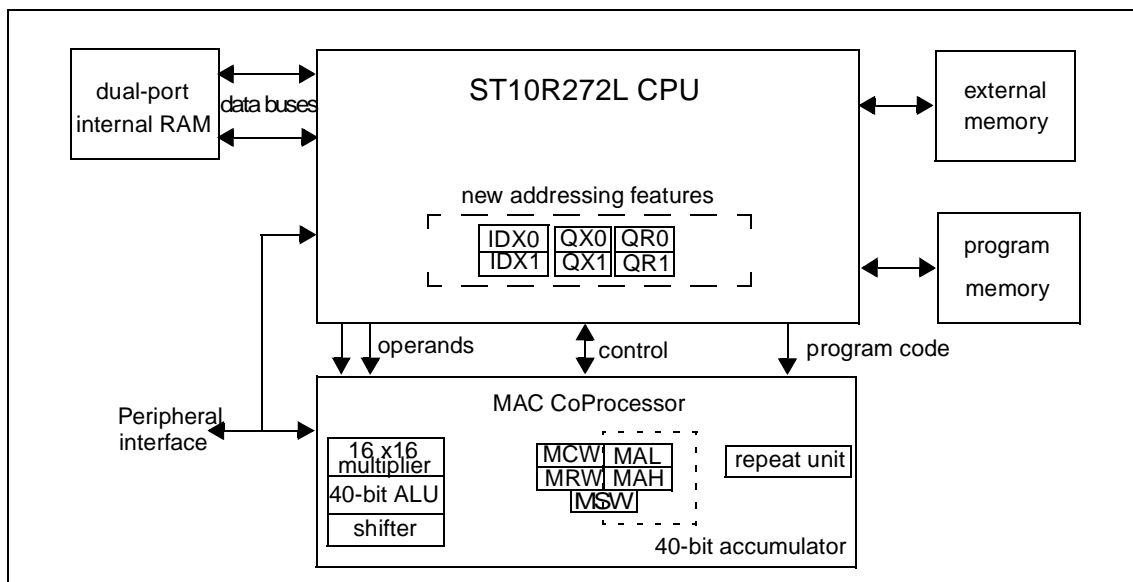
## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

### 5 MULTIPLY-ACCUMULATE UNIT (MAC)

The MAC is a specialized co-processor added to the ST10R272L CPU core to improve the performance of signal processing algorithms. It includes:

- a multiply-accumulate unit
- an address generation unit, able to feed the mac unit with 2 operands per cycle
- a repeat unit, to execute a series of multiply-accumulate instructions

New addressing capabilities enable the CPU to supply the MAC with up to 2 operands per instruction cycle. MAC instructions: multiply, multiply-accumulate, 32-bit signed arithmetic operations and the CoMOV transfer instruction have been added to the standard instruction set. Full details are provided in the 'ST10 Family Programming Manual'.



**Figure 5 MAC architecture**

---

## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

---

### 5.1 MAC Features

#### Enhanced addressing capabilities

- Double indirect addressing mode with pointer post-modification.
- Parallel Data Move allows one operand move during Multiply-Accumulate instructions without penalty.
- CoSTORE instruction (for fast access to the MAC SFRs) and CoMOV (for fast memory to memory table transfer).

#### General

- Two-cycle execution for all MAC operations.
- 16 x 16 signed/unsigned parallel multiplier.
- 40-bit signed arithmetic unit with automatic saturation mode.
- 40-bit accumulator.
- 8-bit left/right shifter.
- Scaler (one-bit left shifter)
- Data limiter
- Full instruction set with multiply and multiply-accumulate, 32-bit signed arithmetic and compare instructions.
- Three 16-bit status and control registers: MSW: MAC Status Word, MCW: MAC Control Word, MRW: MAC Repeat Word.

#### Program control

- Repeat Unit allows some MAC co-processor instructions to be repeated up to 8192 times. Repeated instructions may be interrupted.
- MAC interrupt (Class B Trap) on MAC condition flags.

## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

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### 5.2 MAC Operation

#### Instruction pipelining

All MAC instructions use the 4-stage pipeline. During each stage the following tasks are performed:

- **FETCH:** All new instructions are double-word instructions.
- **DECODE:** If required, operand addresses are calculated and the resulting operands are fetched. IDX and GPR pointers are post-modified if necessary.
- **EXECUTE:** Performs the MAC operation. At the end of the cycle, the Accumulator and the MAC condition flags are updated if required. Modified GPR pointers are written-back during this stage, if required.
- **WRITEBACK:** Operand write-back in the case of parallel data move.

*Note* At least one instruction which does not use the MAC must be inserted between two instructions that read from a MAC register. This is because the Accumulator and the status of the MAC are modified during the Execute stage. The CoSTORE instruction has been added to allow access to the MAC registers immediately after a MAC operation.

#### Address generation

MAC instructions can use some standard ST10 addressing modes such as GPR direct or #data4 for immediate shift value.

New addressing modes have been added to supply the MAC with two new operands per instruction cycle. These allow indirect addressing with address pointer post-modification.

Double indirect addressing requires two pointers. Any GPR can be used for one pointer, the other pointer is provided by one of two specific SFRs IDX0 and IDX1. Two pairs of offset registers QR0/QR1 and QX0/QX1 are associated with each pointer (GPR or IDX<sub>i</sub>). The GPR pointer allows access to the entire memory space, but IDX<sub>i</sub> are limited to the internal Dual-Port RAM, except for the CoMOV instruction.

## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

The following table shows the various combinations of pointer post-modification for each of these 2 new addressing modes. In this document the symbols “[Rw<sub>n</sub>⊗]” and “[IDX<sub>i</sub>⊗]” refer to these addressing modes.

| Symbol                            | Mnemonic                              | Address Pointer Operation  |
|-----------------------------------|---------------------------------------|--|
| “[IDX <sub>i</sub> ⊗]” stands for | [IDX <sub>i</sub> ]                   | (IDX <sub>i</sub> ) ← (IDX <sub>i</sub> ) (no-op)                          |
|                                   | [IDX <sub>i</sub> +] ]                | (IDX <sub>i</sub> ) ← (IDX <sub>i</sub> ) +2 (i=0,1)                       |
|                                   | [IDX <sub>i</sub> - ]                 | (IDX <sub>i</sub> ) ← (IDX <sub>i</sub> ) -2 (i=0,1)                       |
|                                   | [IDX <sub>i</sub> + QX <sub>j</sub> ] | (IDX <sub>i</sub> ) ← (IDX <sub>i</sub> ) + (QX <sub>j</sub> ) (i, j =0,1) |
|                                   | [IDX <sub>i</sub> - QX <sub>j</sub> ] | (IDX <sub>i</sub> ) ← (IDX <sub>i</sub> ) - (QX <sub>j</sub> ) (i, j =0,1) |
| “[Rw <sub>n</sub> ⊗]” stands for  | [Rwn]                                 | (Rwn) ← (Rwn) (no-op)  |
|                                   | [Rwn+] ]                              | (Rwn) ← (Rwn) +2 (n=0-15)  |
|                                   | [Rwn- ]                               | (Rwn) ← (Rwn) -2 (k=0-15)  |
|                                   | [Rwn+QR <sub>j</sub> ]                | (Rwn) ← (Rwn) + (QR <sub>j</sub> ) (n=0-15; j =0,1)                        |
|                                   | [Rwn - QR <sub>j</sub> ]              | (Rwn) ← (Rwn) - (QR <sub>j</sub> ) (n=0-15; j =0,1)                        |

**Table 2 Pointer post-modification combinations for IDX<sub>i</sub> and Rwn**

For the CoMACM class of instruction, Parallel Data Move mechanism is implemented. This class of instruction is only available with double indirect addressing mode. Parallel Data Move allows the operand pointed by IDX<sub>i</sub> to be moved to a new location in parallel with the MAC operation. The write-back address of Parallel Data Move is calculated depending on the post-modification of IDX<sub>i</sub>. It is obtained by the reverse operation than the one used to calculate the new value of IDX<sub>i</sub>. The following table shows these rules.

| Instruction                                     | Writeback Address                    |
|---|--------------------------------------|
| CoMACM [IDX <sub>i</sub> +] ,...                | <IDX <sub>i</sub> -2>                |
| CoMACM [IDX <sub>i</sub> - ] ,...               | <IDX <sub>i</sub> +2>                |
| CoMACM [IDX <sub>i</sub> +QX <sub>j</sub> ],... | <IDX <sub>i</sub> -QX <sub>j</sub> > |
| CoMACM [IDX <sub>i</sub> -QX <sub>j</sub> ],... | <IDX <sub>i</sub> +QX <sub>j</sub> > |

**Table 3 Parallel data move addressing**

## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

The Parallel Data Move shifts a table of operands in parallel with a computation on those operands. Its specific use is for signal processing algorithms like filter computation. The following figure gives an example of Parallel Data Move with CoMACM instruction.

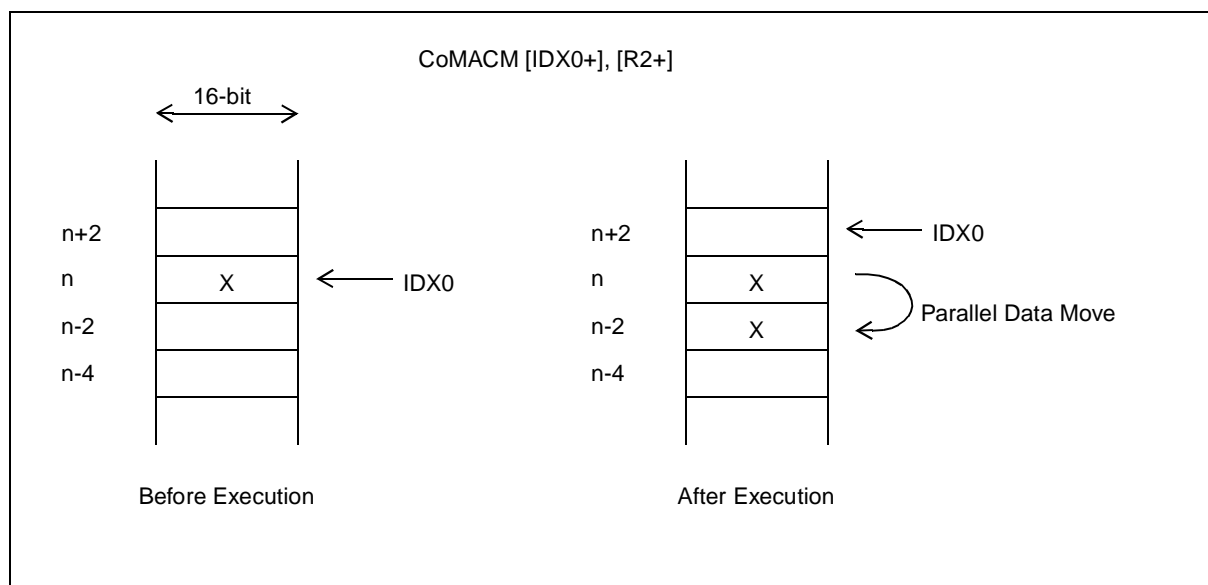


Figure 6 Example of parallel data move

### 16 x 16 signed/unsigned parallel multiplier

The multiplier executes 16 x 16-bit parallel signed/unsigned fractional and integer multiplies. The multiplier has two 16-bit input ports, and a 32-bit product output port. The input ports can accept data from the MA-bus and from the MB-bus. The output is sign-extended and then feeds a scaler that shifts the multiplier output according to the shift mode bit MP specified in the co-processor Control Word (MCW). The product can be shifted one bit left to compensate for the extra sign bit gained in multiplying two 16-bit signed (2's complement) fractional numbers if bit MP is set.

### 40-bit signed arithmetic unit

The arithmetic unit over 32 bits wide to allow intermediate overflow in a series of multiply/accumulate operations. The extension flag E, contained in the most significant byte of MSW, is set when the Accumulator has overflowed beyond the 32-bit boundary, that is, when there are significant (non-sign) bits in the top eight (signed arithmetic) bits of the Accumulator.

The 40-bit arithmetic unit has two 40-bit input ports A and B. The A-input port accepts data from 4 possible sources: 00,0000,0000h, 00,0000,8000h (round), the sign-extended product, or the sign-extended data conveyed by the 32-bit bus resulting from the concatenation of MA- and MB-buses. Product and Concatenation can be shifted left by one according to MP for the multiplier or to the instruction for the concatenation. The B-input port is fed either by the 40-bit shifted/not shifted and inverted/not inverted accumulator or by 00,0000,0000h. A-input and B-

## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

input ports can receive 00,0000,0000h to allow direct transfers from the B-source and A-source, respectively, to the Accumulator (case of Multiplication, Shift.). The output of the arithmetic unit goes to the Accumulator.

It is also possible to saturate the Accumulator on a 32-bit value, automatically after every accumulation. Automatic saturation is enabled by setting the saturation bit MS in the MCW register. When the Accumulator is in the saturation mode and an 32-bit overflow occurs, the accumulator is loaded with either the most positive or the most negative value representable in a 32-bit value, depending on the direction of the overflow. The value of the Accumulator upon saturation is 00,7fff,ffffh (positive) or ff,8000,0000h (negative) in signed arithmetic. Automatic saturation sets the SL flag MSW. This flag is a sticky flag which means it stays set until it is explicitly reset by the user.

40-bit overflow of the Accumulator sets the SV flag in MSW. This flag is also a sticky flag.

### 40-bit accumulator register

The 40-bit Accumulator consists of three SFR registers MAH, MAL and MAE. MAH and MAL are 16-bit wide. MAE is 8-bit wide and is contained within the least significant byte of MSW. Most co-processor operations specify the 40-bit Accumulator register as source and/or destination operand.

### Data limiter

Saturation arithmetic is also provided to selectively limit overflow, when reading the accumulator by means of a CoSTORE <destination> MAS instruction. Limiting is performed on the MAC Accumulator. If the contents of the Accumulator can be represented in the destination operand size without overflow, the data limiter is disabled and the operand is not modified. If the contents of the accumulator cannot be represented without overflow in the destination operand size, the limiter will substitute a 'limited' data as explained in the following table.

| Register | E bit | N bit | Output of the Limiter |
|----------|-------|-------|-----------------------|
| x        | 0     | x     | unchanged             |
| MAS      | 1     | 0     | 7fffh                 |
| MAS      | 1     | 1     | 8000h                 |

**Table 4 Data Limit Values**

*Note* In this case, the accumulator and the status register are not affected. MAS readable from a CoSTORE instruction.

## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

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### Accumulator shifter

The Accumulator shifter is a parallel shifter with a 40-bit input and a 40-bit output. The source operand of the shifter is the Accumulator and the possible shifting operations are:

- No shift (Unmodified)
- Up to 8-bit Arithmetic Left Shift
- Up to 8-bit Arithmetic Right Shift

E, SV and SL bits from MSW are affected by Left shifts, therefore if the saturation mechanism is enabled (MS), the behavior is similar to the one of the arithmetic unit. The carry flag C is also affected by left shifts.

### Repeat unit

The MAC includes a repeat unit allowing the repetition of some co-processor instructions up to  $2^{13}$  (8192) times. The repeat count may be specified either by an immediate value (up to 31 times) or by the content of the Repeat Count (bits 12 to 0) in the MAC Repeat Word (MRW). If the Repeat Count equals "N" the instruction will be executed "N+1" times. At each iteration of a cumulative instruction the Repeat Count is tested for zero. If it is zero the instruction is terminated else the Repeat Count is decremented and the instruction is repeated. During such a repeat sequence, the Repeat Flag in MRW is set until the last execution of the repeated instruction.

The syntax of repeated instructions is shown in the following examples:

```
1      Repeat #24 times
      CoMAC[IDX0+],[R0+]      ; repeated 24 times
```

In example 1, the instruction is repeated according to a 5-bit immediate value. The Repeat Count in MRW is automatically loaded with this value minus one (MRW=23).

```
1      MOV MRW, #00FFh      ; load MRW
      NOP                    ; instruction latency
      Repeat MRW times
      CoMACM [IDX1-],[R2+]  ; repeated 256 times
```

In this example, the instruction is repeated according to the Repeat Count in MRW. Notice that due to the pipeline processing at least one instruction should be inserted between the write of MRW and the next repeated instruction.

Repeat sequences may be interrupted. When an interrupt occurs during a repeat sequence, the sequence is stopped and the interrupt routine is executed. The repeat sequence resumes at the end of the interrupt routine. During the interrupt, MR remains set, indicating that a repeated instruction has been interrupted and the Repeat Count holds the number (minus 1)

## ST10R272L - MULTIPLY-ACCUMULATE UNIT (MAC)

of repetition that remains to complete the sequence. If the Repeat Unit is used in the interrupt routine, MRW must be saved by the user and restored before the end of the interrupt routine.

*Note* The Repeat Count should be used with caution. In this case MR should be written as 0. In general MR should not be set by the user otherwise correct instruction processing can not be guaranteed.

### MAC interrupt

The MAC can generate an interrupt according to the value of the status flags C (carry), SV (overflow), E (extension) or SL (limit) of the MSW. The MAC interrupt is globally enabled when the MIE flag in MCW is set. When it is enabled the flags C, SV, E or SL can triggered a MAC interrupt when they are set provided that the corresponding mask flag CM, VM, EM or LM in MCW is also set. A MAC interrupt request set the MIR flag in MSW, this flag must be reset by the user during the interrupt routine otherwise the interrupt processing restarts when returning from the interrupt routine.

The MAC interrupt is implemented as a Class B hardware trap (trap number Ah - trap priority I). The associated Trap Flag in the TFR register is MACTRP, bit #6 of the TFR (Remember that this flag must also be reset by the user in the case of an MAC interrupt request).

As the MAC status flags are updated (or eventually written by software) during the Execute stage of the pipeline, the response time of a MAC interrupt request is 3 instruction cycles (see Figure 3). It is the number of instruction cycles required between the time the request is sent and the time the first instruction located at the interrupt vector location enters the pipeline. Note that the IP value stacked after a MAC interrupt does not point to the instruction that triggers the interrupt.

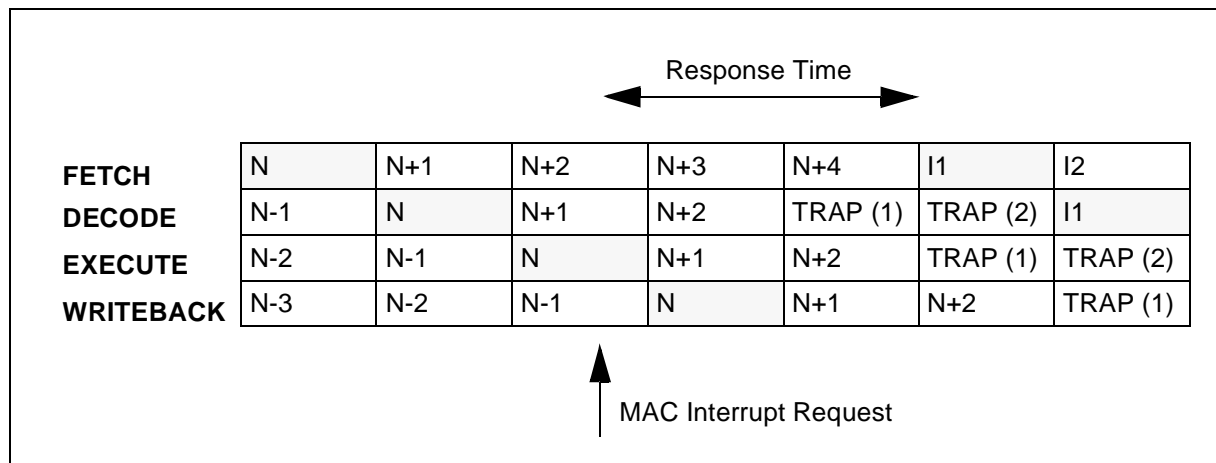


Figure 7 Pipeline diagram for MAC interrupt response time

## ST10R272L - INTERRUPT AND TRAP FUNCTIONS

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### Number representation & rounding

The MAC supports the two's-complement representation of binary numbers. In this format, the sign bit is the MSB of the binary word. This is set to zero for positive numbers and set to one for negative numbers. Unsigned numbers are supported only by multiply/multiply-accumulate instructions which specifies whether each operand is signed or unsigned.

In two's complement fractional format, the N-bit operand is represented using the 1.[N-1] format (1 signed bit, N-1 fractional bits). Such a format can represent numbers between -1 and  $+1 \cdot 2^{-[N-1]}$ . This format is supported when MP of MCW is set.

The MAC implements 'two's complement rounding'. With this rounding type, one is added to the bit to the right of the rounding point (bit 15 of MAL), before truncation (MAL is cleared).

## 6 INTERRUPT AND TRAP FUNCTIONS

The architecture of the ST10R272L supports several mechanisms for fast and flexible response to the service requests that can be generated from various sources, internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced, either by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In a standard interrupt service, program execution is suspended and a branch to the interrupt service routine is performed. For a PEC service, just one cycle is 'stolen' from the current CPU activity. A PEC service is a single, byte or word data transfer between any two memory locations, with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is decremented for each PEC service, except in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are very well suited, for example, to the transmission or reception of blocks of data. The ST10R272L has 8 PEC channels, each of which offers fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield, exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher priority service request. For standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs, feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

**ST10R272L - INTERRUPT AND TRAP FUNCTIONS****6.1 Interrupt Sources**

| <b>Source of Interrupt or PEC Service Request</b> | <b>Request Flag</b> | <b>Enable Flag</b> | <b>Interrupt Vector</b> | <b>Vector Location</b> | <b>Trap Number</b> |
|---|---------------------|--------------------|-------------------------|------------------------|--------------------|
| External Interrupt 0                              | CC8IR               | CC8IE              | CC8INT                  | 60h                    | 18h                |
| External Interrupt 1                              | CC9IR               | CC9IE              | CC9INT                  | 64h                    | 19h                |
| External Interrupt 2                              | CC10IR              | CC10IE             | CC10INT                 | 68h                    | 1Ah                |
| External Interrupt 3                              | CC11IR              | CC11IE             | CC11INT                 | 6Ch                    | 1Bh                |
| GPT1 Timer 2                                      | T2IR                | T2IE               | T2INT                   | 88h                    | 22h                |
| GPT1 Timer 3                                      | T3IR                | T3IE               | T3INT                   | 8Ch                    | 23h                |
| GPT1 Timer 4                                      | T4IR                | T4IE               | T4INT                   | 90h                    | 24h                |
| GPT2 Timer 5                                      | T5IR                | T5IE               | T5INT                   | 94h                    | 25h                |
| GPT2 Timer 6                                      | T6IR                | T6IE               | T6INT                   | 98h                    | 26h                |
| GPT2 CAPREL Register                              | CRIR                | CRIE               | CRINT                   | 9Ch                    | 27h                |
| ASC0 Transmit                                     | S0TIR               | S0TIE              | S0TINT                  | A8h                    | 2Ah                |
| ASC0 Transmit Buffer                              | S0TBIR              | S0TBIE             | S0TBINT                 | 11Ch                   | 47h                |
| ASC0 Receive                                      | S0RIR               | S0RIE              | S0RINT                  | ACh                    | 2Bh                |
| ASC0 Error  | S0EIR               | S0EIE              | S0EINT                  | B0h                    | 2Ch                |
| PWM Channel 3                                     | PWMIR               | PWMIE              | PWMINT                  | FCh                    | 3Fh                |
| SSP Interrupt                                     | XP1IR               | XP1IE              | XP1INT                  | 104h                   | 41h                |
| PLL Unlock  | XP3IR               | XP3IE              | XP3INT                  | 10Ch                   | 43h                |

**Table 5 List of possible interrupt sources, flags, vector and trap numbers**

## ST10R272L - INTERRUPT AND TRAP FUNCTIONS

### 6.2 Hardware Traps

Exceptions or error conditions that arise during run-time are called Hardware Traps. Hardware traps cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can not normally be interrupted by standard or PEC interrupts. The following table shows all of the possible exceptions or error conditions that can arise during run-time:

| Exception Condition         | Trap Flag | Trap Vector | Vector Location                       | Trap Number     | Trap Priority        |
|-----------------------------|-----------|-------------|---------------------------------------|-----------------|----------------------|
| Reset Functions:            |           |             |                                       |                 |                      |
| Hardware Reset              |           | RESET       | 00'0000h                              | 00h             | III                  |
| Software Reset              |           | RESET       | 00'0000h                              | 00h             | III                  |
| Watchdog Timer Overflow     |           | RESET       | 00'0000h                              | 00h             | III                  |
| Class A Hardware Traps:     |           |             |                                       |                 |                      |
| Non-Maskable Interrupt      | NMI       | NMITRAP     | 00'0008h                              | 02h             | II                   |
| Stack Overflow              | STKOF     | STOTRAP     | 00'0010h                              | 04h             | II                   |
| Stack Underflow             | STKUF     | STUTRAP     | 00'0018h                              | 06h             | II                   |
| Class B Hardware Traps:     |           |             |                                       |                 |                      |
| Undefined opcode            | UNDOPC    | BTRAP       | 00'0028h                              | 0Ah             | I                    |
| Protected instruction fault | PRTFLT    | BTRAP       | 00'0028h                              | 0Ah             | I                    |
| Illegal word operand access | ILLOPA    | BTRAP       | 00'0028h                              | 0Ah             | I                    |
| Illegal instruction access  | ILLINA    | BTRAP       | 00'0028h                              | 0Ah             | I                    |
| Illegal external bus access | ILLBUS    | BTRAP       | 00'0028h                              | 0Ah             | I                    |
| MAC trap                    | MACTRP    | BTRAP       | 00'0028h                              | 0Ah             | I                    |
| Reserved                    |           |             | [2Ch – 3Ch]                           | [0Bh – 0Fh]     |                      |
| Software Traps              |           |             |                                       |                 |                      |
| TRAP Instruction            |           |             | Any [00'0000h – 00'01FCh] steps of 4h | Any [00h – 7Fh] | Current CPU Priority |

**Table 6 Exceptions or error conditions**

## 7 PARALLEL PORTS

The ST10R272L provides up to 77 I/O lines organized into 7 input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs by direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation by control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional bus arbitration signals ( $\overline{\text{BREQ}}$ ,  $\overline{\text{HLDA}}$ ,  $\overline{\text{HOLD}}$ ) and chip select signals. Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal  $\overline{\text{BHE}}$  and the system clock output (CLKOUT). Port 5 is used for timer control signals. Port 2 lines can be used as fast external interrupt lines. Port 7 includes alternate function for the PWM signal. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

## 8 EXTERNAL BUS CONTROLLER

All external memory accesses are performed by the on-chip External Bus Controller which can be programmed either to single chip mode when no external memory is required, or to the following external memory access modes:

|                            |                              |
|----------------------------|------------------------------|
| 16-bit data, demultiplexed | 16-/18-/20-/24-bit addresses |
| 16-bit data, multiplexed   | 16-/18-/20-/24-bit addresses |
| 8-bit data, multiplexed    | 16-/18-/20-/24-bit addresses |
| 8-bit data, demultiplexed  | 16-/18-/20-/24-bit addresses |

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0/P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Memory cycle time, memory tri-state time, length of ALE and read write delay are programmable so that a wide range of different memory types and external peripherals can be used. Up to 4 independent address windows can be defined (via ADDRSELx / BUSCONx register pairs) to access different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 etc. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external  $\overline{\text{CS}}$  signals (4 windows plus default) can be generated to reduce external glue logic. Access to very slow memories is supported by the READY function.

A  $\overline{\text{HOLD}}/\overline{\text{HLDA}}$  protocol is available for bus arbitration so that external resources can be shared with other bus masters. In slave mode, the slave controller can be connected to another master controller without glue logic. For applications which require less than 16 MBytes

## ST10R272L - PWM MODULE

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of external memory space, the address space can be restricted to 1 MByte, 256 KByte or to 64 KByte.

### 9 PWM MODULE

A 1-channel Pulse Width Modulation (PWM) Module operates on channel 3. The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. The table below shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

| <b>Mode 0<br/>edge aligned</b>   | <b>Resolution</b> | <b>8-bit</b> | <b>10-bit</b> | <b>12-bit</b> | <b>14-bit</b> | <b>16-bit</b> |
|----------------------------------|-------------------|--------------|---------------|---------------|---------------|---------------|
| CPU clock/1                      | 20ns              | 195.3 KHz    | 48.83KHz      | 12.21KHz      | 3.052KHz      | 762.9Hz       |
| CPU clock/64                     | 1.28ns            | 3.052KHz     | 762.9Hz       | 190.7Hz       | 47.68Hz       | 11.92Hz       |
| <b>Mode 1<br/>center aligned</b> | <b>Resolution</b> | <b>8-bit</b> | <b>10-bit</b> | <b>12-bit</b> | <b>14-bit</b> | <b>16-bit</b> |
| CPU clock/1                      | 20ns              | 97.66KHz     | 24.41KHz      | 6.104KHz      | 1.525KHz      | 381.5Hz       |
| CPU clock/64                     | 1.28ns            | 1.525Hz      | 381.5 Hz      | 95.37Hz       | 23.84Hz       | 0Hz           |

**Table 7 PWM unit frequencies and resolution at 50MHz CPU clock**

## 10 GENERAL PURPOSE TIMERS

The GPTs are flexible multifunctional timer/counters used for time-related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation or pulse multiplication. The GPT unit contains five 16-bit timers, organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

### 10.1 GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer, gated timer, counter mode and incremental interface mode**. In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. In counter mode, the timer is clocked in reference to external events. Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. Table 8 GPT1 timer input frequencies, resolution and periods lists the timer input frequencies, resolution and periods for each pre-scaler option at 50MHz CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

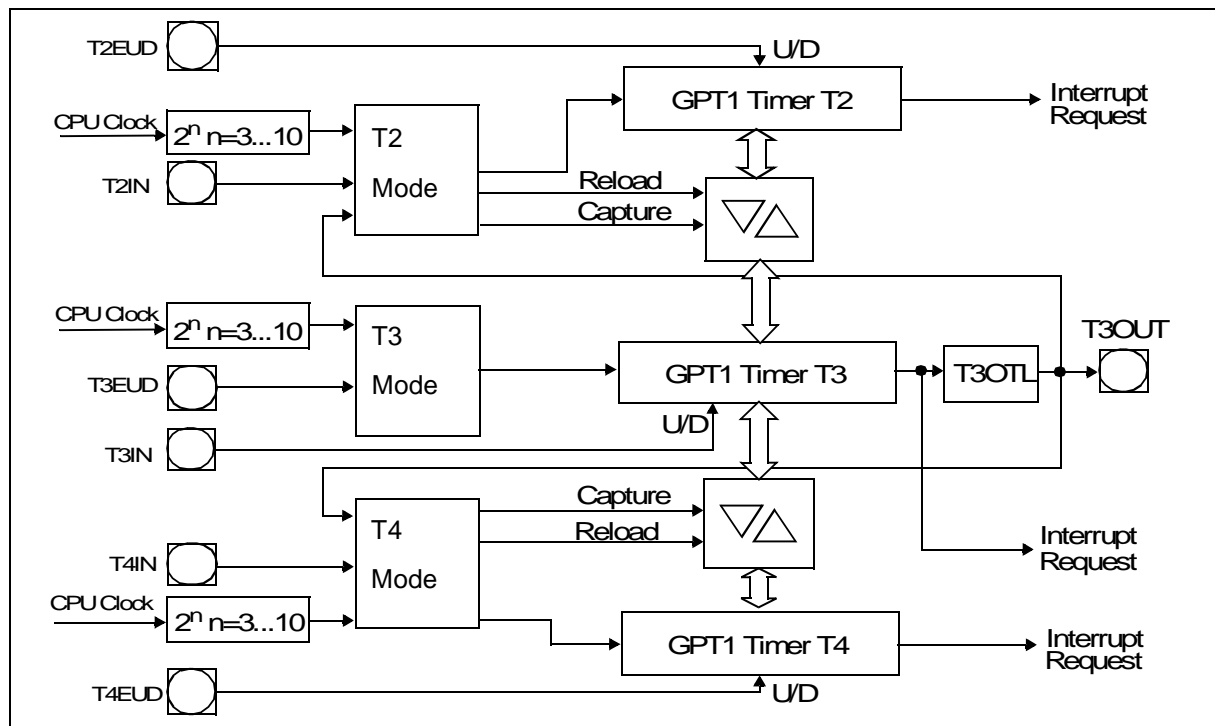
Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow/underflow. The state of this latch may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

## ST10R272L - GENERAL PURPOSE TIMERS

| $F_{CPU}=50\text{MHz}$ | Timer input selection |           |            |         |         |         |          |           |
|------------------------|-----------------------|-----------|------------|---------|---------|---------|----------|-----------|
|                        | 000b                  | 001b      | 010b       | 011b    | 100b    | 101b    | 110b     | 111b      |
| Prescaler Factor       | 8                     | 16        | 32         | 64      | 128     | 256     | 512      | 1024      |
| Input Frequency        | 6.25 MHz              | 3.125 MHz | 1.5625 MHz | 781 KHz | 391 KHz | 195 KHz | 97.5 KHz | 48.83 KHz |
| Resolution             | 160ns                 | 320ns     | 640ns      | 1.28 us | 2.56 us | 5.12 us | 10.24 us | 20.48 us  |
| Period                 | 10.49ms               | 20.97ms   | 41.94ms    | 83.88ms | 168ms   | 336ms   | 672ms    | 1.342s    |

**Table 8 GPT1 timer input frequencies, resolution and periods**



**Figure 8 GPT1 block diagram**

## ST10R272L - GENERAL PURPOSE TIMERS

### 10.2 GPT2

The GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported by the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of T6OTL may be used to clock timer T5, or may be output on a port pin T6OUT. The overflows/underflows of timer T6 reload the CAPREL register. The CAPREL register captures the contents of T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

| $F_{CPU}=50\text{MHz}$ | Timer input selection |          |           |           |         |         |         |          |
|------------------------|-----------------------|----------|-----------|-----------|---------|---------|---------|----------|
|                        | 000b                  | 001b     | 010b      | 011b      | 100b    | 101b    | 110b    | 111b     |
| Prescaler Factor       | 4                     | 8        | 16        | 32        | 64      | 128     | 256     | 512      |
| Input Frequency        | 12.5 MHz              | 6.25 MHz | 3.125 MHz | 1.563 MHz | 781 KHz | 391 KHz | 195 KHz | 97.6 KHz |
| Resolution             | 80ns                  | 160ns    | 320ns     | 640ns     | 1.28 us | 2.56 us | 5.12 us | 10.24 us |
| Period                 | 5.24ms                | 10.49ms  | 20.97ms   | 41.94ms   | 83.88ms | 167.7ms | 335.5ms | 671ms    |

**Table 9 GPT2 timer input frequencies, resolution and periods**

## ST10R272L - SERIAL CHANNELS

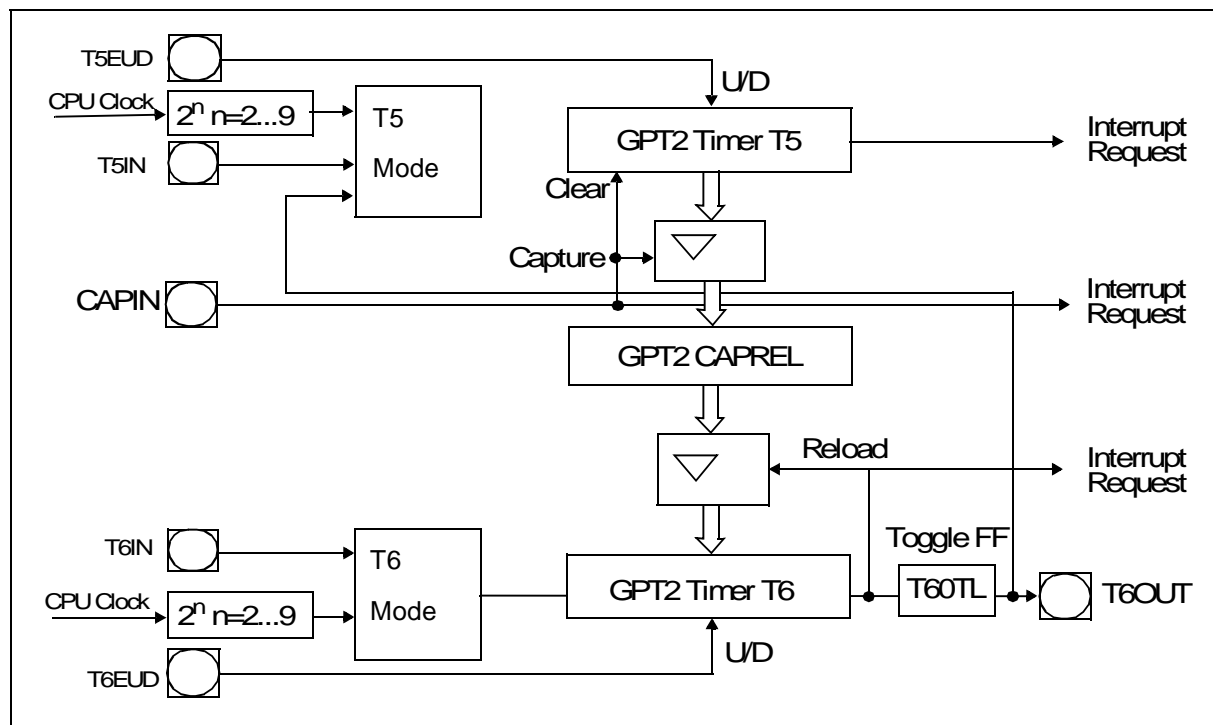


Figure 9 GPT2 block diagram

## 11 SERIAL CHANNELS

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (ASC0) and a Synchronous Serial Port (SSP).

### ASC0

A dedicated baud rate generator sets up standard baud rates without oscillator tuning. 3 separate interrupt vectors are provided for transmission, reception, and erroneous reception. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities have been included to increase the reliability of data transfers. A parity bit can be generated automatically on transmission, or checked on reception. Framing error detection recognizes data frames with missing stop bits. An overrun error is generated if the last character received was not read out of the receive buffer register at the time the reception of a new character is complete. The table below lists

**ST10R272L - SERIAL CHANNELS**

various commonly used baud rates together with the required reload values and the deviation errors compared to the intended baudrate.

| <b>S0BRS = '0', f<sub>CPU</sub> = 50MHz</b> |                        |                                       | <b>S0BRS = '1', f<sub>CPU</sub> = 50MHz</b> |                        |                                       |
|---|------------------------|---------------------------------------|---|------------------------|---------------------------------------|
| <b>Baud Rate (Baud)</b>                     | <b>Deviation Error</b> | <b>Reload Value</b>                   | <b>Baud Rate (Baud)</b>                     | <b>Deviation Error</b> | <b>Reload Value</b>                   |
| 1562500                                     | 0.0% / 0.0%            | 0000 <sub>H</sub> / 0000 <sub>H</sub> | 1041666                                     | 0.0% / 0.0%            | 0000 <sub>H</sub> / 0000 <sub>H</sub> |
| 56000                                       | +3.3% / -0.4%          | 001A <sub>H</sub> / 001B <sub>H</sub> | 56000                                       | +3.3% / -2.1%          | 0011 <sub>H</sub> / 0012 <sub>H</sub> |
| 38400                                       | +1.7% / -0.8%          | 0027 <sub>H</sub> / 0028 <sub>H</sub> | 38400                                       | +0.5% / -3.1%          | 001A <sub>H</sub> / 001B <sub>H</sub> |
| 19200                                       | +0.5% / -0.8%          | 0050 <sub>H</sub> / 0051 <sub>H</sub> | 19200                                       | +0.5% / -1.4%          | 0035 <sub>H</sub> / 0036 <sub>H</sub> |
| 9600  | +0.5% / -0.1%          | 00A1 <sub>H</sub> / 00A2 <sub>H</sub> | 9600  | +0.5% / -0.5%          | 006B <sub>H</sub> / 006C <sub>H</sub> |
| 4800  | +0.2% / -0.1%          | 0144 <sub>H</sub> / 0145 <sub>H</sub> | 4800  | 0.0% / -0.5%           | 00D8 <sub>H</sub> / 00D9 <sub>H</sub> |
| 2400  | 0.0% / -0.1%           | 028A <sub>H</sub> / 028B <sub>H</sub> | 2400  | 0.0% / -0.2%           | 01B1 <sub>H</sub> / 01B2 <sub>H</sub> |
| 1200  | 0.0% / -0.1%           | 0515 <sub>H</sub> / 0516 <sub>H</sub> | 1200  | 0.0% / -0.1%           | 0363 <sub>H</sub> / 0364 <sub>H</sub> |
| 600   | 0.0% / 0.0%            | 0A2B <sub>H</sub> / 0A2C <sub>H</sub> | 600   | 0.0% / -0.1%           | 06C7 <sub>H</sub> / 06C8 <sub>H</sub> |
| 190   | +0.4% / +0.4%          | 1FFF <sub>H</sub> / 1FFF <sub>H</sub> | 75  | 0.0% / 0.0%            | 363F <sub>H</sub> / 3640 <sub>H</sub> |
|   |                        |                                       | 127   | +0.1% / +0.1%          | 1FFF <sub>H</sub> / 1FFF <sub>H</sub> |

**Table 10 Commonly used baud rates, required reload values and deviation errors**

**SSP** transmits 1...3 bytes or receives 1 byte after sending 1...3 bytes synchronously to a shift clock which is generated by the SSP. The SSP can start shifting with the LSB or with the MSB and is used to select shifting and latching clock edges, and clock polarity. Up to two chip select lines may be activated in order to direct data transfers to one or both of two peripheral devices.

When the SSP is enabled, the four upper pins of Port4 can not be used as general purpose IO. Note that the segment address selection done via the system start-up configuration during reset has priority and overrides the SSP functions on these pins.

| <b>SSPCKS Value</b> |                                    | <b>Synchronous baud rate</b> |
|---------------------|------------------------------------|------------------------------|
| 000                 | SSP clock = CPU clock divided by 2 | 25 MBit/s                    |
| 001                 | SSP clock = CPU clock divided by 4 | 12.5 MBit/s                  |
| 010                 | SSP clock = CPU clock divided by 8 | 6.25 MBit/s                  |

**Table 11 Synchronous baud rate and SSPCKS reload values**

**ST10R272L - WATCHDOG TIMER**

| SSPCKS Value |                                      | Synchronous baud rate |
|--------------|--------------------------------------|-----------------------|
| 011          | SSP clock = CPU clock divided by 16  | 3.13 MBit/s           |
| 100          | SSP clock = CPU clock divided by 32  | 1.56 MBit/s           |
| 101          | SSP clock = CPU clock divided by 64  | 781 KBit/s            |
| 110          | SSP clock = CPU clock divided by 128 | 391 KBit/s            |
| 111          | SSP clock = CPU clock divided by 256 | 195 KBit/s            |

**Table 11 Synchronous baud rate and SSPCKS reload values****12 WATCHDOG TIMER**

The Watchdog Timer is a fail-safe mechanism which limits the malfunction time of the controller. The Watchdog Timer is always enabled after device reset and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. In this way, the chip's start-up procedure is always monitored. The software must be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to maintain the Watchdog Timer, it will overflow generating an internal hardware reset and pulling the  $\overline{\text{RSTOUT}}$  pin low to reset external hardware components.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a pre-specified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. The table below shows the watchdog time range which for a 50MHz CPU clock rounded to 3 significant figures.

| Reload value<br>in WDTREL | Prescaler for $f_{\text{CPU}}$ |                   |
|---------------------------|--------------------------------|-------------------|
|                           | 2 (WDTIN = '0')                | 128 (WDTIN = '1') |
| FF <sub>H</sub>           | 10.24 $\mu\text{s}$            | 655 $\mu\text{s}$ |
| 00 <sub>H</sub>           | 2.62 ms                        | 168 ms            |

**Table 12 Watchdog timer range**

## 13 SYSTEM RESET

The following type of reset are implemented on the ST10R272L:

**Asynchronous hardware reset:** Asynchronous reset does not require a stabilized clock signal on XTAL1 as it is not internally resynchronized, it resets the microcontroller into its default reset state. Asynchronous reset is required on chip power-up and can be used during catastrophic situations. The rising edge of the RSTIN pin is internally resynchronized before exiting the reset condition, therefore, only the entry to hardware reset is asynchronous.

**Synchronous hardware reset (warm reset):** A warm synchronous hardware reset is triggered when the reset input signal  $\overline{\text{RSTIN}}$  is latched low and Vpp pin is high. The I/Os are immediately (asynchronously) set in high impedance,  $\overline{\text{RSTOUT}}$  is driven low. After  $\overline{\text{RSTIN}}$  negation is detected, a short transition period elapses, during which pending internal hold states are cancelled and any current internal access cycles are completed, external bus cycles are aborted. Then, the internal reset sequence is active for 1024 TCL (512 CPU clock cycles). During this reset sequence, if bit BDRSTEN was previously set by software (bit 3 in SYSCON register),  $\overline{\text{RSTIN}}$  pin is driven low and internal reset signal is asserted to reset the microcontroller in its default state. Note that after all reset sequence, bit BDRSTEN is cleared. After the reset sequence has been completed, the  $\overline{\text{RSTIN}}$  input is sampled. When the reset input signal is active at that time the internal reset condition is prolonged until  $\overline{\text{RSTIN}}$  becomes inactive.

**Software reset:** The reset sequence can be triggered at any time by the protected instruction SRST (software reset). This instruction can be executed deliberately within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals a system failure. As for a synchronous hardware reset, if bit BDRSTEN was previously set by software (bit 3 in SYSCON register), the reset sequence lasts 1024 TCL (512 CPU clock cycles), and drives the  $\overline{\text{RSTIN}}$  pin low.

**Watchdog timer reset:** When the watchdog timer is not disabled during the initialization or serviced regularly during program execution it will overflow and trigger the reset sequence. Unlike hardware and software resets, the watchdog reset completes a running external bus cycle if this bus cycle does not use  $\overline{\text{READY}}$ , or if  $\overline{\text{READY}}$  is sampled active (low) after the programmed waitstates. When  $\overline{\text{READY}}$  is sampled inactive (high) after the programmed waitstates the running external bus cycle is aborted. Then the internal reset sequence is started. The watchdog reset cannot occur while the ST10R272L is in bootstrap loader mode.

**Bidirectional reset:** The bidirectional reset is activated by setting bit BDRSTEN (bit 3 in SYSCON register). This reset makes the watchdog timer reset and software reset externally visible. It is active for the duration of an internal reset sequences caused by a watchdog timer reset and software reset. Therefore, the bidirectional reset transforms an internal watchdog timer reset or software reset into an external hardware reset with a minimum duration of 1024 TCL.

## ST10R272L - POWER REDUCTION MODES

### 14 POWER REDUCTION MODES

Two different power reduction modes with different levels of power reduction can be entered under software control.

In **Idle mode** the CPU is stopped, while the peripherals continue their operation. Idle mode can be terminated by any reset or interrupt request.

In **Power Down mode** both the CPU and the peripherals are stopped. Power Down mode can now be configured by software in order to be terminated only by a hardware reset or by an external interrupt source on fast external interrupt pins.

All external bus actions are completed before Idle or Power Down mode is entered. However, Idle or Power Down mode is **not** entered if READY is enabled, but has not been activated (driven low for negative polarity, or driven high for positive polarity) during the last bus access.

### 15 SPECIAL FUNCTION REGISTERS

The following table lists all ST10R272L SFRs in alphabetical order.

Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the Extended SFR-Space (ESFRs) are marked with the letter “E” in column “Physical Address”.

An SFR can be specified by its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed by its physical address (using the Data Page Pointers), or by its short 8-bit address (without using the Data Page Pointers).

| Name      | Physical Address | 8-Bit Address | Description                      | Reset Value |
|-----------|------------------|---------------|----------------------------------|-------------|
| ADDRSEL1  | FE18h            | 0Ch           | Address Select Register 1        | 0000h       |
| ADDRSEL2  | FE1Ah            | 0Dh           | Address Select Register 2        | 0000h       |
| ADDRSEL3  | FE1Ch            | 0Eh           | Address Select Register 3        | 0000h       |
| ADDRSEL4  | FE1Eh            | 0Fh           | Address Select Register 4        | 0000h       |
| BUSCON0 b | FF0Ch            | 86h           | Bus Configuration Register 0     | 0XX0h       |
| BUSCON1 b | FF14h            | 8Ah           | Bus Configuration Register 1     | 0000h       |
| BUSCON2 b | FF16h            | 8Bh           | Bus Configuration Register 2     | 0000h       |
| BUSCON3 b | FF18h            | 8Ch           | Bus Configuration Register 3     | 0000h       |
| BUSCON4 b | FF1Ah            | 8Dh           | Bus Configuration Register 4     | 0000h       |
| CAPREL    | FE4Ah            | 25h           | GPT2 Capture/Reload Register     | 0000h       |
| CC8IC b   | FF88h            | C4h           | EX0IN Interrupt Control Register | 0000h       |

**Table 13 Special functional registers**

## ST10R272L - SPECIAL FUNCTION REGISTERS

| Name    | Physical Address | 8-Bit Address | Description                                   | Reset Value |
|---------|------------------|---------------|---|-------------|
| CC9IC   | b FF8Ah          | C5h           | EX1IN Interrupt Control Register              | 0000h       |
| CC10IC  | b FF8Ch          | C6h           | EX2IN Interrupt Control Register              | 0000h       |
| CC11IC  | b FF8Eh          | C7h           | EX3IN Interrupt Control Register              | 0000h       |
| CP      | FE10h            | 08h           | CPU Context Pointer Register                  | FC00h       |
| CRIC    | b FF6Ah          | B5h           | GPT2 CAPREL Interrupt Control Register        | 0000h       |
| CSP     | FE08h            | 04h           | CPU Code Segment Pointer Register (read only) | 0000h       |
| DP0L    | b F100h E        | 80h           | P0L Direction Control Register                | 00h         |
| DP0H    | b F102h E        | 81h           | P0h Direction Control Register                | 00h         |
| DP1L    | b F104h E        | 82h           | P1L Direction Control Register                | 00h         |
| DP1H    | b F106h E        | 83h           | P1h Direction Control Register                | 00h         |
| DP2     | b FFC2h          | E1h           | Port 2 Direction Control Register             | -0--h       |
| DP3     | b FFC6h          | E3h           | Port 3 Direction Control Register             | 0000h       |
| DP4     | b FFCAh          | E5h           | Port 4 Direction Control Register             | 00h         |
| DP6     | b FFCEh          | E7h           | Port 6 Direction Control Register             | 00h         |
| DP7     | b FFD2h          | E9h           | Port 7 Direction Control Register             | -0h         |
| DPP0    | FE00h            | 00h           | CPU Data Page Pointer 0 Register (10 bits)    | 0000h       |
| DPP1    | FE02h            | 01h           | CPU Data Page Pointer 1 Register (10 bits)    | 0001h       |
| DPP2    | FE04h            | 02h           | CPU Data Page Pointer 2 Register (10 bits)    | 0002h       |
| DPP3    | FE06h            | 03h           | CPU Data Page Pointer 3 Register (10 bits)    | 0003h       |
| EBUSCON | b F10Eh E        | 87H           | Extended BUSCON register                      | 0000h       |
| EXICON  | b F1C0h E        | E0h           | External Interrupt Control Register           | 0000h       |
| IDCHIP  | F07Ch E          | 3Eh           | Device Identifier Register                    | 1101h       |
| IDMANUF | F07Eh E          | 3Fh           | Manufacturer/Process Identifier Register      | 0201h       |
| IDMEM   | F07Ah E          | 3Dh           | On-chip Memory Identifier Register            | 0000h       |
| IDPROG  | F078h E          | 3Ch           | Programming Voltage Identifier Register       | 0000h       |
| IDX0    | b FF08h          | 84h           | MAC Unit Address Pointer 0                    | 0000h       |

Table 13 Special functional registers

**ST10R272L - SPECIAL FUNCTION REGISTERS**

| Name  |   | Physical Address | 8-Bit Address | Description                                | Reset Value |
|-------|---|------------------|---------------|--|-------------|
| IDX1  | b | FF0Ah            | 85h           | MAC Unit Address Pointer 1                 | 0000h       |
| MAH   |   | FE5Eh            | 2Fh           | MAC Unit Accumulator - High Word           | 0000h       |
| MAL   |   | FE5Ch            | 2Eh           | MAC Unit Accumulator - Low Word            | 0000h       |
| MCW   |   | FFDCh            | EEh           | MAC Unit Control Word                      | 0000h       |
| MDC   | b | FF0Eh            | 87h           | CPU Multiply Divide Control Register       | 0000h       |
| MDH   |   | FE0Ch            | 06h           | CPU Multiply Divide Register – High Word   | 0000h       |
| MDL   |   | FE0Eh            | 07h           | CPU Multiply Divide Register – Low Word    | 0000h       |
| MRW   | b | FFDAh            | EDh           | MAC Unit Repeat Word                       | 0000h       |
| MSW   | b | FFDEh            | EFh           | MAC Unit Status Word                       | 0200h       |
| ODP2  | b | F1C2h E          | E1h           | Port 2 Open Drain Control Register         | -0--h       |
| ODP3  | b | F1C6h E          | E3h           | Port 3 Open Drain Control Register         | 0000h       |
| ODP6  | b | F1CEh E          | E7h           | Port 6 Open Drain Control Register         | 00h         |
| ODP7  | b | F1D2h E          | E9h           | Port 7 Open Drain Control Register         | -0h         |
| ONES  |   | FF1Eh            | 8Fh           | Constant Value 1's Register (read only)    | FFFFh       |
| P0L   | b | FF00h            | 80h           | Port 0 Low Register (Lower half of PORT0)  | 00h         |
| P0H   | b | FF02h            | 81h           | Port 0 High Register (Upper half of PORT0) | 00h         |
| P1L   | b | FF04h            | 82h           | Port 1 Low Register (Lower half of PORT1)  | 00h         |
| P1H   | b | FF06h            | 83h           | Port 1 High Register (Upper half of PORT1) | 00h         |
| P2    | b | FFC0h            | E0h           | Port 2 Register (4 bits)                   | -0--h       |
| P3    | b | FFC4h            | E2h           | Port 3 Register                            | 0000h       |
| P4    | b | FFC8h            | E4h           | Port 4 Register (8 bits)                   | 00h         |
| P5    | b | FFA2h            | D1h           | Port 5 Register (read only)                | XXXXh       |
| P6    | b | FFCCh            | E6h           | Port 6 Register (8 bits)                   | 00h         |
| P7    | b | FFD0h            | E8h           | Port 7 Register (4 bits)                   | -0h         |
| PECC0 |   | FEC0h            | 60h           | PEC Channel 0 Control Register             | 0000h       |
| PECC1 |   | FEC2h            | 61h           | PEC Channel 1 Control Register             | 0000h       |

**Table 13 Special functional registers**

## ST10R272L - SPECIAL FUNCTION REGISTERS

| Name      | Physical Address | 8-Bit Address | Description  | Reset Value |
|-----------|------------------|---------------|--|-------------|
| PECC2     | FEC4h            | 62h           | PEC Channel 2 Control Register                         | 0000h       |
| PECC3     | FEC6h            | 63h           | PEC Channel 3 Control Register                         | 0000h       |
| PECC4     | FEC8h            | 64h           | PEC Channel 4 Control Register                         | 0000h       |
| PECC5     | FECAh            | 65h           | PEC Channel 5 Control Register                         | 0000h       |
| PECC6     | FECCh            | 66h           | PEC Channel 6 Control Register                         | 0000h       |
| PECC7     | FECEh            | 67h           | PEC Channel 7 Control Register                         | 0000h       |
| PP3       | F03Eh E          | 1Fh           | PWM Module Period Register 3                           | 0000h       |
| PSW b     | FF10h            | 88h           | CPU Program Status Word                                | 0000h       |
| PW3       | FE36h            | 1Bh           | PWM Module Pulse Width Register 3                      | 0000h       |
| PWMCON0 b | FF30h            | 98h           | PWM Module Control Register 0                          | 0000h       |
| PWMCON1 b | FF32h            | 99h           | PWM Module Control Register 1                          | 0000h       |
| PWMIC b   | F17Eh E          | BFh           | PWM Module Interrupt Control Register                  | 0000h       |
| QR0       | F004h E          | 02h           | MAC Unit Offset Register R0 (8 bits)                   | 00h         |
| QR1       | F006h E          | 03h           | MAC Unit Offset Register R1 (8 bits)                   | 00h         |
| QX0       | F000h E          | 00h           | MAC Unit Offset Register X0 (8 bits)                   | 00h         |
| QX1       | F002h E          | 01h           | MAC Unit Offset Register X1 (8 bits)                   | 00h         |
| RP0H b    | F108h E          | 84h           | System Start-up Configuration Register (Rd. only)      | XXh         |
| S0BG      | FEB4h            | 5Ah           | Serial Channel 0 baud rate generator reload reg        | 0000h       |
| S0CON b   | FFB0h            | D8h           | Serial Channel 0 Control Register                      | 0000h       |
| S0EIC b   | FF70h            | B8h           | Serial Channel 0 Error Interrupt Control Register      | 0000h       |
| S0RBUF    | FEB2h            | 59h           | Serial Channel 0 receive buffer reg. (rd only)         | XXh         |
| S0RIC b   | FF6Eh            | B7h           | Serial Channel 0 Receive Interrupt Control Reg.        | 0000h       |
| S0TBIC b  | F19Ch E          | CEh           | Serial Channel 0 transmit buffer interrupt control reg | 0000h       |
| S0TBUF    | FEB0h            | 58h           | Serial Channel 0 transmit buffer register (wr only)    | 00h         |
| S0TIC b   | FF6Ch            | B6h           | Serial Channel 0 Transmit Interrupt Control Register   | 0000h       |

Table 13 Special functional registers

**ST10R272L - SPECIAL FUNCTION REGISTERS**

| Name     | Physical Address | 8-Bit Address | Description                             | Reset Value         |
|----------|------------------|---------------|---|---------------------|
| SP       | FE12h            | 09h           | CPU System Stack Pointer Register       | FC00h               |
| SSPCON0  | EF00h X          | ---           | SSP Control Register 0                  | 0000h               |
| SSPCON1  | EF02h X          | ---           | SSP Control Register 1                  | 0000h               |
| SSPRTB   | EF04h X          | ---           | SSP Receive/Transmit Buffer             | XXXXh               |
| SSPTBH   | EF06h X          | ---           | SSP Transmit Buffer High                | XXXXh               |
| STKOV    | FE14h            | 0Ah           | CPU Stack Overflow Pointer Register     | FA00h               |
| STKUN    | FE16h            | 0Bh           | CPU Stack Underflow Pointer Register    | FC00h               |
| SYSCON b | FF12h            | 89h           | CPU System Configuration Register       | 0xx0h <sup>1)</sup> |
| T2       | FE40h            | 20h           | GPT1 Timer 2 Register                   | 0000h               |
| T2CON b  | FF40h            | A0h           | GPT1 Timer 2 Control Register           | 0000h               |
| T2IC b   | FF60h            | B0h           | GPT1 Timer 2 Interrupt Control Register | 0000h               |
| T3       | FE42h            | 21h           | GPT1 Timer 3 Register                   | 0000h               |
| T3CON b  | FF42h            | A1h           | GPT1 Timer 3 Control Register           | 0000h               |
| T3IC b   | FF62h            | B1h           | GPT1 Timer 3 Interrupt Control Register | 0000h               |
| T4       | FE44h            | 22h           | GPT1 Timer 4 Register                   | 0000h               |
| T4CON b  | FF44h            | A2h           | GPT1 Timer 4 Control Register           | 0000h               |
| T4IC b   | FF64h            | B2h           | GPT1 Timer 4 Interrupt Control Register | 0000h               |
| T5       | FE46h            | 23h           | GPT2 Timer 5 Register                   | 0000h               |
| T5CON b  | FF46h            | A3h           | GPT2 Timer 5 Control Register           | 0000h               |
| T5IC b   | FF66h            | B3h           | GPT2 Timer 5 Interrupt Control Register | 0000h               |
| T6       | FE48h            | 24h           | GPT2 Timer 6 Register                   | 0000h               |
| T6CON b  | FF48h            | A4h           | GPT2 Timer 6 Control Register           | 0000h               |
| T6IC b   | FF68h            | B4h           | GPT2 Timer 6 Interrupt Control Register | 0000h               |
| TFR b    | FFACh            | D6h           | Trap Flag Register                      | 0000h               |
| WDT      | FEAEh            | 57h           | Watchdog Timer Register (read only)     | 0000h               |
| WDTCON   | FFAEh            | D7h           | Watchdog Timer Control Register         | 000xh <sup>2)</sup> |

**Table 13 Special functional registers**

**ST10R272L - SPECIAL FUNCTION REGISTERS**

| <b>Name</b> |   | <b>Physical Address</b> |   | <b>8-Bit Address</b> | <b>Description</b>                      | <b>Reset Value</b> |
|-------------|---|-------------------------|---|----------------------|---|--------------------|
| XP1IC       | b | F18Eh                   | E | C7h                  | SSP Interrupt Control Register          | 0000h              |
| XP3IC       | b | F19Eh                   | E | CFh                  | PLL unlock Interrupt Control Register   | 0000h              |
| ZEROS       | b | FF1Ch                   |   | 8Eh                  | Constant Value 0's Register (read only) | 0000h              |

**Table 13 Special functional registers**

*Note 1. The system configuration is selected during reset.*

*Note 2. Bit WDTR indicates a watchdog timer triggered reset.*

## ST10R272L - ELECTRICAL CHARACTERISTICS

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### 16 ELECTRICAL CHARACTERISTICS

#### 16.1 Absolute Maximum Ratings

- Ambient temperature under bias ( $T_A$ ): ..... -40 to +85 °C
- Storage temperature ( $T_{ST}$ ): ..... – 65 to +150 °C
- Voltage on  $V_{DD}$  pins with respect to ground ( $V_{SS}$ ): ..... – 0.5 to +4.0 V
- Voltage on any pin with respect to ground ( $V_{SS}$ ): ..... –0.5 to  $V_{DD} + 0.5$  V
- Voltage on any 5V tolerant pin with respect to ground ( $V_{SS}$ ): ..... –0.5 to 5.5 V
- Voltage on any 5V fail-safe pin with respect to ground ( $V_{SS}$ ): ..... –0.5 to 5.5 V
- Input current on any pin during overload condition: ..... –10 to +10 mA
- Absolute sum of all input currents during overload condition: ..... |100 mA|
- Power dissipation: ..... 1.0 W

*Note* Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ( $V_{IN} > V_{DD}$  or  $V_{IN} < V_{SS}$ ) the voltage on pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the Absolute Maximum Ratings.

The parameters listed in this section represent both the ST10R272L controller characteristics and the system requirements. To aid parameters interpretation in design evaluation, the a symbol column is marked:

**CC** for **C**ontroller **C**haracteristics: The ST10R272L logic provides signals with the respective timing characteristics.

**SR** for **S**ystem Requirement: The external system must provide signals with the respective timing characteristics to the ST10R272L.

## ST10R272L - ELECTRICAL CHARACTERISTICS

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### Remarks on 5 volt tolerant (5T) and 5 volt fail-safe (5S) pins

The 5V tolerant input and output pins can sustain an absolute maximum external voltage of 5.5V.

However, signals on unterminated bus lines might have overshoot above 5.5V, presenting latchup and hot carrier risks. While these risks are under evaluation, observe the following security recommendations:

- Maximum peak voltage on 5V tolerant pin with respect to ground ( $V_{SS}$ )= +6 V
- If the ringing of the external signal exceeds 6V, then clip the signal to the 5V supply.

### Power supply failure condition

The power supply failure condition is a state where the chip is NOT supplied but is connected to active signal lines. There are several cases:

- 3.3V external lines on 3.3V (3T) pin on the non powered chip: .....NOT Acceptable
- 3.3V external lines on 5V tolerant (5T) pin on the non powered chip: ..... Acceptable  
The 5V tolerant buffer do not leak: external signals not altered. No reliability problem.
- 3.3V external lines on 5V fail-safe (5S) pin on the non powered chip: ..... Acceptable  
The 5V tolerant buffer do not leak: external signals not altered. No reliability problem.
- 5.5V external lines on 5V tolerant (5T) pin on the non powered chip: ..... Acceptable  
For VERY SHORT times only: the buffers do not leak (external signals not altered) but there is a fast degradation of the gate oxides in the buffers. The total maximum time under this stress condition is 2 days. This limits this configuration to short power-up/down sequences. For 10 year life time, the maximum duty factor is 1/1800 allowing e.g. a maximum stress duration of 48 seconds per day.
- 5.5V external lines on 5V fail-safe (5S) pin on the non powered chip: ..... Acceptable
- 6V transient signals on 5V tolerant (5T) pin on the non powered chip: ...NOT Acceptable
- 6V transient signals on 5V fail-safe (5S) pin on the non powered chip:..... Acceptable

**ST10R272L - ELECTRICAL CHARACTERISTICS****16.2 DC Characteristics**

$V_{DD} = 3.3V \pm 0.3V$

$V_{SS} = 0 V$

Reset active

$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$

| Parameter   | Symbol                   |    | Limit Values |                          | Unit                           | Test Condition  |
|---|--------------------------|----|--------------|--------------------------|--------------------------------|---|
|   |                          |    | min.         | max.                     |                                |   |
| Input low voltage   | $V_{IL}$                 | SR | -0.3         | 0.8                      | V                              | -   |
| Input high voltage<br>(all except $\overline{RSTIN}$ and XTAL1)   | $V_{IH}$                 | SR | 2.0          | $V_{DD} + 0.3$           | V                              | -   |
| Input high voltage $\overline{RSTIN}$ , RPD   | $V_{IH1}$                | SR | $0.6 V_{DD}$ | $V_{DD} + 0.3$           | V                              | -   |
| Input high voltage XTAL1  | $V_{IH2}$                | SR | $0.7 V_{DD}$ | $V_{DD} + 0.3$           | V                              | -   |
| Output low voltage<br>(ALE, $\overline{RD}$ , $\overline{WR}$ , $\overline{BHE}$ , CLKOUT,<br>$\overline{RSTIN}$ , $\overline{RSTOUT}$ , $\overline{CSX}$ ) | $V_{OL}$                 | CC | -            | 0.4                      | V                              | $I_{OL} = 4 \text{ mA}$   |
| Output low voltage<br>(all other outputs)   | $V_{OL1}$                | CC | -            | 0.4                      | V                              | $I_{OL1} = 2 \text{ mA}$  |
| Output high voltage<br>ALE, $\overline{RD}$ , $\overline{WR}$ , $\overline{BHE}$ , CLKOUT,<br>$\overline{RSTIN}$ , $\overline{RSTOUT}$ , $\overline{CSX}$ ) | $V_{OH}$                 | CC | 2.4          | -                        | V                              | $I_{OH} = -4 \text{ mA}$  |
| Output high voltage <sup>1)</sup><br>(all other outputs)  | $V_{OH1}$                | CC | 2.4          | -                        | V                              | $I_{OH} = -2 \text{ mA}$  |
| Input leakage current (3T pins)   | $I_{OZ}$                 | CC | -            | $\pm 10$                 | $\mu\text{A}$                  | $0 \text{ V} < V_{IN} < V_{DD}$   |
| Input leakage current (5T, 5S<br>pins)  | $I_{OZ1}$                | CC | -            | $\pm 10$<br>$\pm 100^7)$ | $\mu\text{A}$<br>$\mu\text{A}$ | $0 \text{ V} < V_{IN} < V_{DD}$<br>$V_{DD} < V_{IN} < 5.0 \text{ V}^7)$ |
| $\overline{RSTIN}$ pull-up resistor <sup>2)</sup>   | $R_{RST}$                | CC | 20           | 300                      | $\text{k}\Omega$               | $V_{IN} = 0 \text{ V}$  |
| Read/Write pullup current <sup>3)</sup>   | $I_{RWH}$ <sup>4)</sup>  |    | -            | -40                      | $\mu\text{A}$                  | $V_{OUT} = 2.4 \text{ V}$   |
| Read/Write pullup current <sup>3)</sup>   | $I_{RWL}$ <sup>5)</sup>  |    | -500         | -                        | $\mu\text{A}$                  | $V_{OUT} = 0.4 \text{ V}$   |
| ALE pulldown current <sup>3)</sup>  | $I_{ALEL}$ <sup>4)</sup> |    | 40           | -                        | $\mu\text{A}$                  | $V_{OUT} = 0.4 \text{ V}$   |
| ALE pulldown current <sup>3)</sup>  | $I_{ALEH}$ <sup>5)</sup> |    | -            | 500                      | $\mu\text{A}$                  | $V_{OUT} = 2.4 \text{ V}$   |
| Port 6 ( $\overline{CS}$ ) pullup current <sup>3)</sup>   | $I_{P6H}$ <sup>4)</sup>  |    | -            | -40                      | $\mu\text{A}$                  | $V_{OUT} = 2.4 \text{ V}$   |
| Port 6 ( $\overline{CS}$ ) pullup current <sup>3)</sup>   | $I_{P6L}$ <sup>5)</sup>  |    | -500         | -                        | $\mu\text{A}$                  | $V_{OUT} = 0.4 \text{ V}$   |

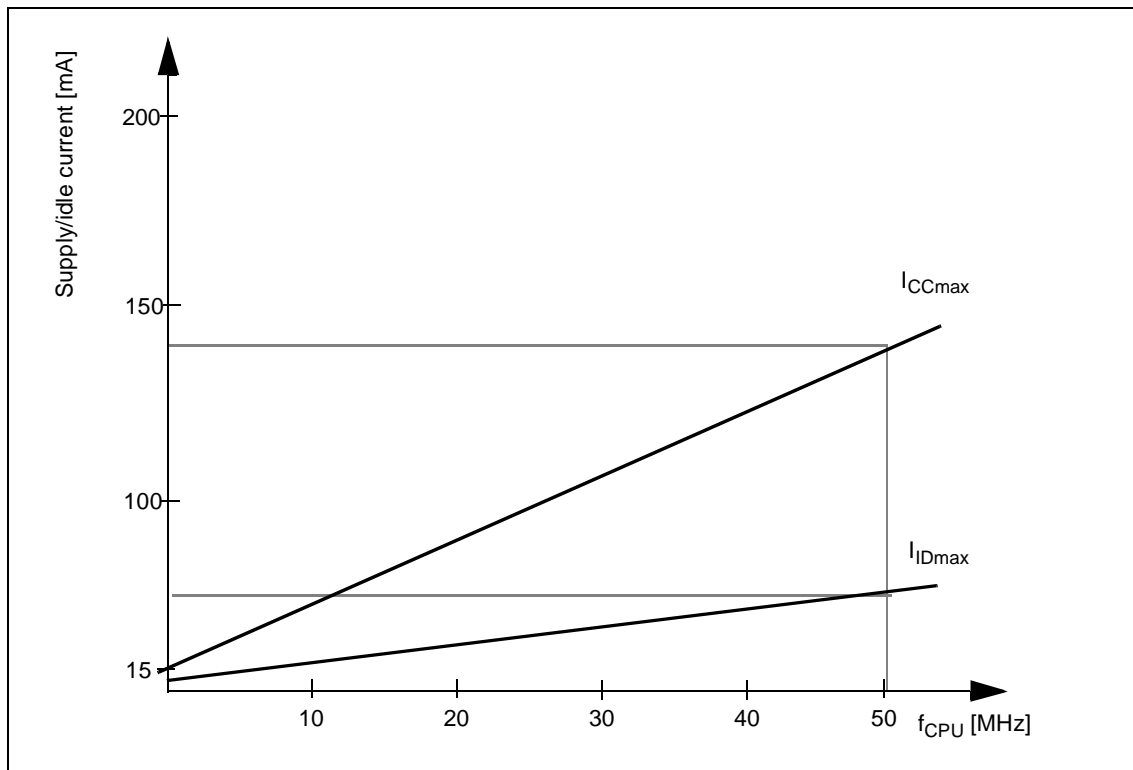
**Table 14 DC characteristics**

## ST10R272L - ELECTRICAL CHARACTERISTICS

| Parameter   | Symbol                 | Limit Values |                      | Unit          | Test Condition   |
|---|------------------------|--------------|----------------------|---------------|--|
|   |                        | min.         | max.                 |               |  |
| PORT0 configuration current <sup>3</sup>                  | $I_{POH}$ <sup>4</sup> | –            | -4                   | $\mu\text{A}$ | $V_{IN} = V_{IHmin}$   |
|   | $I_{POL}$ <sup>5</sup> | -50          | –                    | $\mu\text{A}$ | $V_{IN} = V_{ILmax}$   |
| RPD pulldown current <sup>2</sup>                         | $I_{RPD}$ <sup>5</sup> | 100          | 500                  | $\mu\text{A}$ | $V_{OUT} = V_{DD}$   |
| XTAL1 input current                                       | $I_{IL}$ CC            | –            | $\pm 20$             | $\mu\text{A}$ | $0\text{ V} < V_{IN} < V_{DD}$                                   |
| Pin capacitance <sup>6)</sup><br>(digital inputs/outputs) | $C_{IO}$ CC            | –            | 10                   | pF            | $f = 1\text{ MHz}$<br>$T_A = 25\text{ }^\circ\text{C}$           |
| Power supply current                                      | $I_{CC}$               | –            | $15 + 2.5 * f_{CPU}$ | mA            | $f_{CPU}$ in [MHz] <sup>7)</sup>                                 |
| Idle mode supply current                                  | $I_{ID}$               | –            | $10 + 0.9 * f_{CPU}$ | mA            | $\overline{RSTIN} = V_{IH1}$<br>$f_{CPU}$ in [MHz] <sup>7)</sup> |
| Power-down mode supply current                            | $I_{PD}$ <sup>8</sup>  | –            | 200                  | $\mu\text{A}$ | $V_{DD} = 3.6\text{ V}$ <sup>9)</sup>                            |

Table 14 DC characteristics

- 1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the resulting voltage comes from the external circuitry.
- 2) This specification is only valid during reset, or interruptible power-down mode, after reception of an external interrupt signal that will wake up the CPU.
- 3) This specification is only valid during reset, hold or adapt-mode. Port 6 pins are only affected if they are used for  $\overline{CS}$  output and the open drain function is not enabled.
- 4) The maximum current may be drawn while the signal line remains inactive.
- 5) The minimum current must be drawn in order to drive the signal line active.
- 6) Not 100% tested, guaranteed by design characterization.
- 7) Supply current is a function of operating frequency as illustrated in Figure 10 on page 44. This parameter is tested at  $V_{DDmax}$  and 50 MHz CPU clock with all outputs disconnected and all inputs at  $V_{IL}$  or  $V_{IH}$  with an infinite execution of NOP instruction fetched from external memory (16-bit demux bus mode, no waitstates, no memory tri-state waitstates, normal ALE).
- 8) Typical value at  $25^\circ\text{C} = 20\text{ }\mu\text{A}$ .
- 9) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at  $V_{DD} - 0.1\text{ V}$  to  $V_{DD}$ ,  $V_{REF} = 0\text{ V}$ , all outputs (including pins configured as outputs) disconnected.

**ST10R272L - ELECTRICAL CHARACTERISTICS****Figure 10 Supply/idle current vs operating frequency**

## ST10R272L - ELECTRICAL CHARACTERISTICS

### 16.3 AC Characteristics

#### Test conditions

- Input pulse levels: ..... 0 to +3.0 V
- Input rise and fall times (10%-90%): ..... 2.5 ns
- Input timing reference levels: ..... +1.5 V
- Output timing reference levels: ..... +1.5 V
- Output load: ..... see Figure 12

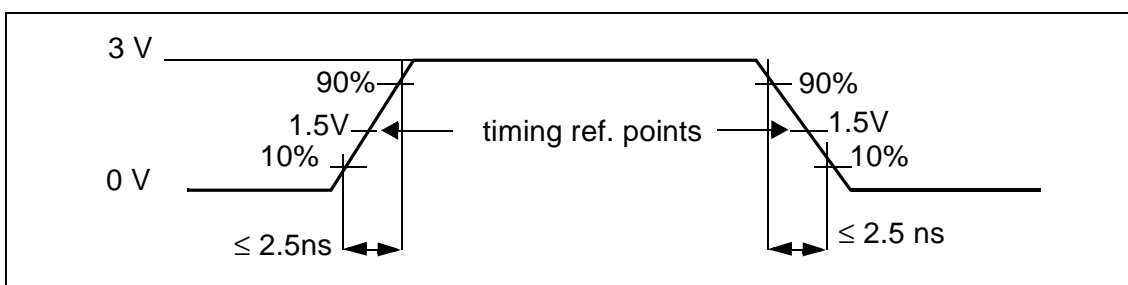


Figure 11 Input waveforms

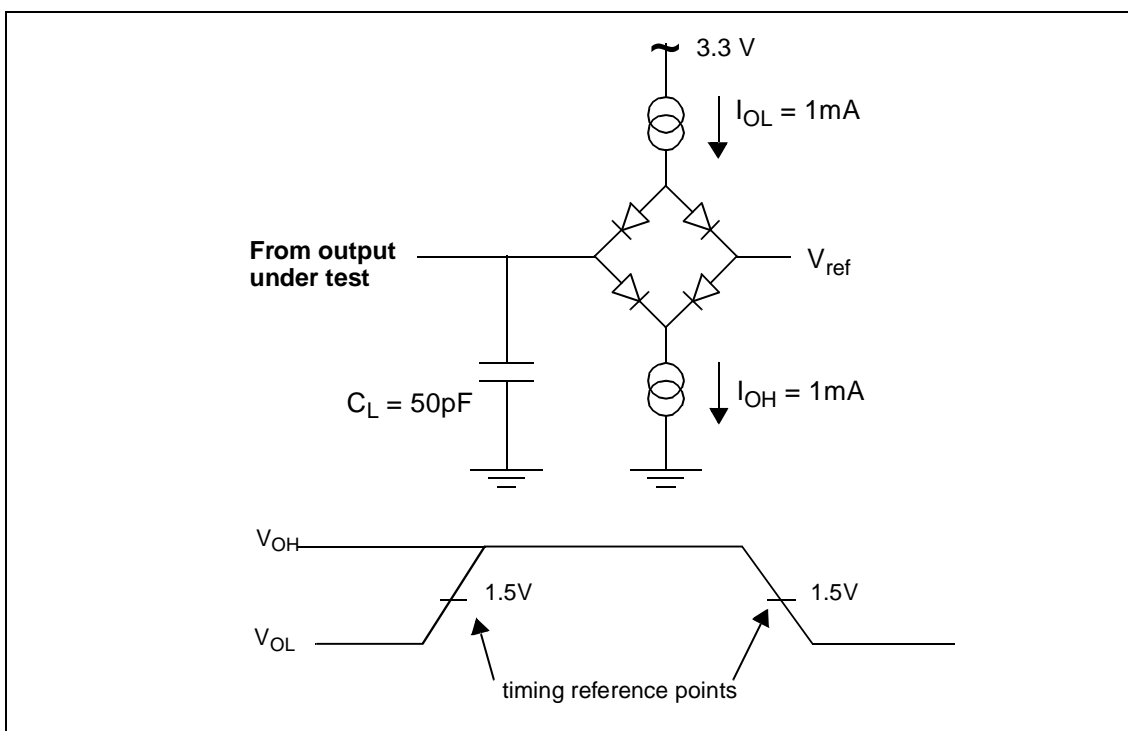
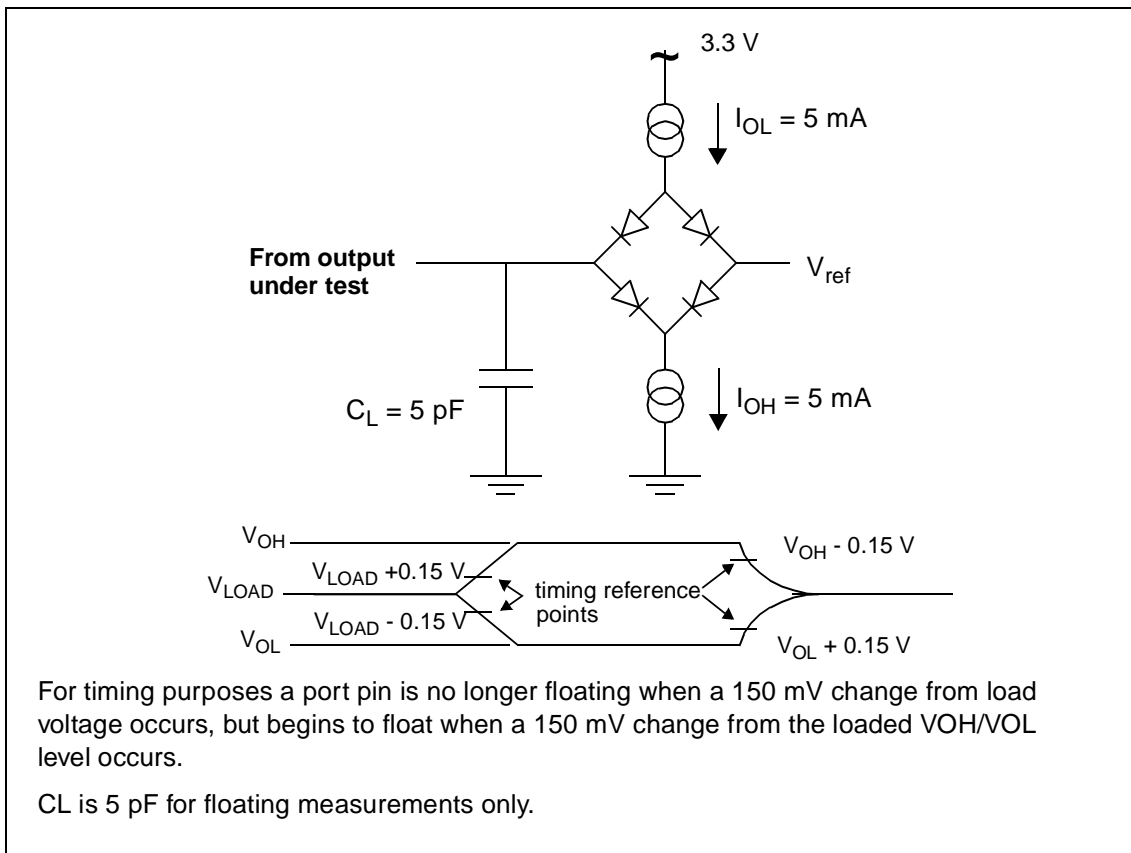


Figure 12 Output load circuit waveform

## ST10R272L - ELECTRICAL CHARACTERISTICS



**Figure 13 Float waveforms**

## ST10R272L - ELECTRICAL CHARACTERISTICS

### 16.3.1 CPU Clock Generation Mechanisms

ST10R272L internal operation is controlled by the CPU clock  $f_{CPU}$ . Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations. The external timing (AC Characteristics) specification therefore depends on the time between two consecutive edges of the CPU clock, called "TCL" (see figure below).

The CPU clock signal can be generated by different mechanisms. The duration of TCLs and their variation (and also the external timing) depends on the  $f_{CPU}$  generation mechanism. This must be considered when calculating ST10R272L timing.

The CPU clock generation mechanism is set during reset by the logic levels on pins P0.15-13 (P0H.7-5).

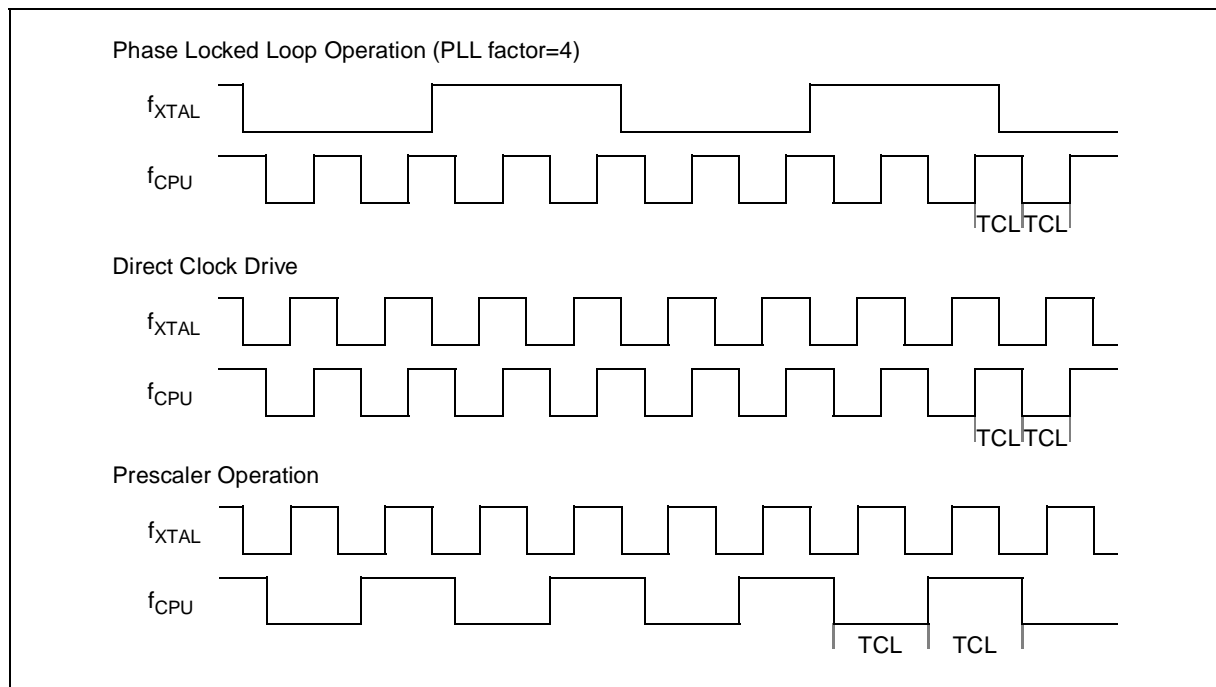


Figure 14 CPU clock generation mechanisms

| P0.15-13 (P0H.7-5) | CPU frequency<br>$f_{CPU} = f_{XTAL} * F$ | External clock<br>input range 10-<br>50MHz | Notes                 |
|--------------------|---|--|-----------------------|
| 1 1 1              | $F_{XTAL} * 4$                            | 2.5 to 12.5 MHz                            | Default configuration |
| 1 1 0              | $F_{XTAL} * 3$                            | 3.33 to 16.66 MHz                          |                       |
| 1 0 1              | $F_{XTAL} * 2$                            | 5 to 25 MHz                                |                       |

Table 15 CPU clock generation mechanisms

## ST10R272L - ELECTRICAL CHARACTERISTICS

| P0.15-13 (P0H.7-5) |   |   | CPU frequency<br>$f_{CPU} = f_{XTAL} * F$ | External clock<br>input range 10-<br>50MHz | Notes                       |
|--------------------|---|---|---|--|-----------------------------|
| 1                  | 0 | 0 | $F_{XTAL} * 5$                            | 2 to 10 MHz                                |                             |
| 0                  | 1 | 1 | $F_{XTAL} * 1$                            | 1 to 50 MHz                                | Direct drive <sup>1)</sup>  |
| 0                  | 1 | 0 | $F_{XTAL} * 1.5$                          | 6.66 to 33.33 MHz                          |                             |
| 0                  | 0 | 1 | $F_{XTAL} / 2$                            | 2 to 100 MHz                               | CPU clock via 2:1 prescaler |
| 0                  | 0 | 0 | $F_{XTAL} * 2.5$                          | 4 to 20 MHz                                |                             |

**Table 15 CPU clock generation mechanisms**

- 1) The maximum depends on the duty cycle of the external clock signal. The maximum input frequency is 25 MHz when using an external crystal oscillator, but higher frequencies can be applied with an external clock source.

### Prescaler operation

Set when pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of  $f_{CPU}$  is half the frequency of  $f_{XTAL}$  and the high and low time of  $f_{CPU}$  (i.e. the duration of an individual TCL) is defined by the period of the input clock  $f_{XTAL}$ .

The timings listed in the AC characteristics that refer to TCLs therefore can be calculated using the period of  $f_{XTAL}$  for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

### Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset, the on-chip phase locked loop is disabled and the CPU clock is driven from the internal oscillator with the input clock signal. The frequency of  $f_{CPU}$  directly follows the frequency of  $f_{XTAL}$  so the high and low time of  $f_{CPU}$  (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock  $f_{XTAL}$ .

The TCL timing below must be calculated using the minimum possible TCL which can be calculated by the formula:  $TCL_{min} = 1/f_{XTAL} \times DC_{min}$  ( $DC$  = duty cycle)

For two consecutive TCLs the deviation caused by the duty cycle of  $f_{XTAL}$  is compensated so the duration of 2TCL is always  $1/f_{XTAL}$ . Therefore, the minimum value  $TCL_{min}$  has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:  $2TCL = 1/f_{XTAL}$ .

## ST10R272L - ELECTRICAL CHARACTERISTICS

*Note* The address float timings in Multiplexed bus mode ( $t_{11}$  and  $t_{45}$ ) use

$$TCL_{max} = 1/f_{XTAL} \times DC_{max} \text{ instead of } TCL_{min}.$$

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

### Oscillator Watchdog (OWD)

When the clock option selected is direct drive or direct drive with prescaler, in order to provide a fail safe mechanism in case of a loss of the external clock, an oscillator watchdog is implemented as an additional functionality of the PLL circuitry. This oscillator watchdog operates as follows:

After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, set bit 4 of SYSCON register OWDDIS.

When the OWD is enabled, the PLL runs on its free-running frequency and increments the Oscillator Watchdog counter. On each transition of the XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exists on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

### Phase locked loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock. The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (i.e.  $f_{CPU} = f_{XTAL} * F$ ). With every F'th transition of  $f_{XTAL}$  the PLL circuit synchronizes the CPU clock to the input clock. In this way,  $f_{CPU}$  is constantly adjusted so it is locked to  $f_{XTAL}$ . The slight variation causes a jitter of  $f_{CPU}$  which affects individual TCL duration. Therefore, AC characteristics that refer to TCLs must be calculated using the minimum possible TCL.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL constantly adjusts its output frequency, it corresponds to the applied input frequency (crystal or oscillator). The relative deviation for periods of more than one TCL is lower than for one single TCL. For a period of  $N * TCL$  the minimum value is computed using the corresponding deviation  $D_N$ :

$$TCL_{min} = TCL_{NOM} \times (1 - |D_N|/100)$$

$$D_N = \pm(4 - N/15)[\%]$$

## ST10R272L - ELECTRICAL CHARACTERISTICS

where  $N$  = number of consecutive TCLs and  $1 \leq N \leq 40$ . So for a period of 3 TCLs (i.e.  $N = 3$ ):

$$\begin{aligned} D_3 &= 4 - 3/15 \\ &= 3,8\% \end{aligned}$$

and

$$\begin{aligned} 3TCL_{min} &= 3TCL_{NOM} \times (1 - 3,8/100) \\ &= 3TCL_{NOM} \times 0,962 (36.07\text{nsec @fcpu=50MHz}) \end{aligned}$$

PLL jitter is an important factor for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

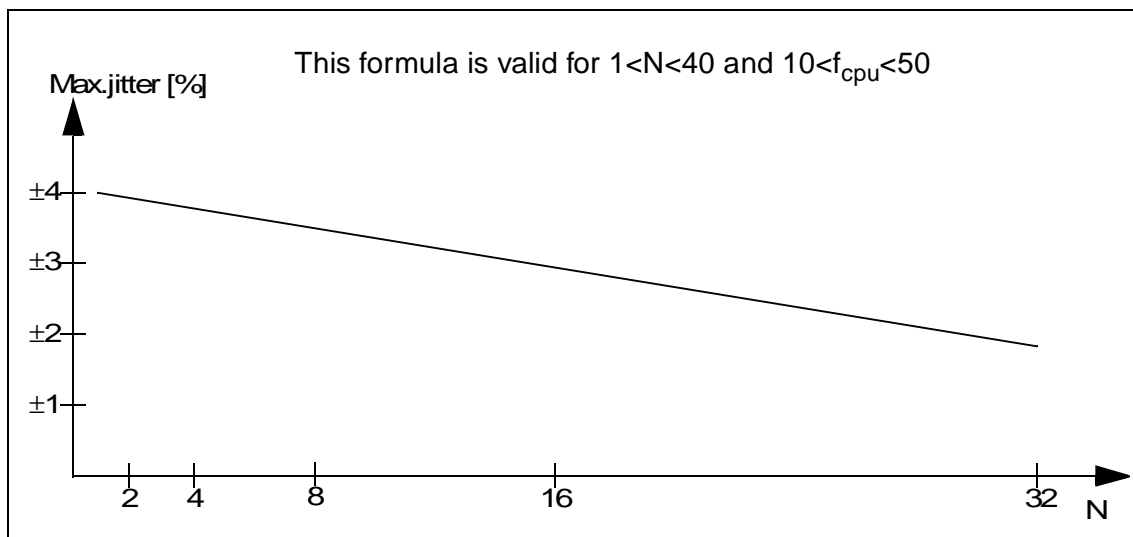


Figure 15 Approximated maximum PLL jitter

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**ST10R272L - ELECTRICAL CHARACTERISTICS**


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**16.3.2 Memory Cycle Variables**

The timing tables below use three variables derived from the BUSCONx registers and represent programmed memory cycle characteristics. Table 16 describes how these variables are computed.

| <b>Description</b>           | <b>Symbol</b> | <b>Values</b>                        |
|------------------------------|---------------|--------------------------------------|
| ALE Extension                | $t_A$         | $TCL * \langle ALECTL \rangle$       |
| Memory Cycle Time Waitstates | $t_C$         | $2TCL * (15 - \langle MCTC \rangle)$ |
| Memory Tristate Time         | $t_F$         | $2TCL * (1 - \langle MTTC \rangle)$  |

**Table 16 Memory cycle variables**

## ST10R272L - ELECTRICAL CHARACTERISTICS

### 16.3.3 Multiplexed Bus

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$      $V_{SS} = 0 \text{ V}$      $T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$      $C_L = 50 \text{ pF}$

ALE cycle time =  $6 \text{ TCL} + 2t_A + t_C + t_F$  (60 ns at 50-MHz CPU clock without waitstates)

| Parameter  | Symbol      | Max. CPU Clock<br>= 50 MHz |                   | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |                                 | Unit |
|--|-------------|----------------------------|-------------------|--|---------------------------------|------|
|  |             | min.                       | max.              | min.                                       | max.                            |      |
| ALE high time  | $t_5$ CC    | $7 + t_A$                  | –                 | $\text{TCL} - 3 + t_A$                     | –                               | ns   |
| Address (P1, P4), $\overline{\text{BHE}}$<br>setup to ALE                              | $t_6$ CC    | $3 + t_A$                  | –                 | $\text{TCL} - 7 + t_A$                     | –                               | ns   |
| Address (P0) setup to ALE  | $t_{6m}$ CC | $5 + t_A$                  | –                 | $\text{TCL} - 5 + t_A$                     | –                               | ns   |
| Address hold after ALE   | $t_7$ CC    | $5 + t_A$                  | –                 | $\text{TCL} - 5 + t_A$                     | –                               | ns   |
| ALE falling edge to $\overline{\text{RD}}$ ,<br>$\overline{\text{WR}}$ (with RW-delay) | $t_8$ CC    | $5 + t_A$                  | –                 | $\text{TCL} - 5 + t_A$                     | –                               | ns   |
| ALE falling edge to $\overline{\text{RD}}$ ,<br>$\overline{\text{WR}}$ (no RW-delay)   | $t_9$ CC    | $-5 + t_A$                 | –                 | $-5 + t_A$                                 | –                               | ns   |
| Address float after $\overline{\text{RD}}$ ,<br>(with RW-delay) <sup>1)</sup>          | $t_{10}$ CC | –                          | $5^1$             | –  | $5^1$                           | ns   |
| Address float after $\overline{\text{RD}}$ ,<br>(no RW-delay) <sup>1)</sup>            | $t_{11}$ CC | –                          | $15^1$            | –  | $\text{TCL} + 5^1$              | ns   |
| $\overline{\text{RD}}$ , $\overline{\text{WR}}$ low time<br>(with RW-delay)            | $t_{12}$ CC | $13 + t_C$                 | –                 | $2\text{TCL} - 7 + t_C$                    | –                               | ns   |
| $\overline{\text{RD}}$ , $\overline{\text{WR}}$ low time<br>(no RW-delay)              | $t_{13}$ CC | $23 + t_C$                 | –                 | $3\text{TCL} - 7 + t_C$                    | –                               | ns   |
| $\overline{\text{RD}}$ to valid data in<br>(with RW-delay)                             | $t_{14}$ SR | –                          | $5 + t_C$         | –  | $2\text{TCL} - 15 + t_C$        | ns   |
| $\overline{\text{RD}}$ to valid data in<br>(no RW-delay)                               | $t_{15}$ SR | –                          | $15 + t_C$        | –  | $3\text{TCL} - 15 + t_C$        | ns   |
| ALE low to valid data in   | $t_{16}$ SR | –                          | $15 + t_A + t_C$  | –  | $3\text{TCL} - 15 + t_A + t_C$  | ns   |
| Address to valid data in   | $t_{17}$ SR | –                          | $20 + 2t_A + t_C$ | –  | $4\text{TCL} - 20 + 2t_A + t_C$ | ns   |

Table 17 Multiplexed bus

## ST10R272L - ELECTRICAL CHARACTERISTICS

| Parameter   | Symbol              | Max. CPU Clock<br>= 50 MHz |                   | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |                          | Unit |
|---|---------------------|----------------------------|-------------------|--|--------------------------|------|
|   |                     | min.                       | max.              | min.                                       | max.                     |      |
| Data hold after $\overline{RD}$ rising edge                             | t <sub>18</sub> SR  | 0                          | –                 | 0  | –                        | ns   |
| Data float after $\overline{RD}$ rising edge <sup>12)</sup>             | t <sub>19</sub> SR  | –                          | $15 + t_F^2$      | –  | $2TCL - 5 + t_F^2$       | ns   |
| Data valid to $\overline{WR}$   | t <sub>22</sub> CC  | $13 + t_C$                 | –                 | $2TCL - 7 + t_C$                           | –                        | ns   |
| Data hold after $\overline{WR}$   | t <sub>23</sub> CC  | $13 + t_F$                 | –                 | $2TCL - 7 + t_F$                           | –                        | ns   |
| ALE rising edge after $\overline{RD}$ , $\overline{WR}$                 | t <sub>25</sub> CC  | $10 + t_F$                 | –                 | $2TCL - 10 + t_F$                          | –                        | ns   |
| Address hold after $\overline{RD}$ , $\overline{WR}$                    | t <sub>27</sub> CC  | $10 + t_F$                 | –                 | $2TCL - 10 + t_F$                          | –                        | ns   |
| Latched $\overline{CS}$ setup to ALE                                    | t <sub>38</sub> CC  | $-7 + t_A$                 | $3 + t_A$         | $-7 + t_A$                                 | $3 + t_A$                | ns   |
| Unlatched $\overline{CS}$ setup to ALE                                  | t <sub>38u</sub> CC | $3 + t_A$                  | –                 | $TCL - 7 + t_A$                            | –                        | ns   |
| Latched $\overline{CS}$ low to Valid Data In                            | t <sub>39</sub> SR  | –                          | $13 + t_C + 2t_A$ | –  | $3TCL - 17 + t_C + 2t_A$ | ns   |
| Unlatched $\overline{CS}$ low to Valid Data In                          | t <sub>39u</sub> SR | –                          | $23 + t_C + 2t_A$ | –  | $4TCL - 17 + t_C + 2t_A$ | ns   |
| Latched $\overline{CS}$ hold after $\overline{RD}$ , $\overline{WR}$    | t <sub>40</sub> CC  | $20 + t_F$                 | –                 | $3TCL - 10 + t_F$                          | –                        | ns   |
| Unlatched $\overline{CS}$ hold after $\overline{RD}$ , $\overline{WR}$  | t <sub>40u</sub> CC | $10 + t_F$                 | –                 | $2TCL - 10 + t_F$                          | –                        | ns   |
| ALE fall. edge to $\overline{RdCS}$ , $\overline{WrCS}$ (with RW delay) | t <sub>42</sub> CC  | $7 + t_A$                  | –                 | $TCL - 3 + t_A$                            | –                        | ns   |
| ALE fall. edge to $\overline{RdCS}$ , $\overline{WrCS}$ (no RW delay)   | t <sub>43</sub> CC  | $-3 + t_A$                 | –                 | $-3 + t_A$                                 | –                        | ns   |
| Address float after $\overline{RdCS}$ (with RW delay) <sup>1</sup>      | t <sub>44</sub> CC  | –                          | $3^1$             | –  | $3^1$                    | ns   |
| Address float after $\overline{RdCS}$ (no RW delay) <sup>1</sup>        | t <sub>45</sub> CC  | –                          | $13^1$            | –  | $TCL + 3^1$              | ns   |

Table 17 Multiplexed bus

## ST10R272L - ELECTRICAL CHARACTERISTICS

| Parameter   | Symbol             | Max. CPU Clock<br>= 50 MHz |                                  | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |  | Unit |
|---|--------------------|----------------------------|----------------------------------|--|--|------|
|   |                    | min.                       | max.                             | min.                                       | max.                                   |      |
| $\overline{\text{RdCS}}$ to Valid Data In<br>(with RW delay)                    | t <sub>46</sub> SR | –                          | 3 + t <sub>C</sub>               | –  | 2TCL - 17<br>+ t <sub>C</sub>          | ns   |
| $\overline{\text{RdCS}}$ to Valid Data In<br>(no RW delay)                      | t <sub>47</sub> SR | –                          | 13 + t <sub>C</sub>              | –  | 3TCL - 17<br>+ t <sub>C</sub>          | ns   |
| $\overline{\text{RdCS}}$ , $\overline{\text{WrCS}}$ Low Time<br>(with RW delay) | t <sub>48</sub> CC | 13 + t <sub>C</sub>        | –                                | 2TCL - 7 + t <sub>C</sub>                  | –                                      | ns   |
| $\overline{\text{RdCS}}$ , $\overline{\text{WrCS}}$ Low Time<br>(no RW delay)   | t <sub>49</sub> CC | 23 + t <sub>C</sub>        | –                                | 3TCL - 7 + t <sub>C</sub>                  | –                                      | ns   |
| Data valid to $\overline{\text{WrCS}}$  | t <sub>50</sub> CC | 10 + t <sub>C</sub>        | –                                | 2TCL - 10 + t <sub>C</sub>                 | –                                      | ns   |
| Data hold after $\overline{\text{RdCS}}$  | t <sub>51</sub> SR | 0                          | –                                | 0  | –                                      | ns   |
| Data float after $\overline{\text{RdCS}}$ <sup>1 2</sup>                        | t <sub>52</sub> SR | –                          | 13 + t <sub>F</sub> <sup>2</sup> | –  | 2TCL - 7 + t <sub>F</sub> <sup>2</sup> | ns   |
| Address hold after<br>$\overline{\text{RdCS}}$ , $\overline{\text{WrCS}}$       | t <sub>54</sub> CC | 10 + t <sub>F</sub>        | –                                | 2TCL - 10 + t <sub>F</sub>                 | –                                      | ns   |
| Data hold after $\overline{\text{WrCS}}$  | t <sub>56</sub> CC | 10 + t <sub>F</sub>        | –                                | 2TCL - 10 + t <sub>F</sub>                 | –                                      | ns   |

Table 17 Multiplexed bus

- 1) Output loading is specified using Figure 13 (CL = 5 pF).
- 2) This delay assumes that the following bus cycle is a multiplexed bus cycle. If next bus cycle is demultiplexed, refer to demultiplexed equivalent AC timing.

## ST10R272L - ELECTRICAL CHARACTERISTICS

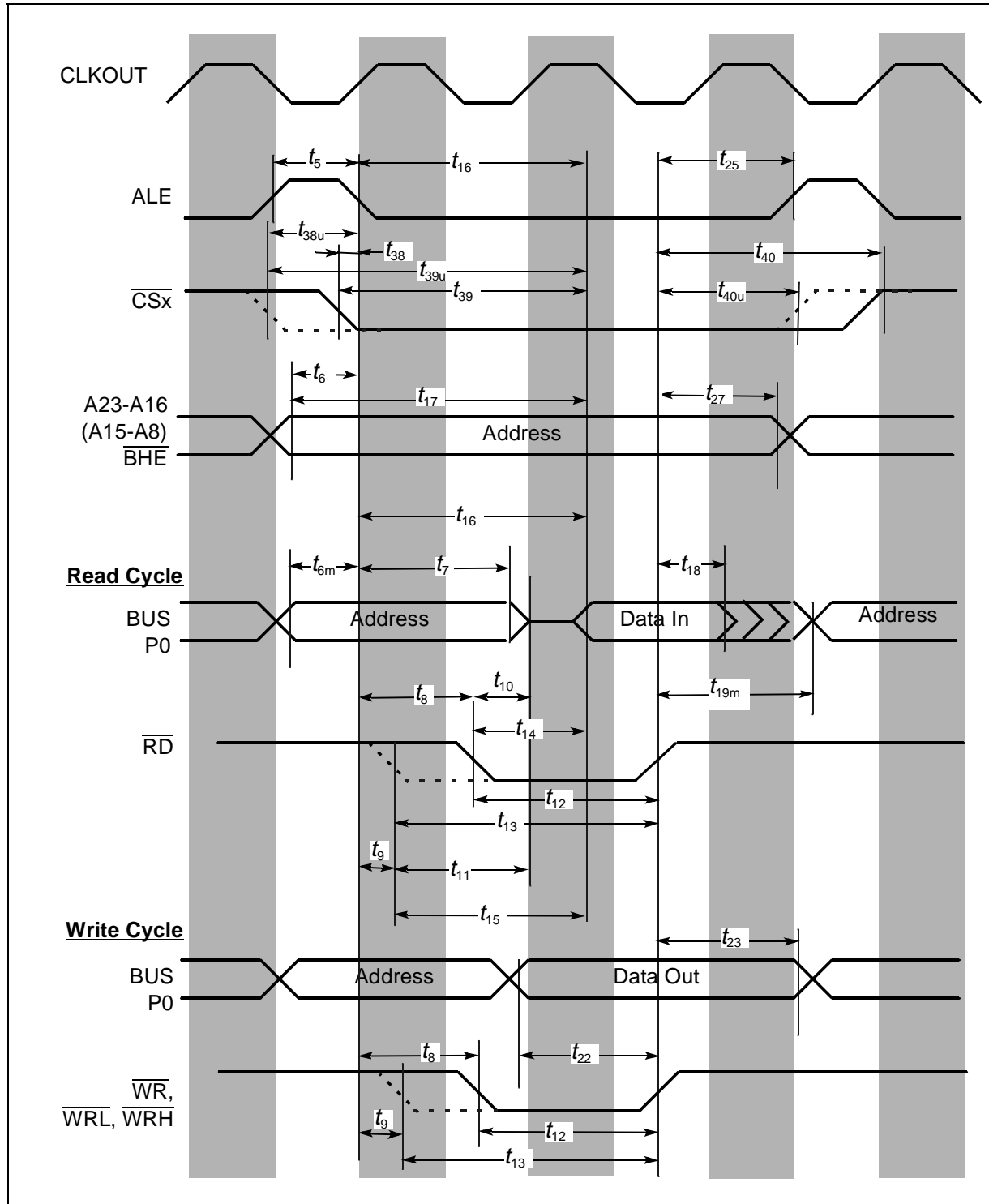
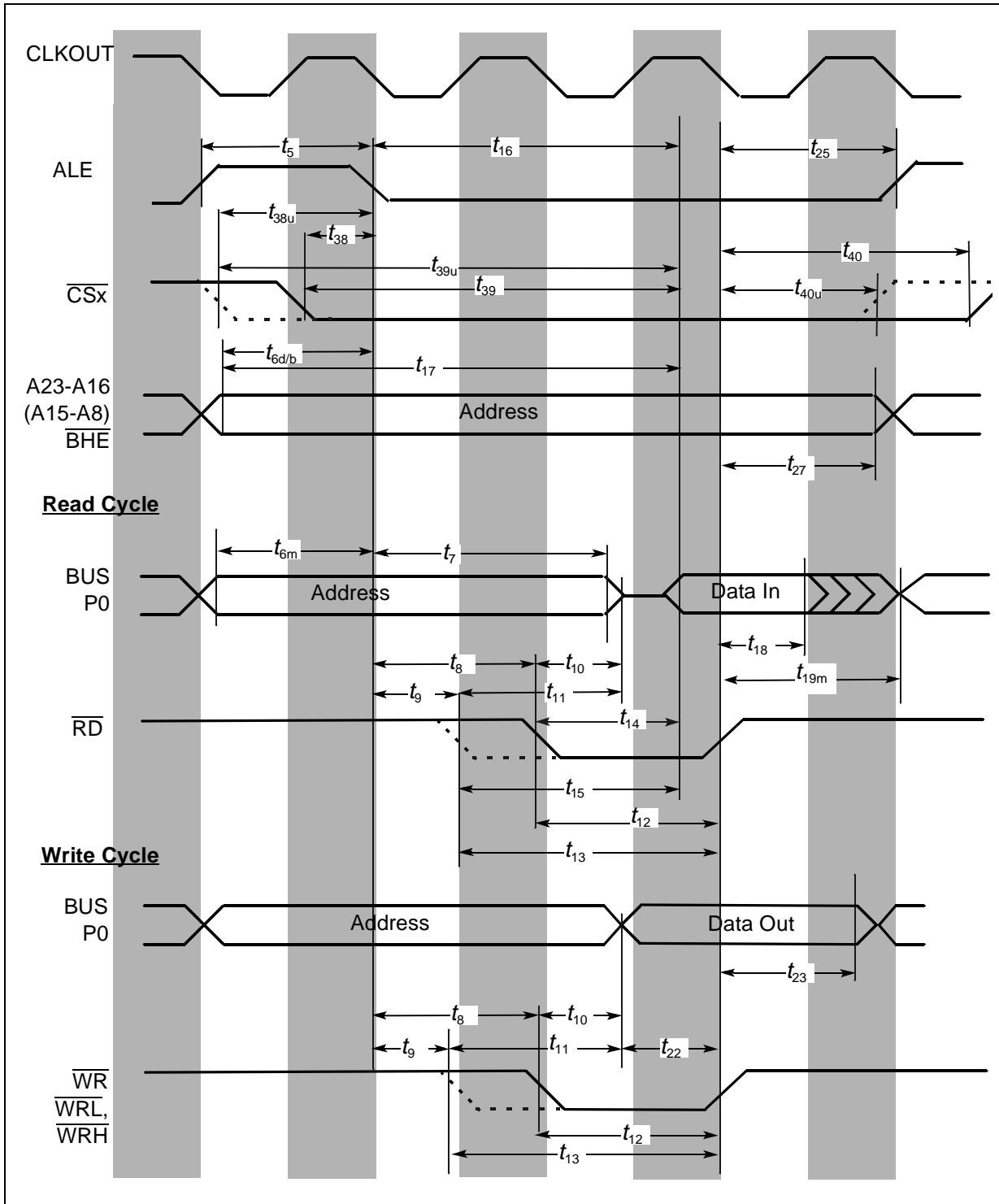


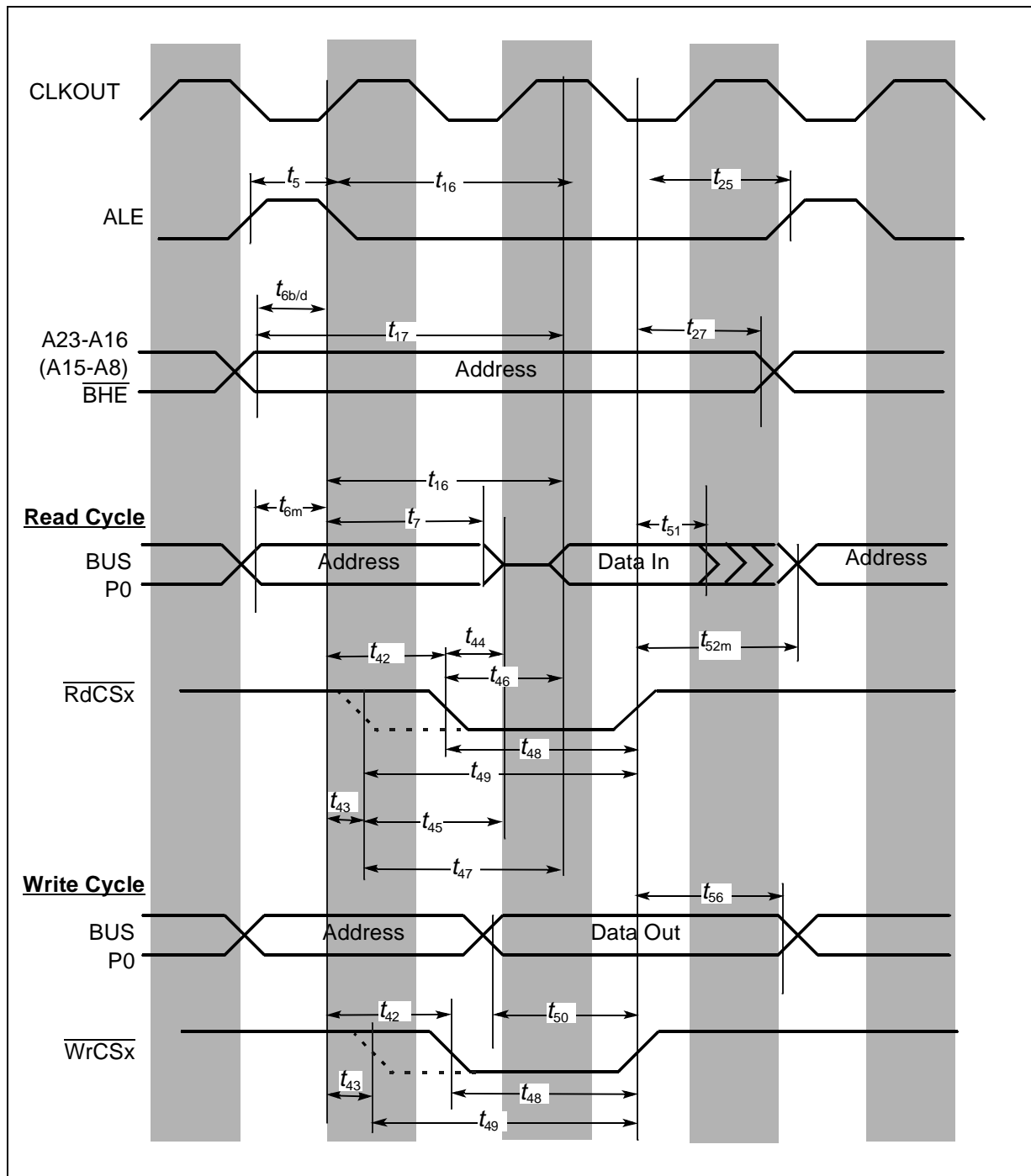
Figure 16 External memory cycle:  
multiplexed bus, with/without read/write delay, normal ALE

**ST10R272L - ELECTRICAL CHARACTERISTICS**



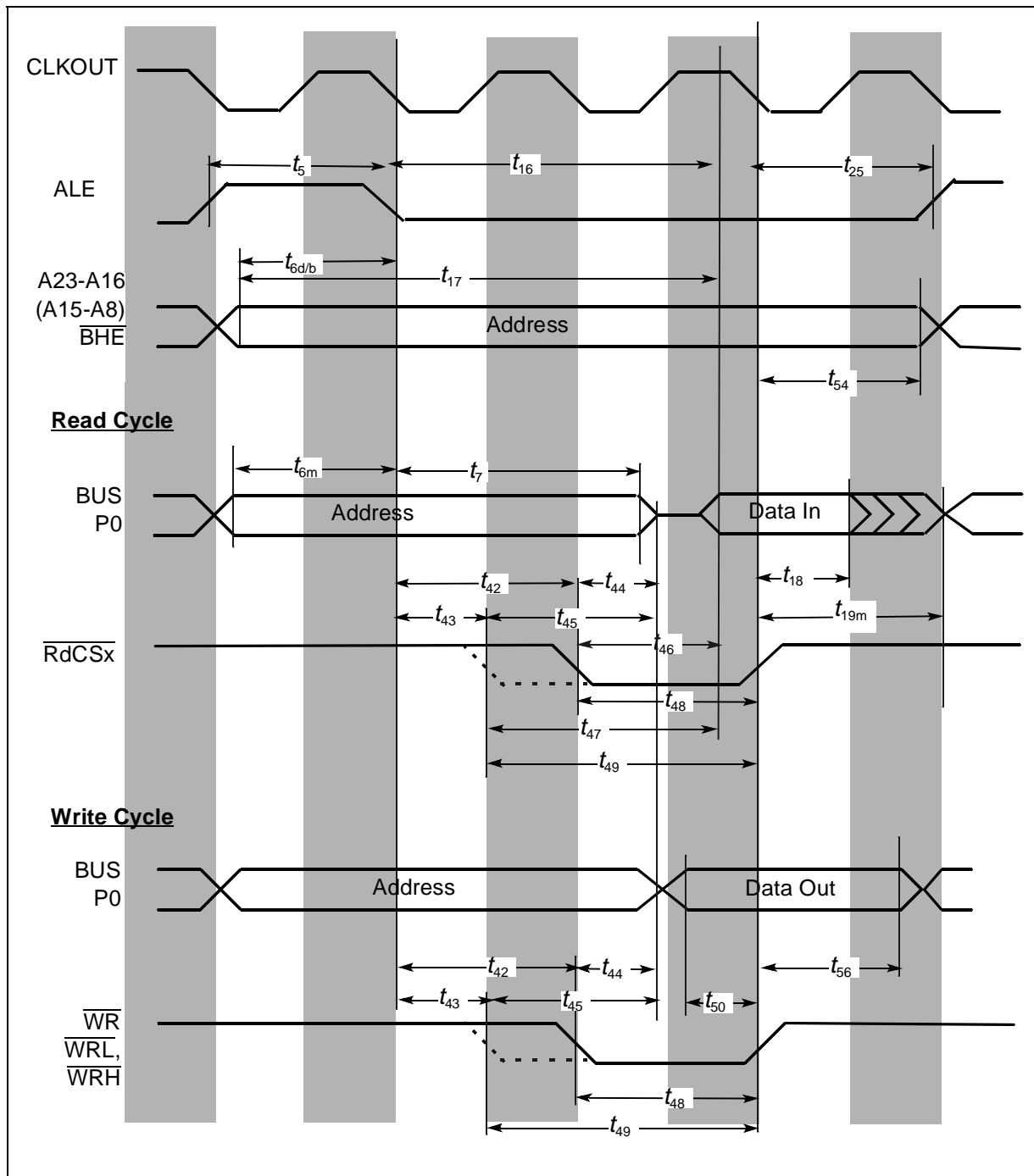
**Figure 17 External memory cycle:  
multiplexed bus, with/without read/write delay, extended ALE**

## ST10R272L - ELECTRICAL CHARACTERISTICS



**Figure 18 External memory cycle:**  
multiplexed bus, with/without read/write delay, normal ALE, read/write chip select

**ST10R272L - ELECTRICAL CHARACTERISTICS**



**Figure 19 External memory cycle: multiplexed bus, with/without read/write delay, extended ale, read/write chip select**

## ST10R272L - ELECTRICAL CHARACTERISTICS

## 16.3.4 Demultiplexed Bus

 $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$      $V_{SS} = 0\text{ V}$      $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$      $C_L = 50\text{ pF}$ 

 ALE cycle time =  $4\text{ TCL} + 2t_A + t_C + t_F$  (40 ns at 50 MHz CPU clock without waitstates)

| Parameter  | Symbol      | Max CPU Clock 50MHz |                     | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |                                  | Unit |
|--|-------------|---------------------|---------------------|--|----------------------------------|------|
|  |             | min.                | max.                | min.                                       | max.                             |      |
| ALE high time  | $t_5$ CC    | $7 + t_A$           | –                   | $\text{TCL} - 3 + t_A$                     | –                                | ns   |
| Address (P1, P4), $\overline{\text{BHE}}$ setup to ALE                               | $t_6$ CC    | $3 + t_A$           | –                   | $\text{TCL} - 7 + t_A$                     | –                                | ns   |
| Address setup to $\overline{\text{RD}}$ , $\overline{\text{WR}}$ (with RW-delay)     | $t_{80}$ CC | $13 + 2t_A$         | –                   | $2\text{TCL} - 7 + 2t_A$                   | –                                | ns   |
| Address setup to $\overline{\text{RD}}$ , $\overline{\text{WR}}$ (no RW-delay)       | $t_{81}$ CC | $3 + 2t_A$          | –                   | $\text{TCL} - 7 + 2t_A$                    | –                                | ns   |
| $\overline{\text{RD}}$ , $\overline{\text{WR}}$ low time (with RW-delay)             | $t_{12}$ CC | $13 + t_C$          | –                   | $2\text{TCL} - 7 + t_C$                    | –                                | ns   |
| $\overline{\text{RD}}$ , $\overline{\text{WR}}$ low time (no RW-delay)               | $t_{13}$ CC | $23 + t_C$          | –                   | $3\text{TCL} - 7 + t_C$                    | –                                | ns   |
| $\overline{\text{RD}}$ to valid data in (with RW-delay)                              | $t_{14}$ SR | –                   | $5 + t_C$           | –  | $2\text{TCL} - 15 + t_C$         | ns   |
| $\overline{\text{RD}}$ to valid data in (no RW-delay)                                | $t_{15}$ SR | –                   | $15 + t_C$          | –  | $3\text{TCL} - 15 + t_C$         | ns   |
| ALE low to valid data in   | $t_{16}$ SR | –                   | $15 + t_A + t_C$    | –  | $3\text{TCL} - 15 + t_A + t_C$   | ns   |
| Address to valid data in   | $t_{17}$ SR | –                   | $20 + 2t_A + t_C$   | –  | $4\text{TCL} - 20 + 2t_A + t_C$  | ns   |
| Data hold after $\overline{\text{RD}}$ rising edge                                   | $t_{18}$ SR | 0                   | –                   | 0  | –                                | ns   |
| Data float after $\overline{\text{RD}}$ rising edge (with RW-delay) <sup>1) 2)</sup> | $t_{20}$ SR | –                   | $15 + t_F + 2t_A^2$ | –  | $2\text{TCL} - 5 + t_F + 2t_A^2$ | ns   |
| Data float after $\overline{\text{RD}}$ rising edge (no RW-delay) <sup>1) 2)</sup>   | $t_{21}$ SR | –                   | $5 + t_F + 2t_A^2$  | –  | $\text{TCL} - 5 + t_F + 2t_A^2$  | ns   |
| Data valid to $\overline{\text{WR}}$   | $t_{22}$ CC | $13 + t_C$          | –                   | $2\text{TCL} - 7 + t_C$                    | –                                | ns   |

Table 18 Demultiplexed bus

## ST10R272L - ELECTRICAL CHARACTERISTICS

| Parameter   | Symbol              | Max CPU Clock 50MHz  |  | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz                         |   | Unit |
|---|---------------------|--|--|--|---|------|
|   |                     | min.   | max.                                     | min.   | max.  |      |
| Data hold after $\overline{WR}$   | t <sub>24</sub> CC  | 5 + t <sub>F</sub>   | –  | TCL - 5 + t <sub>F</sub>   | –   | ns   |
| ALE rising edge after $\overline{RD}$ ,<br>$\overline{WR}$                | t <sub>26</sub> CC  | -5 + t <sub>F</sub>  | –  | -5 + t <sub>F</sub>  | –   | ns   |
| Address hold after $\overline{RD}$ , $\overline{WR}$                      | t <sub>28</sub> CC  | 0 (no t <sub>F</sub> )<br>-9 + t <sub>F</sub> (t <sub>F</sub> >0)  | –  | 0 (no t <sub>F</sub> )<br>-9 + t <sub>F</sub> (t <sub>F</sub> >0)  | –   | ns   |
| Address hold after $\overline{WRH}$                                       | t <sub>28h</sub> CC | -1 (no t <sub>F</sub> )<br>-8 + t <sub>F</sub> (t <sub>F</sub> >0) | –  | -1 (no t <sub>F</sub> )<br>-8 + t <sub>F</sub> (t <sub>F</sub> >0) | –   | ns   |
| Latched $\overline{CS}$ setup to ALE                                      | t <sub>38</sub> CC  | -7 + t <sub>A</sub>  | 3 + t <sub>A</sub>                       | -7 + t <sub>A</sub>  | 3 + t <sub>A</sub>                              | ns   |
| Unlatched $\overline{CS}$ setup to ALE                                    | t <sub>38u</sub> CC | 3 + t <sub>A</sub>   | –  | TCL - 7 + t <sub>A</sub>   | –   | ns   |
| Latched $\overline{CS}$ low to Valid<br>Data In                           | t <sub>39</sub> SR  | –  | 13<br>+ t <sub>C</sub> + 2t <sub>A</sub> | –  | 3TCL - 17<br>+ t <sub>C</sub> + 2t <sub>A</sub> | ns   |
| Unlatched $\overline{CS}$ low to Valid<br>Data In                         | t <sub>39u</sub> SR | –  | 23<br>+ t <sub>C</sub> + 2t <sub>A</sub> | –  | 4TCL - 17<br>+ t <sub>C</sub> + 2t <sub>A</sub> | ns   |
| Latched $\overline{CS}$ hold after $\overline{RD}$ ,<br>$\overline{WR}$   | t <sub>41</sub> CC  | 3 + t <sub>F</sub>   | –  | TCL - 7 + t <sub>F</sub>   | –   | ns   |
| Unlatched $\overline{CS}$ hold after $\overline{RD}$ ,<br>$\overline{WR}$ | t <sub>41u</sub> CC | 0 (no t <sub>F</sub> )<br>-7 + t <sub>F</sub> (t <sub>F</sub> >0)  | –  | 0 (no t <sub>F</sub> )<br>-7 + t <sub>F</sub> (t <sub>F</sub> >0)  | –   | ns   |
| Address setup to $\overline{RdCs}$ ,<br>$\overline{WrCs}$ (with RW-delay) | t <sub>82</sub> CC  | 13 + 2t <sub>A</sub>   | –  | 2TCL - 7 + 2t <sub>A</sub>   | –   | ns   |
| Address setup to $\overline{RdCs}$ ,<br>$\overline{WrCs}$ (no RW-delay)   | t <sub>83</sub> CC  | 3 + 2t <sub>A</sub>  | –  | TCL - 7 + 2t <sub>A</sub>  | –   | ns   |
| $\overline{RdCS}$ to Valid Data In<br>(with RW-delay)                     | t <sub>46</sub> SR  | –  | 3 + t <sub>C</sub>                       | –  | 2TCL - 17 + t <sub>C</sub>                      | ns   |
| $\overline{RdCS}$ to Valid Data In<br>(no RW-delay)                       | t <sub>47</sub> SR  | –  | 13 + t <sub>C</sub>                      | –  | 3TCL - 17 + t <sub>C</sub>                      | ns   |
| $\overline{RdCS}$ , $\overline{WrCS}$ Low Time<br>(with RW-delay)         | t <sub>48</sub> CC  | 11 + t <sub>C</sub>  | –  | 2TCL - 9 + t <sub>C</sub>  | –   | ns   |
| $\overline{RdCS}$ , $\overline{WrCS}$ Low Time<br>(no RW-delay)           | t <sub>49</sub> CC  | 21 + t <sub>C</sub>  | –  | 3TCL - 9 + t <sub>C</sub>  | –   | ns   |
| Data valid to $\overline{WrCS}$   | t <sub>50</sub> CC  | 13 + t <sub>C</sub>  | –  | 2TCL - 7 + t <sub>C</sub>  | –   | ns   |

Table 18 Demultiplexed bus

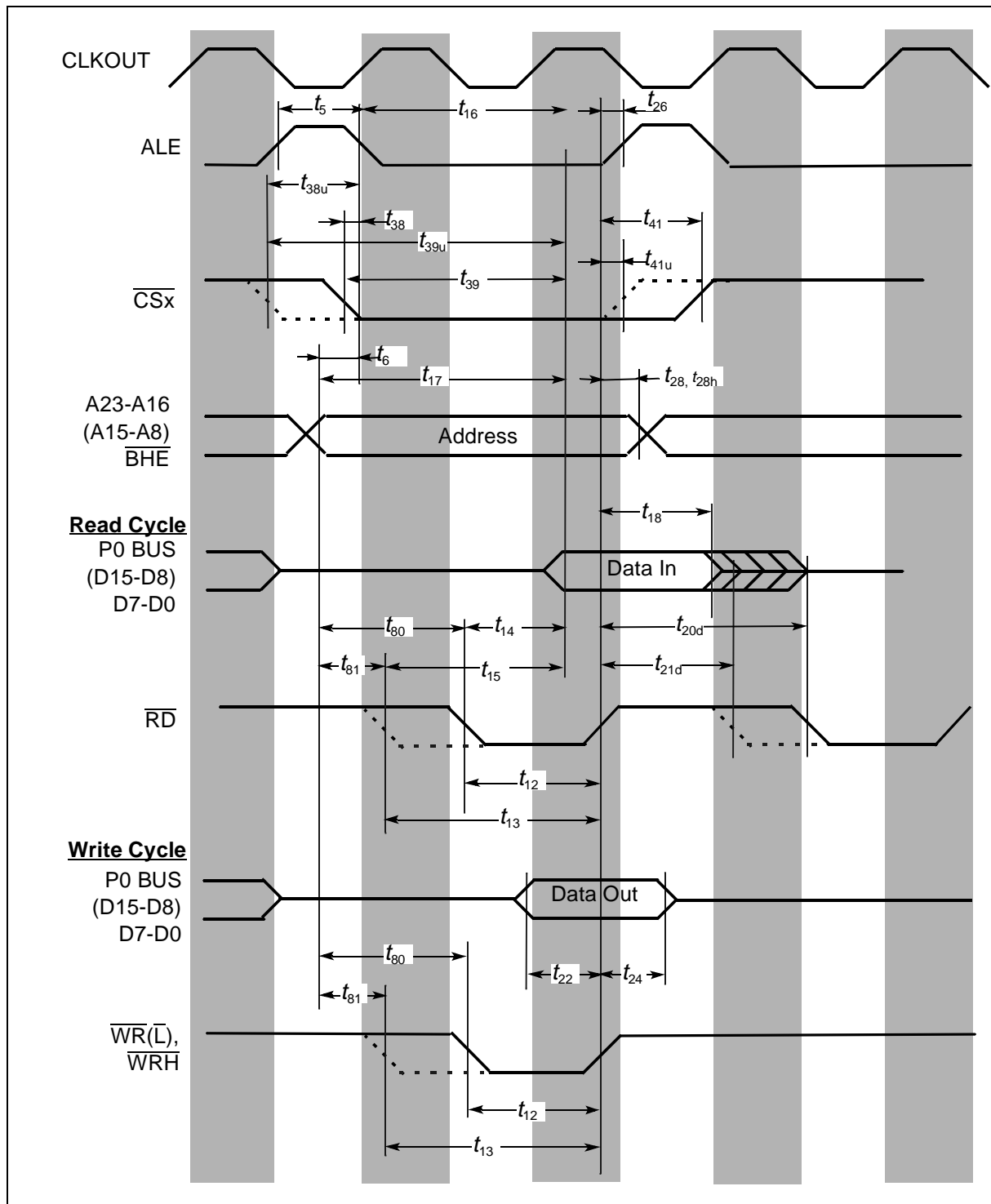
## ST10R272L - ELECTRICAL CHARACTERISTICS

| Parameter   | Symbol             | Max CPU Clock 50MHz |                     | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |                                  | Unit |
|---|--------------------|---------------------|---------------------|--|----------------------------------|------|
|   |                    | min.                | max.                | min.                                       | max.                             |      |
| Data hold after $\overline{\text{RdCS}}$                                    | t <sub>51</sub> SR | 0                   | –                   | 0  | –                                | ns   |
| Data float after $\overline{\text{RdCS}}$<br>(with RW-delay) <sup>1 2</sup> | t <sub>53</sub> SR | –                   | $13 + t_F + 2t_A^2$ | –  | $2\text{TCL} - 7 + t_F + 2t_A^2$ | ns   |
| Data float after $\overline{\text{RdCS}}$<br>(no RW-delay) <sup>1 2</sup>   | t <sub>68</sub> SR | –                   | $3 + t_F + 2t_A^2$  | –  | $\text{TCL} - 7 + t_F + 2t_A^2$  | ns   |
| Address hold after<br>$\overline{\text{RdCS}}$ , $\overline{\text{WrCS}}$   | t <sub>55</sub> CC | $-5 + t_F$          | –                   | $-5 + t_F$                                 | –                                | ns   |
| Data hold after $\overline{\text{WrCS}}$                                    | t <sub>57</sub> CC | $3 + t_F$           | –                   | $\text{TCL} - 7 + t_F$                     | –                                | ns   |

Table 18 Demultiplexed bus

- 1) Output loading is specified using Figure 13 with CL = 5 pF.
- 2) This delay assumes that the following bus cycle is a demultiplexed bus cycle and that the data bus will only be driven externally when the  $\overline{\text{RD}}$  or  $\overline{\text{RdCS}}$  signal becomes active. RW-delay and t<sub>A</sub> refer to the following bus cycle. If the following bus cycle is a multiplexed bus cycle, refer to equivalent multiplexed AC timing (which are still applicable due to automatic insertion an idle state (2TCL) when switching from Demultiplexed to Multiplexed Bus Mode.

**ST10R272L - ELECTRICAL CHARACTERISTICS**



**Figure 20 External memory cycle:  
demultiplexed bus, with/without read/write delay, normal ALE**

ST10R272L - ELECTRICAL CHARACTERISTICS

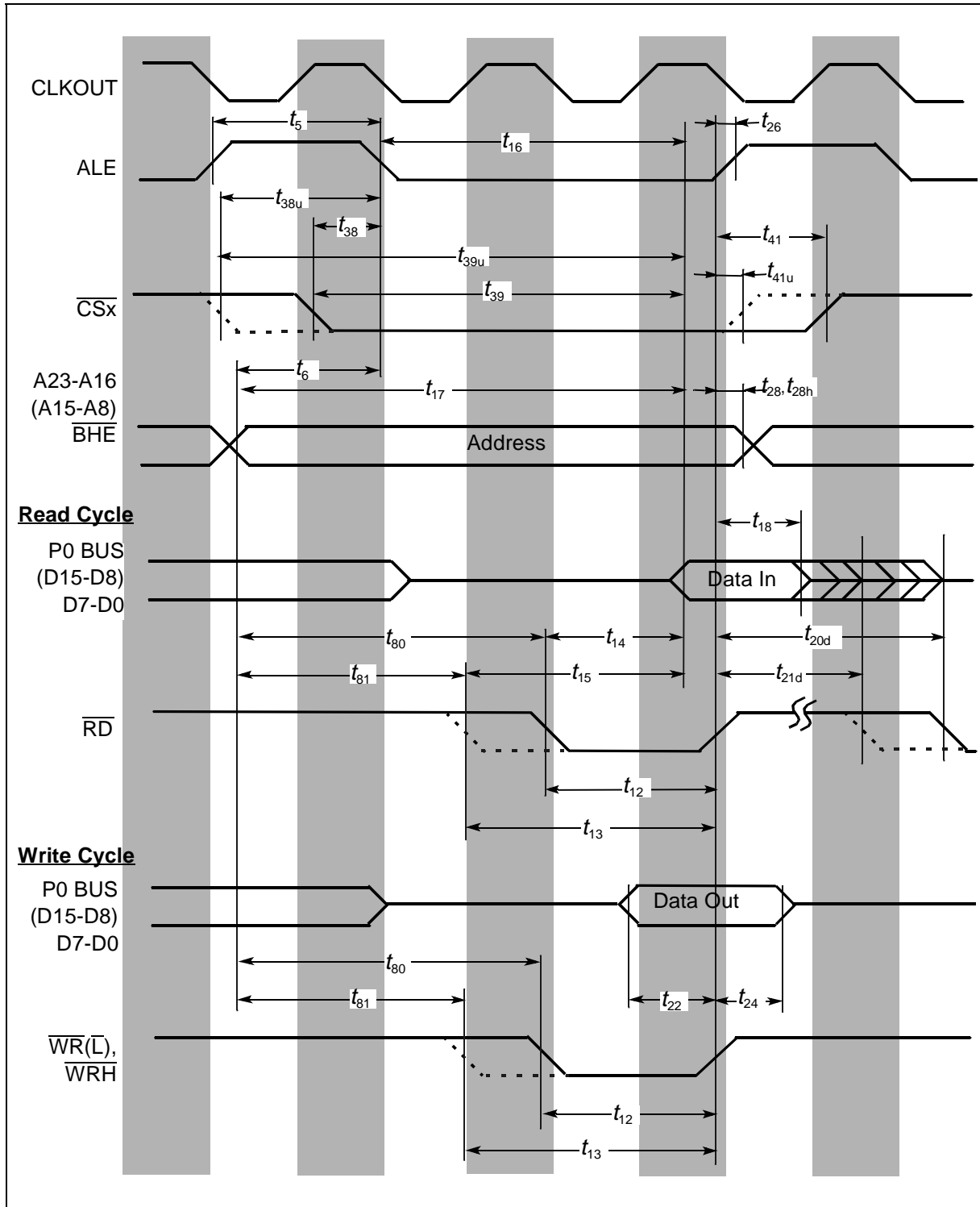


Figure 21 External memory cycle:  
demultiplexed bus, with/without read/write delay, extended ALE

## ST10R272L - ELECTRICAL CHARACTERISTICS

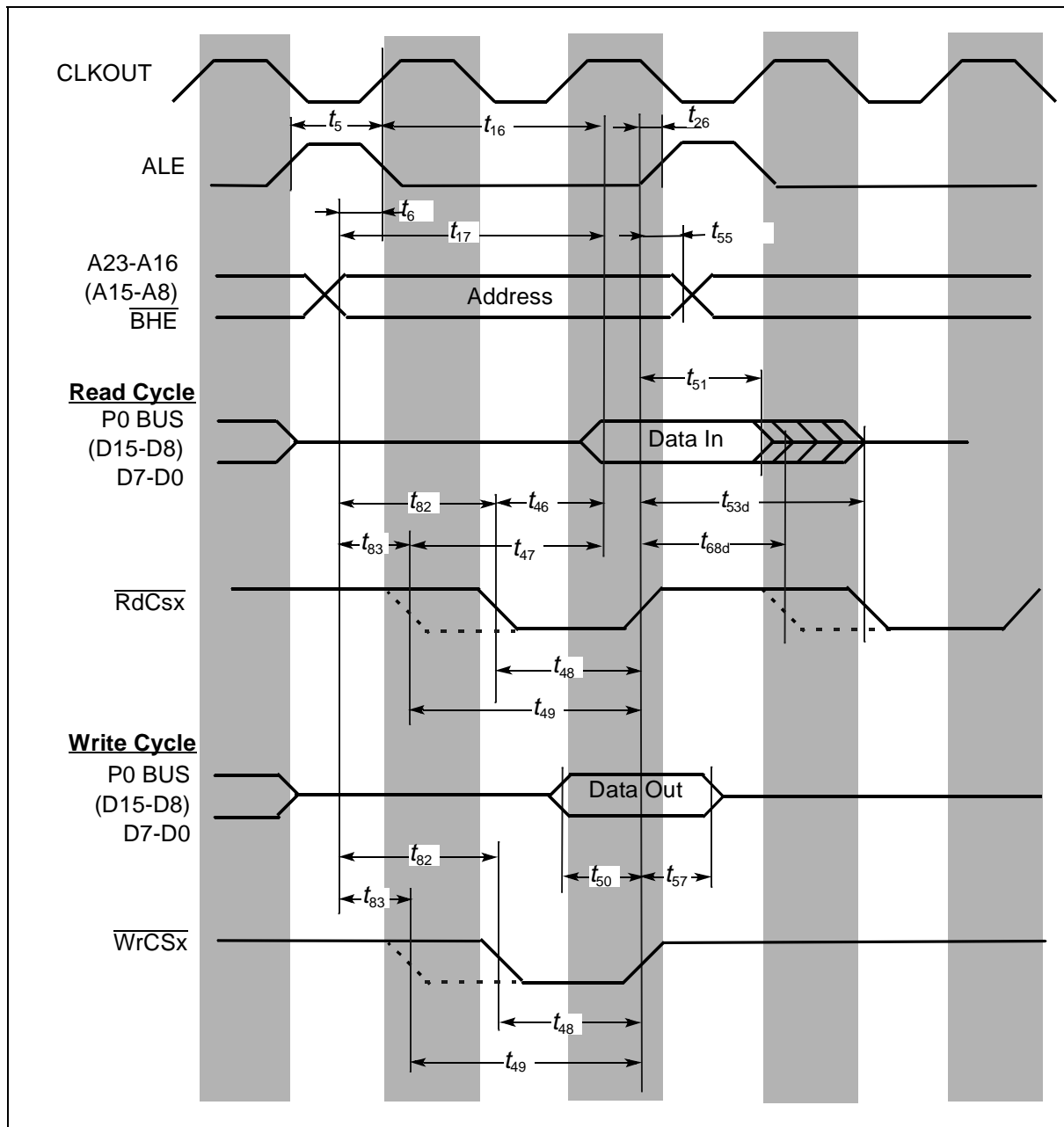
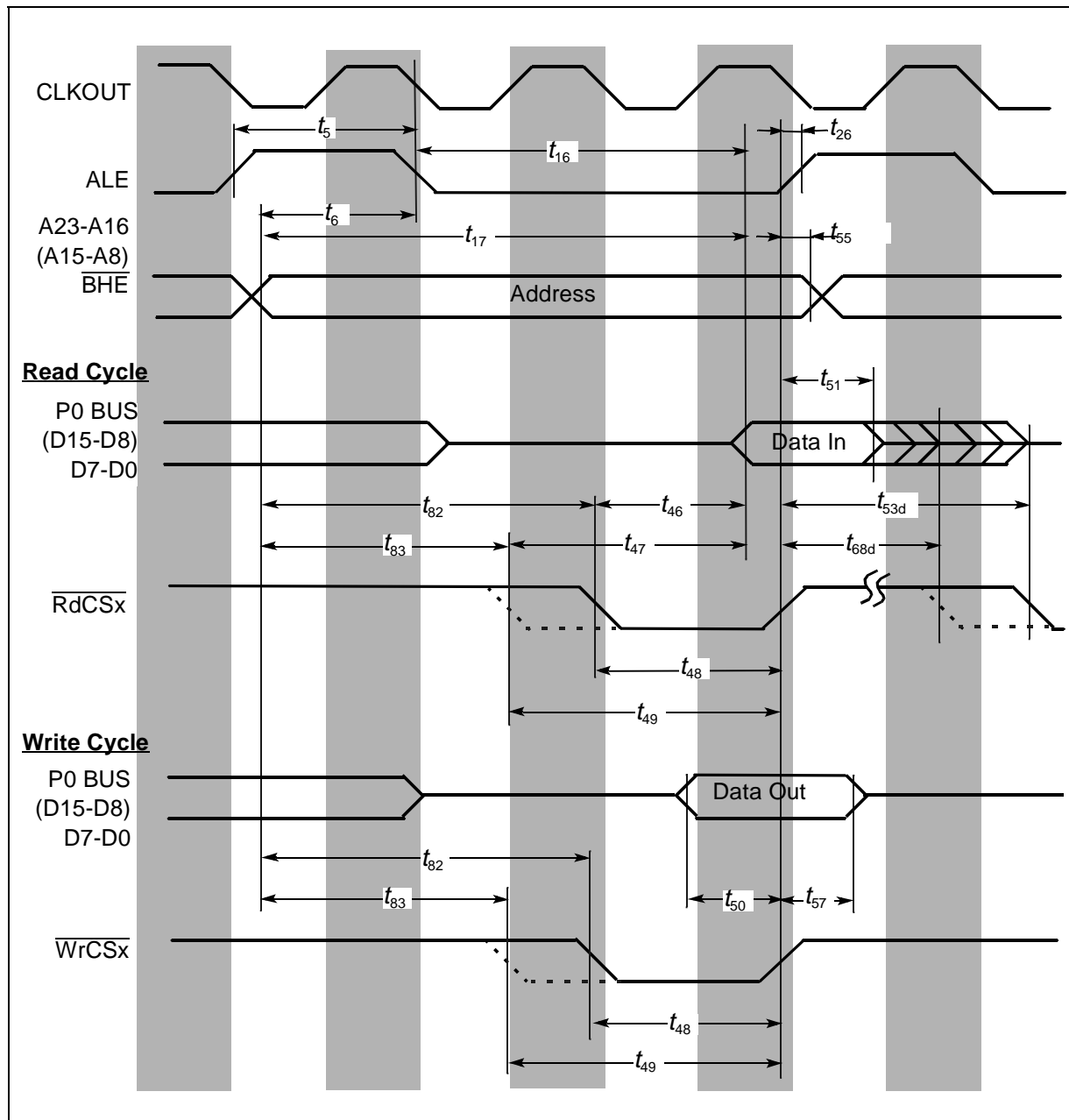


Figure 22 External memory cycle:  
demultiplexed bus, with/without read/write delay, normal ALE, read/write chip select

## ST10R272L - ELECTRICAL CHARACTERISTICS



**Figure 23 External memory cycle:**  
demultiplexed bus, no read/write delay, extended ALE, read/write chip select

**ST10R272L - ELECTRICAL CHARACTERISTICS****16.3.5 CLKOUT and  $\overline{\text{READY}}/\text{READY}$** 

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$

$V_{SS} = 0 \text{ V}$

$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$

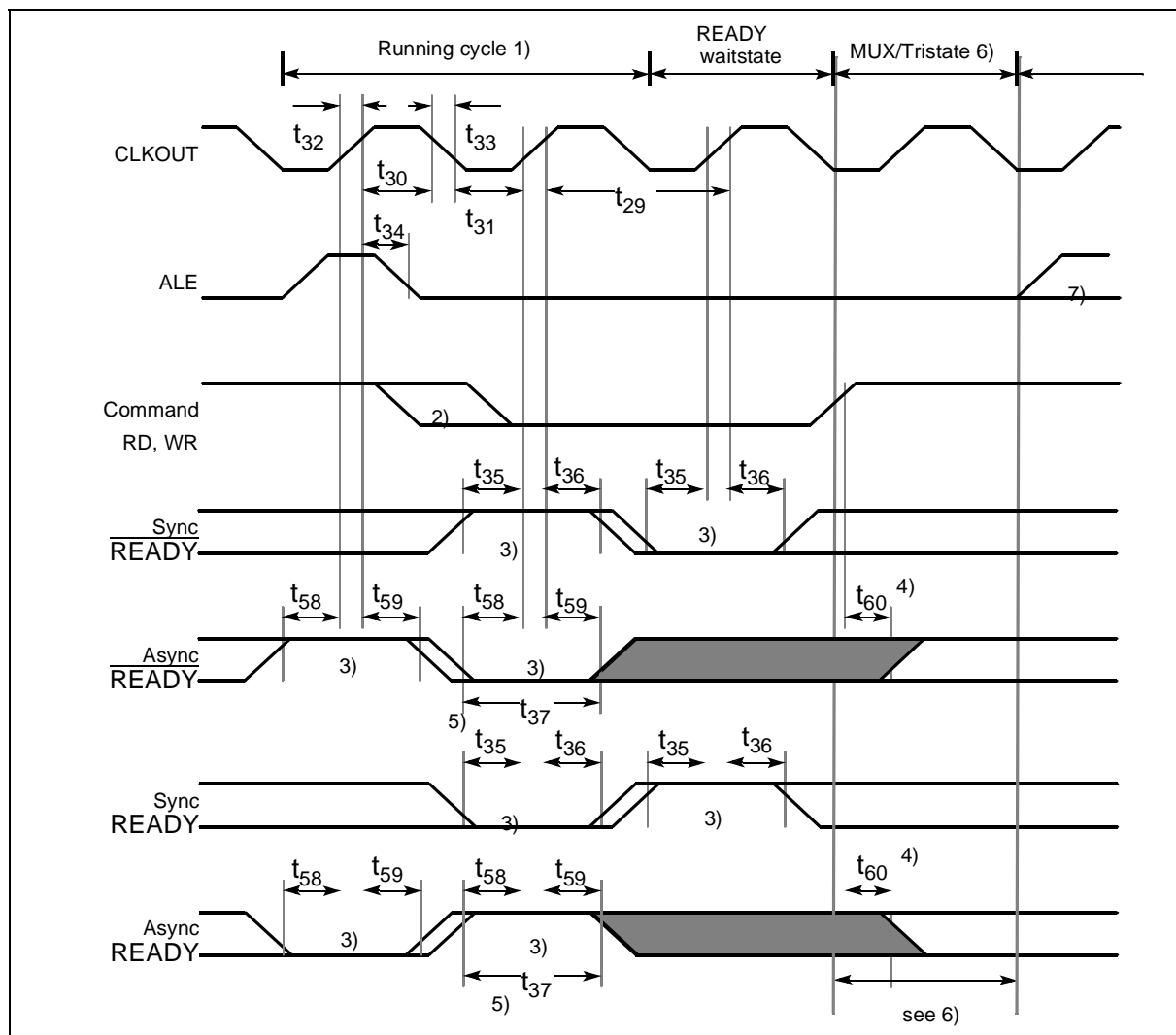
$C_L = 50 \text{ pF}$

| Parameter  | Symbol             | Max. CPU Clock<br>= 50 MHz |   | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |  | Unit |
|--|--------------------|----------------------------|---|--|--|------|
|  |                    | min.                       | max.  | min.                                       | max.   |      |
| CLKOUT cycle time  | t <sub>29</sub> CC | 20                         | 20  | 2TCL                                       | 2TCL   | ns   |
| CLKOUT high time   | t <sub>30</sub> CC | 5                          | –   | TCL – 5                                    | –  | ns   |
| CLKOUT low time  | t <sub>31</sub> CC | 5                          | –   | TCL – 5                                    | –  | ns   |
| CLKOUT rise time <sup>1)</sup>   | t <sub>32</sub> CC | –                          | 3 <sup>1</sup>  | –  | 3 <sup>1</sup>   | ns   |
| CLKOUT fall time <sup>1</sup>  | t <sub>33</sub> CC | –                          | 3 <sup>1</sup>  | –  | 3 <sup>1</sup>   | ns   |
| CLKOUT rising edge to<br>ALE falling edge  | t <sub>34</sub> CC | -3 + t <sub>A</sub>        | 5 + t <sub>A</sub>  | -3 + t <sub>A</sub>                        | 5 + t <sub>A</sub>   | ns   |
| Synchronous $\overline{\text{READY}}$<br>setup time to CLKOUT  | t <sub>35</sub> SR | 9                          | –   | 9  | –  | ns   |
| Synchronous $\overline{\text{READY}}$<br>hold time after CLKOUT  | t <sub>36</sub> SR | 0                          | –   | 0  | –  | ns   |
| Asynchronous $\overline{\text{READY}}$<br>low time   | t <sub>37</sub> SR | 27                         | –   | 2TCL + 7                                   | –  | ns   |
| Asynchronous $\overline{\text{READY}}$<br>setup time <sup>2)</sup>   | t <sub>58</sub> SR | 9                          | –   | 9  | –  | ns   |
| Asynchronous $\overline{\text{READY}}$<br>hold time <sup>2)</sup>  | t <sub>59</sub> SR | 0                          | –   | 0  | –  | ns   |
| Async. $\overline{\text{READY}}$ hold time<br>after $\overline{\text{RD}}$ , $\overline{\text{WR}}$ high (Demulti-<br>plexed Bus) <sup>3)2</sup> | t <sub>60</sub> SR | 0                          | 0<br>+ 2t <sub>A</sub> + t <sub>C</sub> + t <sub>F</sub> <sup>3</sup> | 0  | TCL - 10<br>+ 2t <sub>A</sub> + t <sub>C</sub> + t <sub>F</sub> <sup>3</sup> | ns   |

**Table 19 CLKOUT and  $\overline{\text{READY}}/\text{READY}$** 

- 1) Measured between 0.3 and 2.7 volts
- 2) These timings assure recognition at a specific clock edge for test purposes only.
- 3) Demultiplexed bus is the worst case. For multiplexed bus, 2TCL should be added to the maximum values. This adds even more time for deactivating  $\overline{\text{READY}}$ . 2t<sub>A</sub> and t<sub>C</sub> refer to the following bus cycle, t<sub>F</sub> refers to the current bus cycle.

## ST10R272L - ELECTRICAL CHARACTERISTICS

Figure 24 CLKOUT and  $\overline{\text{READY}}/\text{READY}$ 

- 1 Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 2 The leading edge of the respective command depends on RW-delay.
- 3  $\overline{\text{READY}}$  (or  $\text{READY}$ ) sampled HIGH (resp. LOW) at this sampling point generates a  $\text{READY}$  controlled waitstate,  $\overline{\text{READY}}$  (resp.  $\text{READY}$ ) sampled LOW (resp. HIGH) at this sampling point terminates the currently running bus cycle.
- 4  $\overline{\text{READY}}$  (resp.  $\text{READY}$ ) may be deactivated in response to the trailing (rising) edge of the corresponding command ( $\overline{\text{RD}}$  or  $\overline{\text{WR}}$ ).
- 5 If the Asynchronous  $\overline{\text{READY}}$  (or  $\text{READY}$ ) signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill  $t_{37}$  in order to be safely synchronized. This is guaranteed, if  $\text{READY}$  is removed in response to the command (see Note 4)).

## ST10R272L - ELECTRICAL CHARACTERISTICS

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- 6 Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
- 7 The next external bus cycle may start here.

## ST10R272L - ELECTRICAL CHARACTERISTICS

## 16.3.6 External Bus Arbitration

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$

$V_{SS} = 0 \text{ V}$

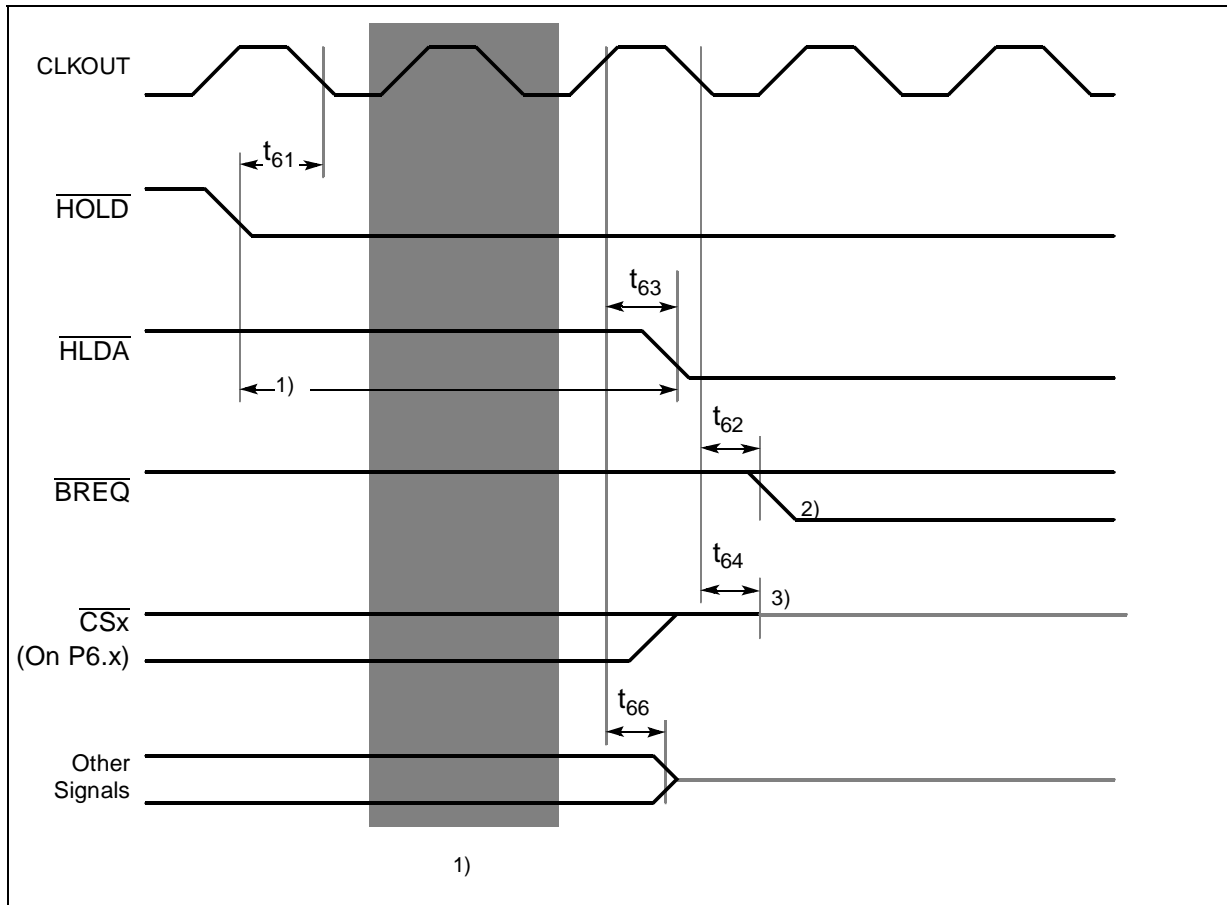
$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$

$C_L = 50 \text{ pF}$

| Parameter  | Symbol      | Max. CPU Clock<br>= 50 MHz |      | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |      | Unit |
|--|-------------|----------------------------|------|--|------|------|
|  |             | min.                       | max. | min.                                       | max. |      |
| $\overline{\text{HOLD}}$ input setup time<br>to CLKOUT                           | $t_{61}$ SR | 15                         | –    | 15   | –    | ns   |
| CLKOUT to $\overline{\text{HLDA}}$ high<br>or $\overline{\text{BREQ}}$ low delay | $t_{62}$ CC | –                          | 10   | –  | 10   | ns   |
| CLKOUT to $\overline{\text{HLDA}}$ low<br>or $\overline{\text{BREQ}}$ high delay | $t_{63}$ CC | –                          | 10   | –  | 10   | ns   |
| $\overline{\text{CSx}}$ release  | $t_{64}$ CC | –                          | 15   | –  | 15   | ns   |
| $\overline{\text{CSx}}$ drive  | $t_{65}$ CC | -3                         | 15   | -3   | 15   | ns   |
| Other signals release  | $t_{66}$ CC | –                          | 15   | –  | 15   | ns   |
| Other signals drive  | $t_{67}$ CC | -3                         | 15   | -3   | 15   | ns   |

Table 20 External bus arbitration

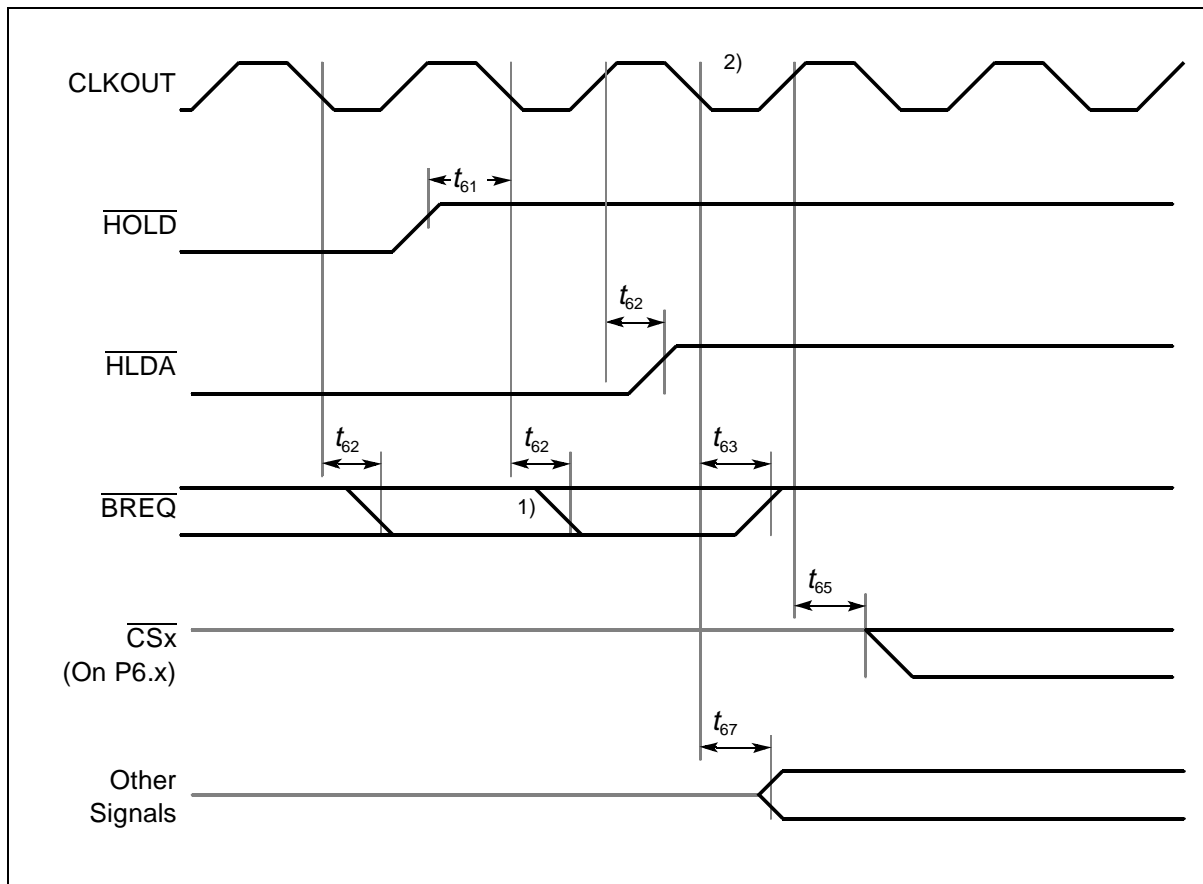
## ST10R272L - ELECTRICAL CHARACTERISTICS



**Figure 25 External bus arbitration, releasing the bus**

- 1 The ST10R272L will complete the running bus cycle before granting bus access.
- 2 This is the first opportunity for  $\overline{\text{BREQ}}$  to become active.
- 3 The  $\overline{\text{CS}}$  outputs will be resistive high (pullup) after  $t_{64}$ .

## ST10R272L - ELECTRICAL CHARACTERISTICS



**Figure 26 External bus arbitration, (regaining the bus)**

- 1 This is the last chance for  $\overline{\text{BREQ}}$  to trigger the regain-sequence indicated. Even if  $\overline{\text{BREQ}}$  is activated earlier, the regain-sequence is initiated by  $\overline{\text{HOLD}}$  going high. Please note that  $\overline{\text{HOLD}}$  may also be de-activated without the ST10R272L requesting the bus.
- 2 The next ST10R272L driven bus cycle may start here.

## ST10R272L - ELECTRICAL CHARACTERISTICS

### 16.3.7 External Hardware Reset

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$

$V_{SS} = 0 \text{ V}$

$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$

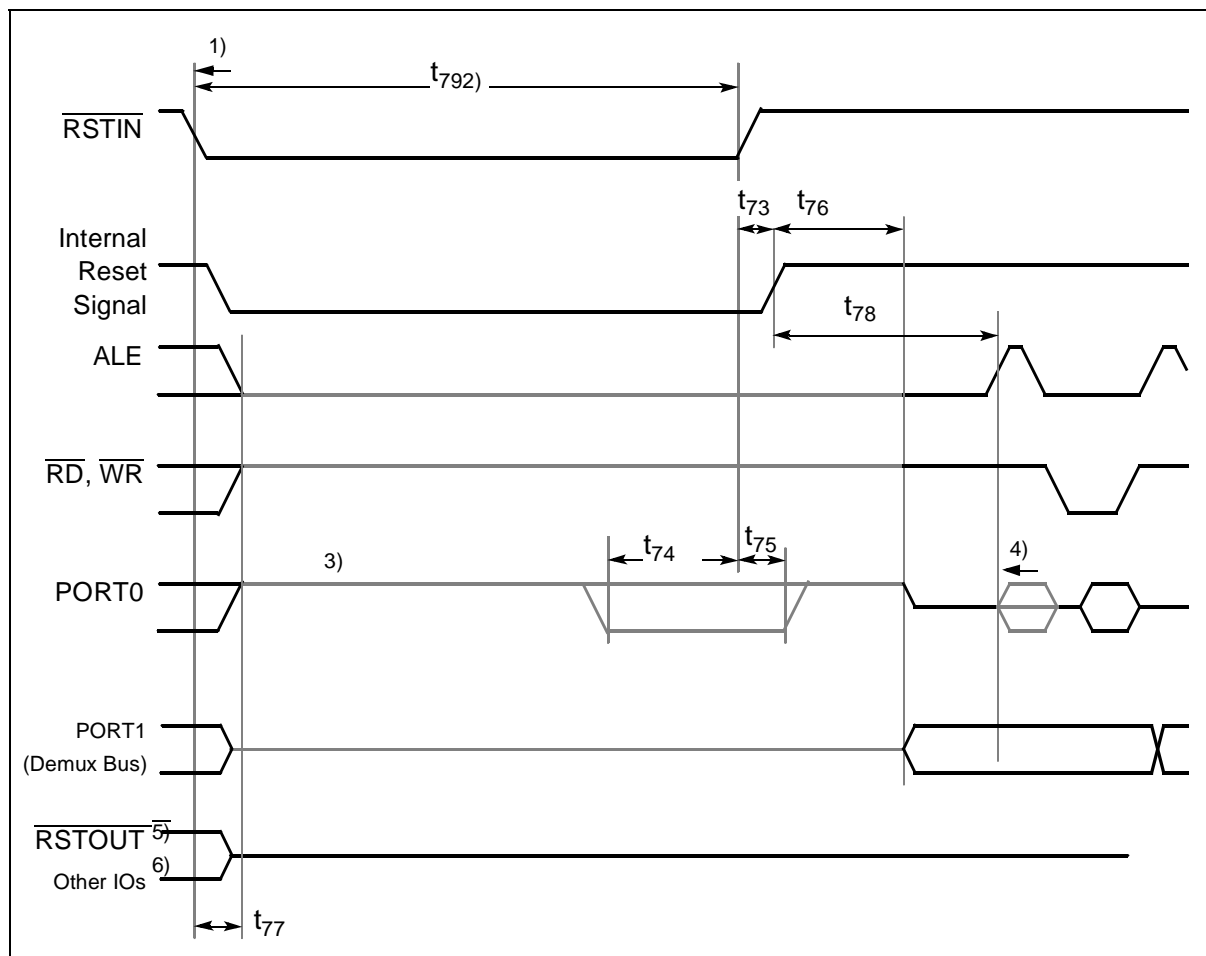
$C_L = 50 \text{ pF}$

| Parameter  | Symbol             | Max. CPU Clock<br>= 50 MHz |      | Variable CPU Clock<br>1/2TCL = 1 to 50 MHz |      | Unit |
|--|--------------------|----------------------------|------|--|------|------|
|  |                    | min.                       | max. | min.                                       | max. |      |
| Sync. $\overline{\text{RSTIN}}$ low time <sup>1)</sup>   | t <sub>70</sub> SR | 50                         | –    | 4 TCL + 10                                 | –    | ns   |
| $\overline{\text{RSTIN}}$ low to internal reset sequence start                                   | t <sub>71</sub> CC | 4                          | 16   | 4  | 16   | TCL  |
| internal reset sequence, ( $\overline{\text{RSTIN}}$ internally pulled low)                      | t <sub>72</sub> CC | 1024                       | 1024 | 1024                                       | 1024 | TCL  |
| $\overline{\text{RSTIN}}$ rising edge to internal reset condition end                            | t <sub>73</sub> CC | 4                          | 6    | 4  | 6    | TCL  |
| PORT0 system start-up configuration setup to $\overline{\text{RSTIN}}$ rising edge <sup>2)</sup> | t <sub>74</sub> SR | 100                        | –    | 100  | –    | ns   |
| PORT0 system start-up configuration hold after $\overline{\text{RSTIN}}$ rising edge             | t <sub>75</sub> SR | 1                          | 6    | 1  | 6    | TCL  |
| Bus signals drive from internal reset end  | t <sub>76</sub> CC | 0                          | 20   | 0  | 20   | ns   |
| $\overline{\text{RSTIN}}$ low to signals release   | t <sub>77</sub> CC | –                          | 50   | –  | 50   | ns   |
| ALE rising edge from internal reset condition end  | t <sub>78</sub> CC | 8                          | 8    | 8  | 8    | TCL  |
| Async. $\overline{\text{RSTIN}}$ low time <sup>1)</sup>  | t <sub>79</sub> SR | 1500                       | –    | 1500                                       | –    | ns   |

**Table 21 External hardware reset**

- 1) On power-up reset, the  $\overline{\text{RSTIN}}$  pin must be asserted until a stable clock signal is available (about 10...50 ms to allow the on-chip oscillator to stabilize) and until System Start-up Configuration is correct on PORT0 (about 50  $\mu\text{s}$  for internal pullup devices to load 50 pF from  $V_{IL\text{min}}$  to  $V_{IH\text{min}}$ ).
- 2) The value of bits 0 (EMU), 1 (ADAPT), 13 to 15 (Clock Configuration) are loaded during hardware reset as long as internal reset signal is active, and have an immediate effect on the system.

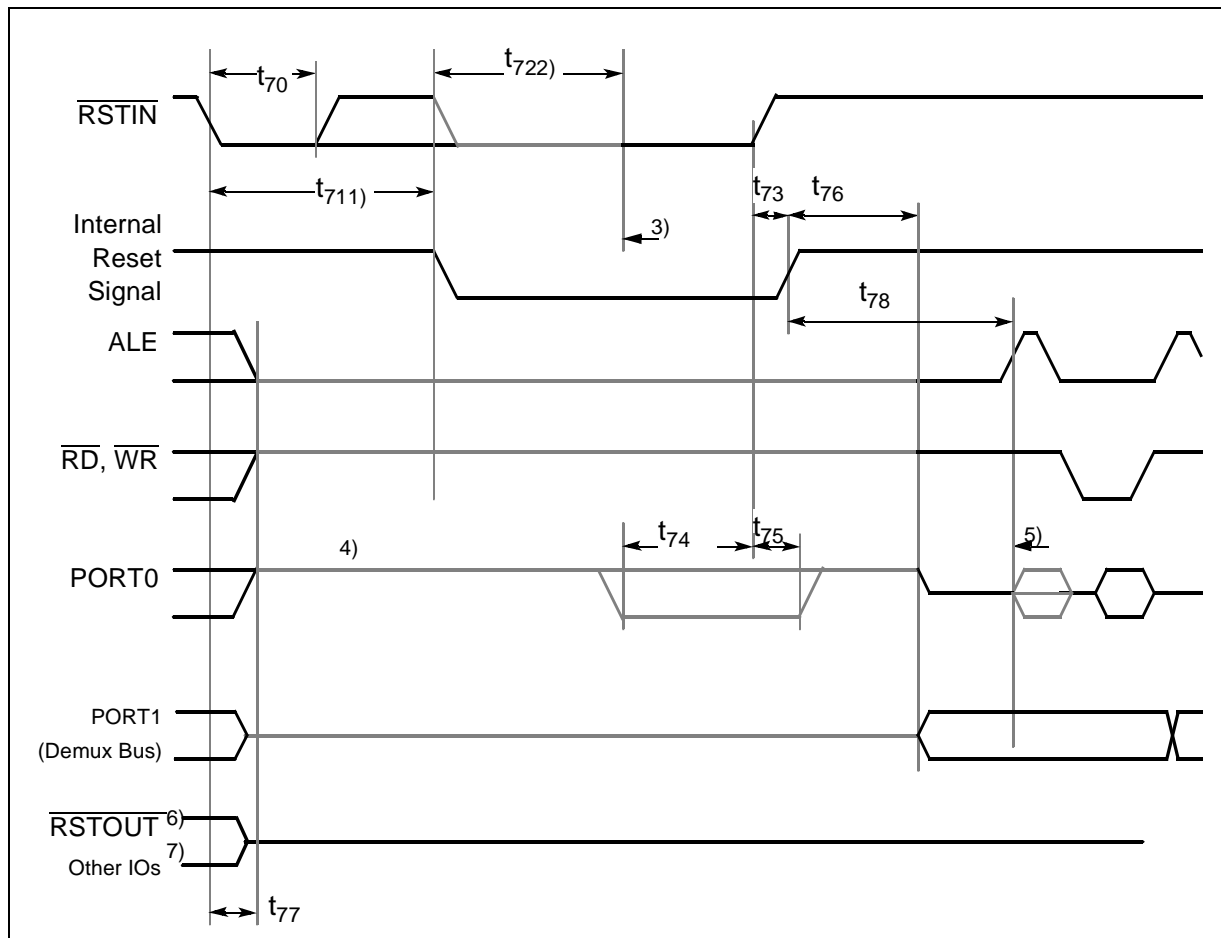
## ST10R272L - ELECTRICAL CHARACTERISTICS



**Figure 27 External asynchronous hardware reset (power-up reset): Vpp low**

- 1 The ST10R272L is reset in its default state asynchronously with  $\overline{\text{RSTIN}}$ . The internal RAM content may be altered if an internal write access is in progress.
- 2 On power-up,  $\overline{\text{RSTIN}}$  must be asserted  $t_{79}$  after a stabilized CPU clock signal is available.
- 3 Internal pullup devices are active on the PORT0 lines, so - input level is high if the respective pin is left open - or is low if the respective pin is connected to an external pulldown device.
- 4 The ST10R272L starts execution here at address 00'0000h.
- 5  $\overline{\text{RSTOUT}}$  stays active until execution of the EINIT (end of initialization) instruction.
- 6 Activation of the IO pins is controlled by software

## ST10R272L - ELECTRICAL CHARACTERISTICS



**Figure 28 External synchronous hardware reset (warm reset): V<sub>pp</sub> high**

- 1 The pending internal hold states are cancelled and the current internal access cycle (if any) is completed.
- 2  $\overline{\text{RSTIN}}$  pulled low by internal device during internal reset sequence.
- 3 The reset condition may ends here if  $\overline{\text{RSTIN}}$  pin is sampled high after t<sub>72</sub>.
- 4 Internal pullup devices are active on the PORT0 lines. Their input level is high if the respective pin is left open, or is low if the respective pin is connected to an external pull-down device by resistive high (pullup) after t<sub>64</sub>.
- 5 The ST10R272L starts execution here at address 00'0000h.
- 6  $\overline{\text{RSTOUT}}$  stays active until execution of the EINIT (End of Initialization) instruction.
- 7 Activation of the IO pins is controlled by software.

## ST10R272L - ELECTRICAL CHARACTERISTICS

## 16.3.8 Synchronous Serial Port Timing

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

$V_{SS} = 0 \text{ V}$

$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$

$C_L = 50 \text{ pF}$

| Parameter                              | Symbol              | Max. Baudrate<br>= 25 MBd |      | Variable Baudrate<br>= 0.2 to 25 MBd |                         | Unit |
|--|---------------------|---------------------------|------|--------------------------------------|-------------------------|------|
|  |                     | min.                      | max. | min.                                 | max.                    |      |
| SSP clock cycle time                   | t <sub>200</sub> CC | 40                        | 40   | 4 TCL                                | 512 TCL                 | ns   |
| SSP clock high time                    | t <sub>201</sub> CC | 13                        | –    | t <sub>200</sub> /2 - 7              | –                       | ns   |
| SSP clock low time                     | t <sub>202</sub> CC | 13                        | –    | t <sub>200</sub> /2 - 7              | –                       | ns   |
| SSP clock rise time                    | t <sub>203</sub> CC | –                         | 3    | –                                    | 3                       | ns   |
| SSP clock fall time                    | t <sub>204</sub> CC | –                         | 3    | –                                    | 3                       | ns   |
| CE active before shift edge            | t <sub>205</sub> CC | 13                        | –    | t <sub>200</sub> /2 - 7              | –                       | ns   |
| CE inactive after latch edge           | t <sub>206</sub> CC | 33                        | 47   | t <sub>200</sub> - 7                 | t <sub>200</sub> + 7    | ns   |
| Write data valid after shift edge      | t <sub>207</sub> CC | –                         | 7    | –                                    | 7                       | ns   |
| Write data hold after shift edge       | t <sub>208</sub> CC | 0                         | –    | 0                                    | –                       | ns   |
| Write data hold after latch edge       | t <sub>209</sub> CC | 15                        | 25   | t <sub>200</sub> /2 - 5              | t <sub>200</sub> /2 + 5 | ns   |
| Read data active after latch edge      | t <sub>210</sub> SR | 27                        | –    | t <sub>200</sub> /2 + 7              | –                       | ns   |
| Read data setup time before latch edge | t <sub>211</sub> SR | 15                        | –    | 15                                   | –                       | ns   |
| Read data hold time after latch edge   | t <sub>212</sub> SR | 0                         | –    | 0                                    | –                       | ns   |

Table 22 Synchronous serial port timing

## ST10R272L - ELECTRICAL CHARACTERISTICS

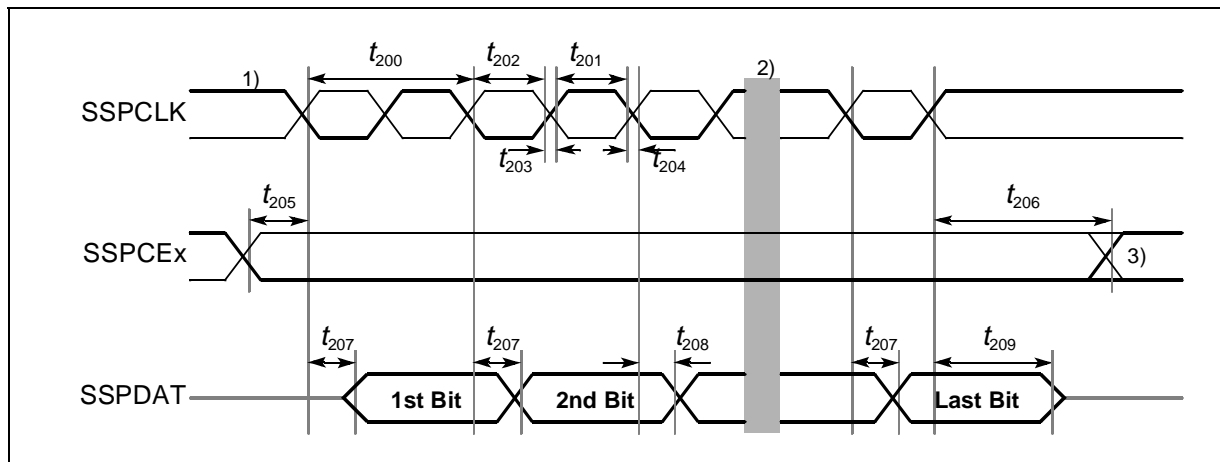


Figure 29 SSP write timing

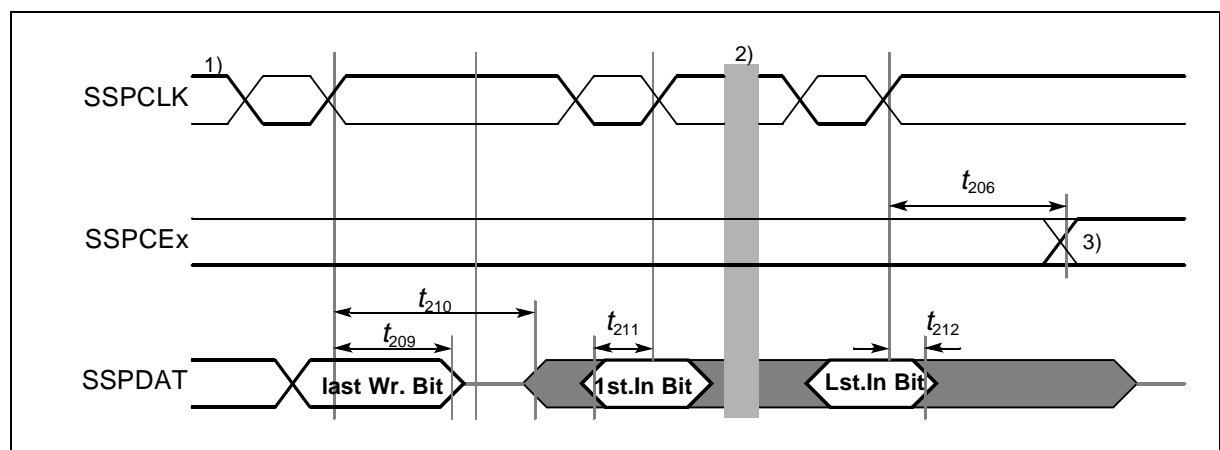
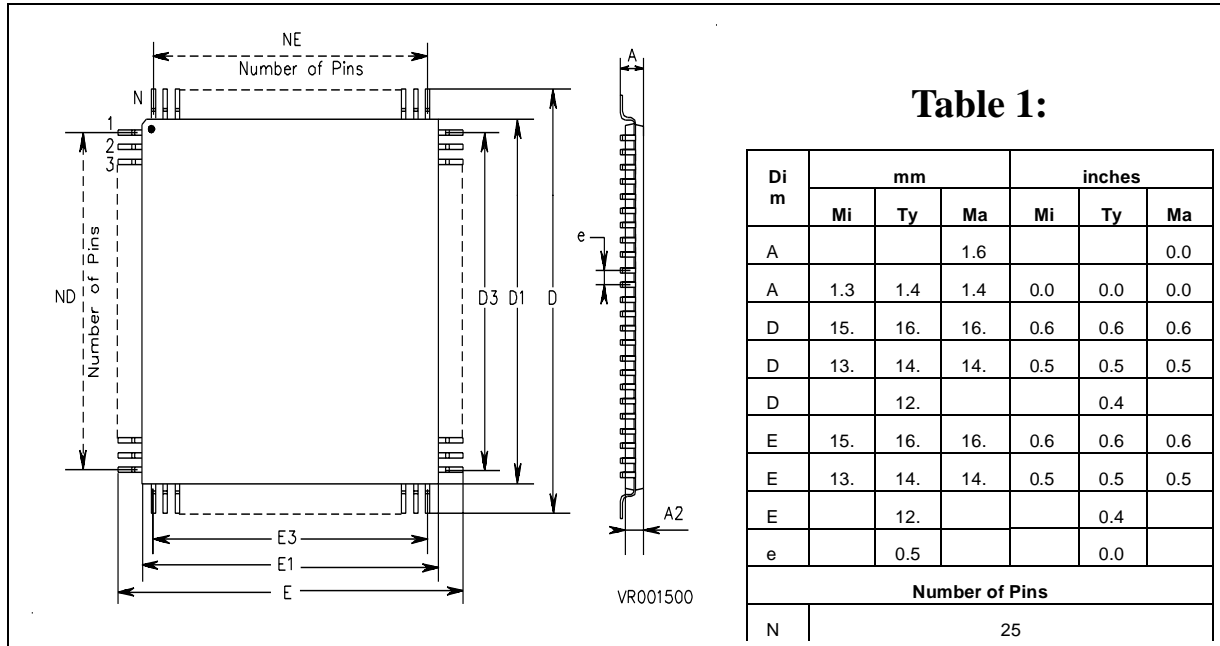


Figure 30 SSP read timing

- 1 The transition of shift and latch edge of SSPCLK is programmable. This figure uses the falling edge as shift edge (drawn bold).
- 2 The bit timing is repeated for all bits to be transmitted or received.
- 3 The active level of the chip enable lines is programmable. This figure uses an active low CE (drawn bold). At the end of a transmission or reception the CE signal is disabled in single transfer mode. In continuous transfer mode it remains active.

**ST10R272L - PACKAGE MECHANICAL DATA**

**17 PACKAGE MECHANICAL DATA**



**Figure 31 Package outline TQFP100 (14 x 14 mm)**

**18 ORDERING INFORMATION**

| Sales type  | Temperature range | Package          |
|-------------|-------------------|------------------|
| ST10R272LT1 | 0°C to 70°C       | TQFP100 (14x 14) |
| ST10R272LT6 | -40°C to +85°C    |                  |

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