

T835-800B Datasheet



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DiGi Electronics Part Number	T835-800B-DG
Manufacturer	STMicroelectronics
Manufacturer Product Number	T835-800B
Description	TRIAC ALTERNISTOR 800V 8A DPAK
Detailed Description	TRIAC Alternistor - Snubberless 800 V 8 A Surface Mount DPAK

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Manufacturer Product Number:

T835-800B

Series:

-

Triac Type:

Alternistor - Snubberless

Current - On State (It (RMS)) (Max):

8 A

Current - Non Rep. Surge 50, 60Hz (I_{tsm}):

80A, 84A

Current - Hold (I_h) (Max):

50 mA

Operating Temperature:

-40°C ~ 125°C (T_J)

Package / Case:

TO-252-3, DPAK (2 Leads + Tab), SC-63

Base Product Number:

T835

Manufacturer:

STMicroelectronics

Product Status:

Active

Voltage - Off State:

800 V

Voltage - Gate Trigger (V_{gt}) (Max):

1.3 V

Current - Gate Trigger (I_{gt}) (Max):

50 mA

Configuration:

Single

Mounting Type:

Surface Mount

Supplier Device Package:

DPAK

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.30.0080

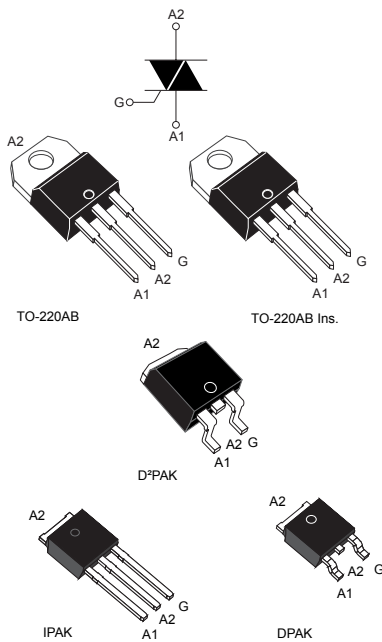
Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

Snubberless™, logic level and standard 8 A Triacs



Features

- On-state rms current, $I_{T(RMS)}$ 8 A
- Repetitive peak off-state voltage, V_{DRM} / V_{RRM} 600 V to 800 V
- Triggering gate current, I_{GT} 5 to 50 mA

Description

Available either in through-hole and surface-mount packages, these devices are suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits or for phase control operation in light dimmers and motor speed controllers, etc.

The Snubberless versions (BTA, BTB08_XXXXW and T8 series) are specially recommended for use on inductive loads, thanks to their high commutation performance.

Logic level versions are designed to interface directly with low power drivers such as Microcontrollers.

By using an internal ceramic pad, the BTA series provide voltage insulated tab (rated at 2500 V_{RMS}) in compliance with UL standards (file ref.: E81734).

Product status link

[BTA08](#)
[BTB08](#)
[T810](#)
[T835](#)
[T850](#)



1 Characteristics

Table 1. Absolute maximum ratings ($T_j = 25\text{ °C}$ unless otherwise stated)

Symbol	Parameter		Value	Unit	
$I_{T(RMS)}$	RMS on-state current (full sine wave)	IPAK, DPAK, TO-220AB, D ² PAK $T_c = 110\text{ °C}$	8	A	
		TO-220AB Ins. $T_c = 100\text{ °C}$			
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)	$f = 50\text{ Hz}$	$t = 20\text{ ms}$	80	A
		$f = 60\text{ Hz}$	$t_p = 16.7\text{ ms}$	84	
I^2t	I^2t value for fusing		$t_p = 10\text{ ms}$	36	A ² s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ ns}$	$f = 120\text{ Hz}$	$T_j = 125\text{ °C}$	50	A/ μ s
I_{GM}	Peak gate current	$t_p = 20\text{ }\mu$ s	$T_j = 125\text{ °C}$	4	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125\text{ °C}$	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	°C

Table 2. Electrical characteristics ($T_j = 25\text{ °C}$, unless otherwise specified) Snubberless and logic level (3 quadrants)

Symbol	Parameter	Quadrant	T8			BTA08/BTB08				Unit	
			10	35	50	TW	SW	CW	BW		
$I_{GT}^{(1)}$	$V_D = 12\text{ V}$, $R_L = 30\text{ }\Omega$	I - II - III	Max.	10	35	50	5	10	35	50	mA
V_{GT}		I - II - III	Max.	1.2				V			
V_{GD}	$V_D = V_{DRM}$, $R_L = 3.3\text{ k}\Omega$, $T_j = 125\text{ °C}$	I - II - III	Min.	0.2				V			
$I_H^{(2)}$	$I_T = 100\text{ mA}$	I - II - III	Max.	15	35	75	10	15	35	50	mA
I_L	$I_G = 1.2 \times I_{GT}$	I - III	Max.	25	50	70	10	25	50	70	mA
		II	Max.	30	60	110	15	30	60	80	
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}$, gate open, $T_j = 125\text{ °C}$		Max.	40	400	1000	20	40	400	1000	V/ μ s
$(di/dt)_c^{(2)}$	$(dV/dt)_c = 0.1\text{ V}/\mu$ s, $T_j = 125\text{ °C}$		Min.	5.4			3.5	5.4			A/ms
	$(dV/dt)_c = 10\text{ V}/\mu$ s, $T_j = 125\text{ °C}$		Min.	2.8			1.5	2.98			
	Without snubber, $T_j = 125\text{ °C}$		Min.		4.5	7			4.5	7	

1. Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

2. For both polarities of A2 referenced to A1



Table 3. Standard (4 quadrants)

Symbol	Parameter	Quadrant		BTA08/BTB08		Unit
				C	B	
$I_{GT}^{(1)}$	$V_D = 12\text{ V}, R_L = 33\ \Omega$	I - II - III	Max.	25	50	mA
		IV		50	100	
V_{GT}		All	Max.	1.3		V
V_{GD}	$V_D = V_{DRM}, R_L = 33\ \text{k}\Omega, T_j = 125\ ^\circ\text{C}$	All	Min.	0.2		V
$I_H^{(2)}$	$I_T = 500\ \text{mA}$	I - II - III	Max.	25	50	mA
I_L	$I_G = 1.2 I_{GT}$	I - III - IV	Max.	40	50	mA
		II		80	100	
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}$ gate open, $T_j = 125\ ^\circ\text{C}$		Min.	200	400	V/ μs
$(dV/dt)_C^{(2)}$	$(dI/dt)_C = 3.5\ \text{A/ms}, T_j = 125\ ^\circ\text{C}$		Min.	5	10	V/ μs

1. Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.
2. For both polarities of A2 referenced to A1

Table 4. Static electrical characteristics

Symbol	Test conditions			Value	Unit
$V_{TM}^{(1)}$	$I_{TM} = 11\ \text{A}, t_p = 380\ \mu\text{s}$	$T_j = 25\ ^\circ\text{C}$	Max.	1.55	V
$V_{TO}^{(1)}$	threshold on-state voltage	$T_j = 125\ ^\circ\text{C}$	Max.	0.85	V
$R_D^{(1)}$	Dynamic resistance	$T_j = 125\ ^\circ\text{C}$	Max.	50	m Ω
$I_{DRM} I_{RRM}$	$V_{DRM} = V_{RRM}$	$T_j = 25\ ^\circ\text{C}$	Max.	5	μA
		$T_j = 125\ ^\circ\text{C}$	Max.	1	mA

1. For both polarities of A2 referenced to A1

Table 5. Thermal resistance

Symbol	Parameter		Value	Unit	
$R_{th(j-c)}$	Max. junction to case thermal resistance (AC)		IPAK / D2PAK / DPAK / TO-220AB	$^\circ\text{C/W}$	
			TO-220AB Insulated		
$R_{th(j-a)}$	Junction to ambient (typ.)	$S = 2\ \text{cm}^2^{(1)}$	D ² PAK	$^\circ\text{C/W}$	
		$S = 1\ \text{cm}^2^{(1)}$	DPAK		
	Junction to ambient (typ.)	TO-220AB / TO-220AB Insulated			60
		IPAK			100

1. S = Copper surface under tab.



1.1 Characteristics (curves)

Figure 1. Maximum power dissipation versus on-state RMS current (full cycle)

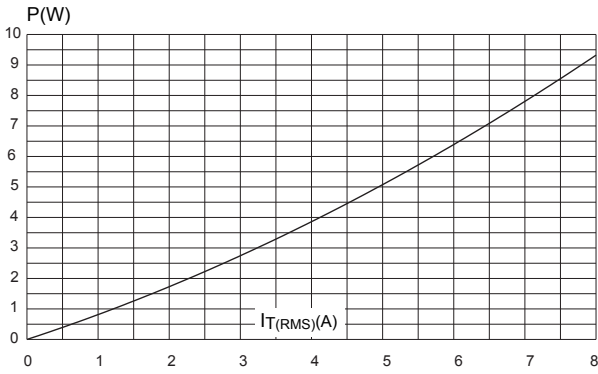


Figure 2. RMS on-state current versus temperature (full cycle)

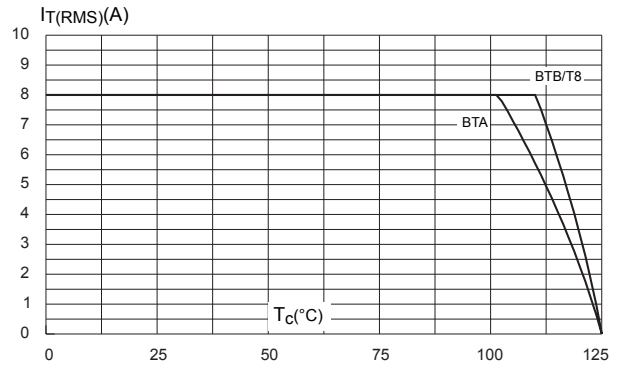


Figure 3. RMS on-state current versus ambient temperature (full cycle)

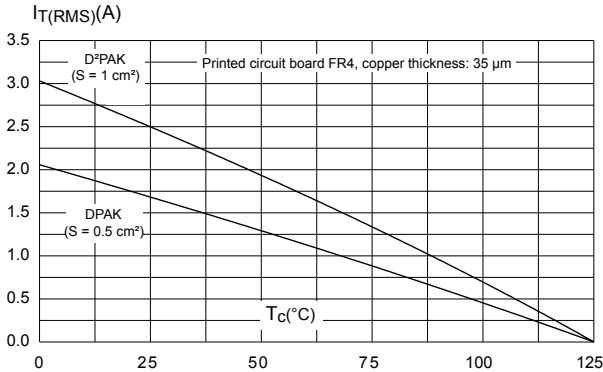


Figure 4. Relative variation of thermal impedance versus pulse duration

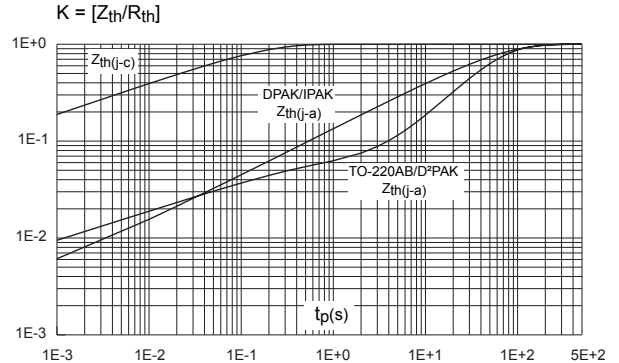




Figure 5. On-state characteristics (maximum values)

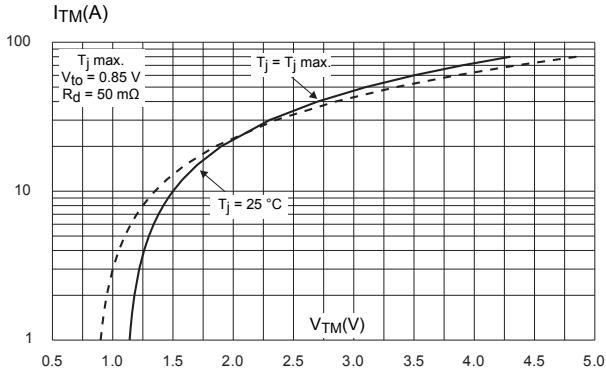


Figure 6. Surge peak on-state current versus number of cycles

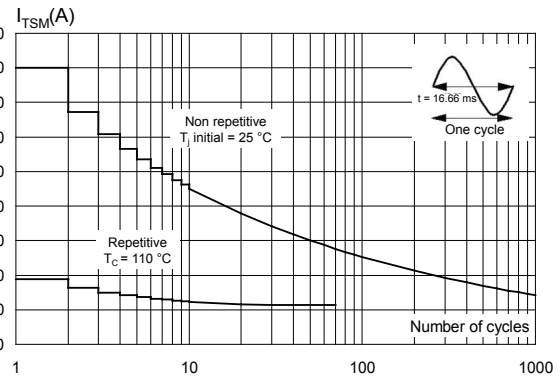


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse ($t_p < 10$ ms)

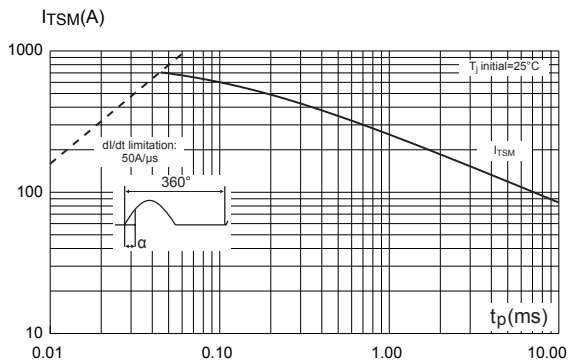


Figure 8. Relative variation of gate trigger current

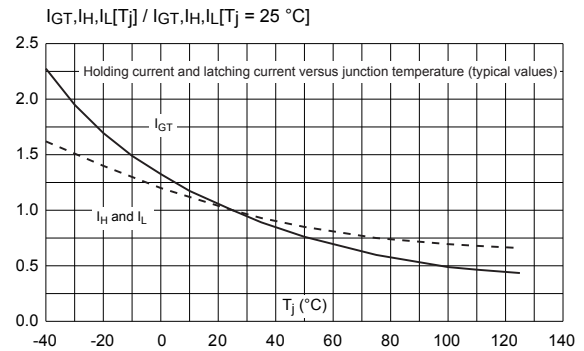


Figure 9. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

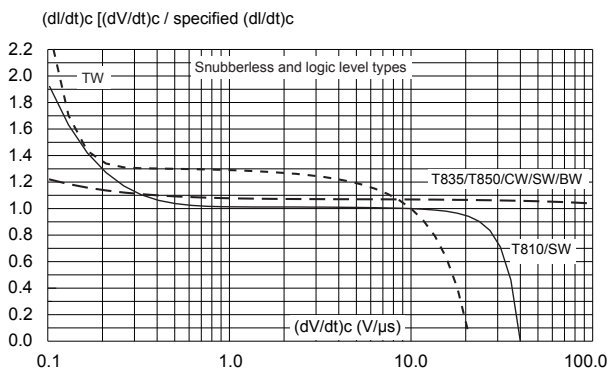


Figure 10. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

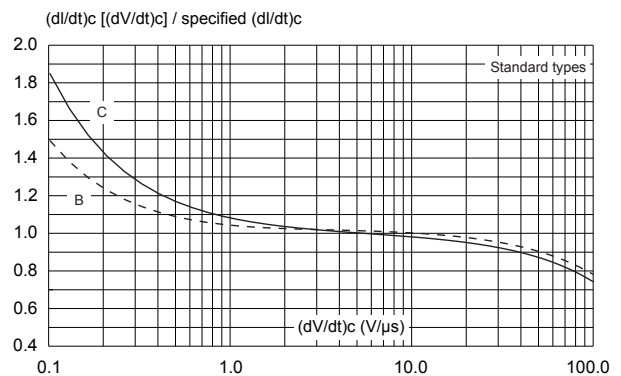




Figure 11. Relative variation of critical rate of decrease of main current versus junction temperature

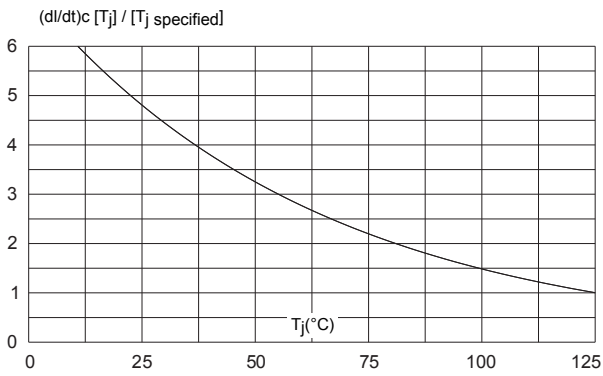
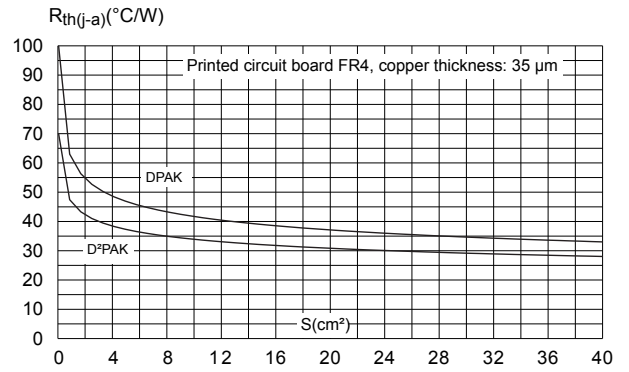


Figure 12. DPAK and D2PAK thermal resistance junction to ambient versus copper surface under tab





2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 DPAK package information

- Epoxy meets UL94, V0
- Lead-free package
- Recommended torque: 0.4 to 0.6 N·m

Figure 13. DPAK package outline

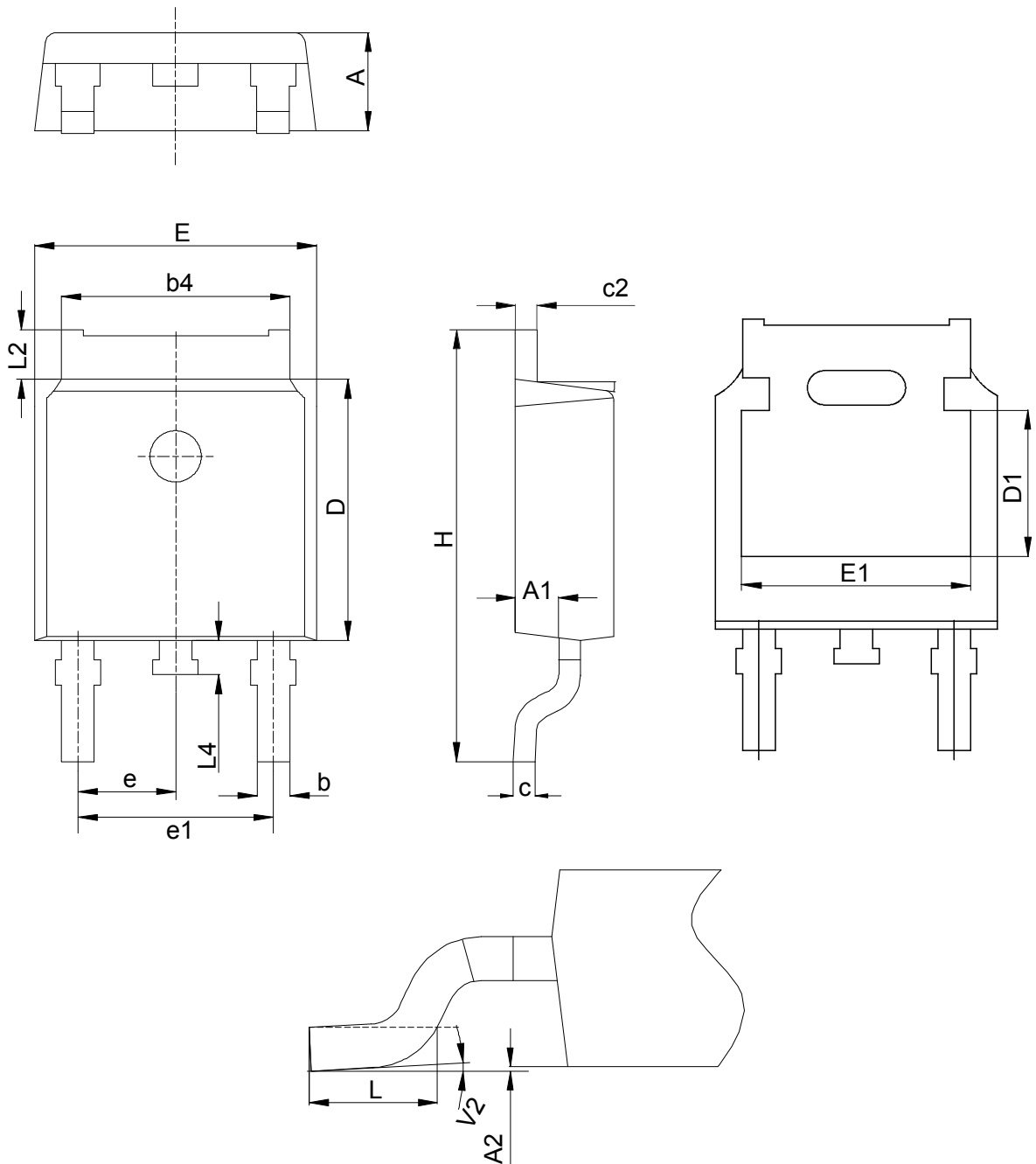


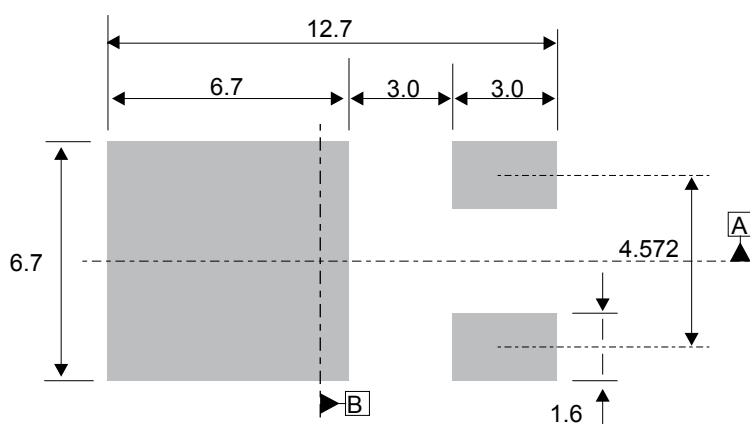
Table 6. DPAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18		2.40	0.0858		0.0945
A1	0.90		1.10	0.0354		0.0433
A2	0.03		0.23	0.0012		0.0091
b	0.64		0.90	0.0252		0.354
b4	4.95		5.46	0.1949		0.2150
c	0.46		0.61	0.0181		0.0240
c2	0.46		0.60	0.0181		0.0236
D	5.97		6.22	0.2350		0.2449
D1	5.10			0.2008		
E	6.35		6.73	0.2500		0.2650
E1	4.32			0.1701		
e		2.29			0.0900	
e1		4.57			0.1800	
H	9.35		10.40	0.3681		0.4094
L	1.00		1.78	0.0394		0.0701
L2			1.27			0.0500
L4	0.60		1.02	0.0236		0.0402
V2	0°		+8°	0°		+8°

1. Dimensions in inches are given for reference only

Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.

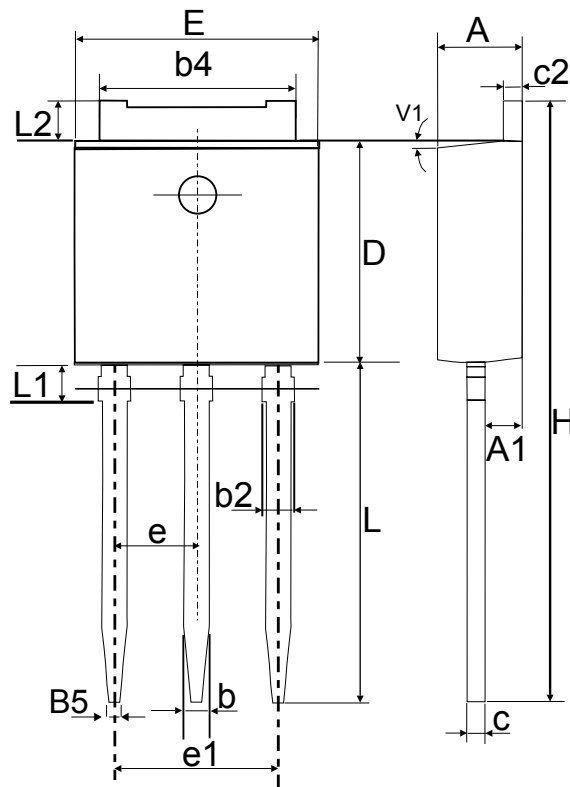
Figure 14. DPAK recommended footprint (dimensions are in mm)



The device must be positioned within $\oplus 0.05 \text{ AB}$

2.2 IPAK package information

Figure 15. IPAK package outline



Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.



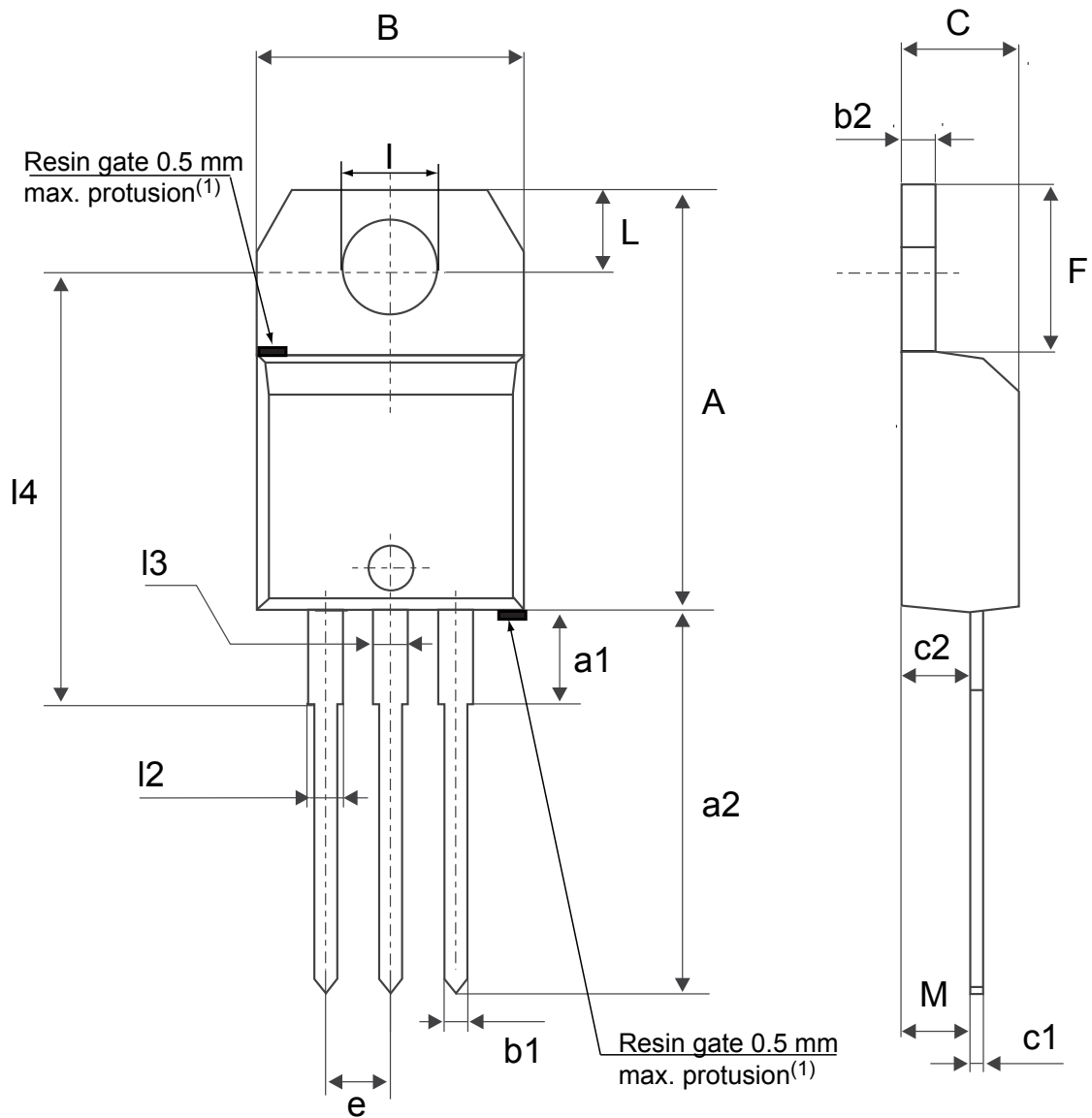
Table 7. IPAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.20		2.40	0.0866		0.0945
A1	0.90		1.10	0.0354		0.0433
b	0.64		0.90	0.0252		0.0354
b2			0.95			0.0374
b4	5.20		5.43	0.2047		0.2138
B5		0.30			0.0118	
c	0.45		0.60	0.0177		0.0236
c2	0.46		0.60	0.0181		0.0236
D	6.00		6.20	0.2362		0.2441
E	6.40		6.65	0.2520		0.2618
e		2.28			0.0898	
e1	4.40		4.60	0.1732		0.1811
H		16.10			0.6339	
L	9.00		9.60	0.3545		0.3780
L1	0.80		1.20	0.0315		0.0472
L2		0.80	1.25		0.0315	0.0492
V1		10°			10°	

1. Inch dimensions are for reference only.

2.3 TO-220AB insulated package information

Figure 16. TO-220AB insulated package outline



(1) Resin gate position accepted in one of the two positions or in the symmetrical opposites.



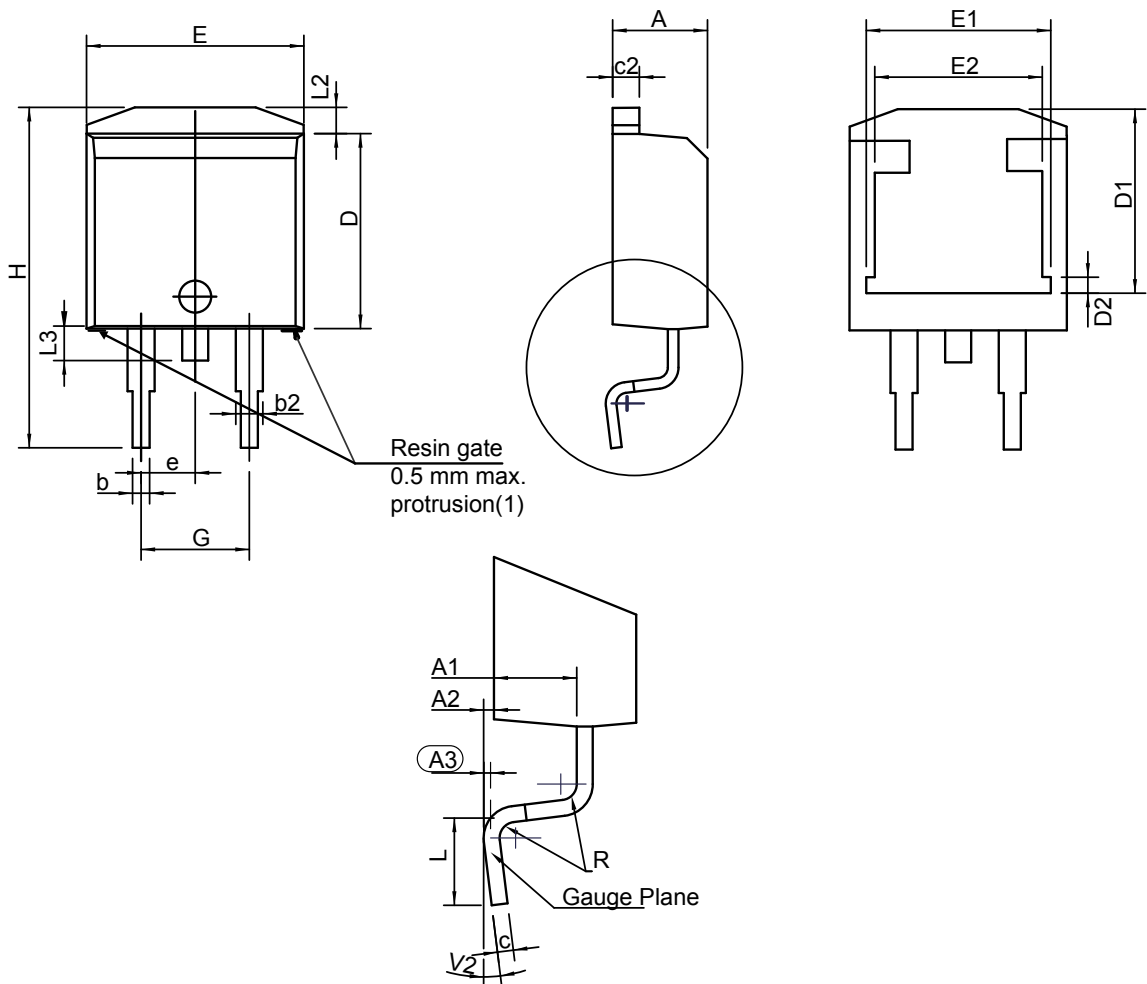
Table 8. TO-220AB insulated package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.5984		0.6260
a1		3.75			0.1476	
a2	13.00		14.00	0.5118		0.5512
B	10.00		10.40	0.3937		0.4094
b1	0.61		0.88	0.0240		0.0346
b2	1.23		1.32	0.0484		0.0520
C	4.40		4.60	0.1732		0.1811
c1	0.49		0.70	0.0193		0.0276
c2	2.40		2.72	0.0945		0.1071
e	2.40		2.70	0.0945		0.1063
F	6.20		6.60	0.2441		0.2598
I	3.73		3.88	0.1469		0.1528
L	2.65		2.95	0.1043		0.1161
I2	1.14		1.70	0.0449		0.0669
I3	1.14		1.70	0.0449		0.0669
I4	15.80	16.40	16.80	0.6220	0.6457	0.6614
M		2.6			0.1024	

1. Inch dimensions are for reference only.

2.4 D²PAK package information

Figure 17. D²PAK package outline

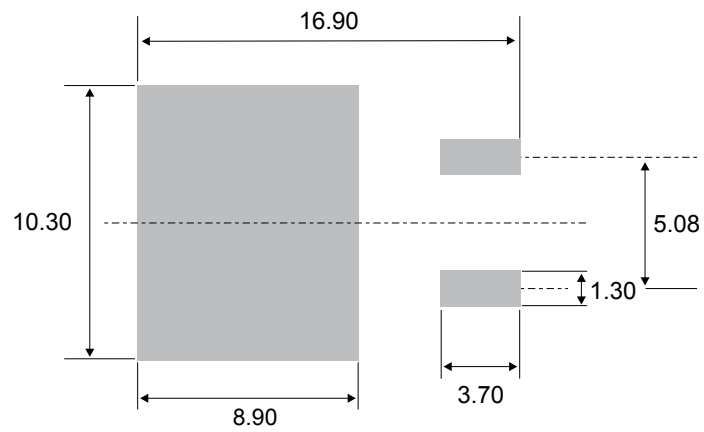


(1) Resin gate position accepted in one of the two positions or in the symmetrical opposites

Table 9. D²PAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.30		4.60	0.1693		0.1811
A1	2.49		2.69	0.0980		0.1059
A2	0.03		0.23	0.0012		0.0091
A3		0.25			0.0098	
b	0.70		0.93	0.0276		0.0366
b2	1.25		1.7	0.0492		0.0669
c	0.45		0.60	0.0177		0.0236
c2	1.21		1.36	0.0476		0.0535
D	8.95		9.35	0.3524		0.3681
D1	7.50		8.00	0.2953		0.3150
D2	1.30		1.70	0.0512		0.0669
e	2.54			0.1		
E	10.00		10.28	0.3937		0.4047
E1	8.30		8.70	0.3268		0.3425
E2	6.85		7.25	0.2697		0.2854
G	4.88		5.28	0.1921		0.2079
H	15		15.85	0.5906		0.6240
L	1.78		2.28	0.0701		0.0898
L2	1.27		1.40	0.0500		0.0551
L3	1.40		1.75	0.0551		0.0689
R		0.40			0.0157	
V2	0°		8°	0°		8°

1. Dimensions in inches are given for reference only

Figure 18. D²PAK recommended footprint (dimensions are in mm)

3 Ordering information

Figure 19. Ordering information scheme (BTA08 and BTB08 series)

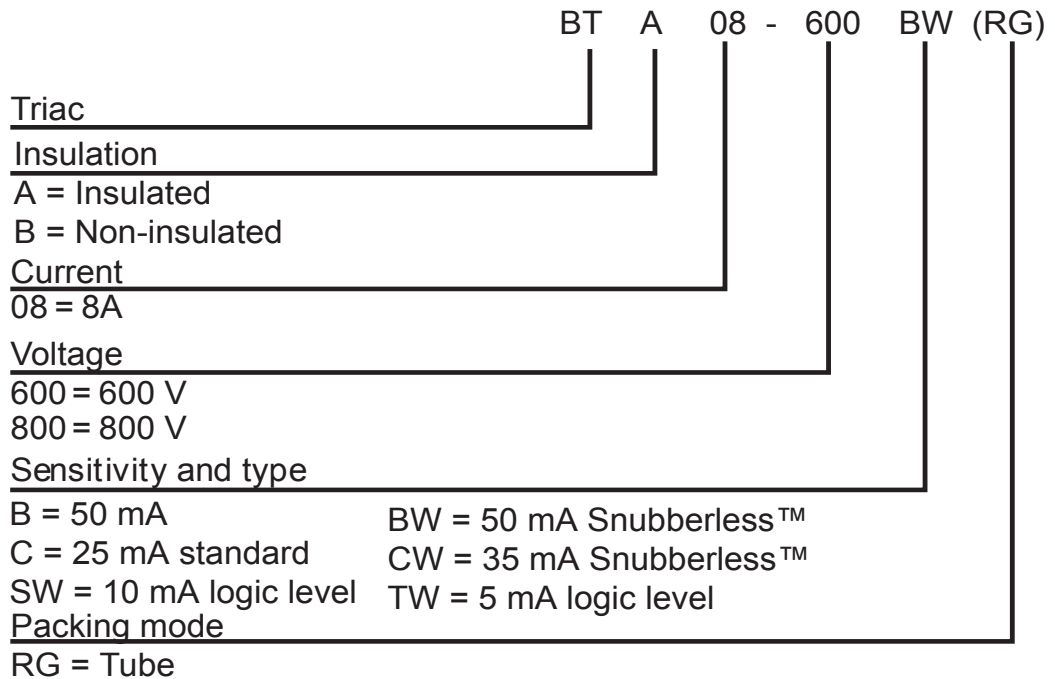


Figure 20. Ordering information scheme (T8 series)

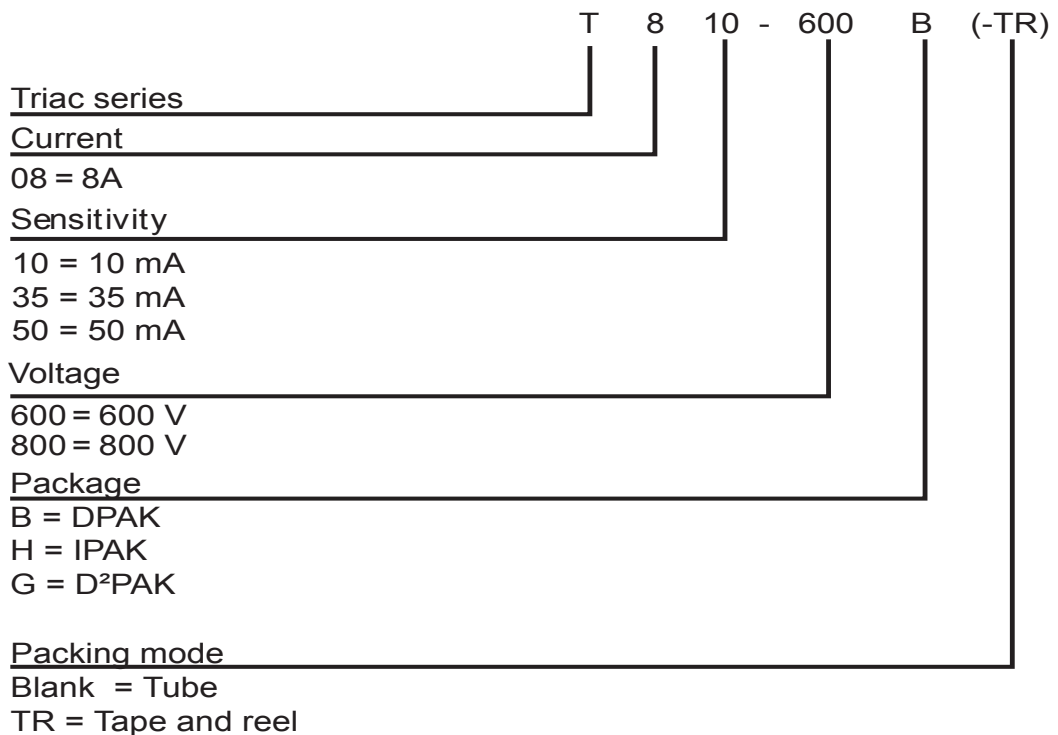




Table 10. Product selector

Part Number	Voltage (xxx)		Sensitivity	Type	Package
	600	800			
T810-xxxB	X	X	10 mA	Logic Level	DPAK
T835-xxxH	X		35 mA	Snubberless™	IPAK
T810-xxxG	X		10 mA	Logic Level	D ² PAK
T835-xxxG	X	X	35 mA	Snubberless™	D ² PAK
T850-xxxG	X	X	50 mA	Snubberless™	D ² PAK
BTA08-xxxS	X		10 mA	Logic Level	TO-220AB Ins.
BTA08-xxxC	X	X	35 mA	Standard	TO-220AB Ins.
BTA08-xxxB	X		50 mA	Standard	TO-220AB Ins.
BTA08-xxxTW	X		5 mA	Logic Level	TO-220AB Ins.
BTA08-xxxSW	X		10 mA	Logic Level	TO-220AB Ins.
BTA08-xxxCW	X		35 mA	Snubberless™	TO-220AB Ins.
BTA08-xxxBW	X	X	50 mA	Snubberless™	TO-220AB Ins.
BTB08-xxxS	X		10 mA	Logic Level	TO-220AB
BTB08-xxxC	X		35 mA	Standard	TO-220AB
BTB08-xxxB	X		50 mA	Standard	TO-220AB
BTB08-xxxTW	X	X	5 mA	Logic Level	TO-220AB
BTB08-xxxSW	X		10 mA	Logic Level	TO-220AB
BTB08-xxxCW	X	X	35 mA	Snubberless™	TO-220AB
BTB08-xxxBW	X		50 mA	Snubberless™	TO-220AB



Table 11. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode				
T810-600B	T8 1060	DPAK	0.30	75	Tube				
T835-600B	T8 3560								
T835-800B	T8 3580								
T810-600B-TR	T8 1060			D ² PAK	1.50	2500	Tape&Reel 13"		
T810-800B-TR	T8 1080								
T835-600B-TR	T8 3560								
T835-800B-TR	T8 3580								
T835-600H	T8 3560	IPAK	0.40	75	Tube				
T835-600G	T835-600G	D ² PAK	1.50	50	Tube				
T835-8G	T835-8G								
T850-6G	T850-6G								
T850-8G	T850-8G								
T810-600G-TR	T810-600G			1000	Tape&Reel 13"				
T835-600G-TR	T835-600G								
T835-8G-TR	T835-8G								
T850-6G-TR	T850-6G								
T850-8G-TR	T850-8G	TO-220AB Ins.	2.30	50	Tube				
BTA08-600SRG	BTA08-600S								
BTA08-600BRG	BTA08-600B								
BTA08-600CRG	BTA08-600C								
BTA08-800CRG	BTA08-800C								
BTA08-600BWRG	BTA08-600BW								
BTA08-600CWRG	BTA08-600CW								
BTA08-600SWRG	BTA08-600SW								
BTA08-600TWRG	BTA08-600TW								
BTA08-800BWRG	BTA08-800BW								
BTB08-600BRG	BTB08-600B					TO-220AB	2.30	50	Tube
BTB08-600CRG	BTB08-600C								
BTB08-600SRG	BTB08-600S								
BTB08-600BWRG	BTB08-600BW								
BTB08-600CWRG	BTB08-600CW								
BTB08-600SWRG	BTB08-600SW								
BTB08-600TWRG	BTB08-600TW								
BTB08-800CWRG	BTB08-800CW								
BTB08-800TWRG	BTB08-800TW								



Table 12. Document revision history

Date	Revision	Changes
Apr-2002	5A	Last update.
13-Feb-2006	6	TO-220AB delivery mode changed from bulk to tube. ECOPACK statement added.
10-Mar-2010	7	Updated ECOPACK statement and Figure 26
02-Jun-2014	8	Updated DPAK and IPAK package information and reformatted to current standard.
07-Nov-2016	9	Updated Table 1 and reformatted to current standard.
06-Jan-2017	10	Updated Figure 20: "Ordering information scheme (T8 series)", Table 10: "Product selector" and Table 11: "Ordering information".
09-Feb-2017	11	Added T850 package information.
24-Apr-2017	12	Updated Figure 6.. Minor text changes to improve readability.
14-Mar-2018	13	Updated Table 2. Electrical characteristics ($T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified) Snubberless and logic level (3 quadrants), cover image, Figure 9. Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values) and Figure 20. Ordering information scheme (T8 series).
14-May-2018	14	Updated product status links.
09-Aug-2018	15	Updated Table 3. Standard (4 quadrants).

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