

# ADS1675IPAG Datasheet

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ADS1675IPAG

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DiGi Electronics Part Number	ADS1675IPAG-DG
Manufacturer	<a href="#">Texas Instruments</a>
Manufacturer Product Number	ADS1675IPAG
Description	IC ADC 24BIT SIGMA-DELTA 64TQFP
Detailed Description	24 Bit Analog to Digital Converter 1 Input 1 Sigma-Delta 64-TQFP (10x10)



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## Purchase and inquiry

Manufacturer Product Number:

ADS1675IPAG

Series:

-

Number of Bits:

24

Number of Inputs:

1

Data Interface:

LVDS - Serial, SPI

Ratio - S/H:ADC:

-

Architecture:

Sigma-Delta

Voltage - Supply, Analog:

5V

Features:

-

Package / Case:

64-TQFP

Mounting Type:

Surface Mount

Manufacturer:

Texas Instruments

Product Status:

Active

Sampling Rate (Per Second):

4M

Input Type:

Differential

Configuration:

ADC

Number of A/D Converters:

1

Reference Type:

External

Voltage - Supply, Digital:

2.7V ~ 3.3V

Operating Temperature:

-40°C ~ 85°C

Supplier Device Package:

64-TQFP (10x10)

Base Product Number:

ADS1675

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

4 (72 Hours)

ECCN:

3A991C4



## 4MSPS, 24-Bit Analog-to-Digital Converter

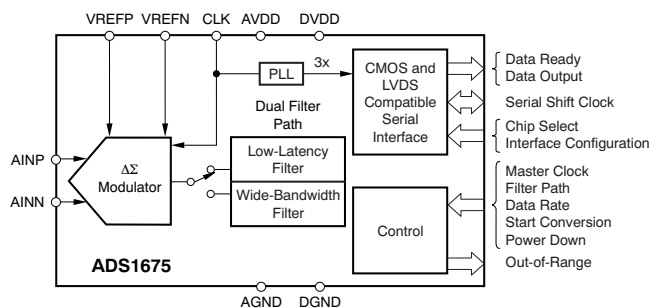
Check for Samples: [ADS1675](#)

### FEATURES

- **AC Performance:**
  - 103dB of Dynamic Range at 4MSPS
  - 111dB of Dynamic Range at 125kSPS
  - 107dB THD
- **DC Accuracy:**
  - 3ppm INL
  - 4 $\mu$ V/°C Offset Drift
  - 4ppm/°C Gain Drift
- **Programmable Digital Filter with User-Selectable Path:**
  - **Low-Latency: Completely settles in 2.65 $\mu$ s**
  - **Wide-Bandwidth: 1.7MHz BW with flat passband**
- **Flexible Read-Only Serial Interface:**
  - Standard CMOS
  - Serialized LVDS
- **Easy Conversion Control with START Pin**
- **Out-of-Range Detection**
- **Supply: Analog +5V, Digital +3V**
- **Power: 575mW**

### APPLICATIONS

- **Automated Test Equipment**
- **Medical Imaging**
- **Scientific Instrumentation**
- **Test and Measurement**



### DESCRIPTION

The ADS1675 is a high-speed, high-precision analog-to-digital converter (ADC). Using an advanced delta-sigma ( $\Delta\Sigma$ ) architecture, it operates at speeds up to 4MSPS with outstanding ac performance and dc accuracy.

The ADS1675 ADC is comprised of a low-drift modulator with out-of-range detection and a dual-path programmable digital filter. The dual filter path allows the user to select between two post-processing filters: Low-Latency or Wide-Bandwidth. The Low-Latency filter settles quickly (as fast as 2.65 $\mu$ s) for applications with large instantaneous changes, such as a multiplexer. The Wide-Bandwidth path provides an optimized frequency response for ac measurements with a passband ripple of less than  $\pm 0.00002$ dB, stop band attenuation of 86dB, and a bandwidth of 1.7MHz.

The device offers two speed modes with distinct interface, resolution, and feature set. In the high-speed mode the device can be set to operate at either 4MSPS or 2MSPS. In the low-speed mode, it can be set to operate at either 1MSPS, 500KSPS, 250KSPS or 125KSPS.

The ADS1675 is controlled through I/O pins—there are no registers to program. A dedicated START pin allows for direct control of conversions: toggle the START pin to begin a conversion, and then retrieve the output data. The flexible serial interface supports data readback with either standard CMOS and LVDS logic levels, allowing the ADS1675 to directly connect to a wide range of microcontrollers, digital signal processors (DSPs), or field-programmable grid arrays (FPGAs).

The ADS1675 operates from an analog supply of 5V and digital supply of 3V, and dissipates 575mW of power. When not in use, the PDWN pin can be used to power down all device circuitry. The device is fully specified over the industrial temperature range and is offered in a TQFP-64 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [ti.com](http://ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		ADS1675	UNIT
AVDD to AGND		-0.3 to +5.5	V
DVDD to DGND		-0.3 to +3.6	V
AGND to DGND		-0.3 to +0.3	V
Input current	Momentary	100	mA
	Continuous	10	mA
Analog I/O to AGND		-0.3 to AVDD +0.3	V
Digital I/O to DGND		-0.3 to DVDD +0.3	V
Maximum junction temperature		+150	°C
Operating temperature range		-40 to +85	°C
Storage temperature range		-60 to +150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## ELECTRICAL CHARACTERISTICS

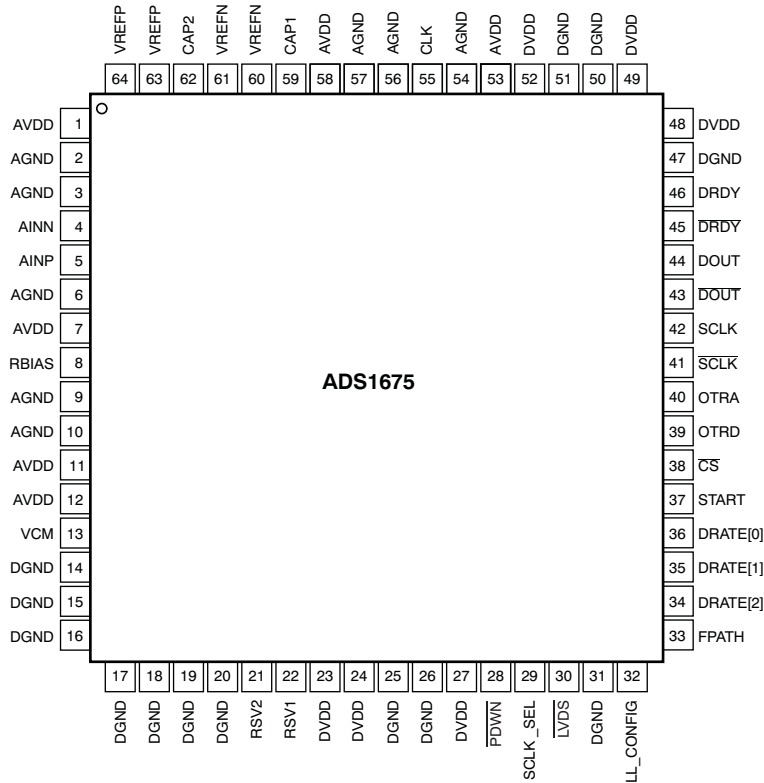
All specifications are at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $AVDD = 5\text{V}$ ,  $DVDD = 3\text{V}$ ,  $f_{\text{CLK}} = 32\text{MHz}$ ,  $V_{\text{REF}} = +3\text{V}$ , and  $R_{\text{BIAS}} = 7.5\text{k}\Omega$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1675			UNIT
		MIN	TYP	MAX	
<b>ANALOG INPUTS</b>					
Full-scale input voltage	$V_{\text{IN}} = (\text{AINP} - \text{AINN})$		$\pm V_{\text{REF}}$		V
Common-mode input voltage	$V_{\text{CM}} = (\text{AINP} + \text{AINN})/2$		2.5		V
<b>AC PERFORMANCE</b>					
Data rate ( $f_{\text{DATA}}$ )		See <a href="#">Table 1</a>			kSPS
Dynamic range	Inputs shorted together, Low-Latency path, $f_{\text{DATA}} = 4\text{MSPS}$	100	103		dB
	Inputs shorted together, Low-Latency path, $f_{\text{DATA}} = 2\text{MSPS}$	100.5	103.5		
	Inputs shorted together, Low-Latency path, $f_{\text{DATA}} = 125\text{kSPS}$	108	111		
Signal-to-noise ratio (SNR)	$f_{\text{IN}} = 10\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 4\text{MSPS}$		92		dB
	$f_{\text{IN}} = 10\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 2\text{MSPS}$		97		
	$f_{\text{IN}} = 1\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 125\text{kSPS}$		107		
Total harmonic distortion (THD)	$f_{\text{IN}} = 10\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 4\text{MSPS}$		-103		dB
	$f_{\text{IN}} = 10\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 2\text{MSPS}$		-103		
	$f_{\text{IN}} = 1\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 125\text{kSPS}$		-107		
Spurious-free dynamic range (SFDR)	$f_{\text{IN}} = 1\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 4\text{MSPS}$ , signal harmonics excluded		120		dB
	$f_{\text{IN}} = 10\text{kHz}$ , $-0.5\text{dBFS}$ , Wide-Bandwidth path, $f_{\text{DATA}} = 4\text{MSPS}$ , signal harmonics excluded		120		
<b>DC PRECISION</b>					
Resolution	Low-speed mode (DRATE = 000 to 011)	24			Bits
	High-speed mode (DRATE = 100, 101)	23			Bits
Differential nonlinearity	Low-speed mode (DRATE = 000 to 011)		24 (monotonic)		Bits
	High-speed mode (DRATE = 100, 101)		23 (monotonic)		Bits
Integral nonlinearity			3	15	ppm of FSR
Offset error	$T_A = +25^\circ\text{C}$	-5		5	mV
Offset error drift			4		$\mu\text{V}/^\circ\text{C}$
Gain error	$T_A = +25^\circ\text{C}$			1	%
Gain error drift			4		ppm/ $^\circ\text{C}$
Noise		See <a href="#">Noise Performance</a> table ( <a href="#">Table 1</a> )			
Common-mode rejection	At dc		71		dB
<b>DIGITAL FILTER CHARACTERISTICS (WIDE-BANDWIDTH PATH)</b>					
Passband		0		$0.424f_{\text{DATA}}$	Hz
Passband ripple				$\pm 0.00002\text{dB}$	dB
Passband transition	-0.1dB attenuation		$0.432f_{\text{DATA}}$		Hz
	-3dB attenuation		$0.488f_{\text{DATA}}$		Hz
Stop band		$0.576f_{\text{DATA}}$	$f_{\text{CLK}} - 0.576f_{\text{DATA}}$		Hz
Stop band attenuation			86		dB
Group delay			28		$t_{\text{DRDY}}$
Settling time		See the <a href="#">Wide-Bandwidth Filter</a> section			

## ELECTRICAL CHARACTERISTICS (continued)

All specifications are at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $AVDD = 5\text{V}$ ,  $DVDD = 3\text{V}$ ,  $f_{\text{CLK}} = 32\text{MHz}$ ,  $V_{\text{REF}} = +3\text{V}$ , and  $R_{\text{BIAS}} = 7.5\text{k}\Omega$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1675			UNIT
		MIN	TYP	MAX	
<b>DIGITAL FILTER CHARACTERISTICS (LOW-LATENCY PATH)</b>					
Bandwidth	-3dB attenuation	See the <a href="#">Low-Latency Filter</a> section			
Settling time	Complete settling	See <a href="#">Table 5</a>			
<b>VOLTAGE REFERENCE INPUTS</b>					
Reference input voltage ( $V_{\text{REF}}$ )	$V_{\text{REF}} = (V_{\text{REFP}} - V_{\text{REFN}})$	2.75	3.0	3.5	V
$V_{\text{REFP}}$		2.75	3.0	3.5	V
$V_{\text{REFN}}$			Short to AGND		V
<b>CLOCK (CLK)</b>					
$V_{\text{IH}}$		0.7AVDD		AVDD	V
$V_{\text{IL}}$		AGND		0.3AVDD	V
<b>DIGITAL INPUTS</b>					
$V_{\text{IH}}$		0.7DVDD		DVDD	V
$V_{\text{IL}}$		DGND		0.3DVDD	V
Input leakage	$DGND < V_{\text{IN}} < DVDD$			$\pm 10$	$\mu\text{A}$
<b>CMOS OUTPUTS</b>					
$V_{\text{OH}}$	$I_{\text{OH}} = -2\text{mA}$	0.8DVDD			V
$V_{\text{OL}}$	$I_{\text{OL}} = 2\text{mA}$			0.2DVDD	V
<b>LVDS OUTPUTS</b>					
$ V_{\text{OD(SS)}} $	Steady-state differential output voltage magnitude		340		mV
$\Delta V_{\text{OD(SS)}} $	Change in steady-state differential output voltage magnitude between logic states		$\pm 50$		mV
$V_{\text{OC(SS)}}$	Steady-state common-mode voltage output		1.2		V
$\Delta V_{\text{OC(SS)}} $	Change in steady-state common-mode output voltage between logic states		$\pm 50$		mV
$V_{\text{OC(pp)}}$	Peak-to-peak change in common-mode output voltage		50	150	mV
Short-circuit output current ( $I_{\text{OS}}$ )	$V_{\text{OY}} \text{ or } V_{\text{OZ}} = 0\text{V}$		3		mA
	$V_{\text{OD}} = 0\text{V}$		3		mA
High-impedance output current ( $I_{\text{OZ}}$ )	$V_{\text{O}} = 0\text{V} \text{ or } +DVDD$		$\pm 5$		$\mu\text{A}$
Load				5	pF
<b>POWER-SUPPLY REQUIREMENTS</b>					
AVDD		4.75	5.0	5.25	V
DVDD		2.85	3.0	3.15	V
AVDD current			70	74	mA
DVDD current	CMOS outputs, $DVDD = 3\text{V}$ , $DRATE = 011$		53	59	mA
	LVDS outputs, $DVDD = 3\text{V}$ , $DRATE = 101$		70	74	mA
Power dissipation	CMOS outputs, $DRATE = 011$ , $AVDD = 5\text{V}$ , $DVDD = 3\text{V}$		510	545	mW
	LVDS outputs, $DRATE = 101$ , $AVDD = 5\text{V}$ , $DVDD = 3\text{V}$		575	600	mW
	Power-down		5		mW

**DEVICE INFORMATION**
**TQFP PACKAGE  
TQFP-64  
(TOP VIEW)**

**TERMINAL FUNCTIONS**

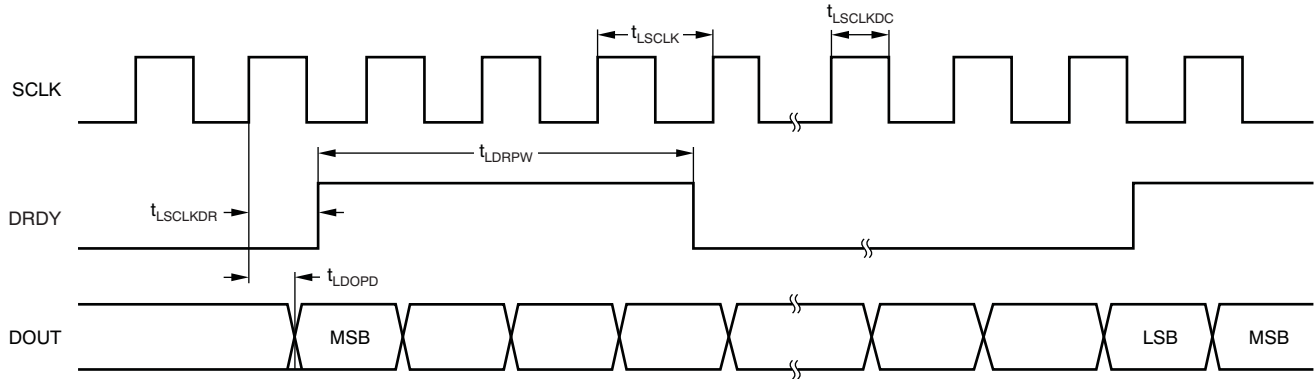
PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AVDD	1, 7, 11, 12, 53, 58	Analog	Analog supply
AGND	2, 3, 6, 9, 10, 54, 56, 57	Analog	Analog ground
AINN	4	Analog input	Negative analog input
AINP	5	Analog input	Positive analog input
RBIAS	8	Analog	Analog bias setting resistor
VCM	13	Analog	Terminal for external bypass capacitor connection to internal common-mode voltage
DGND	14-20, 25, 26, 31, 47, 50, 51	Digital	Digital ground
RSV2	21	Reserved	Short pin to digital ground
RSV1	22	Reserved	Short pin to digital supply
DVDD	23, 24, 27, 48, 49, 52	Digital	Digital supply
$\overline{\text{PDWN}}$	28	Digital input	Power-down control, active low
SCLK_SEL	29	Digital input	Shift-clock source select. <sup>(1)</sup> If SCLK_SEL = '0', then SCLK is internally generated. If SCLK_SEL = '1', then SCLK must be externally generated.
$\overline{\text{LVDS}}$	30	Digital input	Serial interface select. <sup>(1)</sup> If LVDS = '0', then interface is LVDS-compatible. If LVDS = '1', then interface is CMOS-compatible.

(1) Option not available in high-speed mode.

**TERMINAL FUNCTIONS (continued)**

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
LL_CONFIG	32	Digital input	Configure Low-Latency digital filter. <sup>(1)</sup> If LL_CONFIG = '0', then single-cycle settling is selected. If LL_CONFIG = '1', then fast-response is selected.
FPATH	33	Digital input	Digital filter path selection. If FPATH = '0', then path is Wide-Bandwidth. If FPATH = '1', then path is Low-Latency.
DRATE[2:0]	34-36	Digital input	Data rate selection
START	37	Digital input	Start convert, reset, and synchronization control input
$\overline{\text{CS}}$	38	Digital input	Chip select; active low
OTRD	39	Digital output	Digital filter out-of-range indicator
OTRA	40	Digital input	Analog input out-of-range indicator
$\overline{\text{SCLK}}$	41	Digital output	Negative shift clock output. If SCLK_SEL = '0', then $\overline{\text{SCLK}}$ is the complementary shift clock output. If SCLK_SEL = '1', then $\overline{\text{SCLK}}$ always output is 3-state.
SCLK	42	Digital input/output	Positive shift clock output. If SCLK_SEL = '0', then SCLK is an output. If SCLK_SEL = '1', then SCLK is an input.
$\overline{\text{DOUT}}$	43	Digital output	Negative LVDS serial data output
DOUT	44	Digital output	Positive LVDS serial data output
$\overline{\text{DRDY}}$	45	Digital output	Negative data ready output
DRDY	46	Digital output	Positive data ready output
CLK	55	Digital input	Master clock input
CAP1	59	Analog	Terminal for 1 $\mu$ F external bypass capacitor
VREFN	60, 61	Analog	Negative reference voltage. Short to analog ground
CAP2	62	Analog	Terminal for 1 $\mu$ F external bypass capacitor
VREFP	63, 64	Analog	Positive reference voltage

**TIMING CHARACTERISTICS**



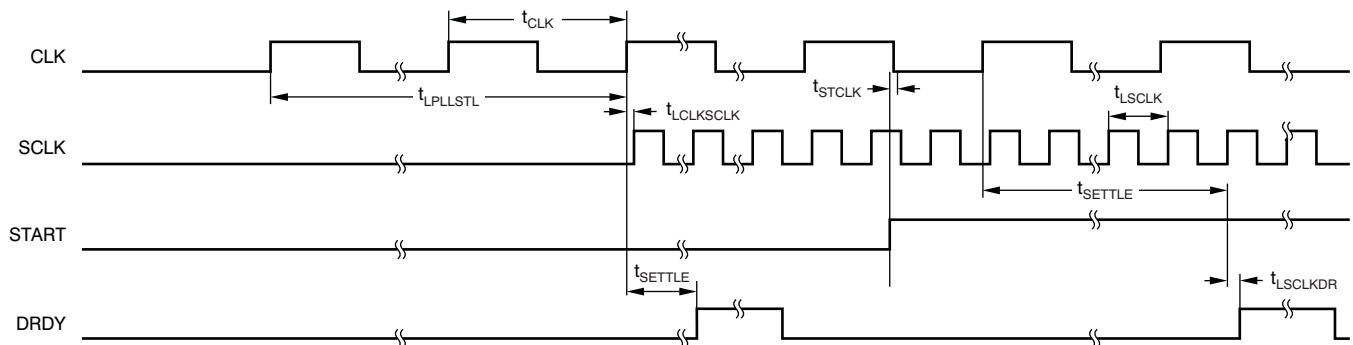
- (1) High-speed LVDS valid only for DRATE = 100 and DRATE = 101.
- (2) Timing shown is the single-end version of the LVDS signal pairs.

**Figure 1. High-Speed LVDS Data Retrieval Timing**

**TIMING REQUIREMENTS: High-Speed LVDS**

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , and  $DVDD = 2.85\text{V}$  to  $3.15\text{V}$ .

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{LDRPW}$	DRDY pulse width	2		4	$t_{LSCLKs}$
$t_{LSCLKDR}$	SCLK to DRDY delay	2		3	ns
$t_{LDOPD}$	Valid data delay time from serial shift clock	1.5		2.5	ns
$t_{LSCLK}$	Period of LVDS serial shift clock (SCLK)		0.33		$t_{CLKs}$
$t_{LSCLKDC}$	Shift clock duty cycle	47		53	%
$t_{CLK}$	CLK period ( $1/f_{CLK}$ )	31.25			ns
$t_{LCLKSCLK}$	Delay from rising edge of CLK to rising edge of SCLK	13		20	ns
$t_{PLLSTL}$	PLL settling time			80	$\mu\text{s}$
$t_{STCLK}$	Setup time, rising edge of START to falling edge of CLK	-3		3	ns
$t_{SETTLE}$	Digital filter settling time	See <a href="#">Table 5</a> and <a href="#">Table 6</a>			



**Figure 2. PLL Timing**

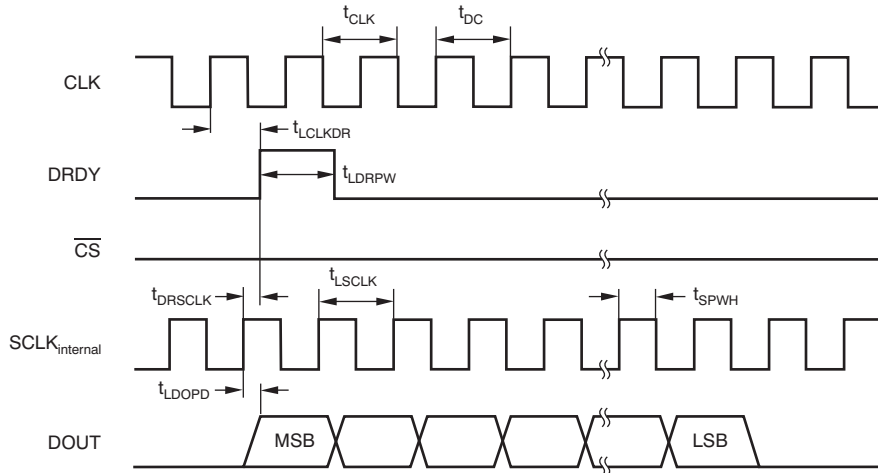
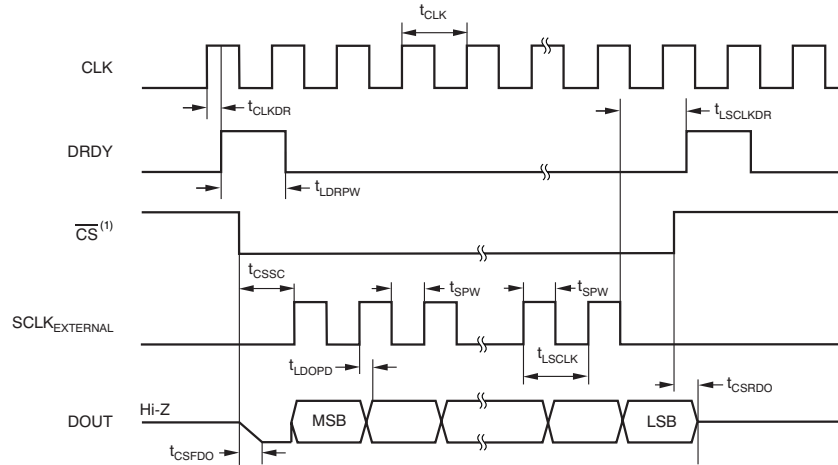


Figure 3. Low-Speed Mode Data Retrieval Timing with Internal SCLK (SCLK\_SEL = 0)

**TIMING REQUIREMENTS: Internal SCLK**

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , and  $DVDD = 2.85\text{V}$  to  $3.15\text{V}$ .

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{DC}$	CLK duty cycle	47	50	53	%
$t_{SPWH}$	SCLK pulse width high		15.6		ns
$t_{CLK}$	CLK period ( $1/f_{CLK}$ )	31.25			ns
$t_{CLKDR}$	CLK to DRDY delay	23		30	ns
$t_{LDRPW}$	DRDY pulse width		1		$t_{CLK}$
$t_{DRISCLK}$	Internal SCLK Rising to DRDY active edge	2.2		4.4	ns
$t_{LSCLK}$	Internally-generated SCLK rising edge to DRDY rising edge		1		$t_{CLK}$
$t_{LDOPD}$	Rising edge of SCLK to new valid data output (propagation delay)	1.9		2.8	ns



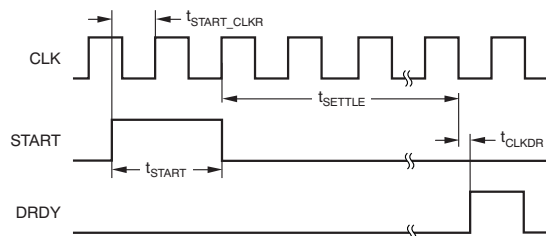
(3)  $\overline{CS}$  may be tied low.

**Figure 4. Low-Speed Mode Data Retrieval Timing with External SCLK (SCLK\_SEL = 1)**

### TIMING REQUIREMENTS: External SCLK

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , and  $DVDD = 2.85\text{V}$  to  $3.15\text{V}$ .

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{\text{CLK}}$	CLK period ( $1/f_{\text{CLK}}$ )	31.25			ns
$t_{\text{CLKDR}}$	CLK to DRDY delay	23		29	ns
$t_{\text{LDRPW}}$	DRDY pulse width		1		$t_{\text{CLK}}$
$t_{\text{CSSC}}$	$\overline{CS}$ active low to first Shift Clock (setup time)	5			ns
$t_{\text{LSCLK}}$	SCLK period ( $1/f_{\text{SCLK}}$ )	25			ns
$t_{\text{SPW}}$	SCLK high or low pulse width	12			ns
$t_{\text{LDOPD}}$	Rising edge of SCLK to new valid data output (propagation delay)	10.5		15	ns
$t_{\text{LSCLKDR}}$	Setup time of DRDY rising after SCLK falling edge	3			$t_{\text{CLK}}$
$t_{\text{CSRDO}}$	$\overline{CS}$ rising edge to DOUT 3-state		8		ns



**Figure 5. START Timing**

### TIMING REQUIREMENTS: START

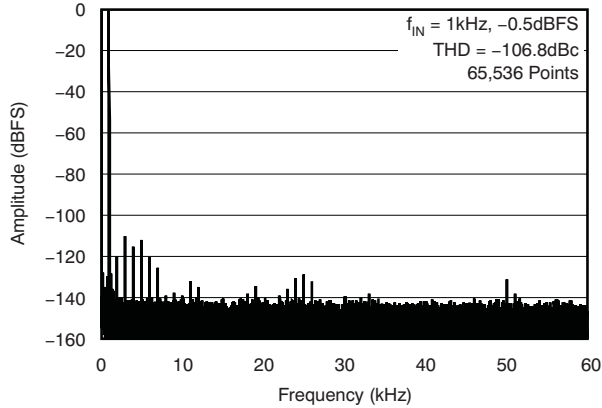
At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , and  $DVDD = 2.85\text{V}$  to  $3.15\text{V}$ .

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{\text{START\_CLKR}}$	Setup time, rising edge of START to rising edge of CLK	0.5			$t_{\text{CLK}}$
$t_{\text{START}}$	Start pulse width	2			$t_{\text{CLK}}$

**TYPICAL CHARACTERISTICS**

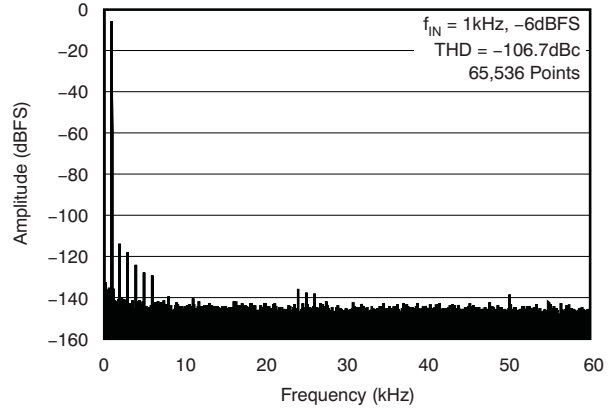
All specifications are at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AVDD = 5\text{V}$ ,  $DVDD = 3\text{V}$ ,  $f_{\text{CLK}} = 32\text{MHz}$ ,  $V_{\text{REF}} = +3\text{V}$ , and  $R_{\text{BIAS}} = 7.5\text{k}\Omega$ , unless otherwise noted.

**SPECTRAL RESPONSE  
(DRATE = 000, WB Filter)**



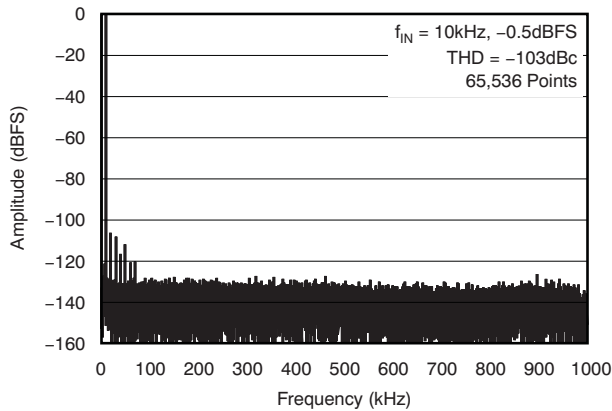
**Figure 6.**

**SPECTRAL RESPONSE  
(DRATE = 000, WB Filter)**



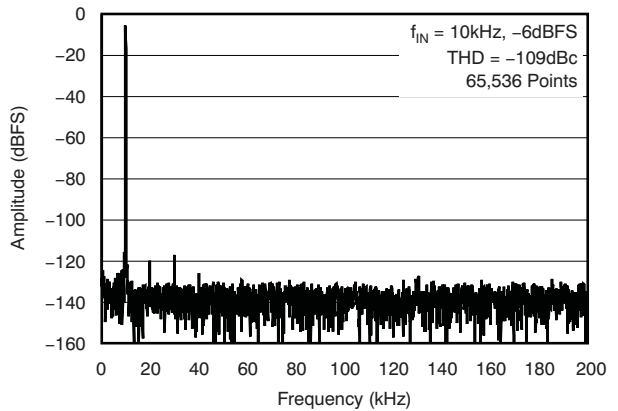
**Figure 7.**

**SPECTRAL RESPONSE  
(DRATE = 100, WB Filter)**



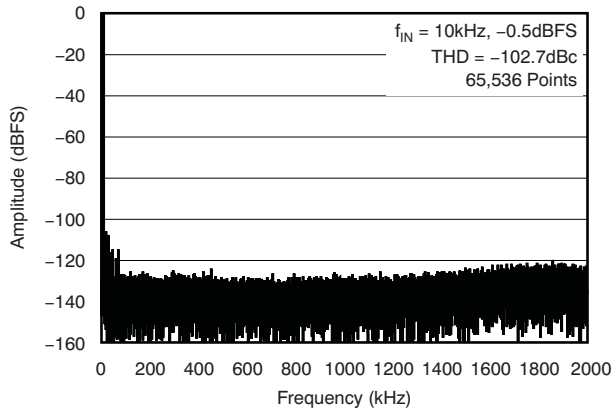
**Figure 8.**

**SPECTRAL RESPONSE  
(DRATE = 100, WB Filter)**



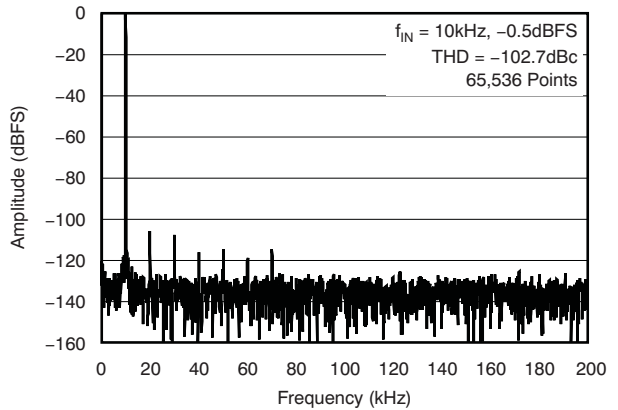
**Figure 9.**

**SPECTRAL RESPONSE  
(DRATE = 101, WB Filter)**



**Figure 10.**

**SPECTRAL RESPONSE  
(DRATE = 101, WB Filter, Detailed View)**



**Figure 11.**

**TYPICAL CHARACTERISTICS (continued)**

All specifications are at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AVDD = 5\text{V}$ ,  $DVDD = 3\text{V}$ ,  $f_{\text{CLK}} = 32\text{MHz}$ ,  $V_{\text{REF}} = +3\text{V}$ , and  $R_{\text{BIAS}} = 7.5\text{k}\Omega$ , unless otherwise noted.

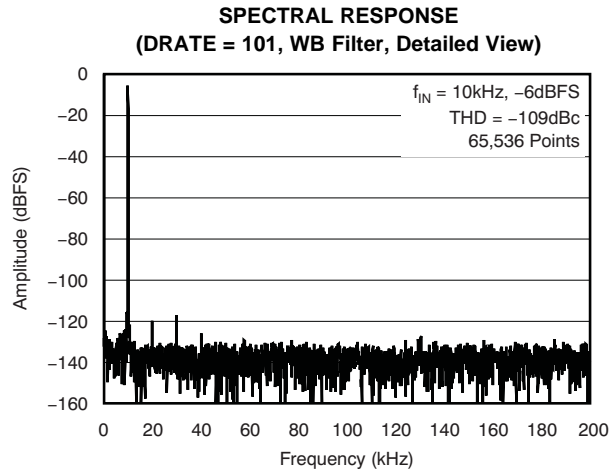


Figure 12.

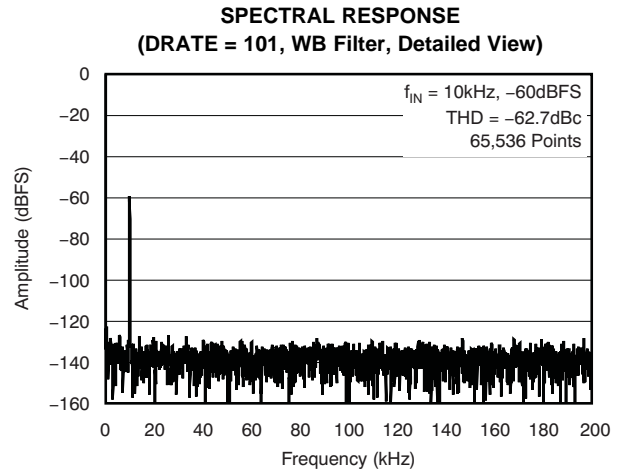


Figure 13.

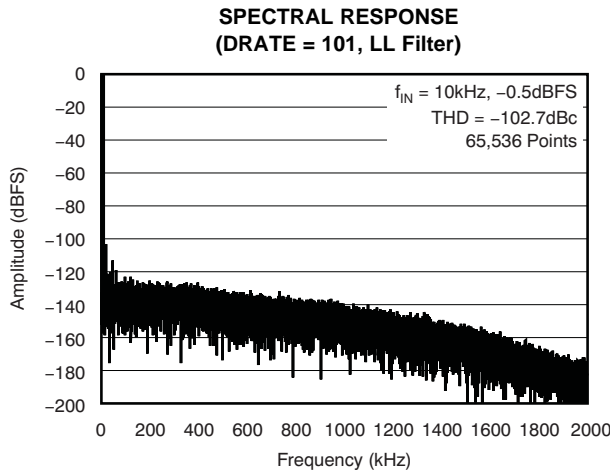


Figure 14.

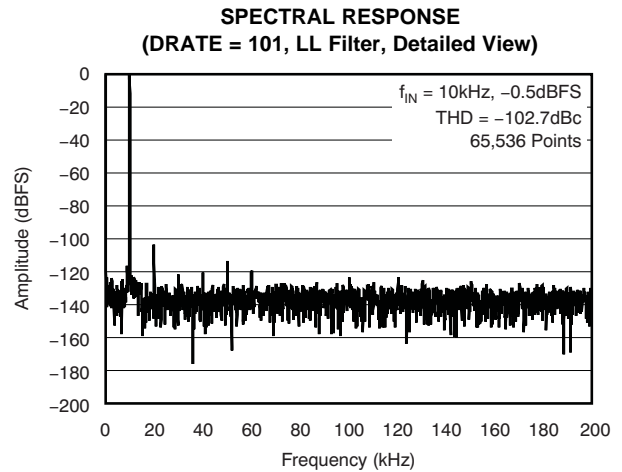


Figure 15.

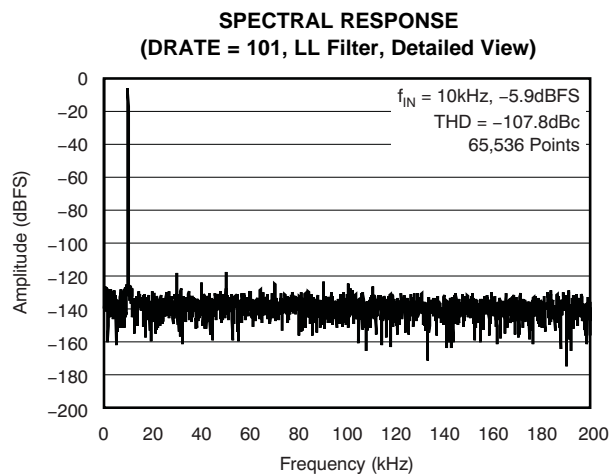


Figure 16.

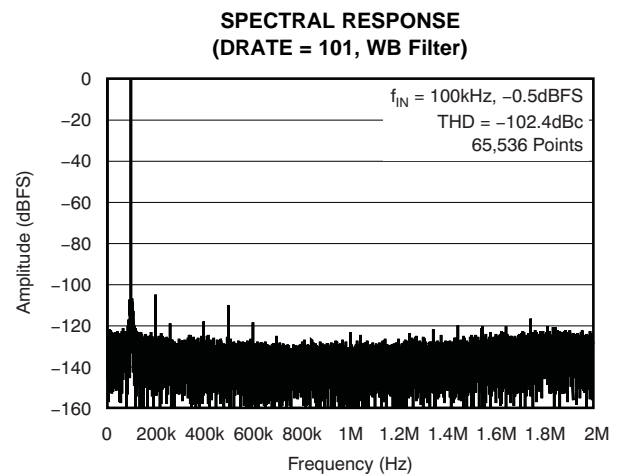
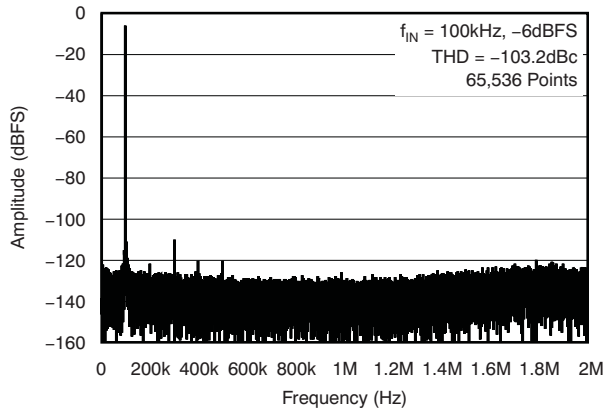


Figure 17.

**TYPICAL CHARACTERISTICS (continued)**

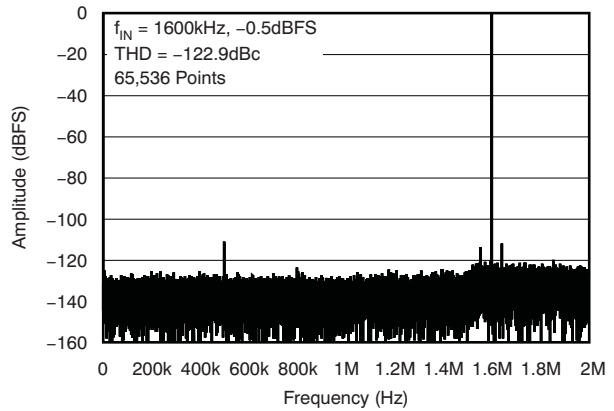
All specifications are at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AVDD = 5\text{V}$ ,  $DVDD = 3\text{V}$ ,  $f_{\text{CLK}} = 32\text{MHz}$ ,  $V_{\text{REF}} = +3\text{V}$ , and  $R_{\text{BIAS}} = 7.5\text{k}\Omega$ , unless otherwise noted.

**SPECTRAL RESPONSE  
(DRATE = 101, WB Filter)**



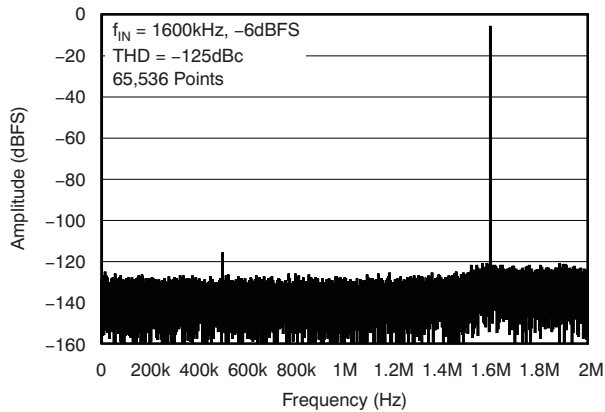
**Figure 18.**

**SPECTRAL RESPONSE  
(DRATE = 101, WB Filter)**



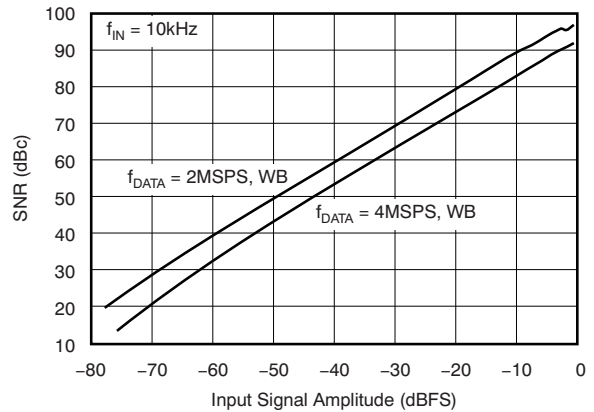
**Figure 19.**

**SPECTRAL RESPONSE  
(DRATE = 101, WB Filter)**



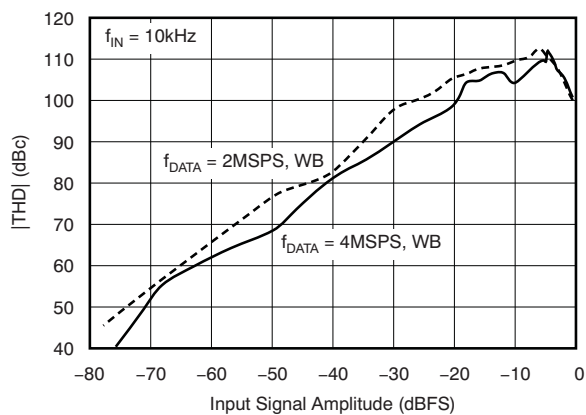
**Figure 20.**

**SIGNAL-TO-NOISE RATIO  
vs INPUT SIGNAL AMPLITUDE**



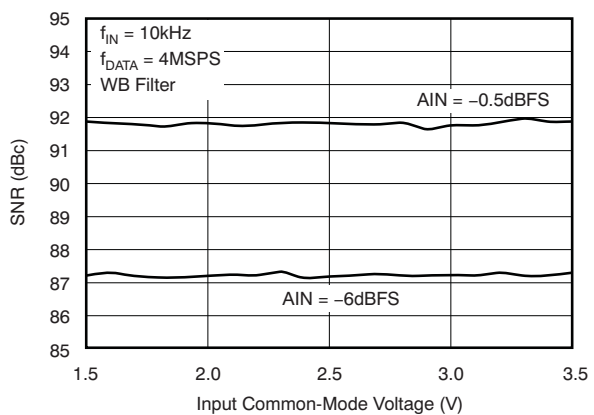
**Figure 21.**

**|TOTAL HARMONIC DISTORTION|  
vs INPUT SIGNAL AMPLITUDE**



**Figure 22.**

**SIGNAL-TO-NOISE RATIO  
vs INPUT COMMON-MODE VOLTAGE**



**Figure 23.**

**TYPICAL CHARACTERISTICS (continued)**

All specifications are at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AVDD = 5\text{V}$ ,  $DVDD = 3\text{V}$ ,  $f_{\text{CLK}} = 32\text{MHz}$ ,  $V_{\text{REF}} = +3\text{V}$ , and  $R_{\text{BIAS}} = 7.5\text{k}\Omega$ , unless otherwise noted.

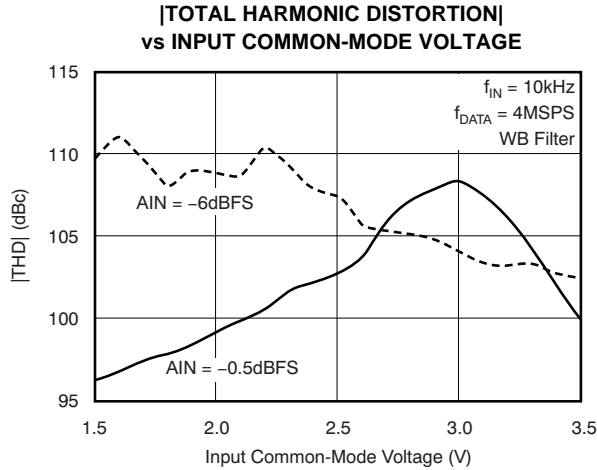


Figure 24.

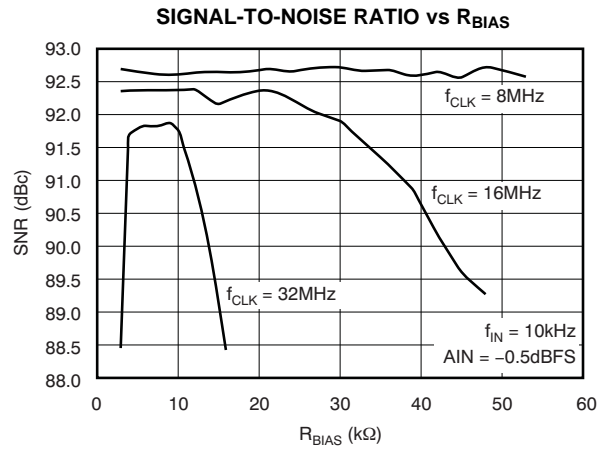


Figure 25.

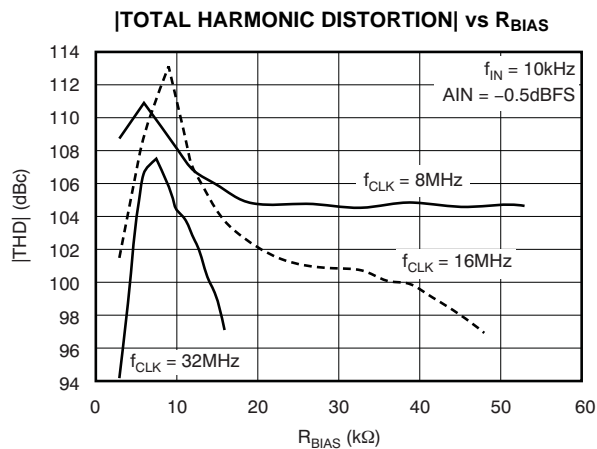


Figure 26.

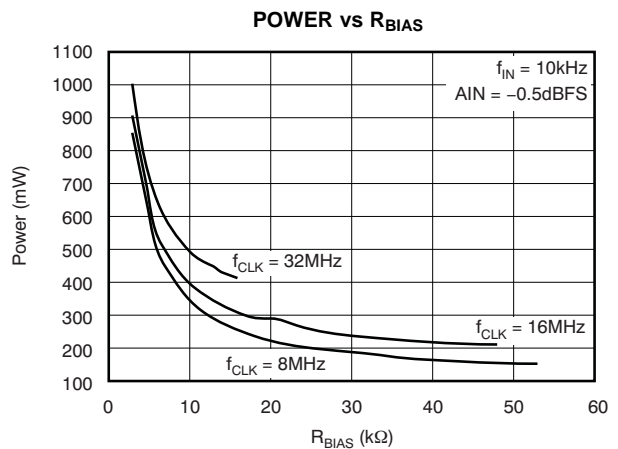


Figure 27.

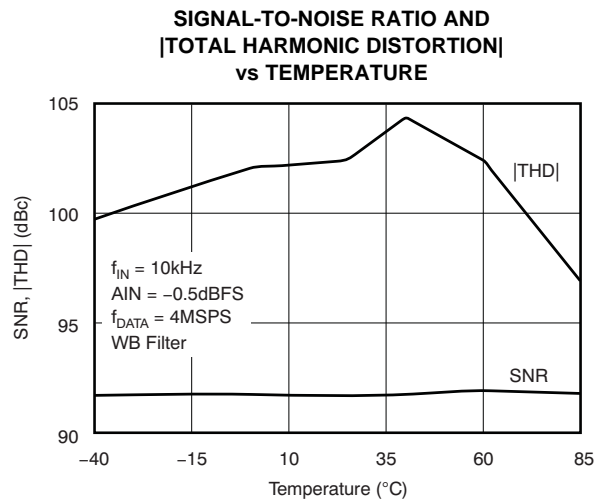


Figure 28.

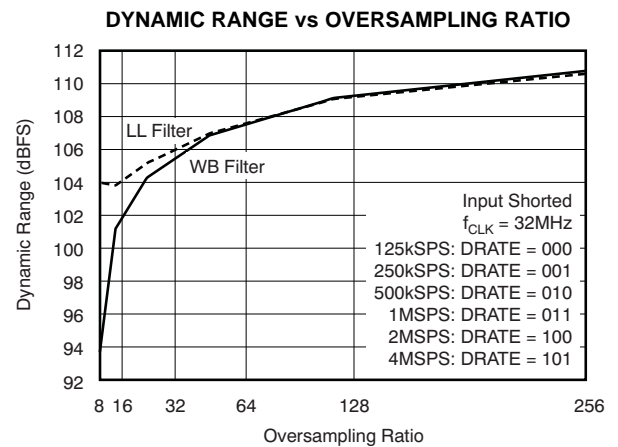


Figure 29.

**TYPICAL CHARACTERISTICS (continued)**

All specifications are at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AVDD = 5\text{V}$ ,  $DVDD = 3\text{V}$ ,  $f_{\text{CLK}} = 32\text{MHz}$ ,  $V_{\text{REF}} = +3\text{V}$ , and  $R_{\text{BIAS}} = 7.5\text{k}\Omega$ , unless otherwise noted.

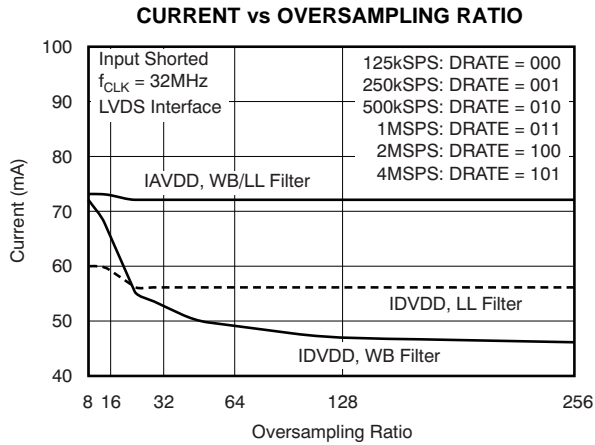


Figure 30.

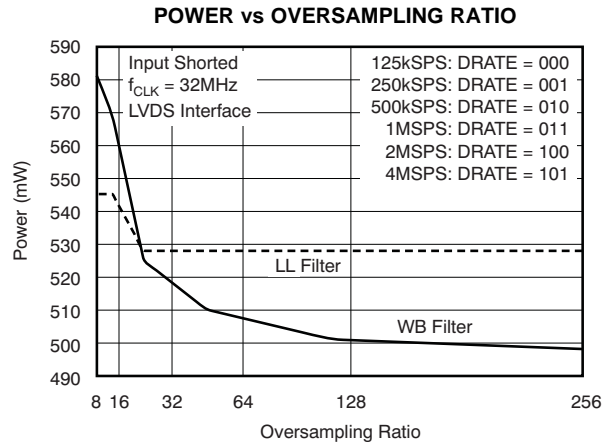


Figure 31.

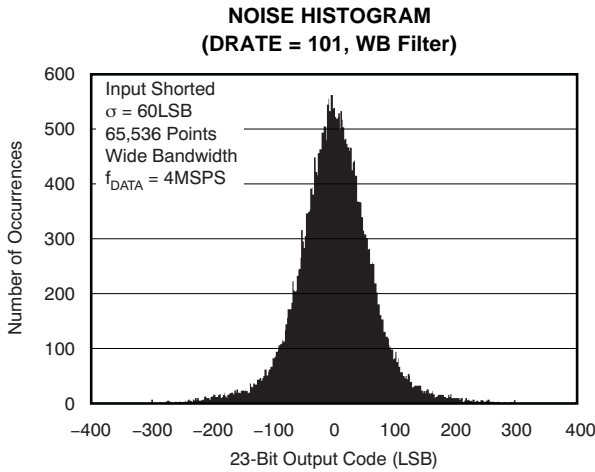


Figure 32.

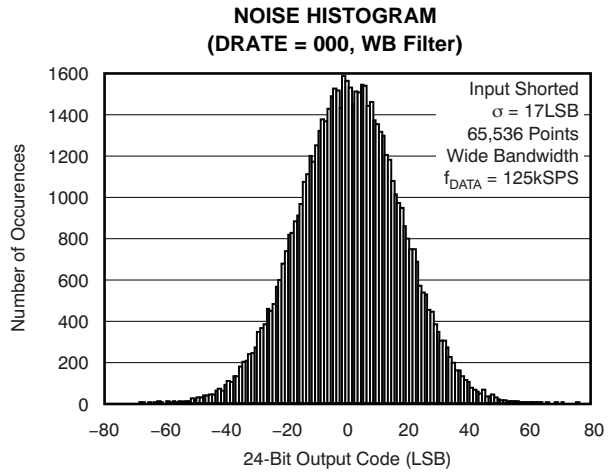


Figure 33.

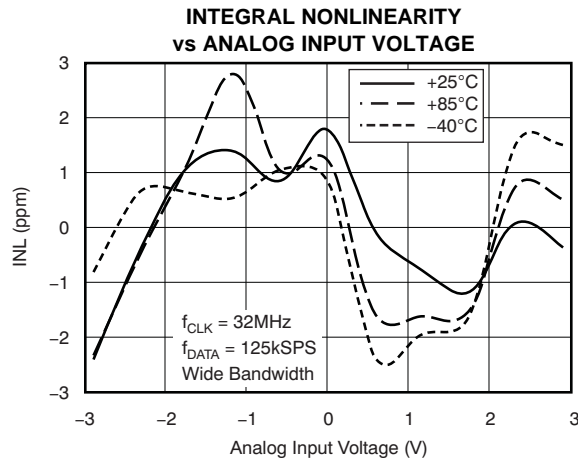


Figure 34.

## OVERVIEW

The ADS1675 is a 24-bit, delta-sigma ( $\Delta\Sigma$ ) analog-to-digital converter (ADC). It provides high-resolution measurements of both ac and dc signals and features an advanced, multi-stage analog modulator with a programmable and flexible digital decimation filter.

Figure 35 shows a block diagram of the ADS1675. The modulator measures the differential input signal  $V_{IN} = (AINP - AINN)$  against the differential reference  $V_{REF} = (VREFP - VREFN)$ . The digital filter receives the modulator signal and processes it through the user-selected path. The Low-Latency path settles quickly, and is ideal when using a multiplexer or when measuring large transients. The Wide-Bandwidth path provides outstanding frequency response with very low passband ripple, a steep transition band, and large stop band attenuation. This path is well-suited for applications that require high-resolution measurements of high-frequency ac signal content.

A dedicated START pin allows precise conversion control; toggle the pin to begin the conversion process. The ADS1675 is configured by setting the appropriate I/O pins—there are no registers to program. Data are retrieved over a serial interface that can support either CMOS or LVDS voltage levels. In addition, the standard CMOS serial interface can be internally or externally clocked. This flexibility allows direct connection to a wide range of digital hosts including DSPs, FPGAs, and microcontrollers. All data rates are available only using the LVDS mode interface.

A detection circuit monitors the conversions to indicate when the inputs are out-of-range for an extended duration. A power-down pin (PDWN) shuts off all circuitry when the ADS1675 is not in use.

The device offers two speed modes with distinct interfaces, resolution, and feature set. The high-speed mode is enabled by setting DRATE[2:0] to either 100 or 101. The rest of the DRATE configurations enable the low-speed mode.

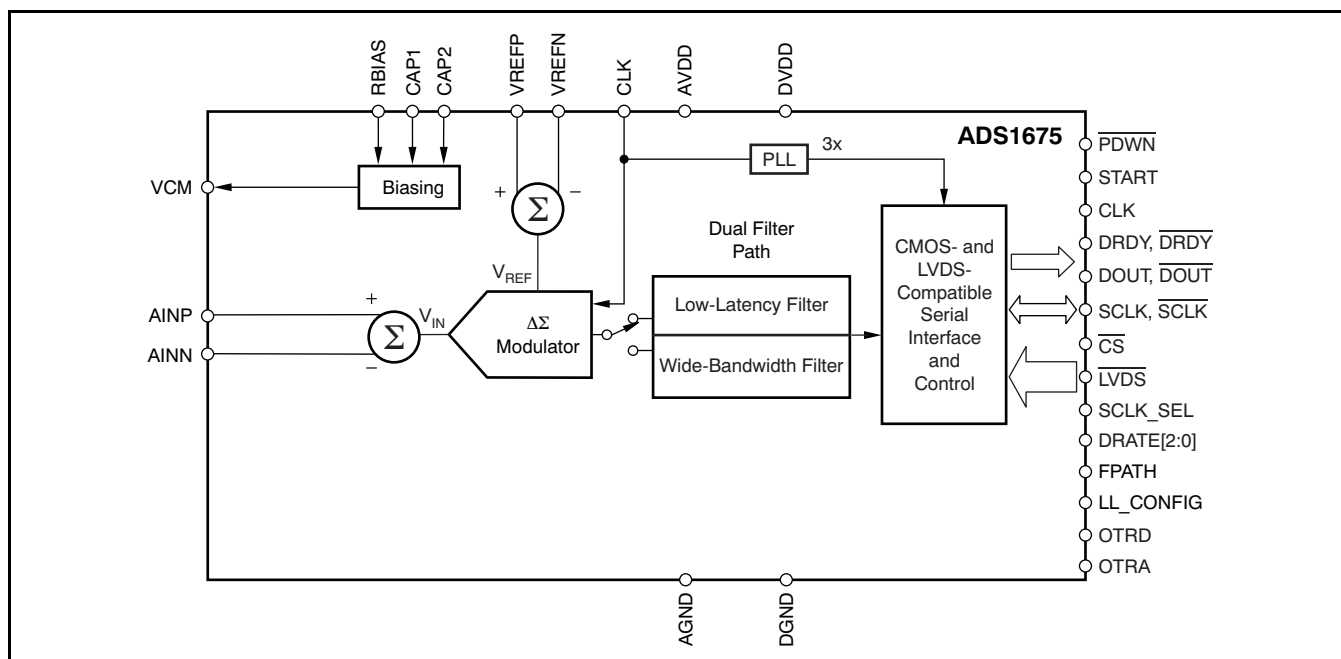


Figure 35. Block Diagram

## NOISE PERFORMANCE

The ADS1675 offers outstanding noise performance that can be optimized by adjusting the data rate. As the averaging is increased (thus reducing the data rate), the noise drops correspondingly. [Table 1](#) shows the noise as a function of data rate for both the Low-Latency and the Wide-Bandwidth filter paths under the conditions shown.

[Table 1](#) lists some of the more common methods of specifying noise. The dynamic range is the ratio of the root-mean-square (RMS) value of a full-scale sine wave to the RMS noise with the inputs shorted together. This value is expressed in decibels relative to full-scale (dBFS). The input-referred noise is the RMS value of the noise with the inputs shorted, referred to the input of the ADS1675. The effective number of bits (ENOB) is calculated from a dc perspective using the formula in [Equation 1](#), where full-scale range equals  $2V_{REF}$ .

$$ENOB = \frac{\ln \left[ \frac{\text{Full-scale range}}{\text{RMS noise}} \right]}{\ln(2)} \tag{1}$$

*Noise-free bits* specifies noise, again from a dc perspective using [Equation 1](#), with peak-to-peak noise substituted for RMS noise.

## ANALOG INPUTS (AINP, AINN)

The ADS1675 measures the differential signal,  $V_{IN} = (AINP - AINN)$ , against the differential reference,  $V_{REF} = (VREFP - VREFN)$ . The most positive measurable differential input is  $V_{REF}$ , which produces the most positive digital output code of 7FFFFFFh. Likewise, the most negative measurable differential input is  $-V_{REF}$ , which produces the most negative digital output code of 800000h.

Analog inputs must be driven with a differential signal to achieve optimum performance. The recommended common-mode voltage is 2.5V. The ADS1675 samples the analog inputs at very high speeds. It is critical that a suitable driver be used. See the [Application Information](#) section for recommended circuit designs.

**Table 1. Noise Performance<sup>(1)</sup>**

FILTER PATH		DATA RATE[2:0]	DATA RATE (kSPS)	DYNAMIC RANGE (dB)	INPUT-REFERRED NOISE ( $\mu V_{RMS}$ )	ENOB	NOISE-FREE BITS
Low-Latency (Fast Response Mode configuration)	Low-speed modes	000	125	111	6.30	19.86	17.14
		001	250	109	7.47	19.61	16.89
		010	500	107	9.51	19.27	16.54
		011	1000	105	11.72	18.97	16.24
	High-speed modes	100	2000	104	13.72	18.74	16.02
		101	4000	103	14.23	18.69	15.96
Wide-Bandwidth	Low-speed modes	000	125	111	6.17	19.89	17.17
		001	250	109	7.44	19.62	16.90
		010	500	107	9.66	19.25	16.52
		011	1000	104	12.99	18.82	16.09
	High-speed modes	100	2000	101	18.64	18.30	15.57
		101	4000	94	44.02	17.06	14.33

(1)  $V_{REF} = 3V, f_{CLK} = 32MHz$ .

## VOLTAGE REFERENCE INPUTS (VREFN, VREFP)

The voltage reference for the ADS1675 is the differential voltage between VREFP and VREFN:

$$V_{REF} = (VREFP - VREFN) \quad (2)$$

A high-quality reference voltage with the appropriate drive strength is essential for achieving the best performance from the ADS1675. Noise and drift on the reference degrade overall system performance. See the [Application Information](#) section for reference circuit examples.

It is recommended that a minimum 10 $\mu$ F and 0.1 $\mu$ F ceramic bypass capacitors be used directly across the reference inputs, VREFP and VREFN. These capacitors should be placed as close as possible to the device under test for optimal performance.

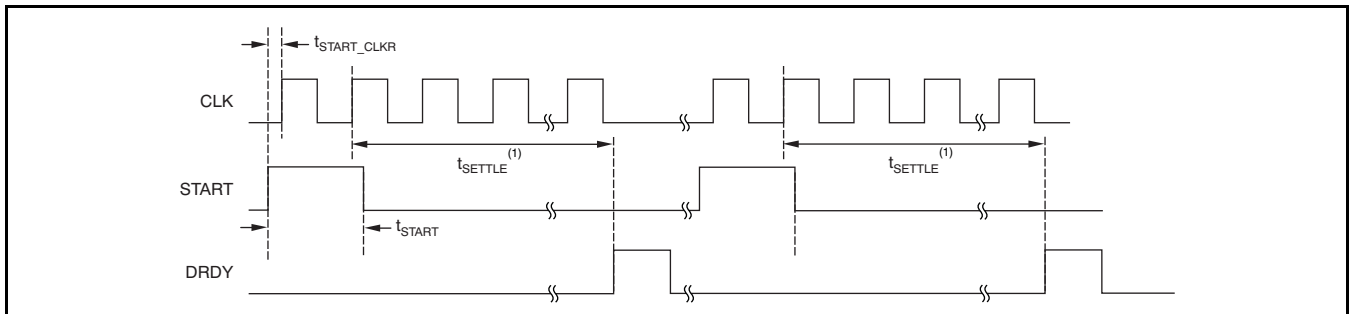
## COMMON-MODE VOLTAGE (VCM)

The VCM pin outputs a voltage of AVDD/2. This pin must be bypassed with a 1 $\mu$ F capacitor placed close to the package pin. The VCM pin connects an external capacitor to compensate the internal amplifier; it is not intended to drive an external load.

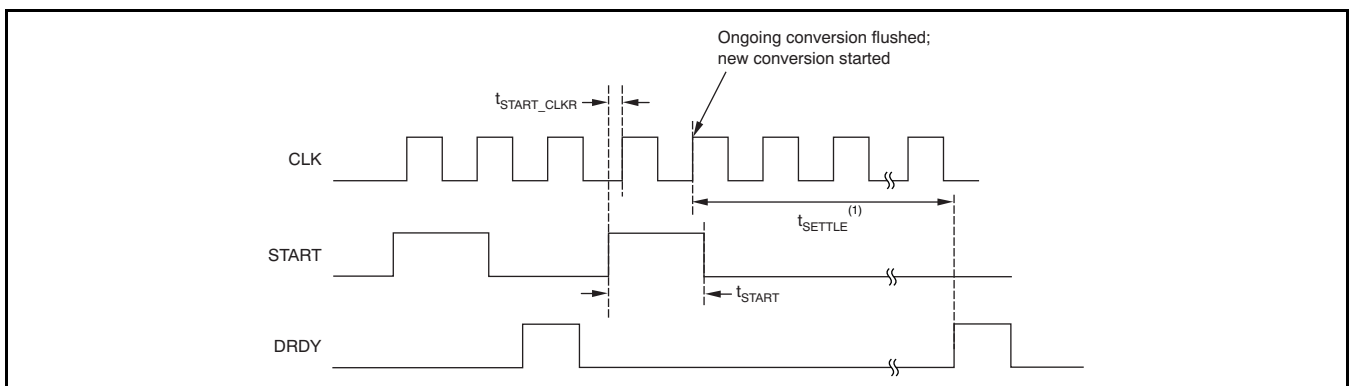
## CONVERSION START

The START pin provides an easy and precise conversion control. To perform a single conversion, pulse the START pin as shown in [Figure 36](#). The START signal is latched internally on the rising edge of CLK. Multiple conversions are performed by continuing to hold START high after the first conversion completes; see the digital filter descriptions for more details on multiple conversions, because the timing depends on the filter path selected.

A conversion can be interrupted by issuing another START pulse before the ongoing conversion completes. When an interruption occurs, the data for the ongoing conversion are flushed and a new conversion begins. DRDY indicates that data are ready for retrieval after the filter has settled, as shown in [Figure 37](#).



**Figure 36. START Pin Used for Single Conversions**



(1) See the [Low-Latency Filter](#) and [Wide-Bandwidth Filter](#) sections for specific values of settling time  $t_{SETTLE}$ .

**Figure 37. Example of Restarting a Conversion with START**

## DIGITAL FILTER

In  $\Delta\Sigma$  ADCs, the digital filter has a critical influence on device performance. The digital filter sets the frequency response, data rate, bandwidth, and settling time. Choosing to optimize some of these features in a filter means that compromises must be made with other specifications. These tradeoffs determine the applications for which the device is best suited.

The ADS1675 offers two digital filters on-chip, and allows the user to direct the output data from the modulator to either the Wide-Bandwidth or Low-Latency filter. These filters allow the user to use one converter design to address multiple applications. The Low-Latency path filter has minimal latency or settling time. This reduction is achieved by reducing the bandwidth of the filter. This path is ideal for measurements with large, quick changes on the inputs (for example, when using a multiplexer). The Low-Latency characteristic allows the user to cycle through the multiplexer at high speeds.

The other path provides a filter with excellent frequency response characteristics. The passband ripple is extremely small, the transition band is very steep, and there is large stop band attenuation. These characteristics are needed for high-resolution measurements of ac signals. The tradeoff here is that settling time increases; for signal processing, however, this increase is not generally a critical concern.

The FPATH digital input pin sets the filter path selection, as shown in Table 2. Note that the START pin must be strobed after a change to the filter path selection or data rate. If a conversion is in process during a filter path or data rate change, the output data are not valid and should be discarded.

**Table 2. ADS1675 Filter Path Selection**

FPATH PIN	SELECTED FILTER PATH
1	Low-Latency path
0	Wide-Bandwidth path

**Table 4. Low-Latency Data Rates with Single-Cycle Settling Configuration**

DRATE[2:0]	DATA RATE (kSPS)	SETTLING TIME, $t_{\text{SETTLE-LL}}$		-3dB BANDWIDTH (kHz) <sup>(1)</sup>
000	57.80	17.375 $\mu$ s	556 $t_{\text{CLK}}$	54
001	107.53	9.375 $\mu$ s	300 $t_{\text{CLK}}$	109
010	188.68	5.375 $\mu$ s	172 $t_{\text{CLK}}$	208
011	277.78	3.625 $\mu$ s	116 $t_{\text{CLK}}$	344

(1) The input signal aliases when its frequency exceeds  $f_{\text{DATA}}/2$ , in accordance with the Nyquist theorem.

## LOW-LATENCY DIGITAL FILTER

The Low-Latency (LL) filter provides a fast settling response targeted for applications that need high-precision measurements with minimal latency. A good example of this type of application is a multiplexer that measures multiple inputs. The faster the ADC settles, the faster the measurement can complete and the multiplexer can advance to the next input.

The ADS1675 LL filter supports two configurations to help optimize performance for these types of applications.

The LL\_CONFIG input pin selects the configuration, as shown in Table 3. Be sure to strobe the START pin after changing the configuration. If a conversion is in process during a configuration change, the output data for that conversion are not valid and should be discarded.

**Table 3. Low-Latency Pin Configurations**

LL_CONFIG PIN	LOW-LATENCY CONFIGURATION
0	Single-cycle settling
1	Fast response

The first configuration is *single-cycle settling*. As the name implies, this configuration allows for the filter to completely settle in one conversion cycle; there is no need to discard data. Each data output is comprised of information taken during only the previous conversion. The DRATE[2:0] digital input pins select the data rate for the Single-Cycle Settling configuration, as shown in Table 4. Note that the START pin must be strobed after a change to the data rate. If a conversion is in process during a data rate change, the output data for that conversion are not valid and should be discarded.

The second configuration is *fast response*. The DRATE[2:0] digital input pins select the data rate for the Fast Response Configuration, as shown in Table 5. When selected, this configuration provides a higher output data rate. The faster output data rate allows for more averaging by a post-processor within a given time interval to reduce noise. It also provides a faster indication of changes on the inputs when monitoring quickly-changing signals (for example, in a control loop application).

**Table 5. Low-Latency Data Rates with Fast-Response Configuration**

DRATE [2:0]	DATA RATE (kSPS)	SETTLING TIME, $t_{SETTLE-LL}$		-3dB BANDWIDTH (kHz)
000	125	17.375 $\mu$ s	556 $t_{CLK}$	54
001	250	9.375 $\mu$ s	300 $t_{CLK}$	109
010	500	5.375 $\mu$ s	172 $t_{CLK}$	208
011	1000	3.625 $\mu$ s	116 $t_{CLK}$	344
100	2000	2.76 $\mu$ s	265 $t_{LSCLK}$	350
101	4000	2.385 $\mu$ s	229 $t_{LSCLK}$	355

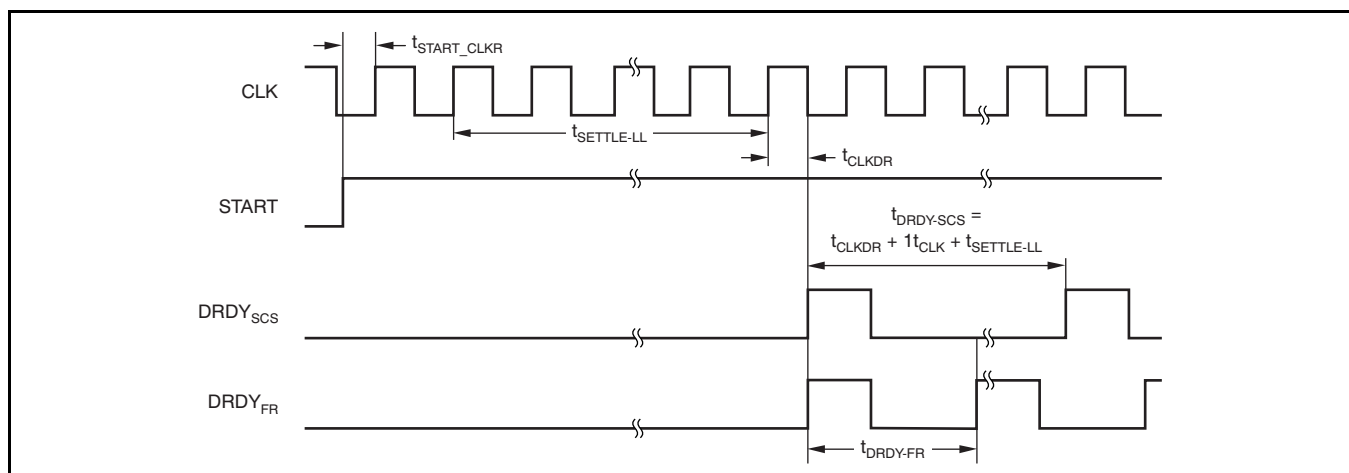
1. The input signal aliases when its frequency exceeds  $f_{DATA}/2$ , in accordance with the Nyquist theorem.
2. For high-speed mode, the first data are unsettled.

### Settling Time

The settling time in absolute time ( $\mu$ s) is the same for both configurations of the Low-Latency filter, as shown in Table 4 and Table 5. The difference between the configurations is seen with the timing of the conversions after the filter has settled from a pulse on the START pin.

Figure 38 illustrates the response of both configurations on approximately the same time scale in order to highlight the differences. With the single-cycle settling configuration, each conversion fully settles; in other words, the conversion period  $t_{DRDY-SCS} = t_{SETTLE-LL}$ . The benefit of this configuration is its simplicity—the ADS1675 functions similar to a successive-approximation register (SAR) converter and there is no need to consider discarding partially-settled data because each conversion is fully settled.

With the fast response configuration, the data rate for conversions after initial settling is faster; that is, the conversion time is less than the settling:  $t_{DRDY-FR} < t_{SETTLE-LL}$ . One benefit of this configuration is a faster response to changes on the inputs, because data are supplied at a faster rate. Another advantage is better support for post-processing. For example, if multiple readings are averaged to reduce noise, the higher data rate of the fast response configuration allows this averaging to happen in less time than it requires with the single-cycle settling filter. A third benefit is the ability to measure higher input frequencies without aliasing as a result of the higher data rate.



NOTE: DRDY<sub>SCS</sub> is the DRDY output with the Low-Latency single-cycle settling configuration. DRDY<sub>FR</sub> is the DRDY output with the Low-Latency fast-response settling configuration.

**Figure 38. Low-Latency Single-Cycle Settling and Fast-Response Configuration Conversion Timing**

It is important to note, however, that the absolute settling time of the Low-Latency path does not change when using the fast response configuration. Changes on the input signal during conversions after the initial settling require multiple cycles to fully settle. To help illustrate this requirement, consider a change on the inputs as shown in Figure 42, where START is assumed to have been taken high before the input voltage was changed.

The readings after a step change in the input is settled as shown in Figure 39 for all different data rates.

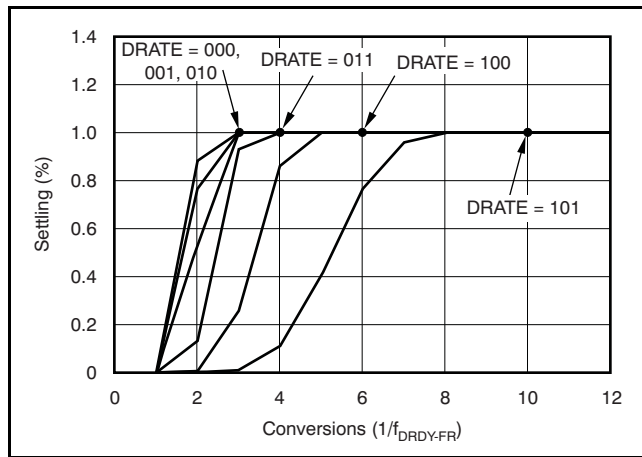


Figure 39. Step Response for Low-Latency Filter with Fast-Response Configuration

**Frequency Response**

Figure 40 shows the frequency response for the Low-Latency filter path normalized to the output data rate,  $f_{DATA}$ . The overall frequency response repeats at the modulator sampling rate, which is the same as the input clock frequency. Figure 41 shows the response with the fastest data rate selected (4 MSPS when  $f_{CLK} = 32\text{MHz}$ ).

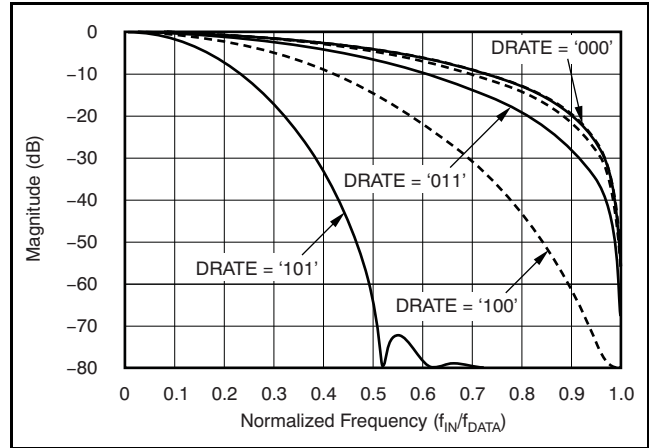


Figure 40. Frequency Response of Low-Latency Filter in Fast-Response Configuration

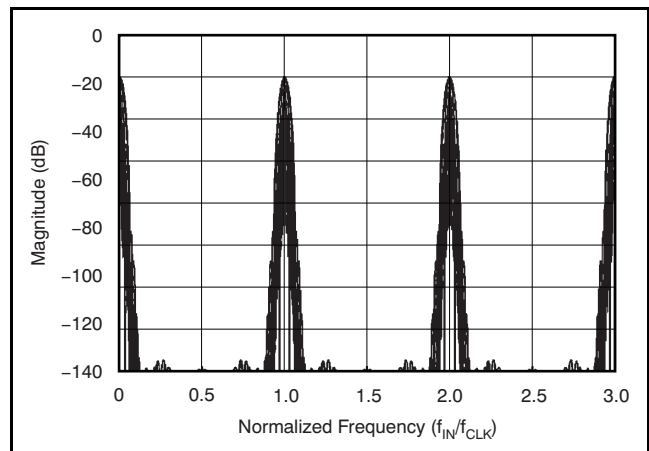
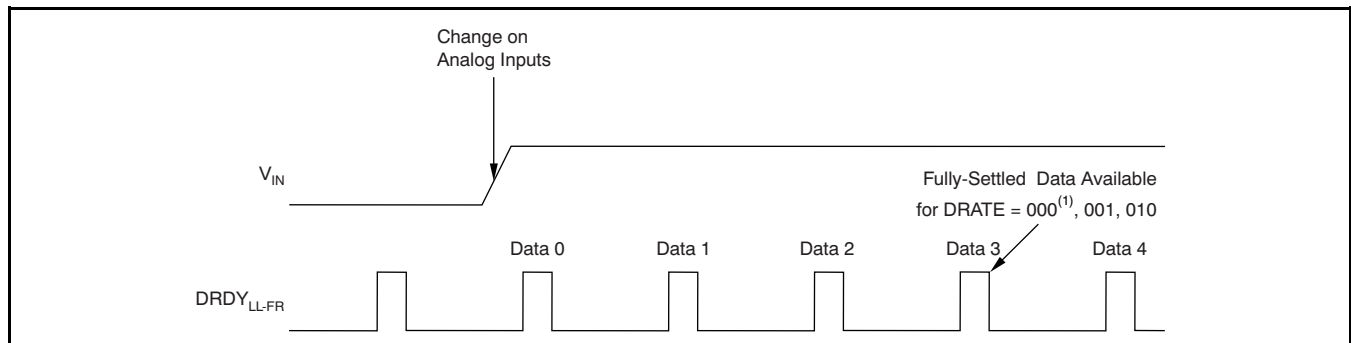


Figure 41. Extended Frequency Response of Low-Latency Path



NOTE: START pin held high previous to change on analog inputs.

(1) Refer to Figure 39 for other modes.

Figure 42. Settling Example with the Low-Latency Filter in Fast-Response Configuration

### Phase Response

The Low-Latency filter uses a multiple-stage, linear-phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (also known as *constant group delay*). This feature of linear phase filters means that the time delay from any instant of the input signal to the corresponding same instant of the output data is constant and independent of the input signal frequency. This behavior results in essentially zero phase error when measuring multi-tone signals.

### WIDE-BANDWIDTH FILTER

The Wide-Bandwidth (WB) filter is well-suited for measuring high-frequency ac signals. This digital filter offers excellent passband and stop band characteristics.

The DRATE[2:0] digital input pins select from the four data rates available with the WB filter, as shown in Table 6. Note that the START pin must be strobed after a change to the data rate. If a conversion is in process during a data rate change, the output data for that conversion are not valid and should be discarded.

While using the Wide-Bandwidth filter path, the LL\_CONFIG pin must be set to logic high. Setting LL\_CONFIG low forces the ADS1675 to switch to a low-latency filter path, overriding the FPATH pin.

Table 6. Wide-Bandwidth Data Rates

DRATE [2:0]	DATA RATE (kSPS)	SETTLING TIME, $t_{SETTLE-LL}$		-3dB BANDWIDTH (kHz)
000	125	439.44 $\mu$ s	14062 $t_{CLK}$	59.375
001	250	219.81 $\mu$ s	7074 $t_{CLK}$	118.75
010	500	110.00 $\mu$ s	3520 $t_{CLK}$	237.5
011	1000	55.04 $\mu$ s	1763 $t_{CLK}$	475
100	2000	27.52 $\mu$ s	2642 $t_{LSCLK}$	950
101	4000	13.79 $\mu$ s	1324 $t_{LSCLK}$	1900

- The input signal aliases when its frequency exceeds  $f_{DATA}/2$ , in accordance with the Nyquist theorem.

### Frequency Response

Figure 43 shows the frequency response for the Wide-Bandwidth filter path normalized to the output data rate,  $f_{DATA}$ . Figure 44 shows the passband ripple, and the transition from passband to stop band is illustrated in Figure 45. These three plots are valid for all of the data rates available on the ADS1675. Simply substitute the selected data rate to express the x-axis in absolute frequency.

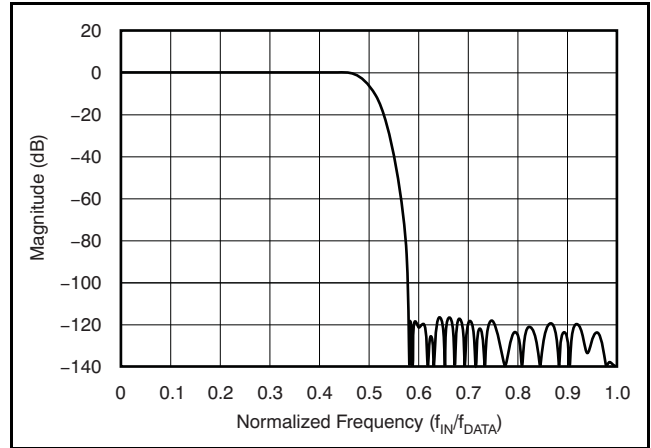


Figure 43. Frequency Response of Wide-Bandwidth Filter

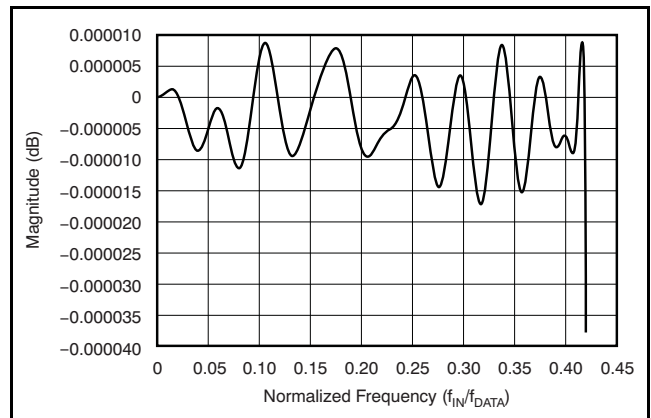


Figure 44. Passband Response for Wide-Bandwidth Filter

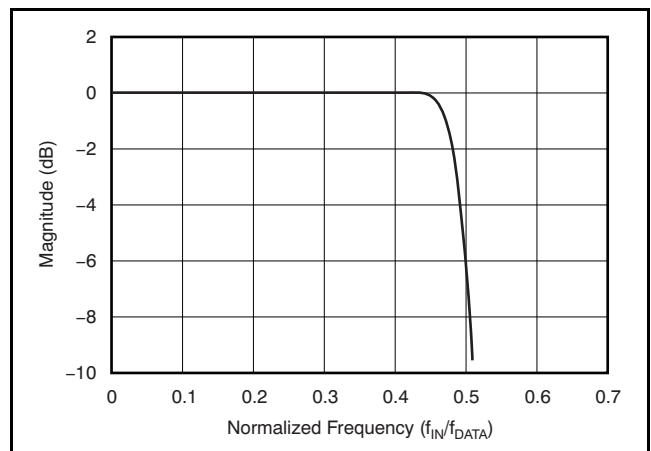


Figure 45. Transition Band Response for Wide-Bandwidth Filter

The overall frequency response repeats at the modulator sampling rate, which is the same as the input clock frequency. Figure 46 shows the response with the fastest data rate selected (4 MSPS when  $f_{CLK} = 32\text{MHz}$ ).

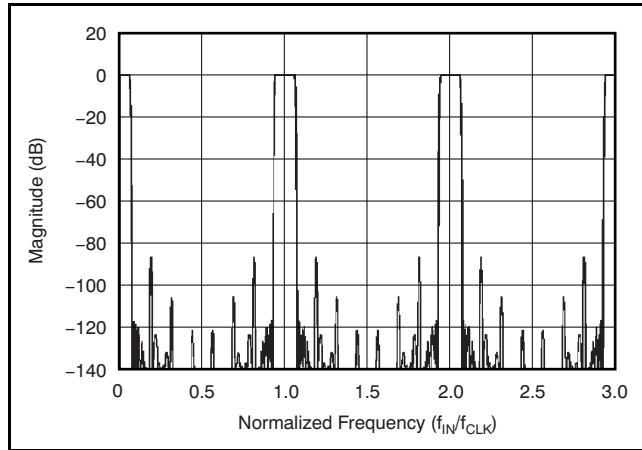


Figure 46. Extended Frequency Response of Wide-Bandwidth Path

### Phase Response

The Wide-Bandwidth filter uses a multiple-stage, linear-phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (also know as *constant group delay*). This feature means that the time delay from any instant of the input signal to the corresponding same instant of the output data is constant and independent of the input signal frequency. This behavior results in essentially zero phase error when measuring multi-tone signals.

### Settling Time

The Wide-Bandwidth filter fully settles before indicating data are ready for retrieval after the START pin is taken high, as shown in Figure 48. For this filter, the settling time is larger than the conversion time:  $t_{SETTLE-WB} > t_{DRDY-WB}$ . Instantaneous steps on the input require multiple conversions to settle if START is not pulsed. Figure 47 shows the settling response with the x-axis normalized to conversions or data-ready cycles. The output is fully settled after 55 data-ready cycles.

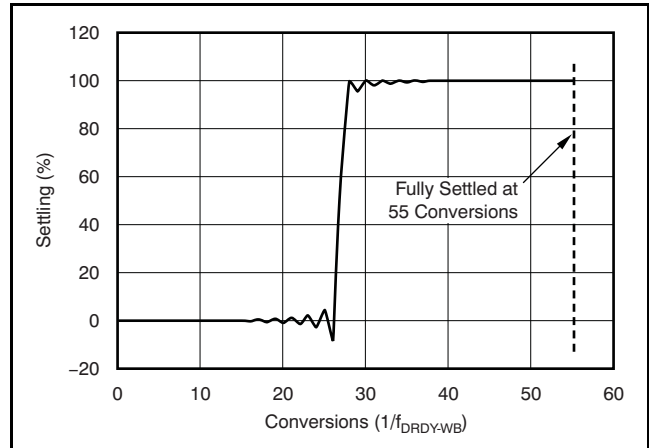
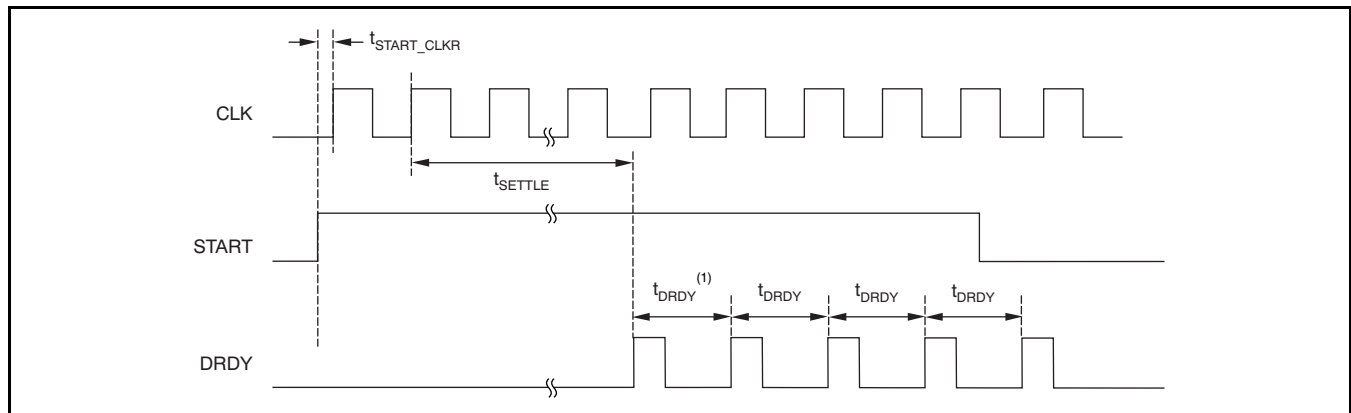


Figure 47. Step Response for Wide-Bandwidth Filter



(1)  $t_{DRDY} = 1/f_{DATA}$ . See Table 6 for the relationship between  $t_{SETTLE}$  and  $t_{DRDY}$  when using the Wide-Bandwidth filter.

Figure 48. START Pin Used for Multiple Conversions with Wide-Bandwidth Filter Path

## OTRA, OTRD FUNCTIONS

The ADS1675 provides two out-of-range pins (OTRD, OTRA) that can be used in feedback loops to set the dynamic range of the input signal.

The OTRA signal is triggered when the analog input to the modulator exceeds the positive or the negative full-scale range, as shown in Figure 49. This signal is triggered synchronous to CLK and returns low when the input becomes within range. The falling edge of OTRA is synchronized with the falling edge of DRDY. OTRA can be used in feedback loops to correct input over range conditions quicker instead of waiting for the digital filter to settle.

The OTRD function is triggered when the output code of the digital filter exceeds the positive or negative full-scale range. OTRD goes high on the rising edge of DRDY. When the digital output code returns within the full-scale range, OTRD returns low on the next rising edge of DRDY. OTRD can also be used when small out-of-range input glitches must be ignored.

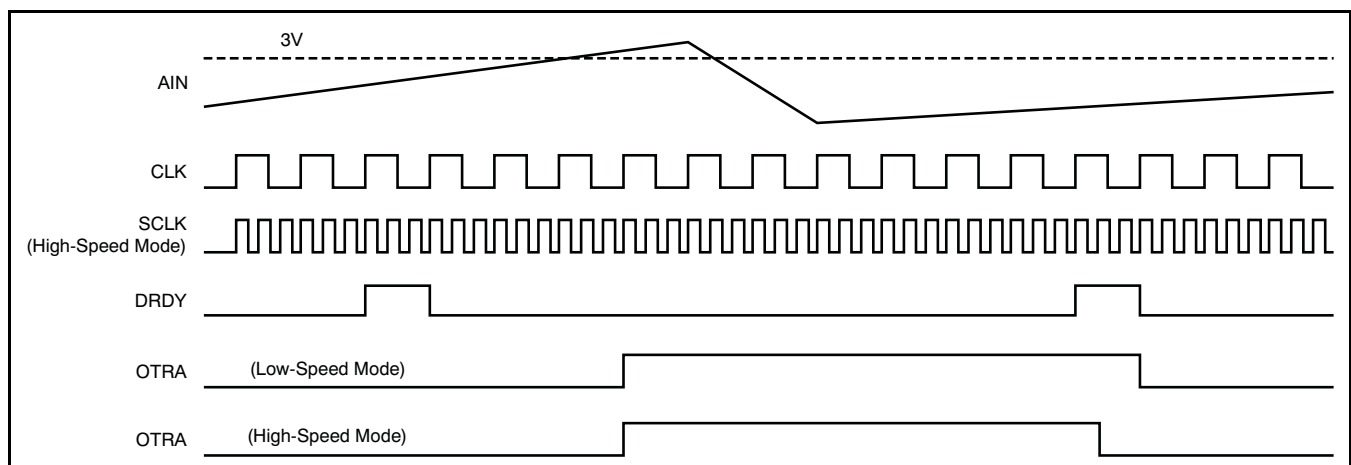
OTRA can be used in feedback loops to correct input over-range conditions quickly.

## SERIAL INTERFACE

The ADS1675 offers a flexible and easy-to-use, read-only serial interface designed to connect to a wide range of digital processors, including DSPs, microcontrollers, and FPGAs. In the low-speed modes (DRATE = 000 to 011) the ADS1675 serial interface can be configured to support either standard CMOS voltage swings or low-voltage differential swings (LVDS). In addition, when using standard CMOS voltage swings, SCLK can be internally or externally generated.

The high-speed modes (DRATE = 100, 101) are supported in high-speed LVDS interface mode only. The state of the LVDS pin and the SCLK\_SEL are ignored. In these two modes, an on-chip PLL is used to multiply the input clock (CLK) by three, to be used for the serial interface. This high-speed clock enables all 23-bit output data to be shifted out at the high data rate. The DRDY pulse in this case is three serial clocks wide. The on-chip PLL can lock to input clocks ranging from 8MHz to 32MHz. To conserve power, the PLL is enabled only in the high-speed modes. After power up as well as after the CLK signal is issued, if the CLK frequency is changed, and when switching from low-speed mode to high-speed mode, the PLL needs at least  $t_{LPLLSTL}$  to lock on and generate a proper LVDS serial shift clock. Switching among the high-speed modes does not require the user to wait for the PLL to lock. While the PLL is locking on, DOUT and SCLK are held low. After the PLL has locked on, the SCLK pin outputs a continuous clock that is three times the frequency of CLK. The device gives out a DRDY pulse (regardless of the status of the START signal) to indicate that the lock is complete. Disregard the data associated with this DRDY pulse. After this DRDY pulse, it is recommended that the user toggle the start signal before starting to capture data.

The ADS1675 is entirely controlled by pins; there are no registers to program. Connect the I/O pins to the appropriate level to set the desired function. Whenever changing the digital I/O pins that control the ADS1675, be sure to issue a START pulse immediately after the change in order to latch the new values.



**Figure 49. OTRA Signal Trigger**

## USING LVDS OUTPUT SWINGS

When the  $\overline{\text{LVDS}}$  pin is set to '0', the ADS1675 outputs are LVDS TIA/EIA-644A compliant. The data out, shift clock, and data ready signals are output on the differential pairs of pins  $\text{DOUT}/\overline{\text{DOUT}}$ ,  $\text{SCLK}/\overline{\text{SCLK}}$ , and  $\text{DRDY}/\overline{\text{DRDY}}$ , respectively. The voltage on the outputs is centered on 1.2V and swings approximately 350mV differentially. For more information on the LVDS interface, refer to the document *Low-Voltage Differential Signaling (LVDS) Design Notes* (literature number SLLA014) available for download at [www.ti.com](http://www.ti.com).

When using LVDS,  $\text{SCLK\_SEL}$  must be internally generated. The states of  $\text{SCLK\_SEL}$  pin is ignored. Do not leave these pins floating; they must be tied high or low.

## USING CMOS OUTPUT SWINGS

When the  $\overline{\text{LVDS}}$  pin is set to '1', the ADS1675 outputs are CMOS-compliant and swing from rail to rail. The data out and data ready signals are output on the differential pairs of pins  $\text{DOUT}/\overline{\text{DOUT}}$  and  $\text{DRDY}/\overline{\text{DRDY}}$ , respectively. Note that these are the same pins used to output LVDS signals when the  $\overline{\text{LVDS}}$  pin is set to '0'.  $\text{DOUT}$  and  $\overline{\text{DRDY}}$  are complementary outputs provided for convenience. When not in use, these pins should be left floating.

See the *Serial Shift Clock* section for a description of the SCLK and  $\overline{\text{SCLK}}$  pins.

## DATA OUTPUT ( $\text{DOUT}$ , $\overline{\text{DOUT}}$ )

Data are output serially from the ADS1675, MSB first, on the  $\text{DOUT}$  and  $\overline{\text{DOUT}}$  pins. When LVDS signal swings are used, these two pins act as a differential pair to produce the LVDS-compatible differential output signal. When CMOS signal swings are used, the  $\overline{\text{DOUT}}$  pin is the complement of  $\text{DOUT}$ . If  $\overline{\text{DOUT}}$  is not used, it should be left floating.

## DATA READY ( $\text{DRDY}$ , $\overline{\text{DRDY}}$ )

Data ready for retrieval are indicated on the  $\text{DRDY}$  and  $\overline{\text{DRDY}}$  pins. When LVDS signal swings are used, these two pins act as a differential pair to produce the LVDS-compatible differential output signal. When CMOS signal swings are used, the  $\overline{\text{DRDY}}$  pin is the complement of  $\text{DRDY}$ . If one of the data ready pins is not used when CMOS swings are selected, it should be left floating.

The  $\text{DRDY}$  pulse is the primary indicator from the ADS1675 that data are available for retrieval. [Table 5](#) and [Table 6](#) only give approximate values for settling time after a START signal. The rising edge of  $\text{DRDY}$  should be used as an indicator to start the data capture with the serial shift clock.

## SERIAL SHIFT CLOCK ( $\text{SCLK}$ , $\overline{\text{SCLK}}$ , $\text{SCLK\_SEL}$ )

The serial shift clock SCLK is used to shift out the conversion data, MSB first, onto the Data Output pins. Either an internally- or externally-generated shift clock can be selected using the  $\text{SCLK\_SEL}$  pin. If  $\text{SCLK\_SEL}$  is set to '0', a free-running shift clock is generated internally from the master clock and outputs on the SCLK and  $\overline{\text{SCLK}}$  pins. The LVDS pin determines if the output voltages are CMOS or LVDS. If  $\text{SCLK\_SEL}$  is set to '1' and LVDS is set to '1', the SCLK pin is configured as an input to accept an externally-generated shift clock. In this case, the  $\overline{\text{SCLK}}$  pin enters a high-impedance state. When  $\text{SCLK\_SEL}$  is set to '0', the SCLK and  $\overline{\text{SCLK}}$  pins are configured as outputs, and the shift clock is generated internally using the master clock input (CLK).

When LVDS signal swings are used, the shift clock is automatically generated internally regardless of the state of  $\text{SCLK\_SEL}$ . In this case,  $\text{SCLK\_SEL}$  cannot be left floating; it must be tied high or low.

[Table 7](#) summarizes the supported serial clock configurations for the ADS1675.

**Table 7. Supported Serial Clock Configurations**

DIGITAL OUTPUTS	SHIFT CLOCK (SCLK)
LVDS	Internal
CMOS	Internal ( $\text{SCLK\_SEL} = '0'$ )
	External ( $\text{SCLK\_SEL} = '1'$ )

## CHIP SELECT ( $\overline{\text{CS}}$ )

The chip select input ( $\overline{\text{CS}}$ ) allows multiple devices to share a serial bus. When  $\overline{\text{CS}}$  is inactive (high), the serial interface is reset and the data output pins  $\text{DOUT}$  and  $\overline{\text{DOUT}}$  enter a high-impedance state. SCLK is internally generated; the SCLK and  $\overline{\text{SCLK}}$  output pins also enter a high-impedance state when  $\overline{\text{CS}}$  is inactive. The  $\text{DRDY}$  and  $\overline{\text{DRDY}}$  outputs are always active, regardless of the state of the  $\overline{\text{CS}}$  output.  $\overline{\text{CS}}$  may be permanently tied low when the outputs do not share a bus.

## DATA FORMAT

In the low-speed modes, the ADS1675 outputs 24 bits of data in twos complement format. A positive full-scale input produces an output code of 7FFFFFFh, and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale. Table 8 summarizes the ideal output codes for different input signals. When the input is positive out-of-range, exceeding the positive full-scale value of  $V_{REF}$ , the output clips to all 7FFFFFFh. Likewise, when the input is negative out-of-range by going below the negative full-scale value of  $-V_{REF}$ , the output clips to 800000h.

**Table 8. Ideal Output Code vs Input Signal**

INPUT SIGNAL $V_{IN} = (AINP - AINN)$	IDEAL OUTPUT CODE
$\geq V_{REF}$	7FFFFFFh
$\frac{+V_{REF}}{2^{23} - 1}$	000001h
0	000000h
$\frac{-V_{REF}}{2^{23} - 1}$	FFFFFFh
$\leq -V_{REF} \left( \frac{2^{23}}{2^{23} - 1} \right)$	800000h

1. Excludes effects of noise, INL, offset and gain errors.

In the high-speed modes, the ADS1675 has 23 bits of resolution. The 24th bit in these modes is held low.

## CLOCK INPUT (CLK)

The ADS1675 requires an external clock signal to be applied to the CLK input pin. The sampling of the modulator is controlled by this clock signal. As with any high-speed data converter, a high-quality clock is essential for optimum performance. Crystal clock oscillators are the recommended CLK source; other sources, such as frequency synthesizers, are usually inadequate. Make sure to avoid excess ringing on the CLK input; keep the trace as short as possible.

For best performance, the CLK duty cycle should be very close to 50%. The rise and fall times of the clock should be less than 1ns and clock amplitude should be equal to AVDD.

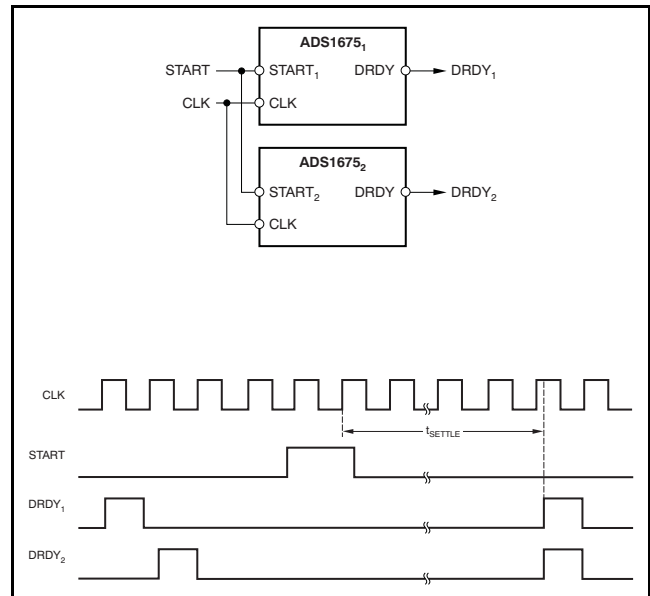
Measuring high-frequency, large amplitude signals requires tight control of clock jitter. The uncertainty during sampling of the input from clock jitter limits the maximum achievable SNR. This effect becomes more pronounced with higher frequency and larger magnitude inputs. Fortunately, the ADS1675 oversampling topology reduces clock jitter sensitivity over that of Nyquist rate converters, such as pipeline and SAR converters, by at least a factor of  $\sqrt{8}$ .

## SYNCHRONIZING MULTIPLE ADS1675s

The START pin should be applied at power-up and resets the ADS1675 filters. START begins the conversion process, and the START pin enables simultaneous sampling with multiple ADS1675s in multichannel systems. All devices to be synchronized must use a common CLK input.

It is recommended that the START pin be aligned to the falling edge of CLK to ensure proper synchronization because the START signal is internally latched by the ADS1675 on the rising edge of CLK.

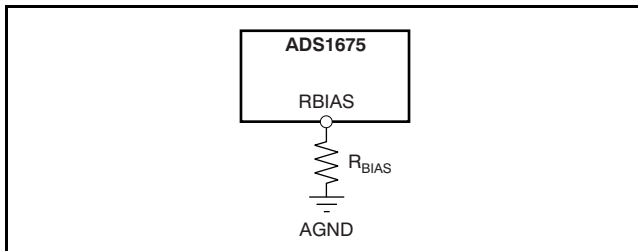
With the CLK inputs running, pulse START on the falling edge of CLK, as shown in Figure 50. Afterwards, the converters operate synchronously with the  $\overline{DRDY}$  outputs updating simultaneously. After synchronization,  $\overline{DRDY}$  is held high until the digital filter has fully settled.



**Figure 50. Synchronizing Multiple Converters**

## ANALOG POWER DISSIPATION

An external resistor connected between the RBIAS pin and the analog ground sets the analog current level, as shown in Figure 51. The current is inversely proportional to the resistor value. Figure 24 to Figure 26 (in the Typical Characteristics) show power and typical performance at values of  $R_{BIAS}$  for different CLK frequencies. Notice that the analog current can be reduced when using a slower frequency CLK input because the modulator has more time to settle. Avoid adding any capacitance in parallel to  $R_{BIAS}$ , because this additional capacitance interferes with the internal circuitry used to set the biasing.



**Figure 51. External Resistor Used to Set Analog Power Dissipation (Depends on  $f_{CLK}$ )**

## POWER DOWN ( $\overline{PDWN}$ )

When not in use, the ADS1675 can be powered down by taking the  $\overline{PDWN}$  pin low. All circuitry shuts down,

including the voltage reference. To minimize the digital current during power down, stop the clock signal supplied to the CLK input. Make sure to allow time for the reference to start up after exiting power-down mode.

After the reference has stabilized, allow for the modulator and digital filter to settle before retrieving data.

## POWER SUPPLIES

Two supplies are used on the ADS1675: analog (AVDD) and digital (DVDD). Each supply must be suitably bypassed to achieve the best performance. It is recommended that a  $1\mu\text{F}$  and  $0.1\mu\text{F}$  ceramic capacitor be placed as close to each supply pin as possible. AVDD must be very clean and stable in order to achieve optimum performance from the device.

Connect each supply-pin bypass capacitor to the associated ground. Each main supply bus should also be bypassed with a bank of capacitors from  $47\mu\text{F}$  to  $0.1\mu\text{F}$ . Figure 52 illustrates the recommended method for ADS1675 power-supply decoupling.

Power-supply pins 53 and 54 are used to drive the internal clock supply circuits and, as such, are very noisy. It is highly recommended that the traces from these pins not be shared or run close to any of the adjacent AVDD or AGND pins of the ADS1675. These pins should be well-decoupled, using a  $0.1\mu\text{F}$  ceramic capacitor close to the pins, and immediately terminated into power and ground planes.

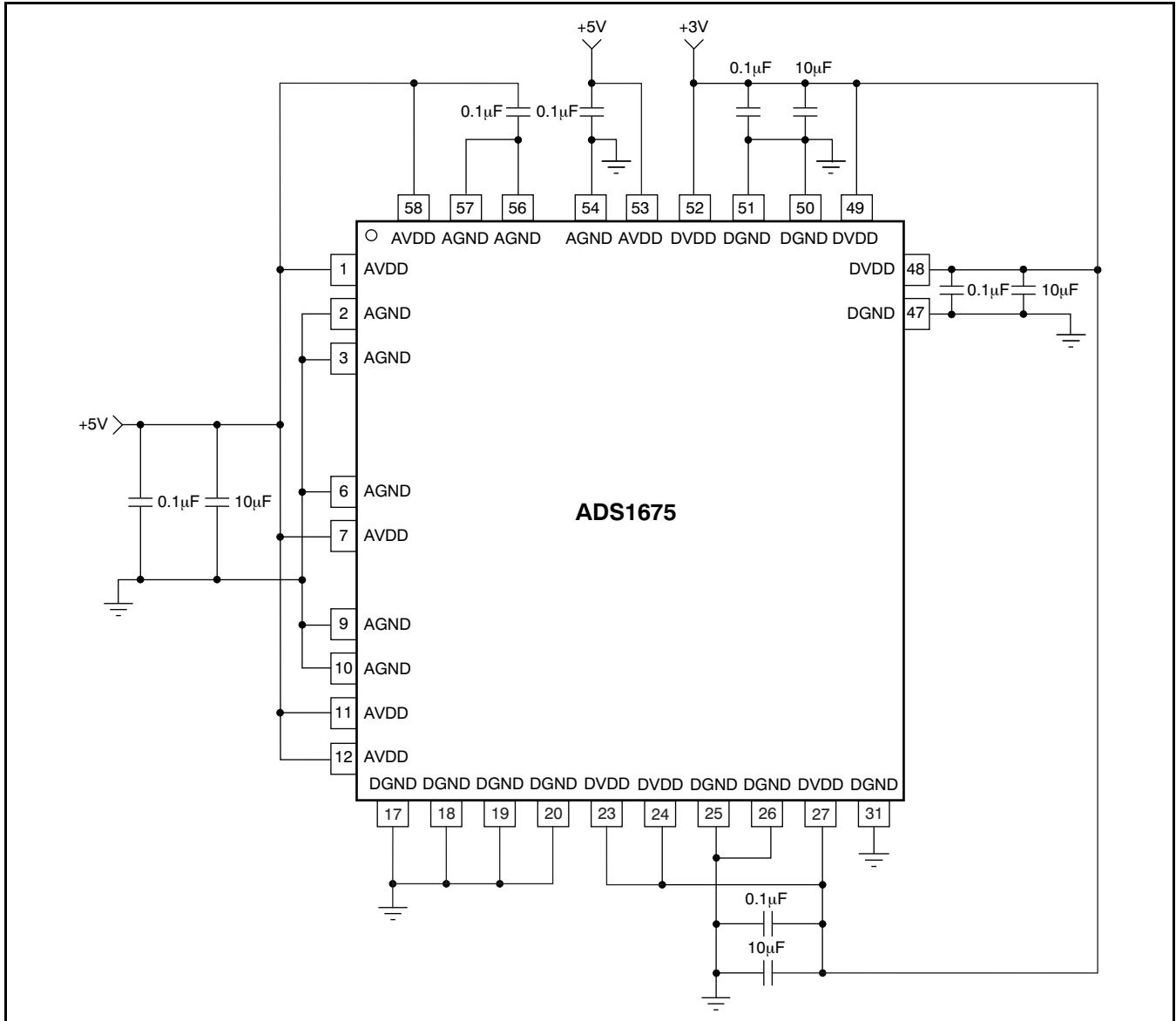


Figure 52. Power-Supply Decoupling

## APPLICATION INFORMATION

To obtain the specified performance from the ADS1675, the following layout and component guidelines should be considered.

- 1. Power Supplies:** The device requires two power supplies for operation: DVDD and AVDD. A very clean and stable AVDD supply is needed to achieve optimal performance from the device. For both supplies, use a 10 $\mu$ F tantalum capacitor, bypassed with a 0.1 $\mu$ F ceramic capacitor, placed close to the device pins. Alternatively, a single 10 $\mu$ F ceramic capacitor can be used. The supplies should be relatively free of noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power-supply source is used, the voltage ripple should be low (less than 2mV). The power supplies may be sequenced in any order.
- 2. Ground Plane:** A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter.
- 3. Digital Inputs:** Source terminate the digital inputs to the device with 50 $\Omega$  series resistors. The resistors should be placed close to the driving end of the digital source (oscillator, logic gates, DSP, etc.). These resistors help reduce ringing on the digital lines, which may lead to degraded ADC performance.
- 4. Analog/Digital Circuits:** Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.
- 5. Reference Inputs:** The ADS1675 reference input has 400 $\Omega$  across VREFP and VREFN. The driving amplifier must source current for this static current, as well as dynamic switching current as a result of the 32MHz clock. The reference driving amplifier should be ready to source at least 10.5mA.
- 6. Analog Inputs:** The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (ac applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks. A 750pF capacitor should be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) should be used to maintain low THD. Capacitors from each analog input to ground should be used. They should be no larger than 1/10 the size of the difference capacitor (typically 100pF) to preserve the ac common-mode performance.
- 7. Component Placement:** Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This placement is particularly important for the small-value ceramic capacitors. Surface-mount components are recommended to avoid the higher inductance of leaded components.

Figure 53 through Figure 55 illustrate the basic connections and interfaces that can be used with the ADS1675.

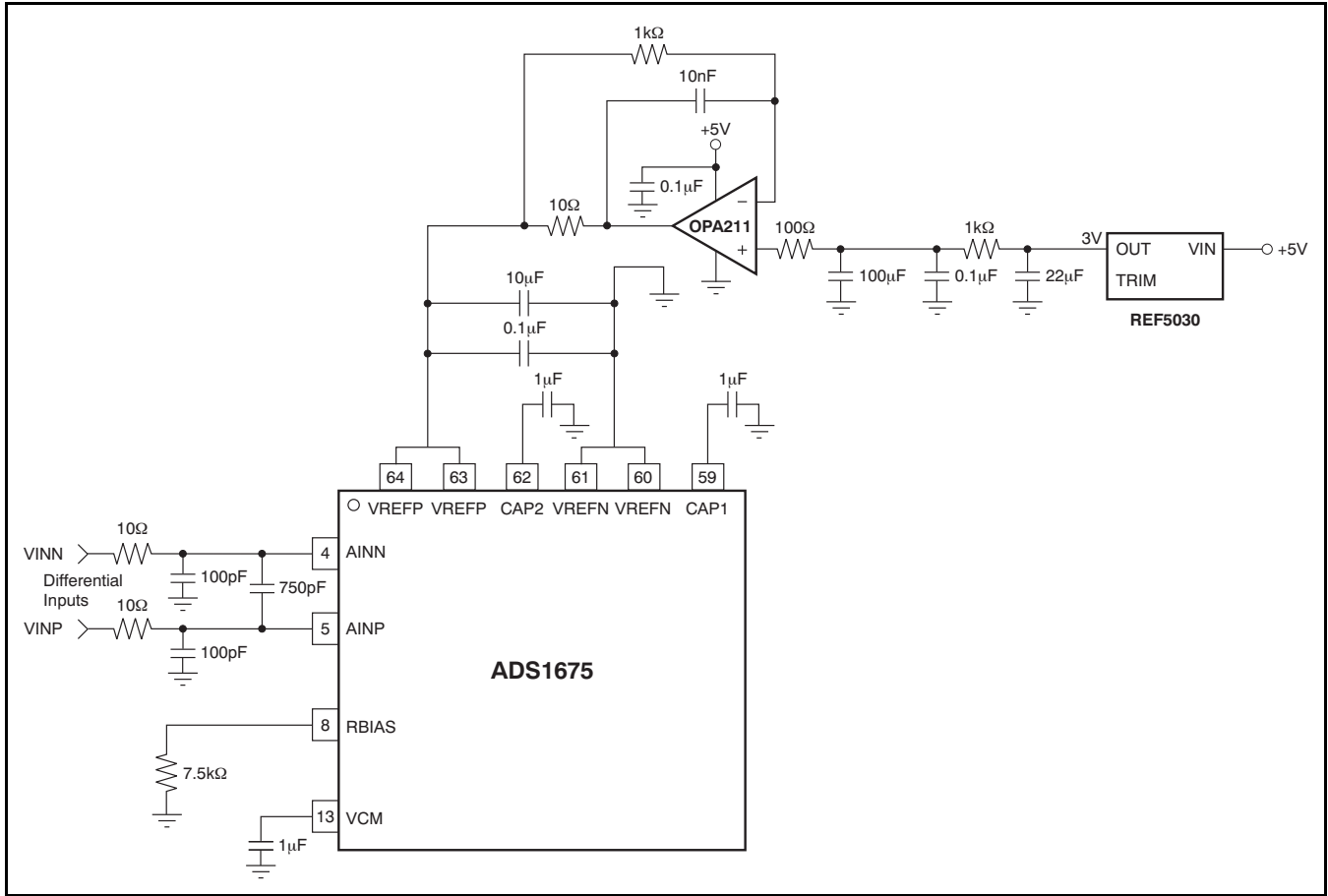


Figure 53. Basic Analog Signal Connection

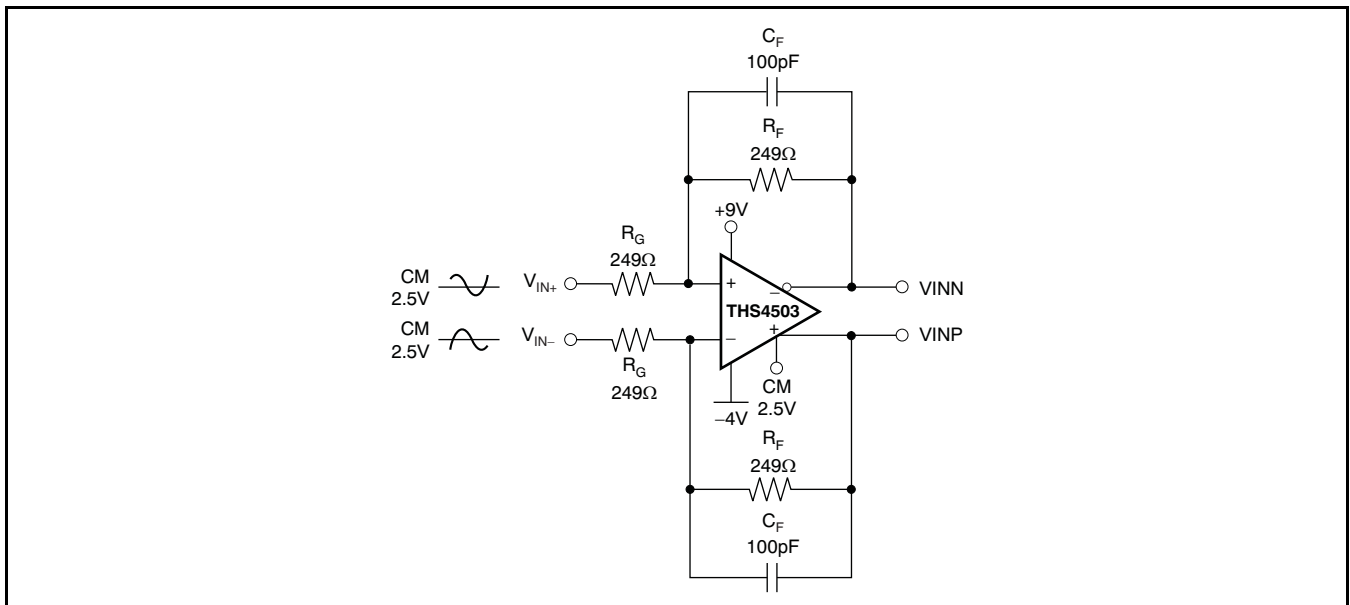


Figure 54. Basic Differential Input Signal Interface

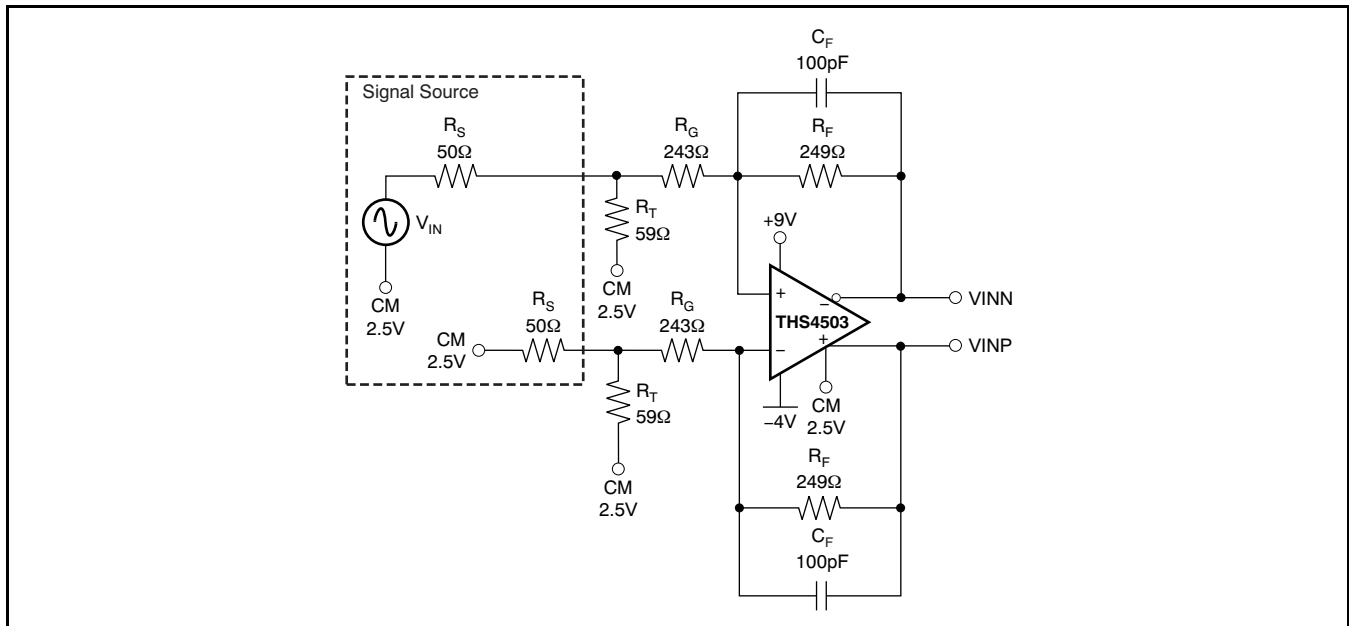


Figure 55. Basic Single-Ended Input Signal Interface

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (September 2009) to Revision D</b>	<b>Page</b>
• Changed 115dB to 86dB in second paragraph of Description section .....	1
• Changed AC Performance, <i>Total harmonic distortion</i> ( $f_{DATA} = 4MSPS$ ) typical specification in Electrical Characteristics table .....	3
• Changed Digital Filter Characteristics (Wide-Bandwidth Path), <i>Stop band attenuation</i> typical specification in Electrical Characteristics table .....	3
• Added footnote 2 to <a href="#">Figure 1</a> .....	7
• Updated <a href="#">Figure 3</a> .....	8
• Changed description of $t_{DRSCLK}$ parameter in internal SCLK timing requirements table .....	8
• Changed description of $t_{LSCLK}$ parameter in internal SCLK timing requirements table .....	8
• Deleted footnote 1 from <a href="#">Figure 5</a> .....	9
• Changed the description of the <i>Common-Mode Voltage</i> section .....	17
• Added description of 24th bit to <i>Data Format</i> section .....	25
• Changed description of the <i>Reference Inputs</i> guideline in Application Information section .....	28
<hr/>	
<b>Changes from Revision June 2009 (B) to Revision C</b>	<b>Page</b>
• Changed [1:0] to [2:0] in DRATE column of <a href="#">Table 6</a> .....	21
• Changed REF5030 connections in <a href="#">Figure 53</a> .....	29

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ADS1675IPAG</a>	Active	Production	TQFP (PAG)   64	160   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS1675I
ADS1675IPAG.A	Active	Production	TQFP (PAG)   64	160   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS1675I
ADS1675IPAGG4	Active	Production	TQFP (PAG)   64	160   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS1675I
ADS1675IPAGG4.A	Active	Production	TQFP (PAG)   64	160   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS1675I
<a href="#">ADS1675IPAGR</a>	Active	Production	TQFP (PAG)   64	1500   LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS1675I
ADS1675IPAGR.A	Active	Production	TQFP (PAG)   64	1500   LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS1675I

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

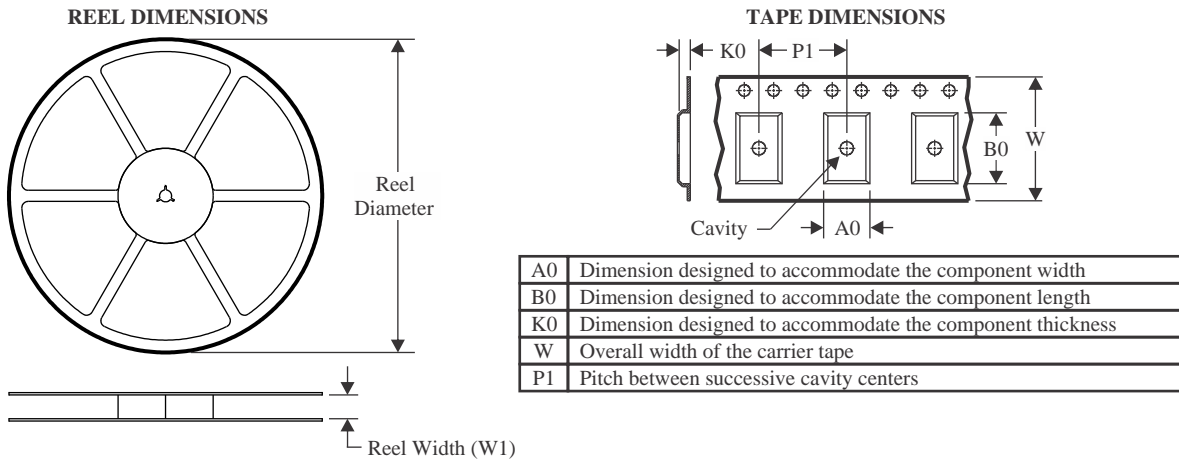
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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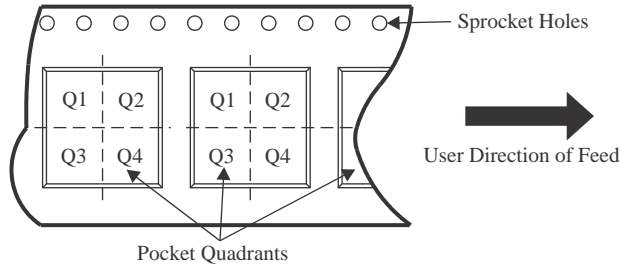
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



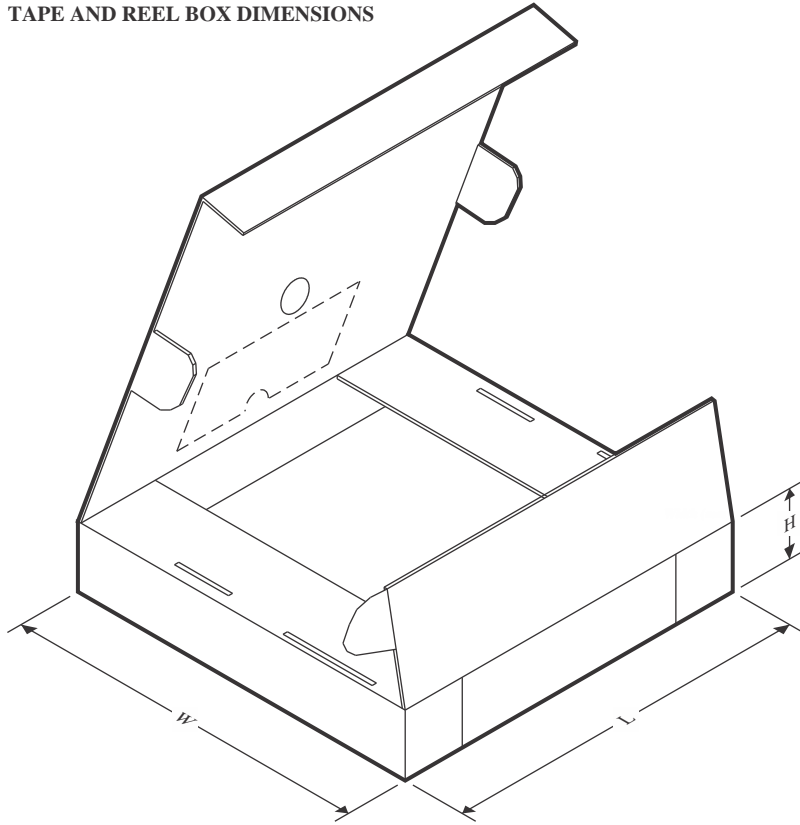
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1675IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

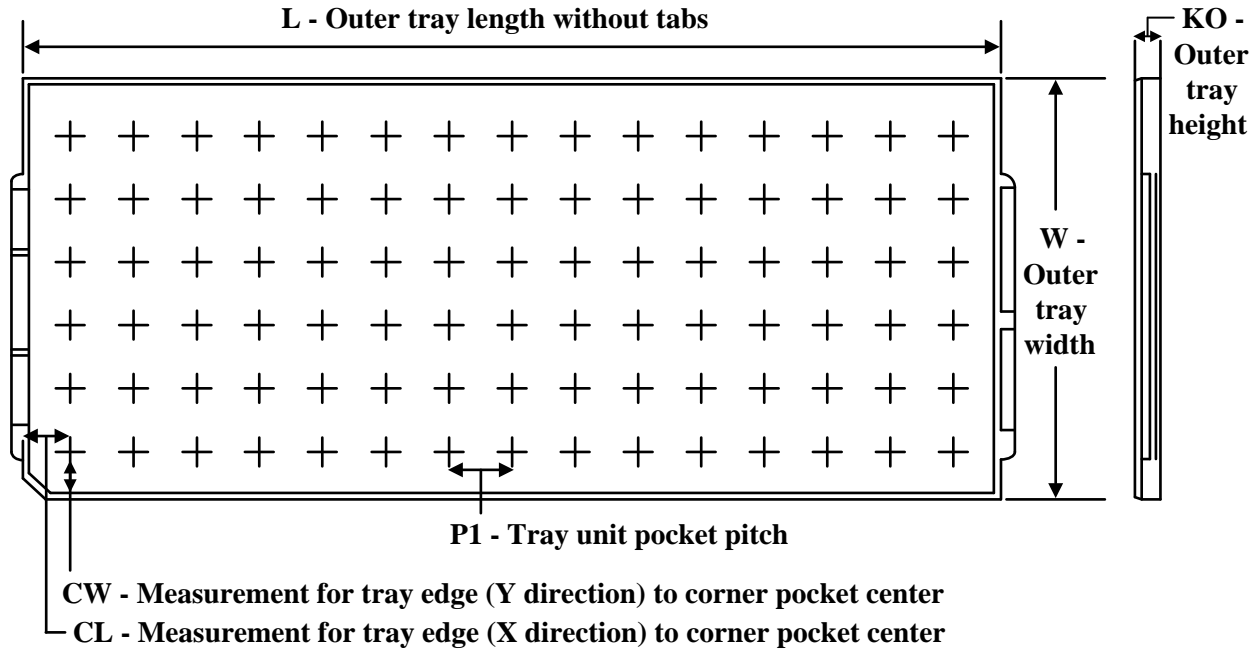
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1675IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0

TRAY



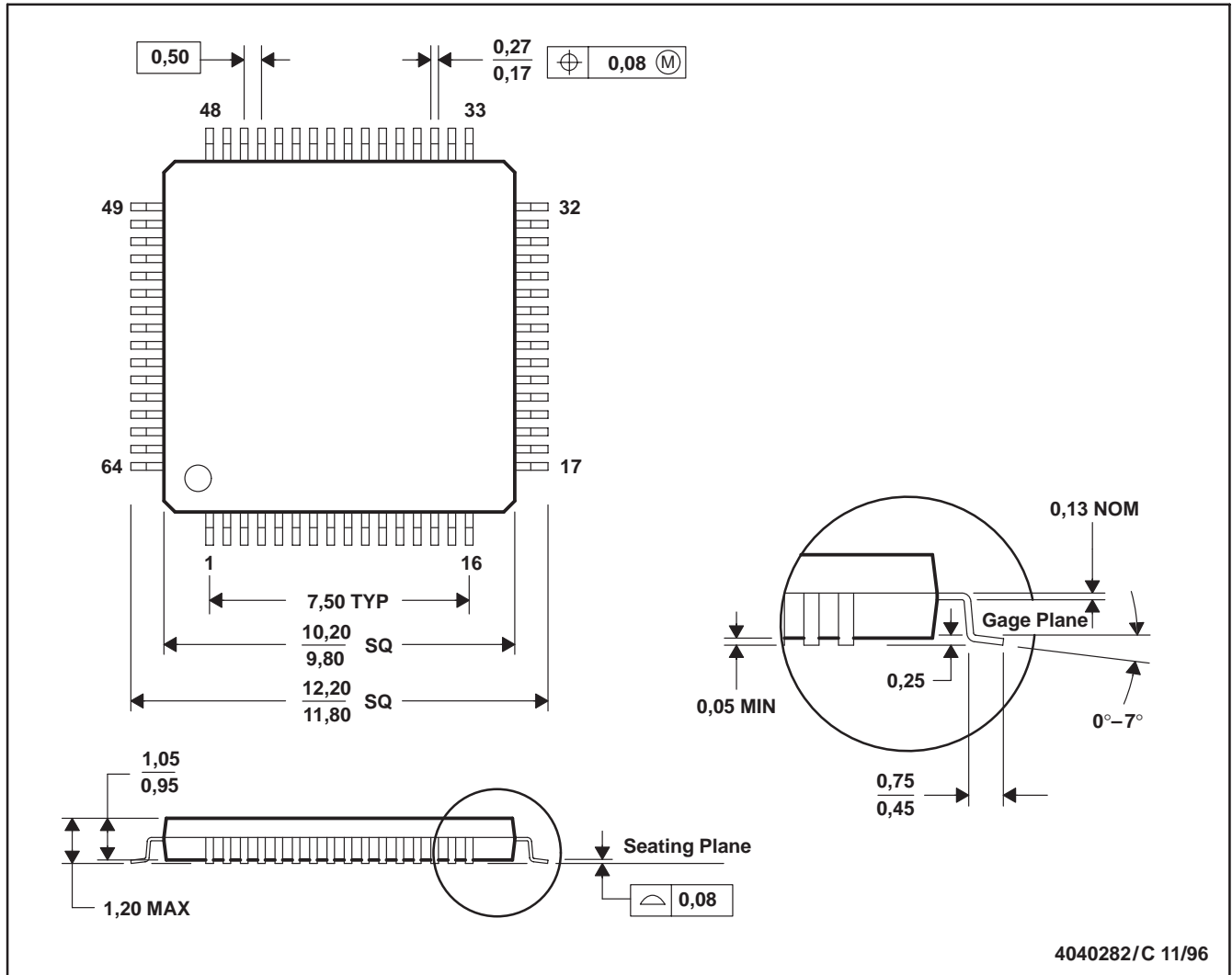
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS1675IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS1675IPAG.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS1675IPAGG4	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS1675IPAGG4.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK

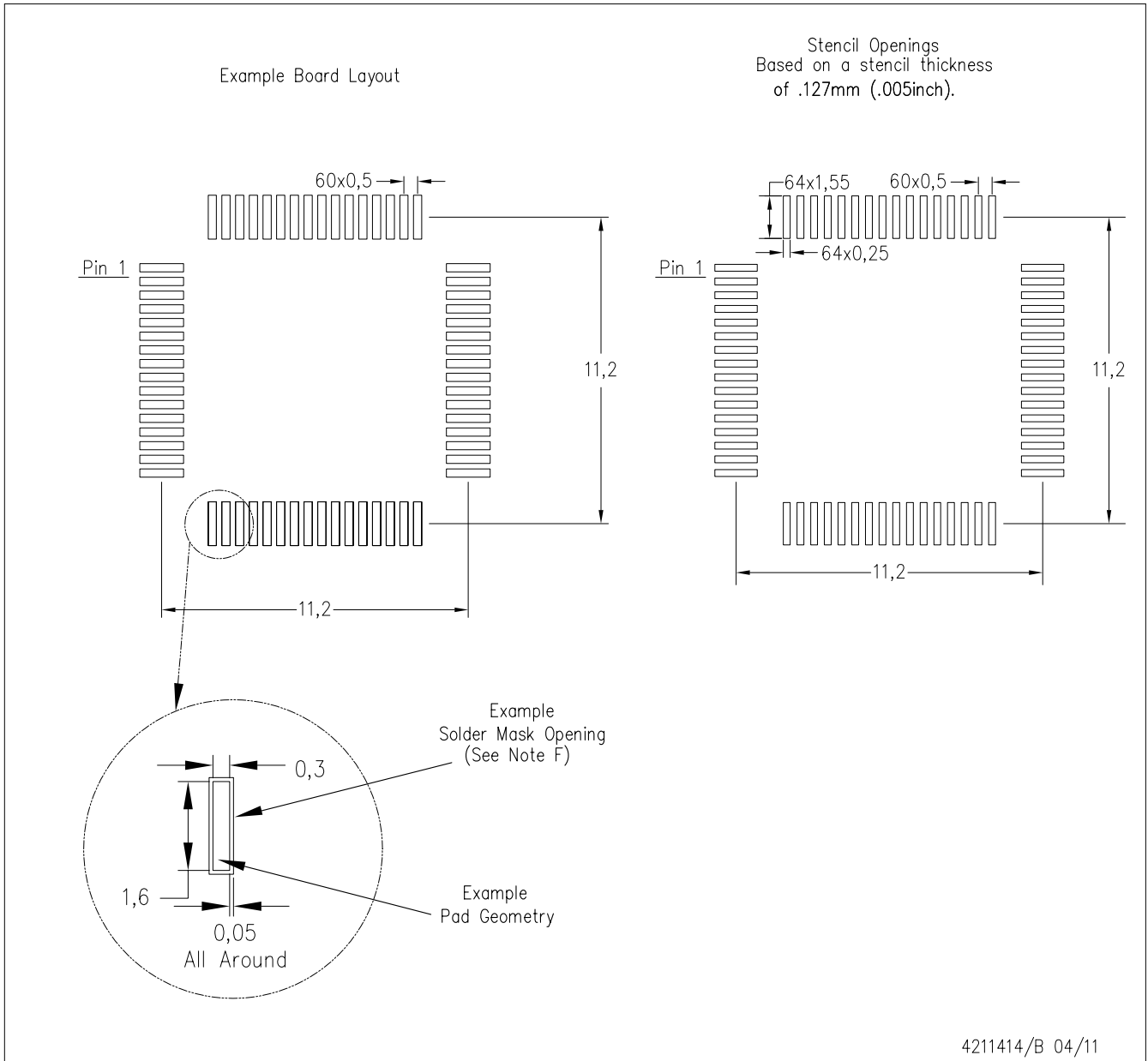


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026

**LAND PATTERN DATA**

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK

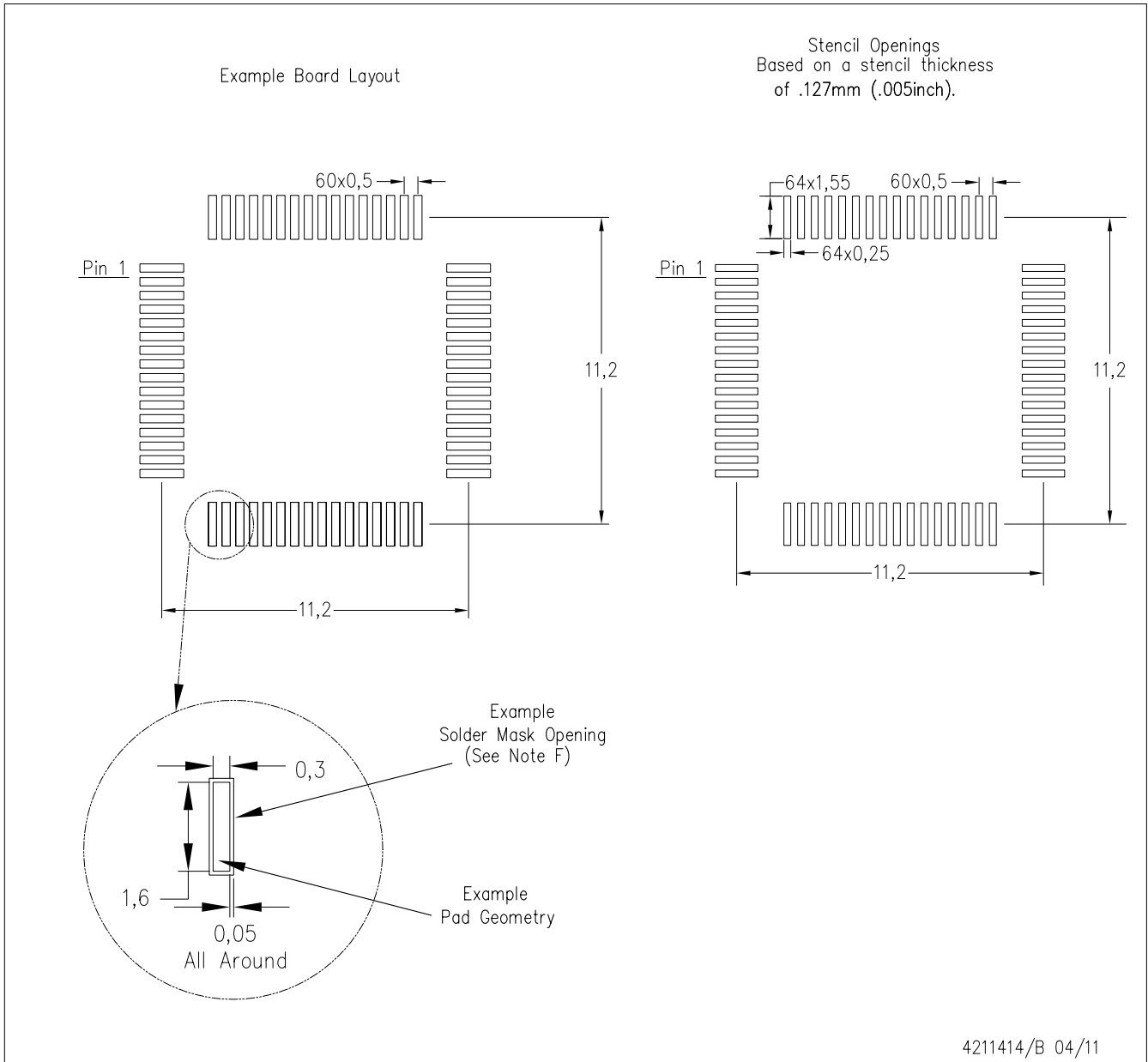


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**LAND PATTERN DATA**

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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