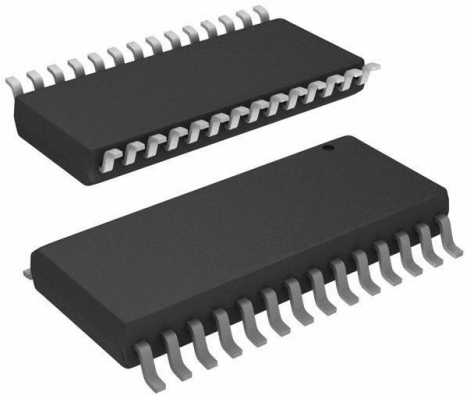


ADS7804U Datasheet

www.digi-electronics.com



ADS7804U

<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--|
| DiGi Electronics Part Number | ADS7804U-DG |
| Manufacturer | Texas Instruments |
| Manufacturer Product Number | ADS7804U |
| Description | IC ADC 12BIT SAR 28SOIC |
| Detailed Description | 12 Bit Analog to Digital Converter 1 Input 1 SAR 28-SOIC |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

ADS7804U

Series:

-

Number of Bits:

12

Number of Inputs:

1

Data Interface:

Parallel

Ratio - S/H:ADC:

1:1

Architecture:

SAR

Voltage - Supply, Analog:

5V

Features:

-

Package / Case:

28-SOIC (0.295", 7.50mm Width)

Mounting Type:

Surface Mount

Manufacturer:

Texas Instruments

Product Status:

Last Time Buy

Sampling Rate (Per Second):

100k

Input Type:

Single Ended

Configuration:

S/H-ADC

Number of A/D Converters:

1

Reference Type:

External, Internal

Voltage - Supply, Digital:

5V

Operating Temperature:

-40°C ~ 85°C

Supplier Device Package:

28-SOIC

Base Product Number:

ADS7804

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

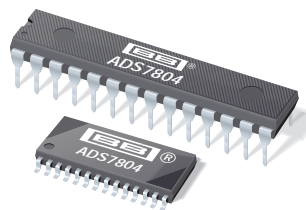
ECCN:

EAR99



Burr-Brown Products
from Texas Instruments

ADS7804



SBAS019A – JANUARY 1992 – REVISED MAY 2003

12-Bit 10 μ s Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

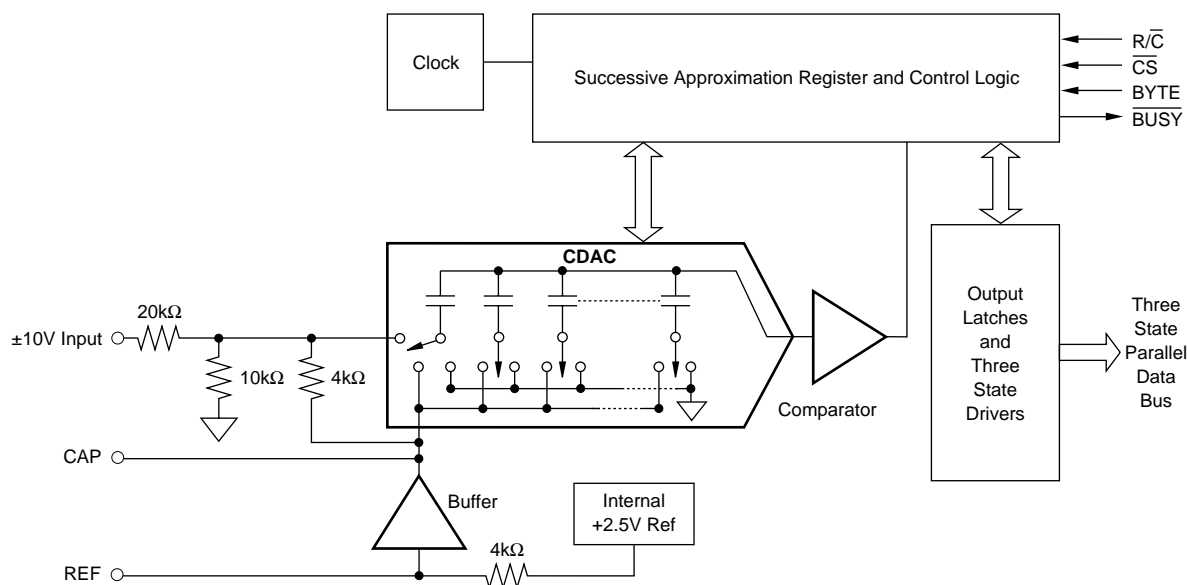
- 100kHz min SAMPLING RATE
- STANDARD ± 10 V INPUT RANGE
- 72dB min SINAD WITH 45kHz INPUT
- ± 0.45 LSB max INL
- DNL: 12 Bits "No Missing Codes"
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7805
- USES INTERNAL OR EXTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SO PACKAGES

DESCRIPTION

The ADS7804 is a complete 12-bit sampling analog-to-digital (A/D) converter using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, SAR A/D converter with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7804 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ± 10 V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7804 is available in plastic 0.3" DIP and SO packages, both fully specified for operation over the industrial -40°C to $+85^{\circ}\text{C}$ range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**
www.ti.com

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ABSOLUTE MAXIMUM RATINGS

| | |
|--|---|
| Analog Inputs: V_{IN} | $\pm 25V$ |
| CAP | $+V_{ANA} +0.3V$ to AGND2 $-0.3V$ |
| REF | Indefinite Short to AGND2 Momentary Short to V_{ANA} |
| Ground Voltage Differences: DGND, AGND1, AGND2 | $\pm 0.3V$ |
| V_{ANA} | 7V |
| V_{DIG} to V_{ANA} | $+0.3V$ |
| V_{DIG} | 7V |
| Digital Inputs | $-0.3V$ to $+V_{DIG} +0.3V$ |
| Maximum Junction Temperature | $+165^{\circ}C$ |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | $+300^{\circ}C$ |



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE+DISTORTION) RATIO (LSB) | PACKAGE-LEAD (DESIGNATOR) ⁽¹⁾ | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|-----------|-------------------------------|--|--|----------------------------------|-----------------|-----------------|---------------------------|
| ADS7804P | ± 0.9 | 70 | DIP-28 (NT) | $-40^{\circ}C$ to $+85^{\circ}C$ | ADS7804P | ADS7804P | Tube, 13 |
| ADS7804PB | ± 0.45 | 72 | DIP-28 (NT) | $-40^{\circ}C$ to $+85^{\circ}C$ | ADS7804PB | ADS7804PB | Tube, 13 |
| ADS7804U | ± 0.9 | 70 | SO-28 (DW) | $-40^{\circ}C$ to $+85^{\circ}C$ | ADS7804U | ADS7804U | Tube, 28 |
| " | " | " | " | " | " | ADS7804U/1K | Tape and Reel, 1000 |
| ADS7804UB | ± 0.45 | 72 | SO-28 (DW) | $-40^{\circ}C$ to $+85^{\circ}C$ | ADS7804UB | ADS7804UB | Tube, 28 |
| " | " | " | " | " | " | ADS7804UB/1K | Tape and Reel, 1000 |

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $f_S = 100kHz$, and $V_{DIG} = V_{ANA} = +5V$, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7804P, U | | | ADS7804PB, UB | | | UNITS |
|---|-------------------------|-------------|-----------------------------|-----------|---------------|---------|------------|--------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| RESOLUTION | | | | 12 | | | * | Bits |
| ANALOG INPUT | | | | | | | | |
| Voltage Ranges | | | $\pm 10V$ | | | * | | V |
| Impedance | | | 23 | | | * | | k Ω |
| Capacitance | | | 35 | | | * | | pF |
| THROUGHPUT SPEED | | | | | | | | |
| Conversion Time | | | 5.7 | 8 | | * | * | μs |
| Complete Cycle | Acquire and Convert | | | 10 | | | * | μs |
| Throughput Rate | | 100 | | | * | | | kHz |
| DC ACCURACY | | | | | | | | |
| Integral Linearity Error | | | | ± 0.9 | | | ± 0.45 | LSB ⁽¹⁾ |
| Differential Linearity Error | | | | ± 0.9 | | | ± 0.45 | LSB |
| No Missing Codes | | | Ensured | | | * | | Bits |
| Transition Noise ⁽²⁾ | | | 0.1 | | | * | | LSB |
| Full Scale Error ^(3,4) | | | | ± 0.5 | | | ± 0.25 | % |
| Full Scale Error Drift | | | ± 7 | | | ± 5 | | ppm/ $^{\circ}C$ |
| Full Scale Error ^(3,4) | Ext. 2.5000V Ref | | | ± 0.5 | | | ± 0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ± 2 | | | * | | ppm/ $^{\circ}C$ |
| Bipolar Zero Error ⁽³⁾ | | | ± 2 | ± 10 | | | ± 10 | mV |
| Bipolar Zero Error Drift | | | ± 2 | | | * | | ppm/ $^{\circ}C$ |
| Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$) | $+4.75V < V_D < +5.25V$ | | | ± 0.5 | | | * | LSB |
| AC ACCURACY | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN} = 45kHz$ | 80 | | | * | | * | dB ⁽⁵⁾ |
| Total Harmonic Distortion | $f_{IN} = 45kHz$ | | | -80 | | | | dB |
| Signal-to-(Noise+Distortion) | $f_{IN} = 45kHz$ | 70 | | | 72 | | | dB |
| Signal-to-Noise | $f_{IN} = 45kHz$ | 70 | | | 72 | | | dB |
| Full-Power Bandwidth ⁽⁶⁾ | | | 250 | | | * | | kHz |
| SAMPLING DYNAMICS | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | Sufficient to meet AC specs | | | | * | |
| Transient Response | FS Step | | | 2 | | | * | μs |
| Overvoltage Recovery ⁽⁷⁾ | | | 150 | | | * | * | ns |

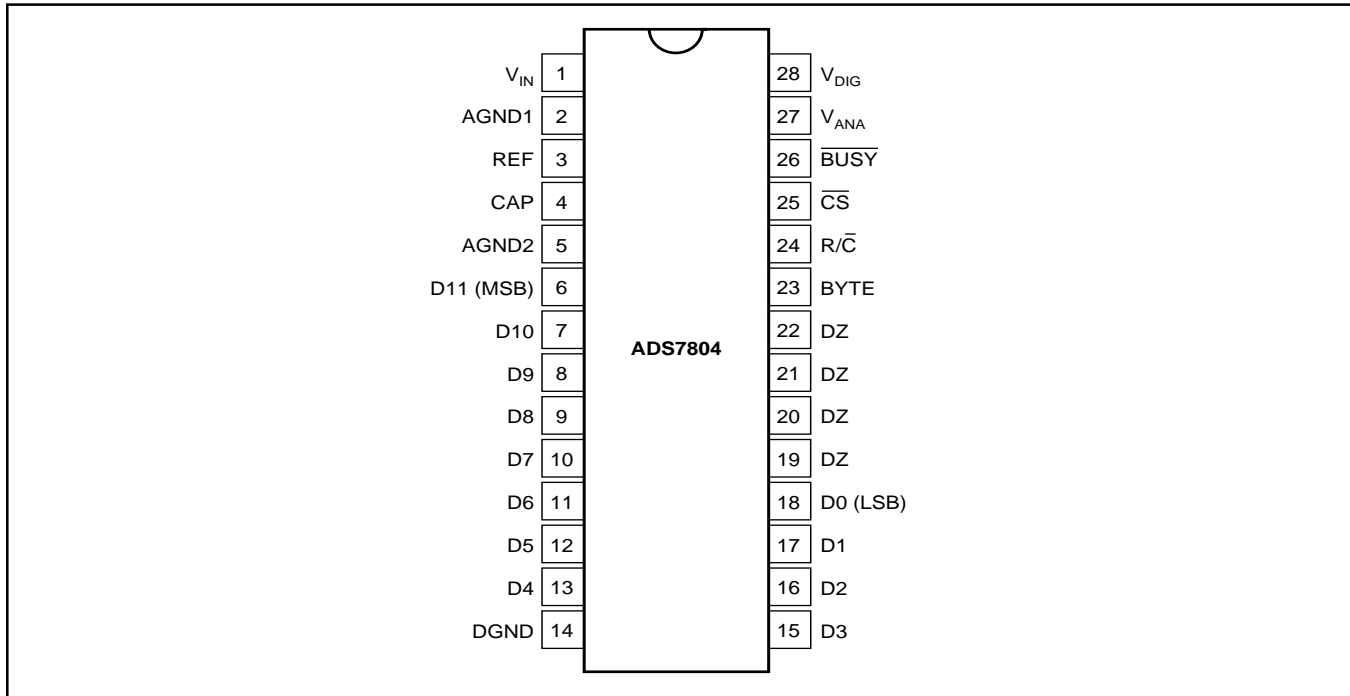
ELECTRICAL CHARACTERISTICS (Cont.)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $f_S = 100\text{kHz}$, and $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7804P, U | | | ADS7804PB, UB | | | UNITS |
|--|---|-------------|-----|------------------------------|---------------|-----|-----|-----------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| REFERENCE | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | * | * | * | μA |
| Internal Reference Drift | | | 8 | | | | | ppm/ $^{\circ}\text{C}$ |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | μA |
| DIGITAL INPUTS | | | | | | | | |
| Logic Levels | | | | | | | | |
| V_{IL} | | -0.3 | | +0.8 | * | | * | V |
| V_{IH} | | +2.0 | | $V_{\text{D}} + 0.3\text{V}$ | * | | * | V |
| I_{IL} | | | | ± 10 | | | * | μA |
| I_{IH} | | | | ± 10 | | | * | μA |
| DIGITAL OUTPUTS | | | | | | | | |
| Data Format | | | | Parallel 12 Bits | | | | |
| Data Coding | | | | Binary Two's Complement | | | | |
| V_{OL} | | | | +0.4 | | * | * | V |
| V_{OH} | | | | | | * | * | V |
| Leakage Current | $I_{\text{SINK}} = 1.6\text{mA}$ $I_{\text{SOURCE}} = 500\mu\text{A}$ High-Z State, $V_{\text{OUT}} = 0\text{V}$ to V_{DIG} High-Z State | +4 | | ± 5 | | | * | μA |
| Output Capacitance | | | | 15 | | | 15 | pF |
| DIGITAL TIMING | | | | | | | | |
| Bus Access Time | | | | 83 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |
| POWER SUPPLIES | | | | | | | | |
| Specified Performance | | | | | | | | |
| V_{DIG} | Must be $\leq V_{\text{ANA}}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| V_{ANA} | | +4.75 | +5 | +5.25 | * | * | * | V |
| $+I_{\text{DIG}}$ | | | 0.3 | | | * | | mA |
| $+I_{\text{ANA}}$ | | | 16 | | | * | | mA |
| Power Dissipation | $f_S = 100\text{kHz}$ | | | 100 | | | * | mW |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | -40 | | +85 | * | | * | $^{\circ}\text{C}$ |
| Derated Performance | | -55 | | +125 | * | | * | $^{\circ}\text{C}$ |
| Storage | | -65 | | +150 | * | | * | $^{\circ}\text{C}$ |
| Thermal Resistance (θ_{JA}) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | $^{\circ}\text{C}/\text{W}$ |
| SO | | | 75 | | | * | | $^{\circ}\text{C}/\text{W}$ |

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, $\pm 10\text{V}$ input ADS7804, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale $\pm 10\text{V}$ input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

PIN CONFIGURATION



| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|-------|-------------------|-------------|---|
| 1 | V _{IN} | | Analog Input. See Figure 7. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. |
| 3 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 4 | CAP | | Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D11 (MSB) | O | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 7 | D10 | O | Data Bit 10. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 8 | D9 | O | Data Bit 9. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 9 | D8 | O | Data Bit 8. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 10 | D7 | O | Data Bit 7. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 11 | D6 | O | Data Bit 6. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 12 | D5 | O | Data Bit 5. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 13 | D4 | O | Data Bit 4. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 14 | DGND | | Digital Ground. |
| 15 | D3 | O | Data Bit 3. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 16 | D2 | O | Data Bit 2. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 17 | D1 | O | Data Bit 1. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 18 | D0 (LSB) | O | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 19 | DZ | O | LOW when \overline{CS} LOW, R/\overline{C} HIGH. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 20 | DZ | O | LOW when \overline{CS} LOW, R/\overline{C} HIGH. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 21 | DZ | O | LOW when \overline{CS} LOW, R/\overline{C} HIGH. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 22 | DZ | O | LOW when \overline{CS} LOW, R/\overline{C} HIGH. Hi-Z state when \overline{CS} is HIGH, or when R/\overline{C} is LOW. |
| 23 | BYTE | I | Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH). |
| 24 | R/ \overline{C} | I | With \overline{CS} LOW and $BUSY$ HIGH, a Falling Edge on R/\overline{C} Initiates a New Conversion. With \overline{CS} LOW, a rising edge on R/\overline{C} enables the parallel output. |
| 25 | \overline{CS} | I | Internally OR'd with R/\overline{C} . If R/\overline{C} LOW, a falling edge on \overline{CS} initiates a new conversion. |
| 26 | \overline{BUSY} | O | At the start of a conversion, \overline{BUSY} goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated. |
| 27 | V _{ANA} | | Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 28 | V _{DIG} | | Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V _{ANA} . |

TABLE I. Pin Assignments.

BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7804 with a full parallel data output. Taking $\overline{R/C}$ (pin 24) LOW for a minimum of 40ns ($6\mu\text{s}$ max) will initiate a conversion. \overline{BUSY} (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. \overline{BUSY} going HIGH can be used to latch the data. All convert commands will be ignored while \overline{BUSY} is LOW.

The ADS7804 will begin tracking the input signal at the end of the conversion. Allowing $10\mu\text{s}$ between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the Calibration section).

STARTING A CONVERSION

The combination of \overline{CS} (pin 25) and $\overline{R/C}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7804 in the hold state and starts conversion 'n'. \overline{BUSY} (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during \overline{BUSY} LOW will be ignored. \overline{CS} and/or $\overline{R/C}$ must go HIGH before \overline{BUSY} goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7804 will begin tracking the input signal at the end of the conversion. Allowing $10\mu\text{s}$ between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of \overline{CS} , $\overline{R/C}$, and \overline{BUSY} states and Figures 3 through 5 for timing diagrams.

| \overline{CS} | $\overline{R/C}$ | \overline{BUSY} | OPERATION |
|-----------------|------------------|-------------------|--|
| 1 | X | X | None. Databus is in Hi-Z state. |
| ↓ | 0 | 1 | Initiates conversion 'n'. Databus remains in Hi-Z state. |
| 0 | ↓ | 1 | Initiates conversion 'n'. Databus enters Hi-Z state. |
| 0 | 1 | ↑ | Conversion 'n' completed. Valid data from conversion 'n' on the databus. |
| ↓ | 1 | 1 | Enables databus with valid data from conversion 'n'. |
| ↓ | 1 | 0 | Enables databus with valid data from conversion 'n-1'(*). Conversion n in process. |
| 0 | ↑ | 0 | Enables databus with valid data from conversion 'n-1'(*). Conversion 'n' in process. |
| 0 | 0 | ↑ | New conversion initiated without acquisition of a new signal. Data will be invalid. \overline{CS} and/or $\overline{R/C}$ must be HIGH when \overline{BUSY} goes HIGH. |
| X | X | 0 | New convert commands ignored. Conversion 'n' in process. |

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for Read and Convert.

\overline{CS} and $\overline{R/C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that \overline{CS} or $\overline{R/C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, \overline{CS} can be tied LOW using $\overline{R/C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output will become active whenever $\overline{R/C}$ goes HIGH. Refer to the Reading Data section.

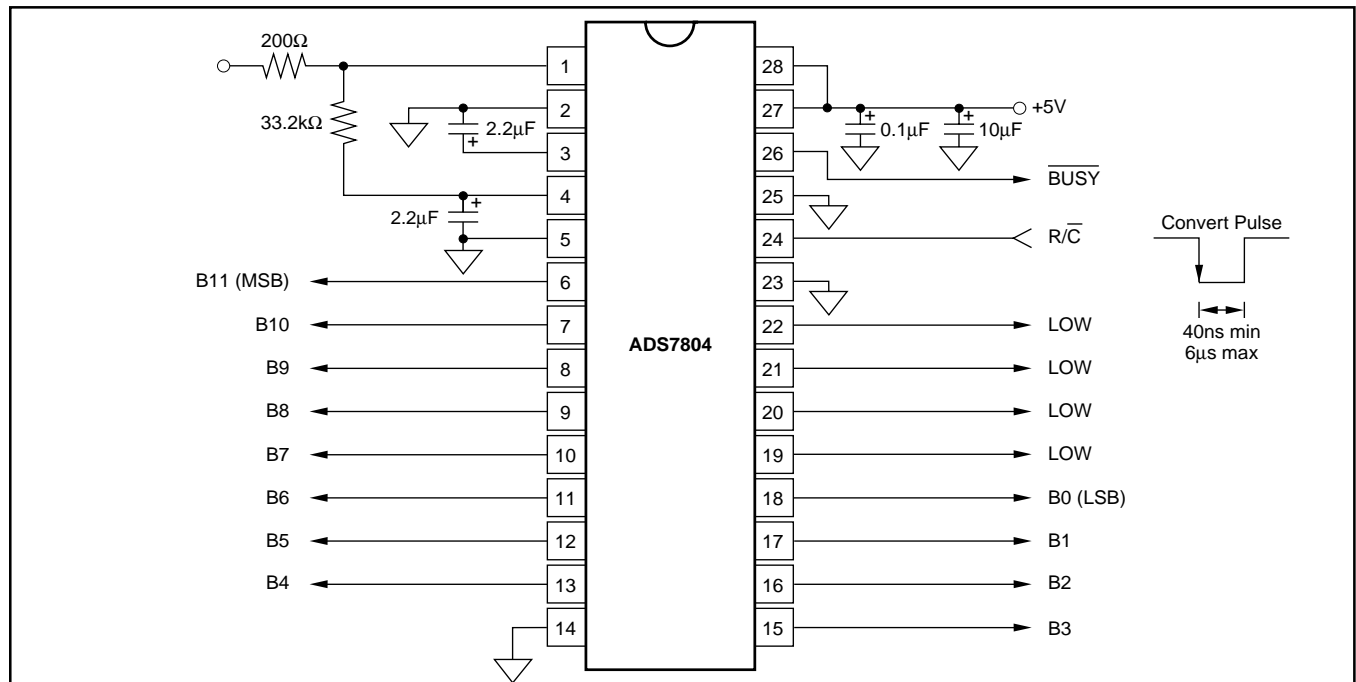


FIGURE 1. Basic Operation.

READING DATA

The ADS7804 outputs full or byte-reading parallel data in Binary Two's Complement data output format. The parallel output will be active when $\overline{R/C}$ (pin 24) is HIGH and \overline{CS} (pin 25) is LOW. Any other combination of \overline{CS} and $\overline{R/C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

| DESCRIPTION | ANALOG INPUT | DIGITAL OUTPUT BINARY TWO'S COMPLEMENT | |
|-----------------------------|--------------|---|----------|
| | | BINARY CODE | HEX CODE |
| Full Scale Range | $\pm 10V$ | | |
| Least Significant Bit (LSB) | 4.88mV | | |
| +Full Scale (10V - 1LSB) | 9.99512V | 0111 1111 1111 | 7FF |
| Midscale | 0V | 0000 0000 0000 | 000 |
| One LSB below Midscale | -4.88mV | 1111 1111 1111 | FFF |
| -Full Scale | -10V | 1000 0000 0000 | 800 |

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, \overline{BUSY} (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D11-D0 (pin 6-13 and 15-18 when BYTE is LOW). \overline{BUSY} going HIGH can be used to latch the data. Refer to Table IV and Figures 3 and 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 16 μ s after the start of conversion 'n'. Do not attempt to read data from 16 μ s after the start of conversion 'n' until \overline{BUSY} (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 and 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tying \overline{CS} LOW while using $\overline{R/C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|-------------|---|-----|-----|------|---------|
| t_1 | Convert Pulse Width | 40 | | 6000 | ns |
| t_2 | Data Valid Delay after $\overline{R/C}$ LOW | | | 8 | μ s |
| t_3 | \overline{BUSY} Delay from $\overline{R/C}$ LOW | | | 65 | ns |
| t_4 | \overline{BUSY} LOW | | | 8 | μ s |
| t_5 | \overline{BUSY} Delay after End of Conversion | | 220 | | ns |
| t_6 | Aperture Delay | | 40 | | ns |
| t_7 | Conversion Time | | 7.6 | 8 | μ s |
| t_8 | Acquisition Time | | | 2 | μ s |
| t_9 | Bus Relinquish Time | 10 | 35 | 83 | ns |
| t_{10} | \overline{BUSY} Delay after Data Valid | 50 | 200 | | ns |
| t_{11} | Previous Data Valid after $\overline{R/C}$ LOW | | 7.4 | | μ s |
| $t_7 + t_6$ | Throughput Time | | 9 | 10 | μ s |
| t_{12} | $\overline{R/C}$ to \overline{CS} Setup Time | 10 | | | ns |
| t_{13} | Time Between Conversions | 10 | | | μ s |
| t_{14} | Bus Access Time and BYTE Delay | 10 | | 83 | ns |

TABLE IV. Conversion Timing.

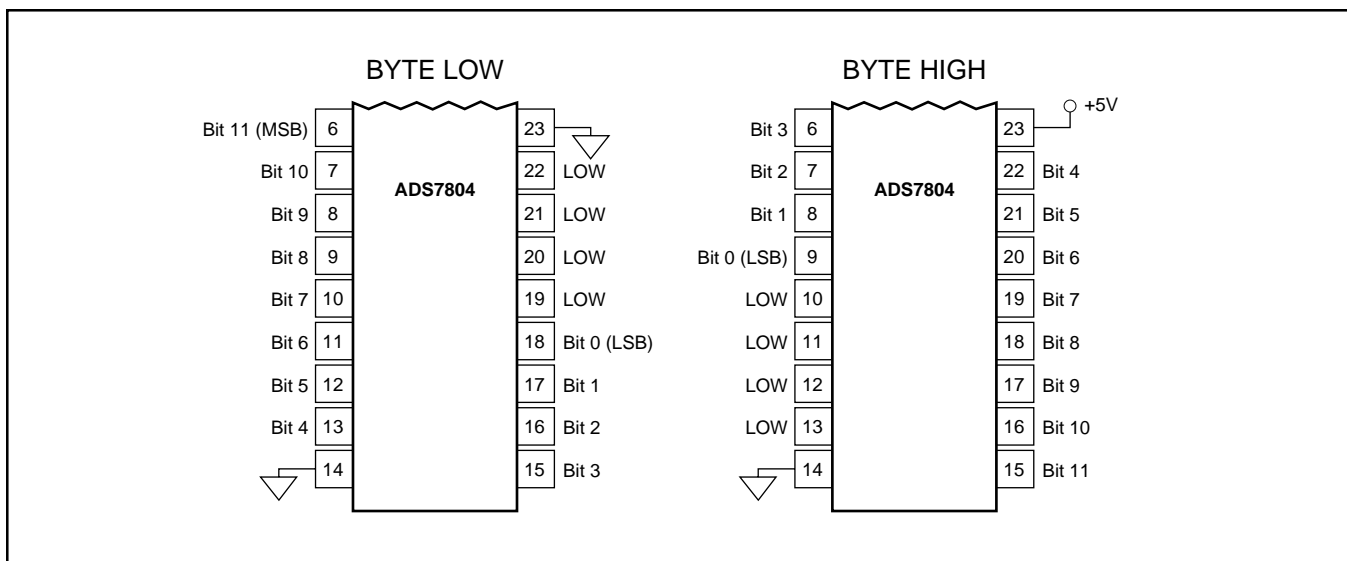


FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

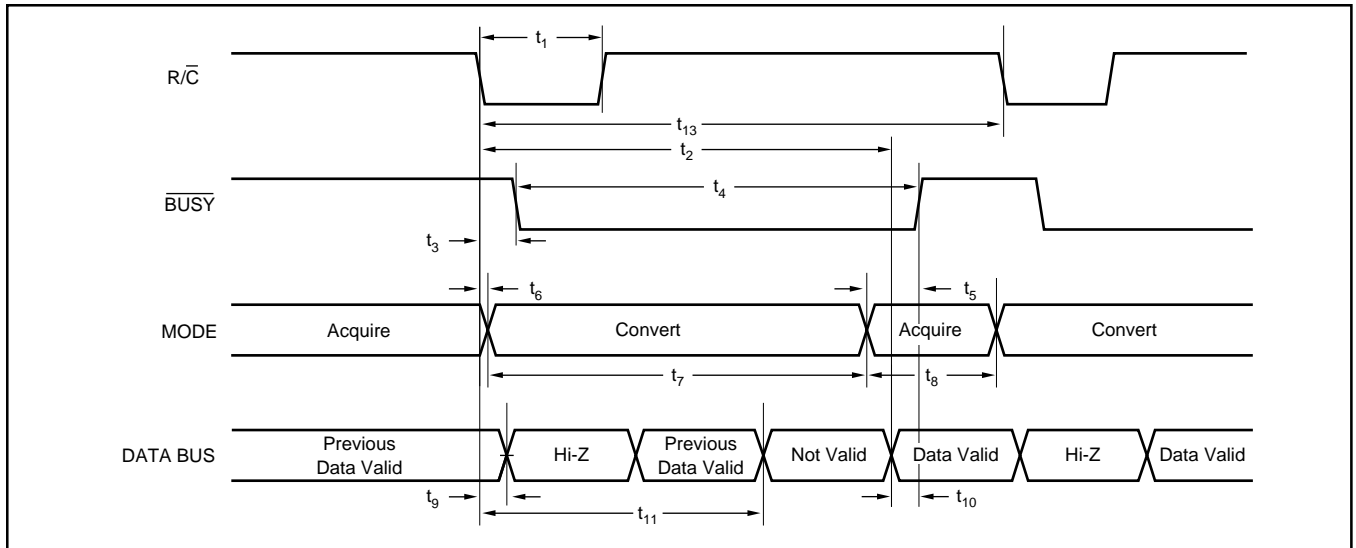


FIGURE 3. Conversion Timing with Outputs Enabled after Conversion (\overline{CS} Tied LOW.)

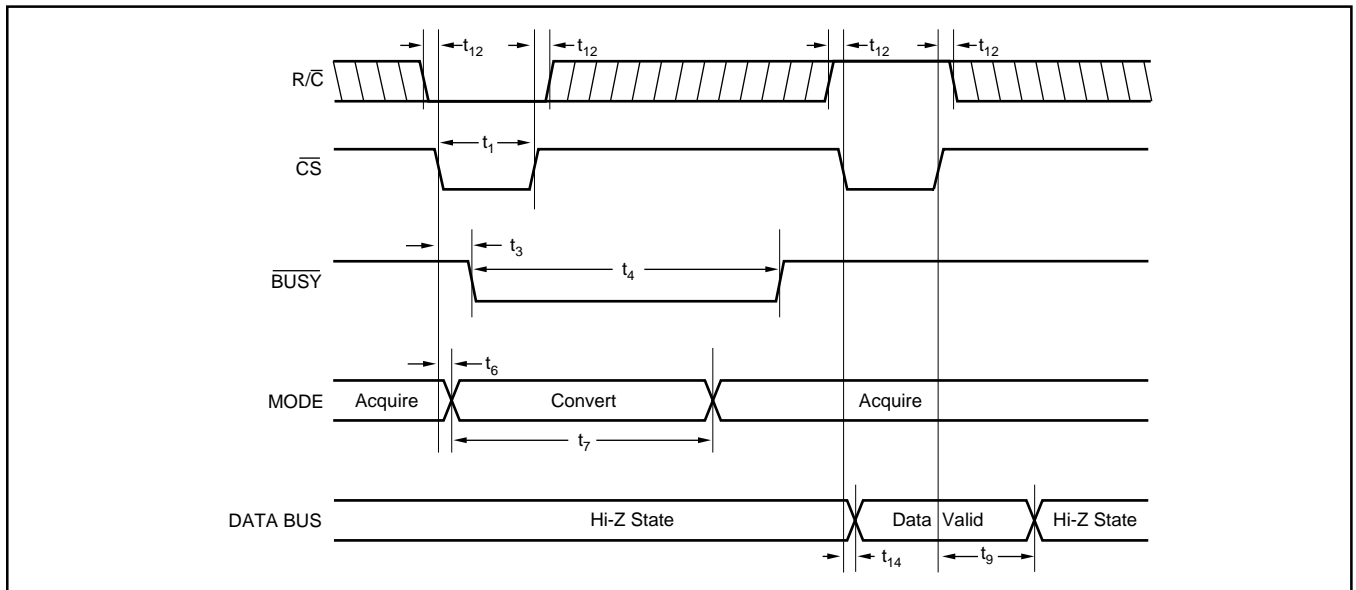


FIGURE 4. Using \overline{CS} to Control Conversion and Read Timing.

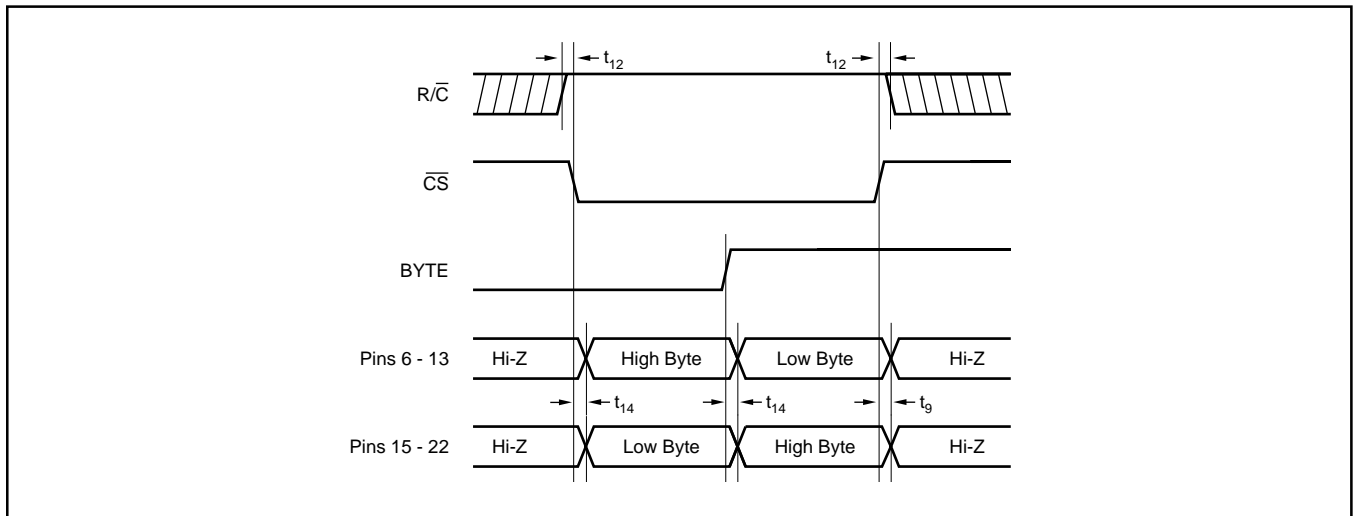


FIGURE 5. Using \overline{CS} and BYTE to Control Data Bus.

INPUT RANGES

The ADS7804 offers a standard $\pm 10V$ input range. Figure 6 shows the necessary circuit connections for the ADS7804 with and without hardware trim. Offset and full scale error⁽¹⁾ specifications are tested and guaranteed with the fixed resistors shown in Figure 6b. Adjustments for offset and gain are described in the Calibration section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the Calibration section).

The nominal input impedance of 23k Ω results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection guaranteed to at least $\pm 25V$. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and -FS.

CALIBRATION

The ADS7804 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7804, install the proper resistors and potentiometers as shown in Figure 6a. The calibration range is $\pm 15mV$ for the offset and $\pm 60mV$ for the gain.

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7804 in software, no external resistors are required. See the No Calibration section for details on the effects of the external resistors. Refer to Table V for range of offset and gain errors with and without external resistors.

NO CALIBRATION

See Figure 6b for circuit connections. The external resistors shown in Figure 6b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer function of the ADS7804 will be bound by the shaded region seen in Figure 7 with a typical offset of $-30mV$ and a typical gain error of -1.5% . Refer to Table V for range of offset and gain errors with and without external resistors.

| | WITH EXTERNAL RESISTORS | WITHOUT EXTERNAL RESISTORS | UNITS |
|------------|--|--|------------|
| BPZ | $-10 < BPZ < 10$ $-2 < BPZ < 2$ | $-45 < BPZ < 5$ $-8 < BPZ < 1$ | mV LSBs |
| Gain Error | $-0.5 < \text{error} < 0.5$ $-0.25 < \text{error} < 0.25^{(1)}$ | $-0.6 < \text{error} < -0.55$ $-0.45 < \text{error} < -0.3^{(1)}$ | % of FSR |

NOTE: (1) High Grade.

TABLE VII. Bipolar Offset and Gain Errors With and Without External Resistors.

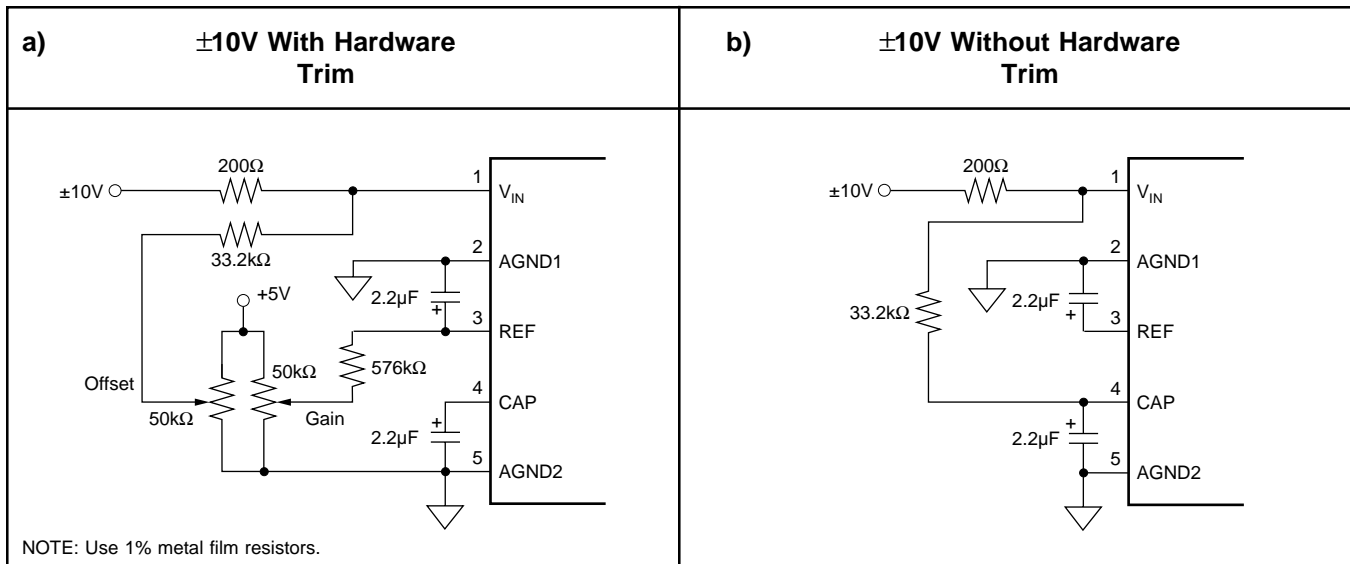


FIGURE 6. Circuit Diagram With and Without External Resistors.

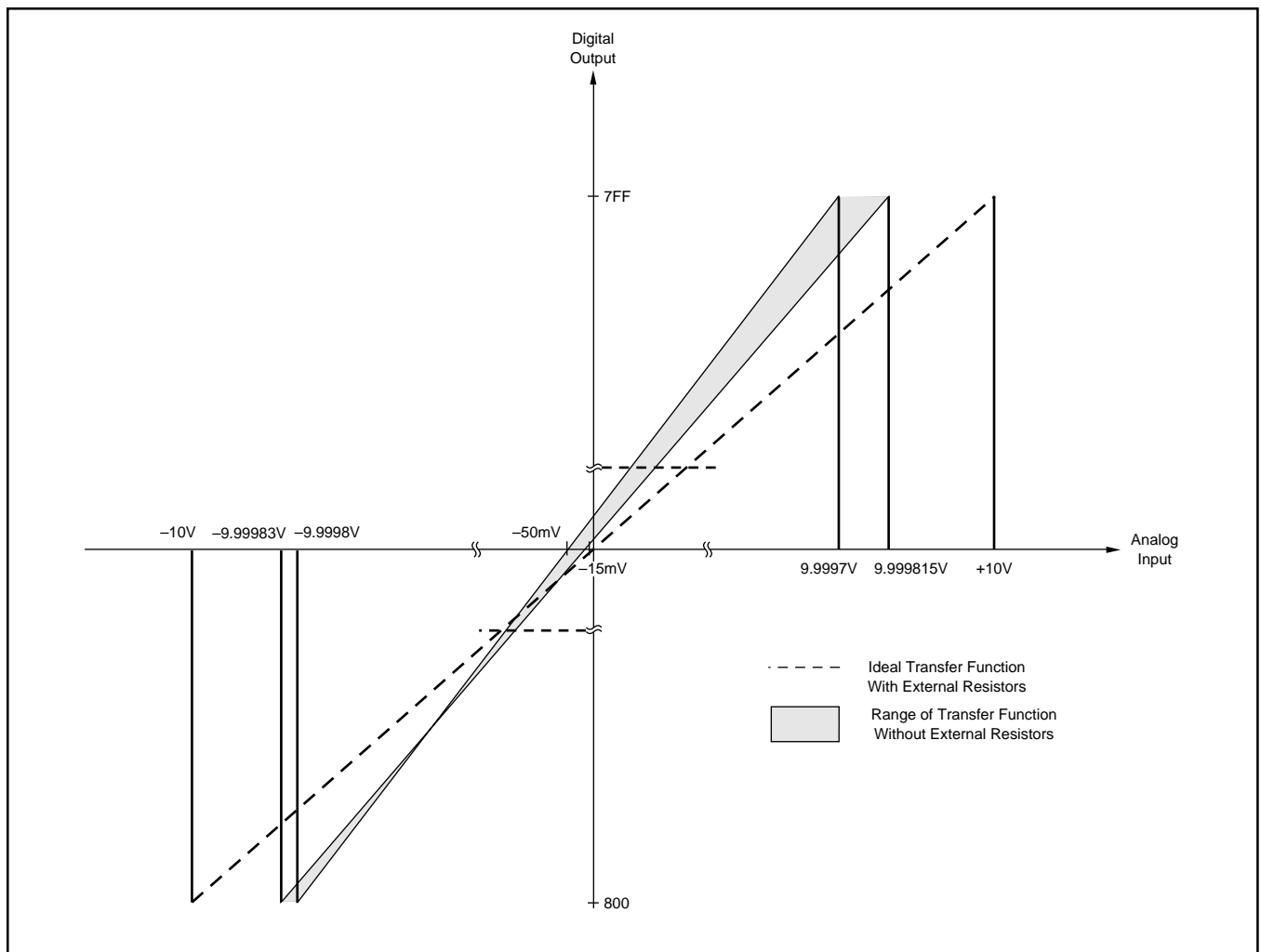


FIGURE 7. Full Scale Transfer Function.

REFERENCE

The ADS7804 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = $\pm 0.5\%$ for low grade, $\pm 0.25\%$ for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2 μ F capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2 μ F capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1 μ F can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2 μ F will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a DC load. DC loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7804. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7804 uses 90% of its power for the analog circuitry. The ADS7804 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7804. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7804, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7804.

The resistive front end of the ADS7804 also provides a guaranteed $\pm 25V$ overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7804 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

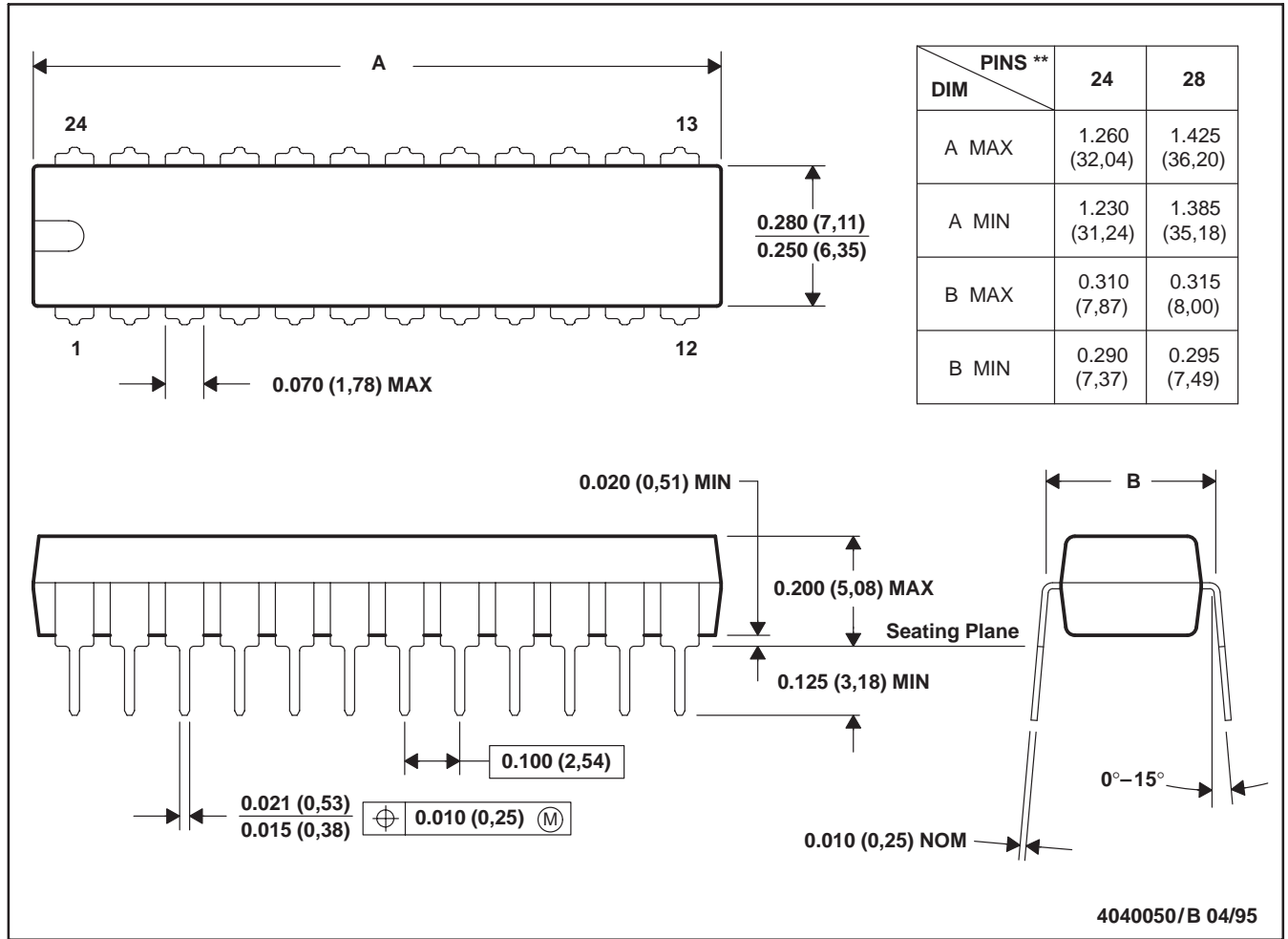
Intermediate latches are beneficial on any monolithic A/D converter. The ADS7804 has an internal LSB size of $610\mu V$. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effects of this phenomenon will be more obvious when using the pin-compatible ADS7805 or any of the other 16-bit converters in the ADS Family. This is due to the smaller internal LSB size of $38\mu V$.

PACKAGE DRAWINGS

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



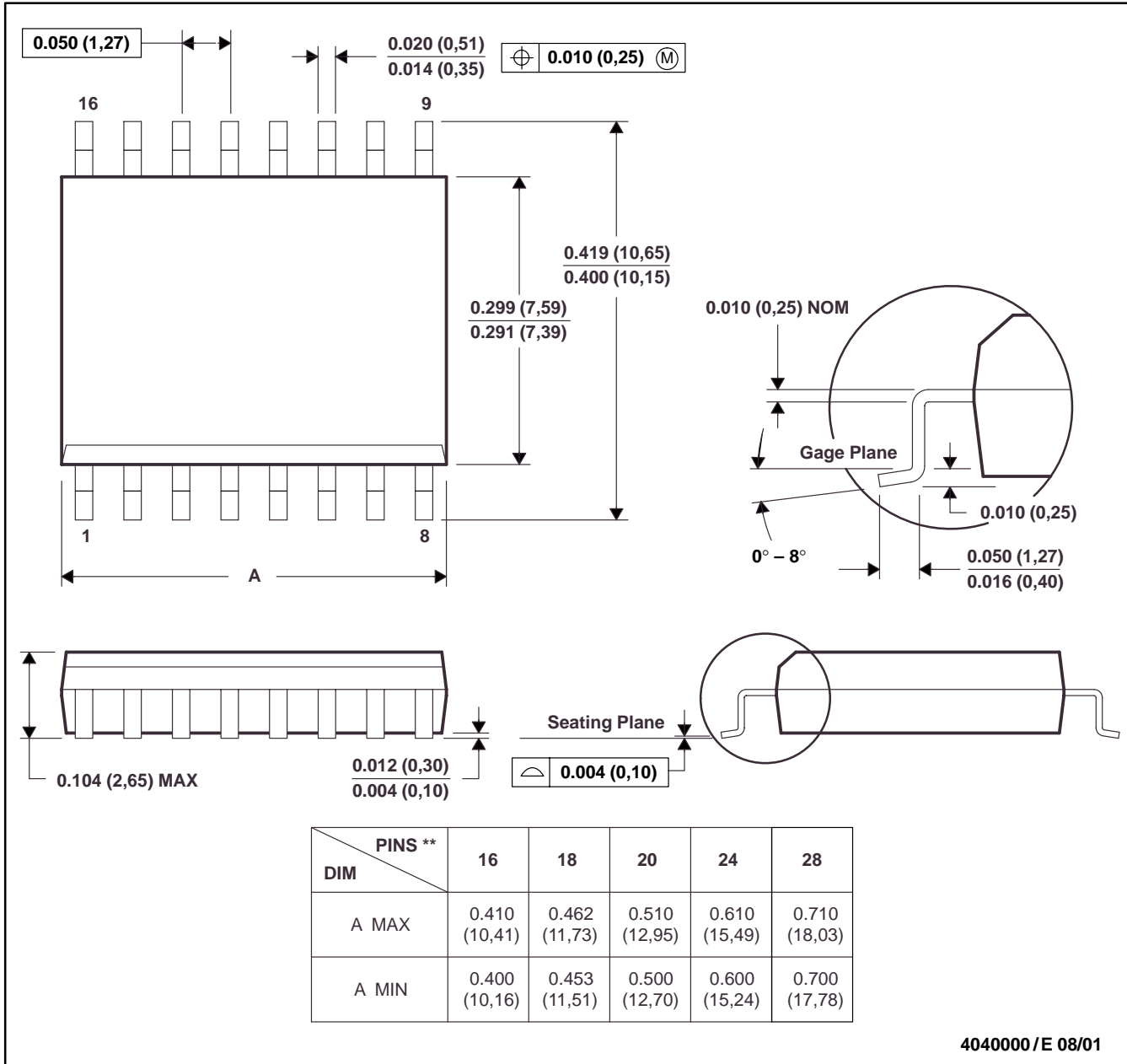
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

PACKAGE DRAWINGS (Cont.)

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| ADS7804U | Active | Production | SOIC (DW) 28 | 20 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS7804U B |
| ADS7804U.A | Active | Production | SOIC (DW) 28 | 20 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS7804U B |
| ADS7804U/1K | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | Call TI | Level-3-260C-168 HR | -40 to 85 | ADS7804U B |
| ADS7804U/1K.A | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | Call TI | Level-3-260C-168 HR | -40 to 85 | ADS7804U B |
| ADS7804UB | Active | Production | SOIC (DW) 28 | 20 TUBE | Yes | Call TI | Level-3-260C-168 HR | -40 to 85 | ADS7804U |
| ADS7804UB.A | Active | Production | SOIC (DW) 28 | 20 TUBE | Yes | Call TI | Level-3-260C-168 HR | -40 to 85 | ADS7804U |
| ADS7804UG4 | Active | Production | SOIC (DW) 28 | 20 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS7804U B |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

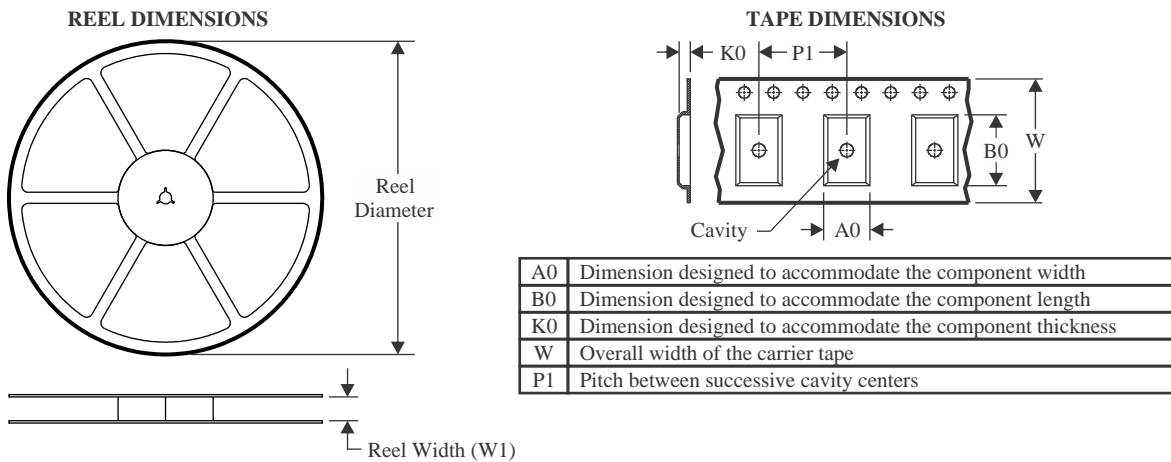
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

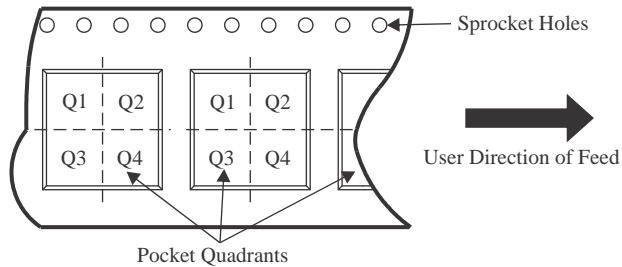
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TAPE AND REEL INFORMATION



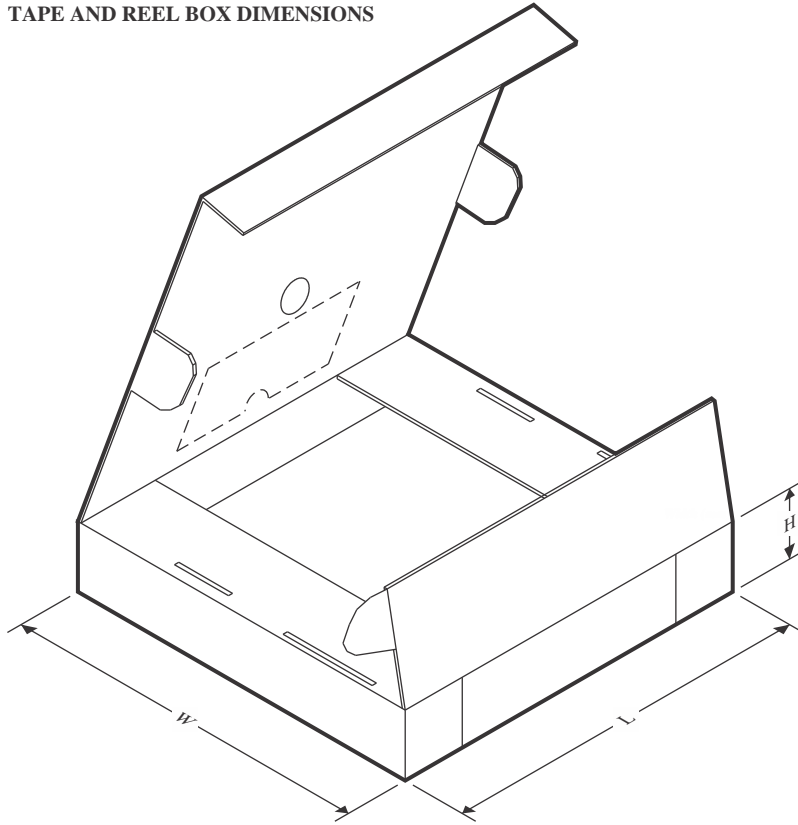
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS7804U/1K | SOIC | DW | 28 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

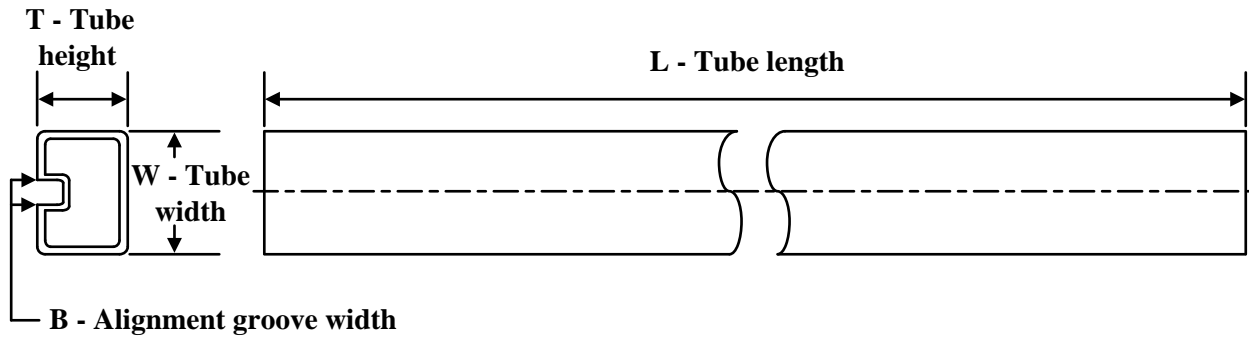
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS7804U/1K | SOIC | DW | 28 | 1000 | 356.0 | 356.0 | 53.0 |

TUBE



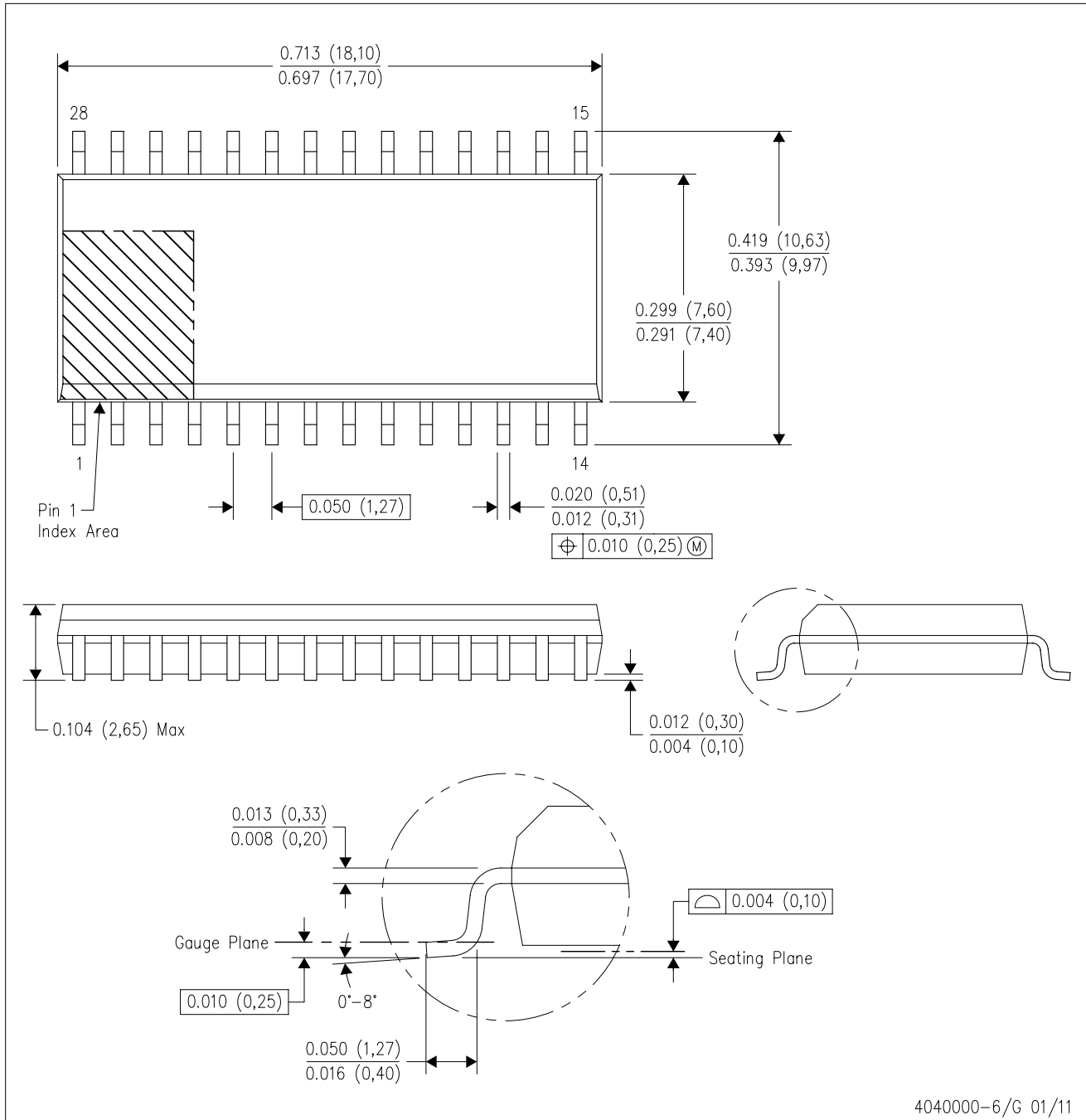
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| ADS7804U | DW | SOIC | 28 | 20 | 507 | 12.83 | 5080 | 6.6 |
| ADS7804U.A | DW | SOIC | 28 | 20 | 507 | 12.83 | 5080 | 6.6 |
| ADS7804UB | DW | SOIC | 28 | 20 | 507 | 12.83 | 5080 | 6.6 |
| ADS7804UB.A | DW | SOIC | 28 | 20 | 507 | 12.83 | 5080 | 6.6 |
| ADS7804UG4 | DW | SOIC | 28 | 20 | 507 | 12.83 | 5080 | 6.6 |

MECHANICAL DATA

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

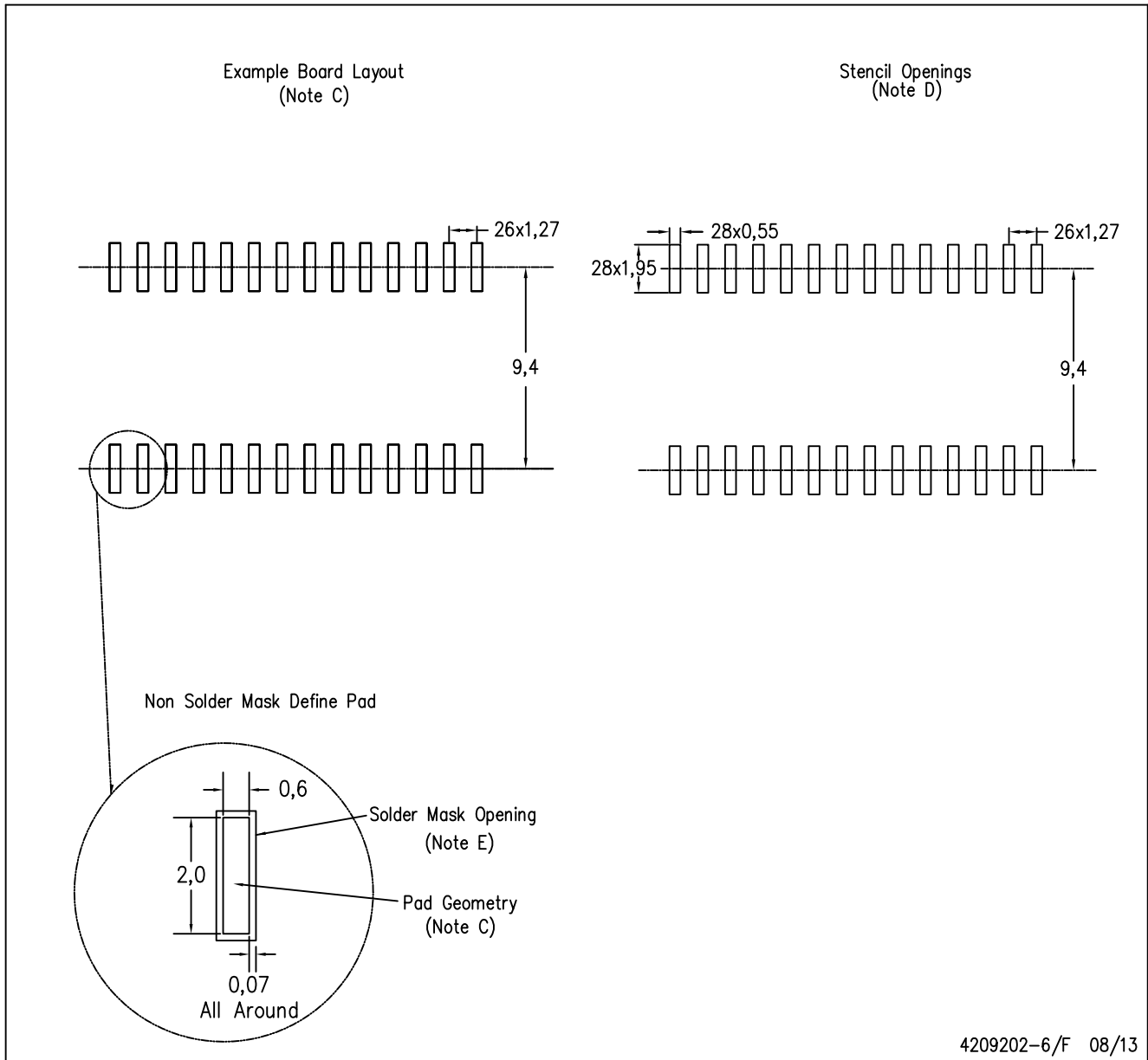


- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AE.

LAND PATTERN DATA

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Refer to IPC7351 for alternate board design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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