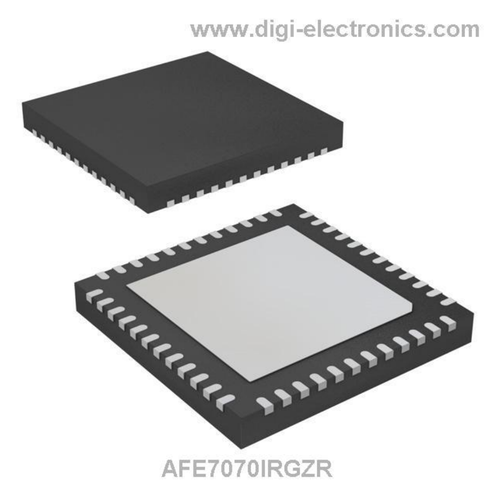
AFE7070IRGZR Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	AFE7070IRGZR-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	AFE7070IRGZR
Description	IC DAC 14BIT V-OUT 48VQFN
Detailed Description	14 Bit Digital to Analog Converter 2 48-VQFN (7x7)

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
AFE7070IRGZR	Texas Instruments
Series:	Product Status:
-	Active
DiGi-Electronics Programmable:	Number of Bits:
Not Verified	14
Number of D/A Converters:	Settling Time:
2	-
Output Type:	Differential Output:
Voltage - Buffered	No
Data Interface:	Reference Type:
Parallel	Internal
Voltage - Supply, Analog:	Voltage - Supply, Digital:
1.71V ~ 1.89V, 3.15V ~ 3.45V	1.71V ~ 1.89V
INL/DNL (LSB):	Architecture:
-	-
Operating Temperature:	Package / Case:
-40°C ~ 85°C	48-VFQFN Exposed Pad
Supplier Device Package:	Mounting Type:
48-VQFN (7x7)	Surface Mount
Base Product Number:	
AFE7070	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

Dual 14-Bit 65-MSPS Digital-to-Analog Converter With Integrated Analog Quadrature Modulator

Check for Samples: AFE7070

FEATURES

- **Maximum Sample Rate: 65 MSPS**
- **Low Power:**
    - **325 mW LVDS Output Mode**
    - **334 mW Analog Output Mode**
- **Interleaved CMOS Input, 1.8–3.3 V IOVDD**
- **Input FIFO for Independent Data and DAC Clocks**
- **3- or 4-pin SPI Interface for Register Programming**
- **Complex NCO (DDS): 32-Bit Frequency, 16-Bit Phase**
- **Quadrature Modulator Correction: Gain, Phase, Offset for Sideband and LO Suppression**
- **Analog Baseband Filter With Programmable Bandwidth: 20-MHz Maximum RF Bandwidth**
- **RF Ouput: Analog (linear) or LVDS (Clock)**
- **RF Frequency Range: 100 MHz to 2.7 GHz**
- **Package: 48-Pin QFN (7-mm × 7-mm)**

APPLICATIONS

- **Low-Power, Compact Software-Defined Radios**
- **Femto- and Pico-Cell BTS**
- **Clock Frequency Translation**

DESCRIPTION

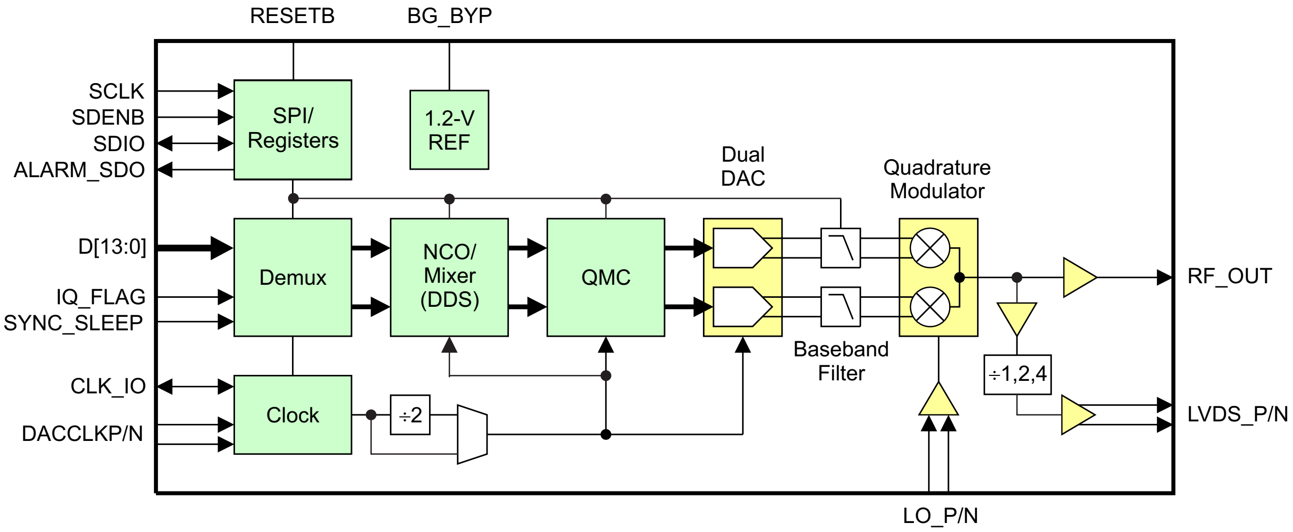
The AFE7070 is a dual 14-bit 65-MSPS digital-to-analog converter (DAC) with integrated, programmable fourth-order baseband filter and analog quadrature modulator. The AFE7070 includes additional digital signal-processing features such as a numerically controlled oscillator for frequency generation/translation, and a quadrature modulator correction circuit, providing LO and sideband suppression capability. The AFE7070 has an interleaved 14-bit 1.8-V to 3.3-V CMOS input. The AFE7070 provides 20 MHz of RF signal bandwidth with an RF output frequency range of 100 MHz to 2.7 GHz. An optional LVDS output can be used to convert the quadrature modulator output to a clock signal up to 800 MHz. Total power consumption is less than 350 mW with the LVDS output and 334 mW with the analog RF output.

The AFE7070 package is a 7-mm × 7mm 48-pin QFN package. The AFE7070 is specified over the full industrial temperature range (–40°C to 85°C).

AVAILABLE OPTIONS

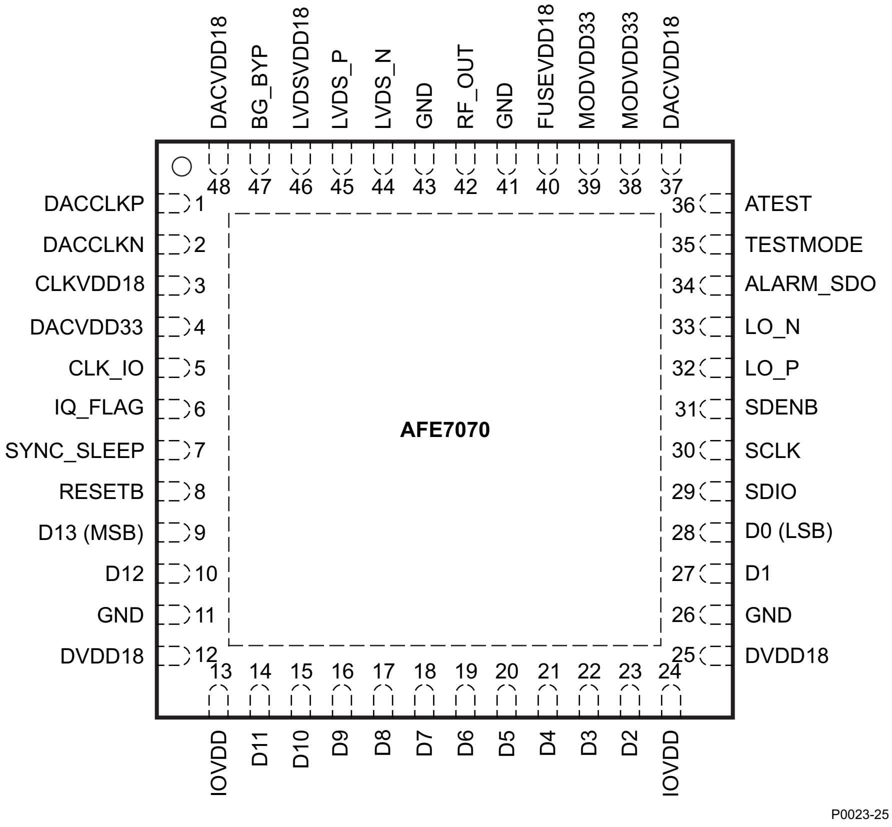
T_A	ORDER CODE	PACKAGE DRAWING/TYPE	TRANSPORT MEDIA	QUANTITY
–40°C to 85°C	AFE7070IRGZ25	RGZ / 48QFN quad flatpack no-lead	Tape and reel	25
	AFE7070IRGZT			250
	AFE7070IRGZR			2500

BLOCK DIAGRAM



PIN CONFIGURATION

RGZ Package
(Top View)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
MISC/SERIAL			
ALARM_SDO	34	O	CMOS output for ALARM condition, active-low. The ALARM output functionality is defined through the CONFIG7 registers. Optionally, it can be used as the unidirectional data output in 4-pin serial interface mode (CONFIG3 sif_4pin = 1). 1.8-V to 3.3-V CMOS, set by IOVDD.
RESETB	8	I	Resets the chip when low. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pullup
SCLK	30	I	Serial interface clock. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pulldown
SDENB	31	I	Active-low serial data enable, always an input. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pullup
SDIO	29	I/O	Bidirectional serial data in 3-pin mode (default). In 4-pin interface mode (CONFIG3 sif_4pin), the SDIO pin is an input only. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pulldown
DATA/CLOCK INTERFACE			
CLK_IO	5	I/O	Single-ended input or output CMOS level clock for latching input data. 1.8-V to 3.3-V CMOS, set by IOVDD.
D[13:0]	9, 10, 14–23, 27, 28	I	Data bits 0 through 13. D13 is the MSB, D0 is the LSB. For complex data, channel I and channel Q are multiplexed. For NCO phase data, either 14 bits are transferred at the internal sample clock rate, or 8 MSBs and 8 LSBs are interleaved on D[13:6]. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pulldown
DACCLKP, DACCLKN	1, 2	I	Differential input clock for DACs.
IQ_FLAG	6	I	When register CONFIG1 iqswap is 0, IQ-FLAG high identifies the DACA sample in dual-input or dual-output clock modes. 1.8-V or 3.3-V CMOS, set by IOVDD. Internal pulldown
SYNC_SLEEP	7	I	Multi-function. Sync signal for signal processing blocks, TX ENABLE or SLEEP function. Selectable via SPI. 1.8-V to 3.3-V CMOS, set by IOVDD.
RF			
LO_P, LO_N	32, 33	I	Local oscillator input. Can be used differentially or single-ended by terminating the unused input through a capacitor and 50-Ω resistor to GND.
LVDS_P, LVDS_N	45, 44	O	Differential LVDS output
RF_OUT	42	O	Analog RF output
REFERENCE			
ATEST	36	O	Factory use only. Do not connect.
BG_BYP	47	I	Reference voltage decoupling – connect 0.1 µF to GND.
TESTMODE	35	I	Factory use only. Connect to GND.
POWER			
IOVDD	13, 24	I	1.8-V to 3.3-V supply for CMOS I/Os
CLKVDD18	3	I	1.8 V
DVDD18	12, 25	I	1.8 V
LVDSVDD18	46	I	1.8 V
DACVDD18	37, 48	I	1.8 V
DACVDD33	4	I	3.3 V
MODVDD33	38, 39	I	3.3 V
FUSEVDD18	40	I	Connect to 1.8 V to 3.3 V supply (1.8 V is preferred to lower power dissipation).
GND	11, 26, 41, 43	I	Ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE
Supply voltage range	DACVDD33, MODVDD33, FUSEVDD18, IOVDD(2)	–0.5 V to 4 V
	DVDD18, CLKVDD18, DACVDD18(2)	–0.5 V to 2.3 V
Supply voltage range(2)		–0.5 V to 4 V
	D[13..0], IQ FLAG, SYNC_SLEEP, SCLK, SDENB, SDIO, ALARM_SDO, RESETB , CLK_IO, TESTMODE	–0.5 V to IOVDD + 0.5 V
	DACCLKP, DACCLKN	–0.5 V to CLKVDD18 + 0.5 V
	LVDS_P, LVDS_N	–0.5 V to LVDSVDD18 + 0.5 V
	BG_BYP, ATEST	–0.5 V to DACVDD33 + 0.5 V
	RFOUT, LO_P, LO_N	–0.5 V to MODVDD33 + 0.5 V
Operating free-air temperature range, T_A		–40°C to 85°C
Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Measured with respect to GND

DC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC SPECIFICATIONS						
	DAC resolution		14			Bits
REFERENCE OUTPUT						
	Reference voltage		1.14	1.2	1.26	V
POWER SUPPLY						
IOVDD	I/O supply voltage		1.71		3.6	V
DVDD18	Digital supply voltage		1.71	1.8	1.89	V
CLKVDD18	Clock supply voltage		1.71	1.8	1.89	V
DACVDD18	DAC 1.8-V analog supply voltage		1.71	1.8	1.89	V
LVDSVDD18	LVDS analog supply voltage		1.71	1.8	1.89	V
FUSEVDD18	FUSE analog supply voltage	Connect to 1.8-V supply for lower power	1.71	1.8	3.6	V
DACVDD33	DAC 3.3-V analog supply voltage		3.15	3.3	3.45	V
MODVDD33	Modulator analog supply voltage		3.15	3.3	3.45	V
I_{IOVDD}	I/O supply current					mA
I_{DVDD18}	Digital supply current			18		mA
$I_{CLKVDD18}$	Clock supply current					mA
$I_{DACVDD18}$	DAC 1.8-V supply current					mA
$I_{LVDSVDD18}$	LVDS output supply current					mA
$I_{FUSEVDD18}$	FUSE supply current			21		mA
$I_{DACVDD33}$	DAC 3.3-V supply current					mA
$I_{MODVDD33}$	Modulator supply current			68		mA
	Power dissipation	LVDS output: NCO, QMC active, f_{DAC} = 40 MHz, IOVDD = 2.5 V		337	380	mW
		Analog output: NCO off, QMC active, f_{DAC} = 65 MHz, IOVDD = 2.5 V		335	380	mW
		Sleep mode with clock, internal reference on, IOVDD = 2.5 V		80		mW
		Sleep mode without clock, internal reference off, IOVDD = 2.5 V		5	25	mW
POWER SUPPLY vs MODE						
	3.3-V supplies (DACVDD33, MODVDD33, IOVDD)	NCO = 1 MHz, LVDS on, RF out off, no input data, 65 MSPS		72		mA
	1.8-V supplies (DVDD18, CLKVDD18, DACVDD18, FUSEVD18, LVDSVDD18)			47		mA
	Power dissipation			322		mW

DC ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	3.3-V supplies (DACVDD33, MODVDD33, IOVDD)	NCO = 1 MHz, LVDS on, RF out off, no input data, 40 MSPS		71		mA
	1.8-V supplies (DVDD18, CLKVDD18, DACVDD18, FUSEVDD18, LVDSVDD18)			32		mA
	Power dissipation			337		mW
	3.3-V supplies (DACVDD33, MODVDD33, IOVDD)	1 MHz full-scale input, RF out on, LVDS output off, NCO off, QMC on, 65 MSPS		102		mA
	1.8-V supplies (DVDD18, CLKVDD18, DACVDD18, FUSEVD18, LVDSVDD18)			36		mA
	Power dissipation			334		mW
	3.3-V supplies (DACVDD33, MODVDD33, IOVDD)	1 MHz full-scale input, RF out on, LVDS output off, NCO off, QMC off, 32.5 MSPS		101		mA
	1.8-V supplies (DVDD18, CLKVDD18, DACVDD18, FUSEVD18, LVDSVDD18)			22		mA
	Power dissipation			325		mW

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (D[13:0], IQ_FLAG, SDI, SCLK, SDENB, RESETB, SYNC_SLEEP, ALARM_SDO, CLK_IO)						
V_{IH}	High-level input voltage	IOVDD = 3.3 V	2.3			V
		IOVDD = 2.5 V	1.75			
		IOVDD = 1.8 V	1.25			
V_{IL}	Low-level input voltage	IOVDD = 3.3 V			1	V
		IOVDD = 2.5 V			0.75	
		IOVDD = 1.8 V			0.54	
I_{IH}	High-level input current	IOVDD = 3.3 V	–80		80	µA
I_{IL}	Low-level input current	IOVDD = 3.3 V	–80		80	µA
C_i	Input capacitance			5		pF
f_{DAC}	DAC sample rate	Interleaved data, f_{DAC} = 1/2 × f_{INPUT}	0		65	MSPS
f_{INPUT}	Input data rate	Interleaved data, f_{INPUT} = 2 × f_{DAC}	0		130	MSPS
DIGITAL OUTPUTS (ALARM_SDO, SDIO, CLK_IO)						
V_{OH}	High-level output voltage	I_{LOAD} = –100 µA	IOVDD – 0.2			V
		I_{LOAD} = –2 mA	0.8 × IOVDD			V
V_{OL}	Low-level output voltage	I_{LOAD} = 100 µA			0.2	V
		I_{LOAD} = 2 mA			0.22 × IOVDD	V
CLOCK INPUT (DACCLKP/DACCLKN)						
	DACCLKP/N duty cycle		40%		60%	
	DACCLKP/N differential voltage		0.4		1	V
Timing Parallel Data Input (D[13:0], IQ_FLAG, SYNC_SLEEP) – Dual Input Clock Mode						
t_{SU}	Input setup time	Relative to CLK_IO rising edge		1		ns
t_H	Input hold time	Relative to CLK_IO rising edge		1		ns
t_{LPH}	Input clock pulse high time			3		ns
Timing Parallel Data Input (D[13:0], IQ_FLAG, SYNC_SLEEP) – Dual Output Clock Mode						
t_{SU}	Input setup time	Relative to CLK_IO rising edge	1	0.2		ns
t_H	Input hold time	Relative to CLK_IO rising edge	1	0.2		ns
Timing Parallel Data Input (D[13:0], IQ_FLAG, SYNC_SLEEP) – Single Differential DDR and SDR Clock Modes						
t_{SU}	Input setup time	Relative to DACCLKP/N rising edge	0	–0.8		ns
t_H	Input hold time	Relative to DACCLKP/N rising edge	2	1		ns
Timing – Serial Data Interface						
$t_{S(SDENB)}$	Setup time, SDENB to rising edge of SCLK			20		ns
$t_{S(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK			10		ns
$t_{H(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK			5		ns
t_{SCLK}	Period of SCLK			100		ns
t_{SCLKH}	High time of SCLK			40		ns
t_{SCLKL}	Low time of SCLK			40		ns
$t_{D(DATA)}$	Data output delay after falling edge of SCLK			10		ns
t_{RESET}	Minimum RESETB pulse duration			25		ns

AC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LO INPUT						
f_{LO}	LO frequency range		0.1		2.7	GHz
P_{LO_IN}	LO input power		–5		5	dBm
	LO port return loss			15		
LVDS OUTPUT						
f_{LVDS_OUT}	LVDS output frequency		100		800	MHz
INTEGRATED BASEBAND FILTER						
	Baseband attenuation at setting Filtertune = 8 relative to low-frequency signal	2.5 MHz		1		dB
		5 MHz		18		
		10 MHz		42		
		20 MHz		65		
	Baseband attenuation at setting Filtertune = 0 relative to low-frequency signal	10 MHz		1		dB
		20 MHz		18		
		40 MHz		42		
		55 MHz		58		
	Baseband filter phase linearity	RMS phase deviation from linear phase across minimum or maximum cutoff frequency		2		Degrees
	Baseband filter amplitude ripple	Frequency < 0.9 × nominal cutoff frequency		0.5		dB
RF Output Parameters – f_{LO} = 100 MHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power	Full-scale 50-kHz digital sine wave		–1		dBm
IP2	Output IP2	Maximum LPF BW setting, f_{BB} = 4.5, 5.5 MHz		63		dBm
IP3	Output IP3	Maximum LPF BW setting, f_{BB} = 4.5, 5.5 MHz		18		dBm
	Carrier feedthrough	Unadjusted, f_{BB} = 50 kHz, full scale		45		dBc
	Sideband suppression	Unadjusted, f_{BB} = 50 kHz, full scale		27		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		137		dBc/Hz
	Output return loss			8.5		dB
RF Output Parameters – f_{LO} = 450 MHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power	Full-scale 50-kHz digital sine wave		0.2		dBm
IP2	Output IP2	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		67		dBm
IP3	Output IP3	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		19		dBm
	Carrier feedthrough	Unadjusted, f_{BB} = 50 kHz, full scale		45		dBc
	Sideband Suppression	Unadjusted, f_{BB} = 50 kHz, full scale		38		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		143		dBc/Hz
	Output return loss			8.5		dB
RF Output Parameters – f_{LO} = 850 MHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power	Full-scale 50-kHz digital sine wave		0.3		dBm
IP2	Output IP2	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		64		dBm
IP3	Output IP3	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		19		dBm
	Carrier feedthrough	Unadjusted, f_{BB} = 50 kHz, full scale		41		dBc
	Sideband suppression	Unadjusted, f_{BB} = 50 kHz, full scale		37		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		143		dBc/Hz
	Output return loss			8.5		dB
ACPR	Adjacent-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		65		dBc
		10-MHz LTE, PAR = 10 dB, P_{OUT} = –10 dBFS		61		dBc

AC ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ALT1	Alternate-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		66		dBc
RF Output Parameters – f_{LO} = 2.1 GHz, Analog Output						
P_{OUT_FS}	Fullscale RF output power			–1.5		dBm
IP2	Output IP2			50		dBm
IP3	Output IP3			19		dBm
	Carrier feedthrough			38		dBc
	Sideband suppression			42		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		141		dBc/Hz
	Output return loss			8.5		dB
ACPR	Adjacent-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		65		dBc
		20 MHz LTE, PAR = 10 dB, P_{OUT} = - 10 dBFS		61		dBc
ALT1	Alternate-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		65		dBc
RF Output Parameters – f_{LO} = 2.7 GHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power			–3.6		dBm
IP2	Output IP2			48		dBm
IP3	Output IP3			17		dBm
	Carrier feedthrough			36		dBc
	Sideband suppression			35		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		139		dBc/Hz
	Output return loss			8.5		dB
RF Output Parameters – f_{LO} = 622 MHz, LVDS Output, ÷4						
V_{OD}	Differential output voltage	Assumes a 100-Ω differential load	247	350	454	mV
V_{OC}	Common-mode output voltage		1.125	1.25	1.375	V
	Output noise floor	≥ 13 MHz offset, f_{BB} = 1 MHz				
	Carrier feedthrough	Unadjusted, f_{BB} = 50 kHz, full scale		40		dBc
	Sideband suppression	Unadjusted, f_{BB} = 50 kHz, full cale		40		dBc

TYPICAL PERFORMANCE PLOTS

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

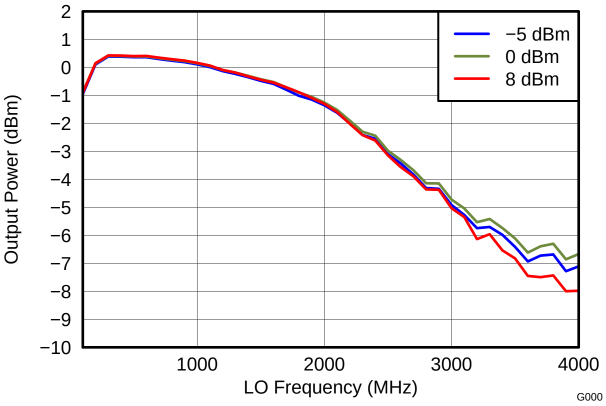


Figure 1. Output Power vs LO Frequency and LO Power

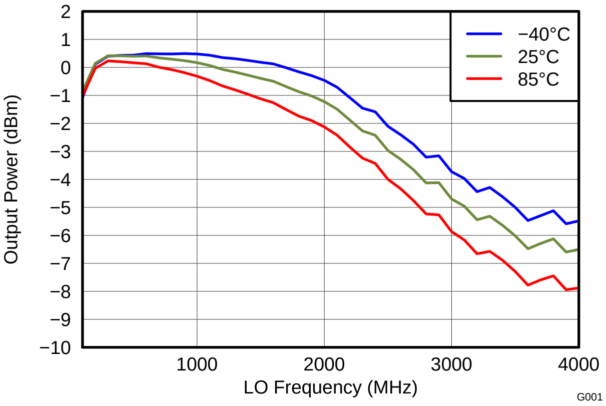


Figure 2. Output Power vs LO Frequency and Temperature

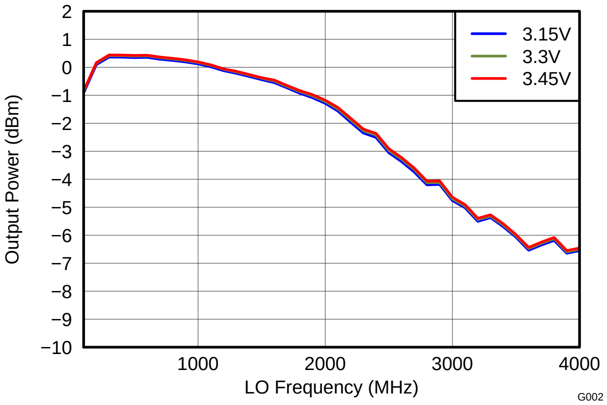


Figure 3. Output Power vs LO Frequency and Supply Voltage

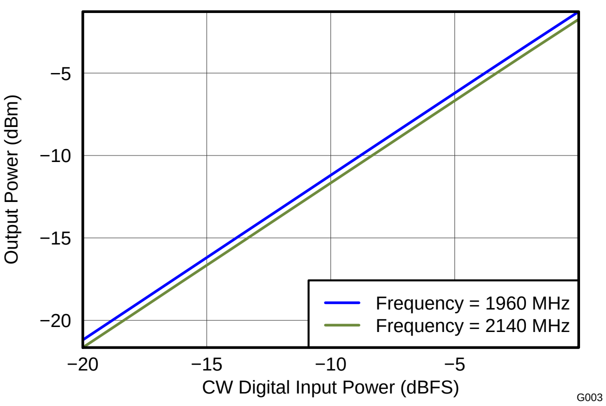


Figure 4. Output Power vs Input Power and LO Frequency

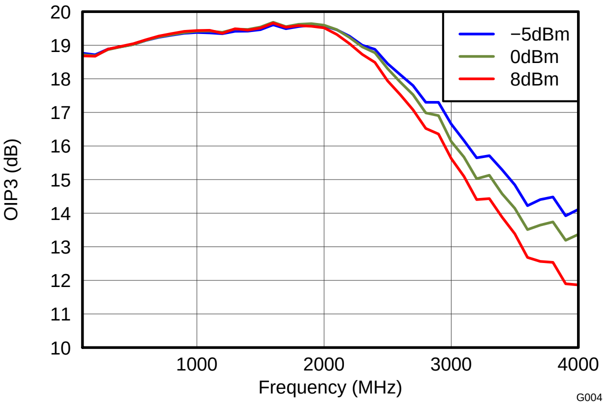


Figure 5. OIP3 vs LO Frequency and LO Power

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

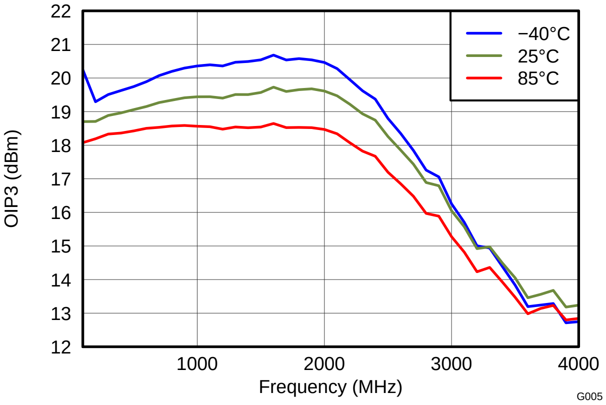


Figure 6. OIP3 vs LO Frequency and Temperature

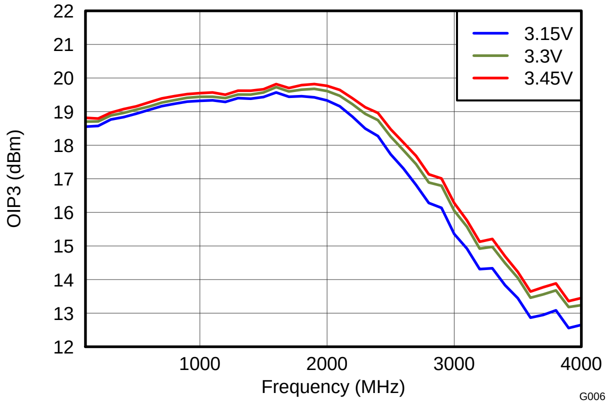


Figure 7. OIP3 vs LO Frequency and Supply Voltage

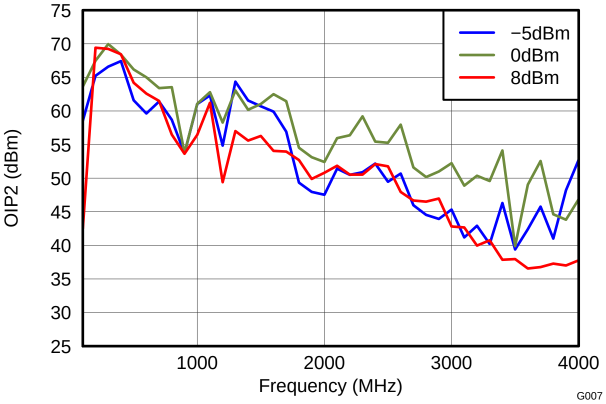


Figure 8. OIP2 vs LO Frequency and LO Power

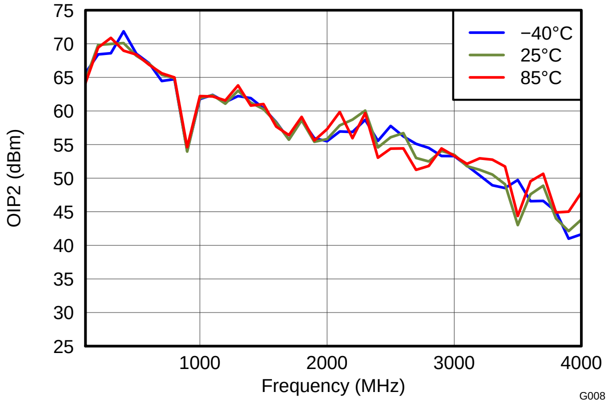


Figure 9. OIP2 vs LO Frequency and Temperature

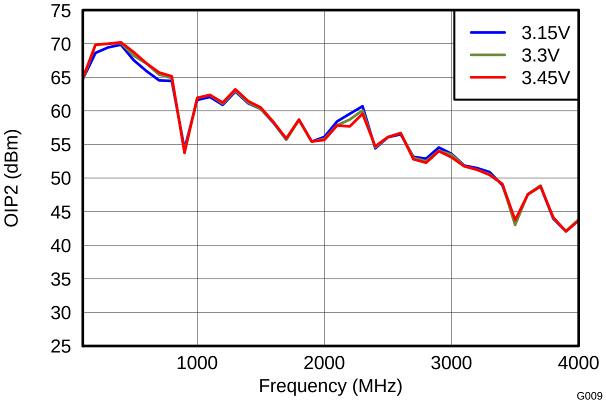


Figure 10. OIP2 vs LO Frequency and Supply Voltage

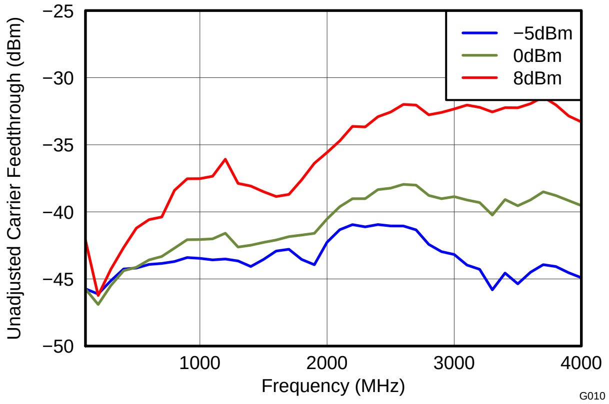


Figure 11. Unadjusted Carrier Feethrough vs LO Frequency and LO Power

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

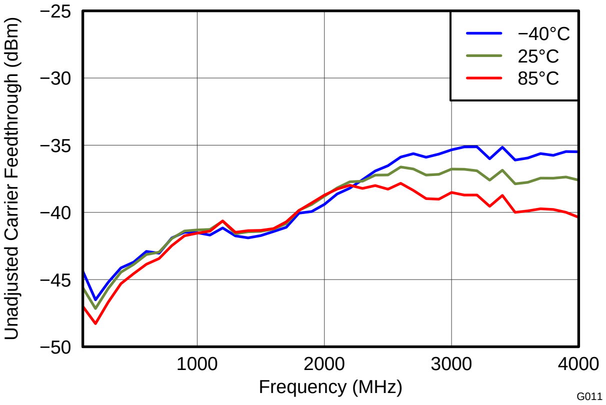


Figure 12. Unadjusted Carrier Feethrough vs LO Frequency and Temperature

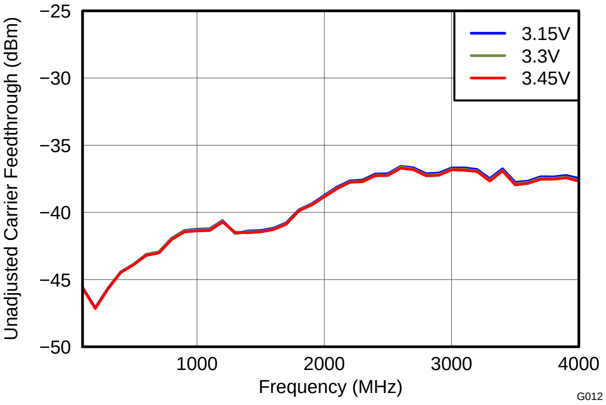


Figure 13. Unadjusted Carrier Feethrough vs LO Frequency and Supply Voltage

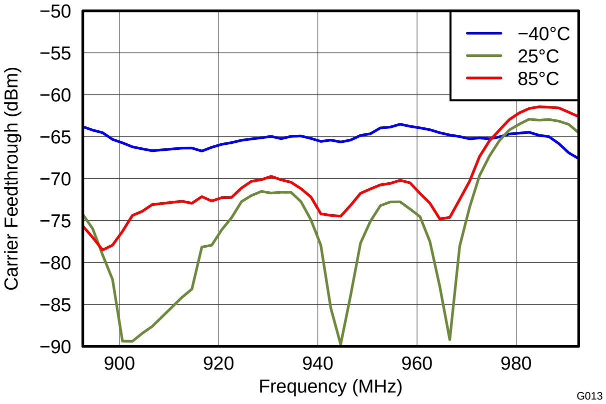


Figure 14. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 940 MHz

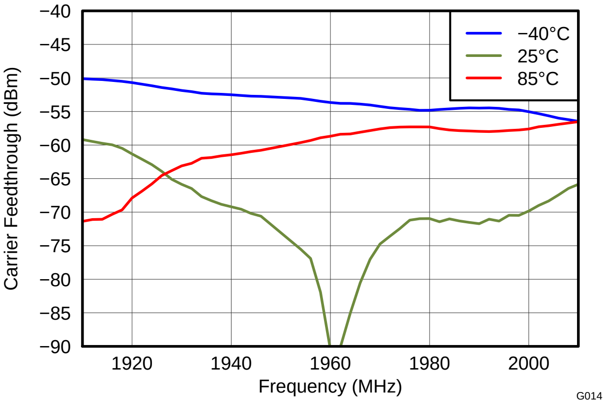


Figure 15. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 1960 MHz

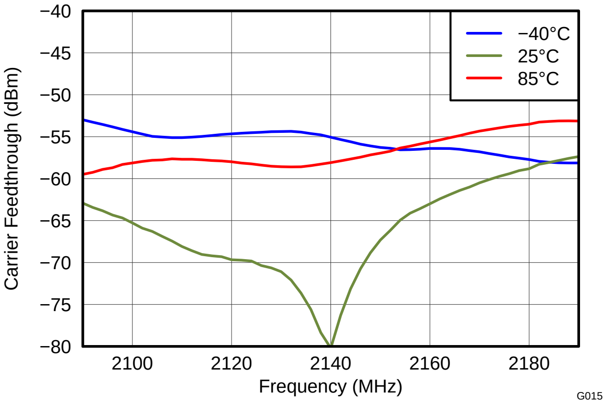


Figure 16. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 2140 MHz

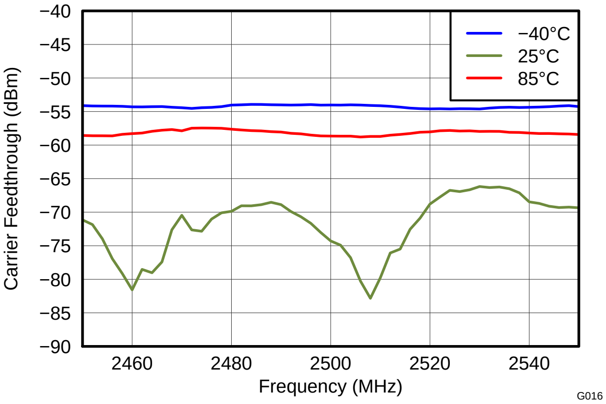


Figure 17. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 2500 MHz

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

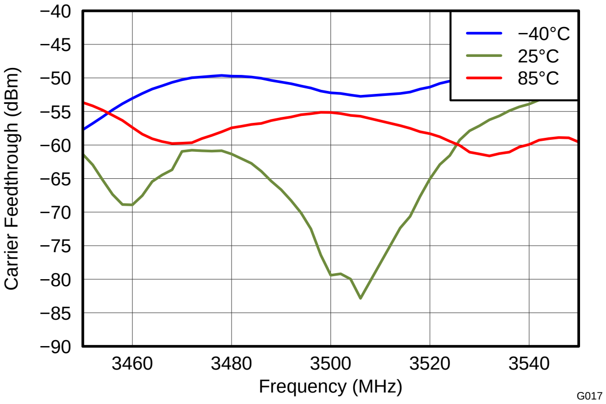


Figure 18. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 3500 MHz

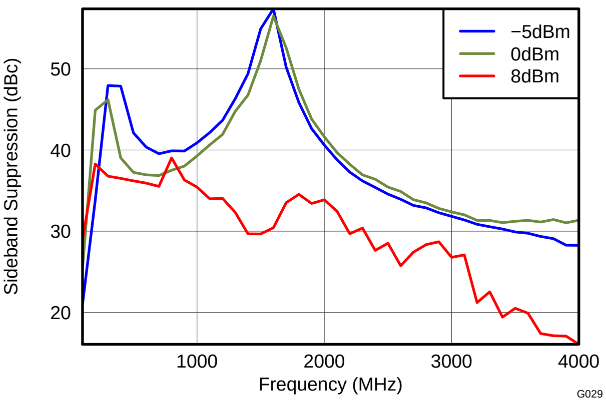


Figure 19. Unadjusted Sideband Suppression vs LO Frequency and LO Power

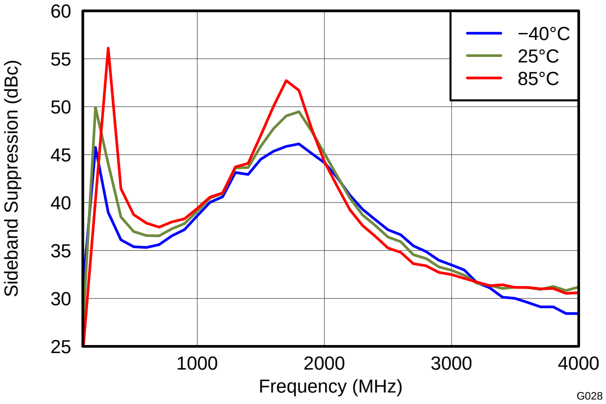


Figure 20. Unadjusted Sideband Suppression vs LO Frequency and Temperature

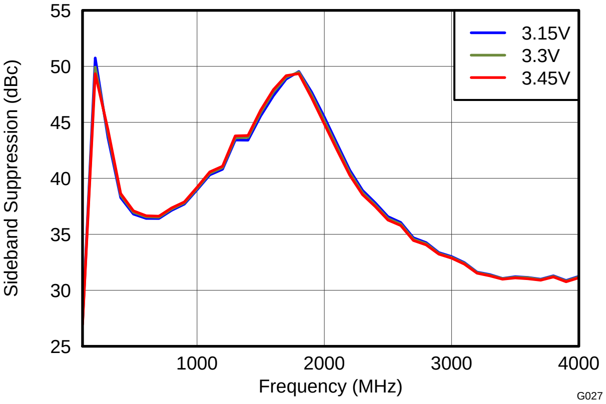


Figure 21. Unadjusted Sideband Suppression vs LO Frequency and Supply Voltage

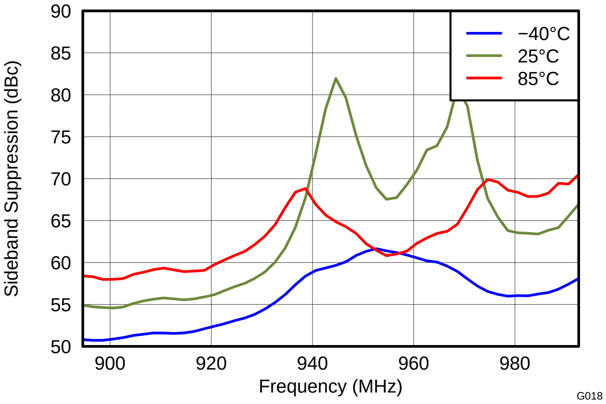


Figure 22. Adjusted Sideband Suppression vs LO Frequency and Temperature at 940 MHz

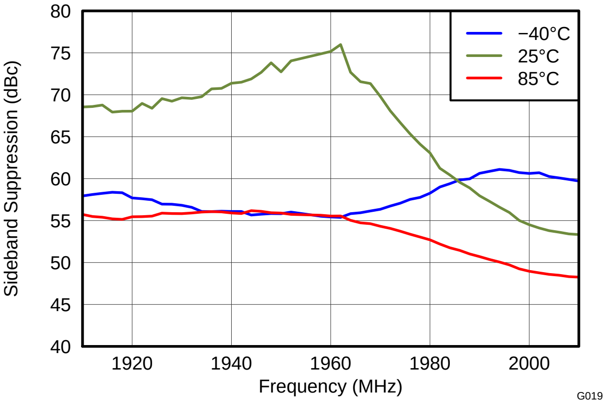


Figure 23. Adjusted Sideband Suppression vs LO Frequency and Temperature at 1960 MHz

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

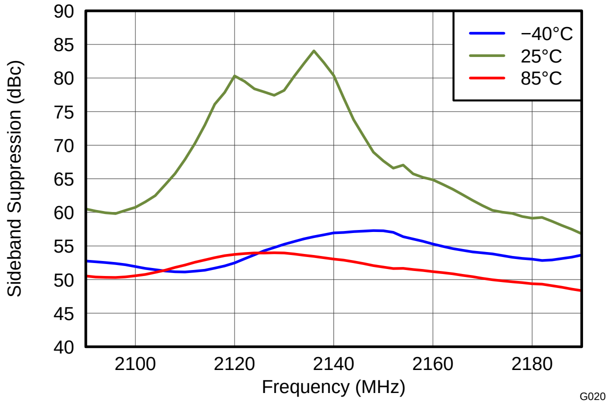


Figure 24. Adjusted Sideband Suppression vs LO Frequency and Temperature at 2140 MHz

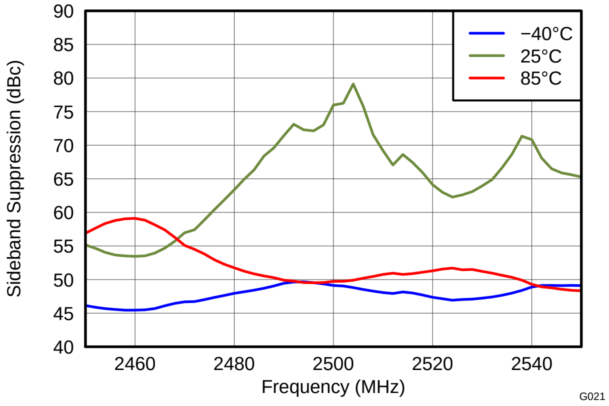


Figure 25. Adjusted Sideband Suppression vs LO Frequency and Temperature at 2500 MHz

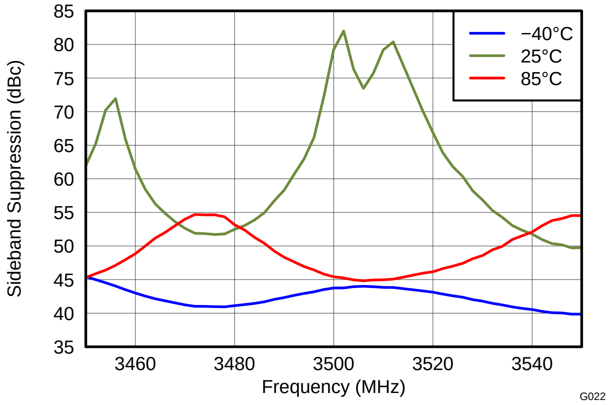


Figure 26. Adjusted Sideband Suppression vs LO Frequency and Temperature at 3500 MHz

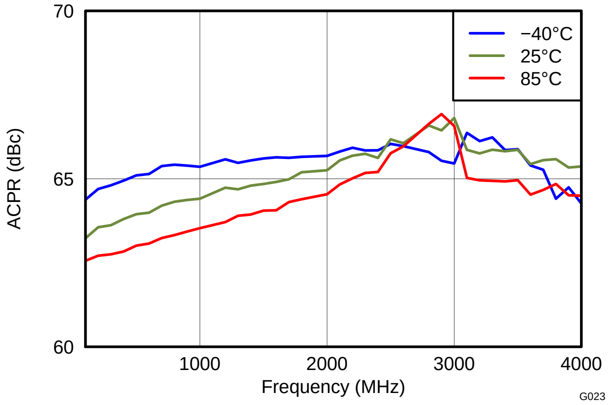


Figure 27. WCDMA Adjacent-Channel Power Ratio (ACPR) vs Temperature

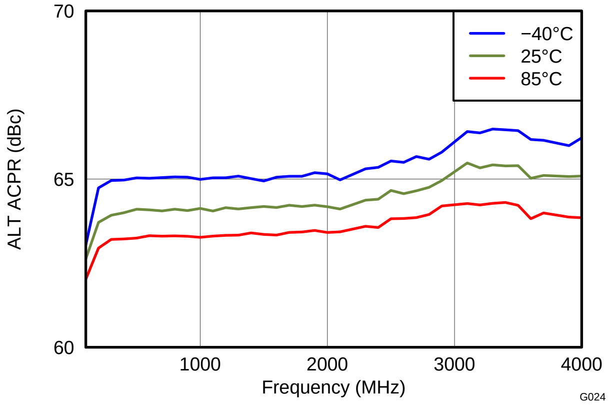


Figure 28. WCDMA Adjacent-Channel Power Ratio (Alt-ACPR) vs Temperature

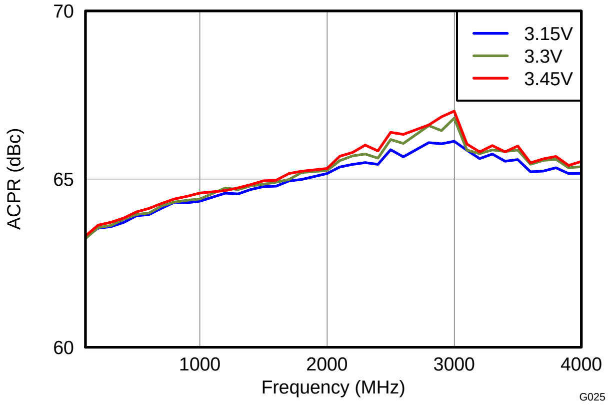


Figure 29. WCDMA Adjacent-Channel Power Ratio (ACPR) vs Supply Voltage

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

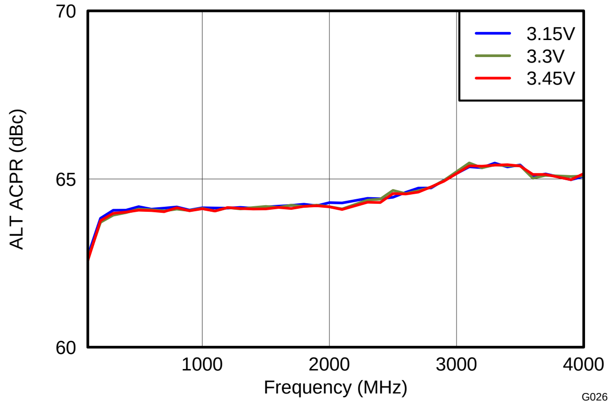


Figure 30. WCDMA Adjacent-Channel Power Ratio (Alt-ACPR) vs Supply Voltage

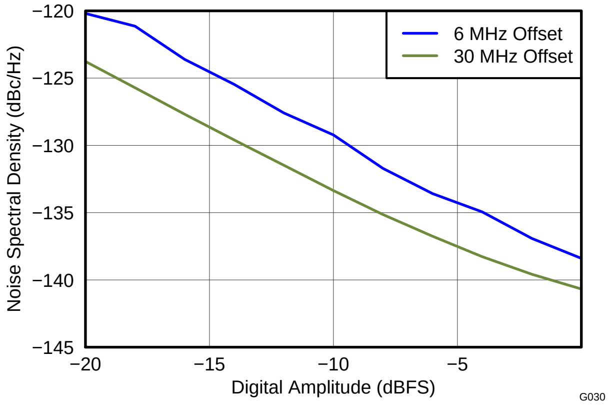


Figure 31. Noise Spectral Density (NSD) vs Input Power and LO Frequency

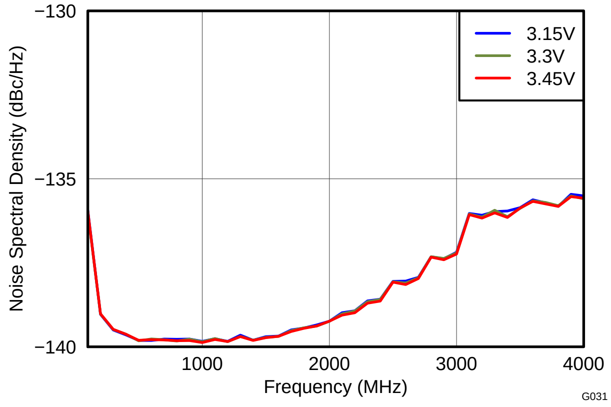


Figure 32. Noise Spectral Density (NSD) at 6-MHz Offset vs LO Frequency and Supply Voltage

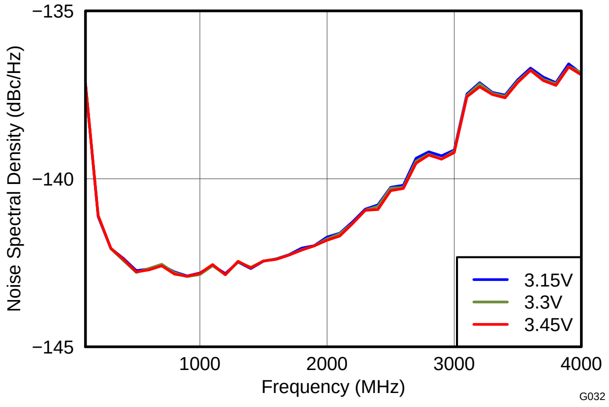


Figure 33. Noise Spectral Density (NSD) at 30-MHz Offset vs LO Frequency and Supply Voltage

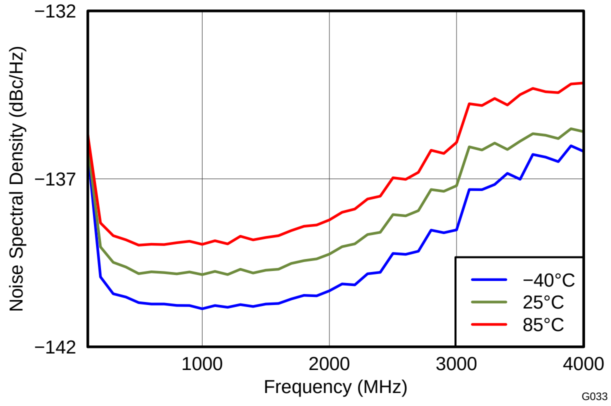


Figure 34. Noise Spectral Density (NSD) at 6-MHz Offset vs LO Frequency and Temperature

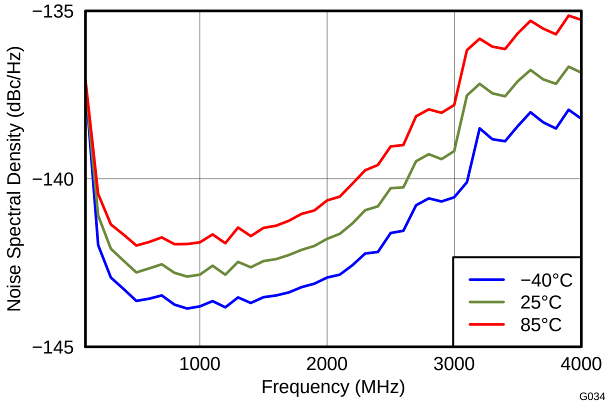


Figure 35. Noise Spectral Density (NSD) at 30-MHz Offset vs. LO Frequency and Temperature

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

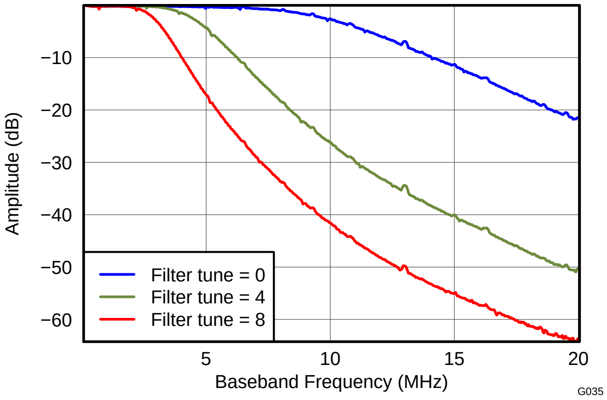


Figure 36. Baseband Filter Response

SERIAL INTERFACE

The serial port of the AFE7070 is a flexible serial interface which communicates with industry-standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of the AFE7070. The serial port is compatible with most synchronous transfer formats and can be configured as a 3- or 4-pin interface by **sif_4pin** in **CONFIG3 (bit6)**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For the 3-pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For the 4-pin configuration, **SDIO** is data-in only and **ALARM_SDO** is data-out only. Data is input into the device with the rising edge of **SCLK**. Data is output from the device on the falling edge of **SCLK.**

Each read/write operation is framed by signal **SDENB** (serial data-enable bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle, which identifies the following data transfer cycle as read or write, how many bytes to transfer, and the address to which to transfer the data. Table 1 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 through 5 comprise the data transfer cycle.

Table 1. Instruction Byte of the Serial Interface

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

R/W	Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from the AFE7070, and a low indicates a write operation to the AFE7070.
[N1 : N0]	Identifies the number of data bytes to be transferred, as listed in Table 2. Data is transferred MSB first.

Table 2. Number of Transferred Bytes Within One Communication Frame

N1	N0	DESCRIPTION
0	0	Transfer 1 byte
0	1	Transfer 2 bytes
1	0	Transfer 3 bytes
1	1	Transfer 4 bytes

[A4 : A0]	Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the AFE7070 MSB first and counts down for each byte.

Figure 37 shows the serial interface timing diagram for an AFE7070 write operation. **SCLK** is the serial interface clock input to AFE7070. Serial data enable **SDENB** is an active-low input to the AFE7070. **SDIO** is serial data in. Input data to the AFE7070 is clocked on the rising edges of **SCLK**.

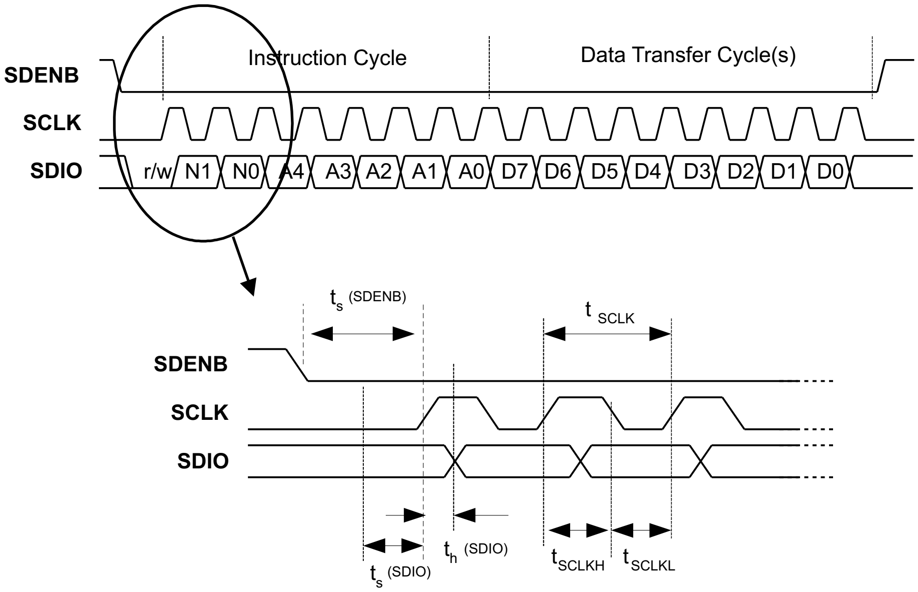


Figure 37. Serial Interface Write Timing Diagram

Figure 38 shows the serial interface timing diagram for an AFE7070 read operation. **SCLK** is the serial interface clock input to AFE7070. Serial data enable **SDENB** is an active-low input to the AFE7070. **SDIO** is serial data-in during the instruction cycle. In the 3-pin configuration, **SDIO** is data-out from the AFE7070 during the data transfer cycle(s), while **ALARM_SDO** is in a high-impedance state. In the 4-pin configuration, **ALARM_SDO** is data-out from the AFE7070 during the data transfer cycle(s). At the end of the data transfer, **ALARM_SDO** outputs low on the final falling edge of **SCLK** until the rising edge of **SDENB**, when it enters the high-impedance state.

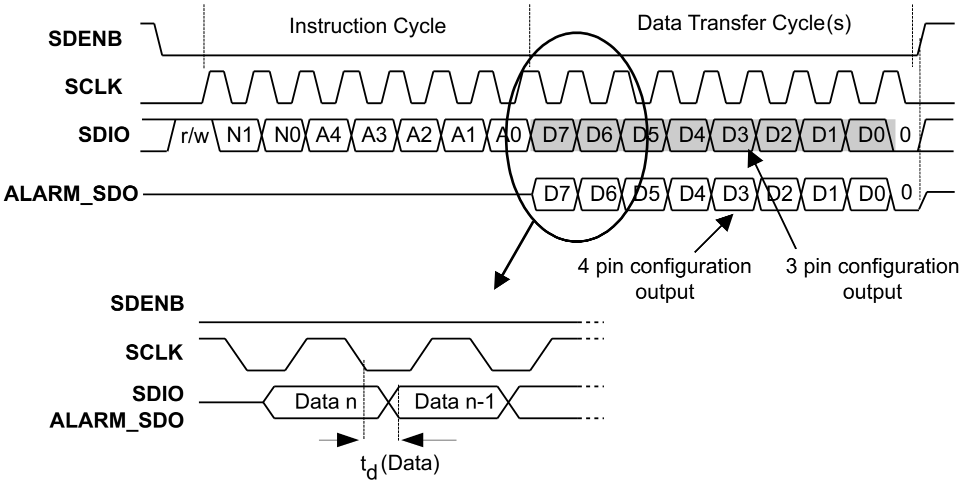


Figure 38. Serial Interface Read Timing Diagram

REGISTER DESCRIPTIONS

In the SIF interface there are three types of registers, *NORMAL, READ_ONLY*, and *WRITE_TO_CLEAR*. The *NORMAL* register type allows data to be written and read from the register. All 8 bits of the data are registered at the same time, but there is no synchronizing with an internal clock. All register writes are asynchronous with respect to internal clocks. *READ_ONLY* registers only allow reading of the registers—writing to them has no effect. *WRITE_TO_CLEAR* registers are just like *NORMAL* registers in that they can be written and read; however, when the internal signals set a bit high in these registers, that bit stays high until it is written to 0. This way, interrupts are captured and constant until dealt with and cleared.

Register Map

Name	Address	Default	(MSB) bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	(LSB) bit 0
CONFIG0	0x00	0x10	div2_dacclk_ena	div2_sync_ena	clkio_sel	clkio_out_ena_n	data_clk_sel	data_type	fifo_ena	sync_IorQ
CONFIG1	0x01	0x10	twos	iqswap	trim_clk_rc_fltr		daca_ complement	dacb_ complement	lvds_clk_div	
CONFIG2	0x02	0xXX	Unused	Unused	Unused	Unused	Unused	Unused	Alarm_fifo_ 2away	Alarm_fifo_1away
CONFIG3	0x03	0x10	alarm_or_sdo_ ena	sif_4pin	SLEEP	TXENABLE	SYNC	sync_sleep_txenable_sel		msb_out
CONFIG4	0x04	0x0F	fuse_pd	mixer_gain	pd_clkrcvr	pd_clkrcvr_ mask	coarse_dac(3:0)			
CONFIG5	0x05	0x00	offset_ena	qmc_corr_ena	mixer_ena	filter_tune(4:0)				
CONFIG6	0x06	0x00	pd_lvds	pd_rf_out	pd_dac	pd_analogout	pd_lvds_mask	pd_tf_out_ mask	pd_dac_mask	pd_analogout_ mask
CONFIG7	0x07	0x13	mask_2away	mask_1away	fifo_sync_mask	fifo_offset	alarm2away_ ena			alarm_1away_ ena
CONFIG8	0x08	0x00	qmc_offseta (7:0)							
CONFIG9	0x09	0x7A	qmc_offsetb (7:0)							
CONFIG10	0x0A	0xB6	qmc_offseta(12:8)					Unused	Unused	Unused
CONFIG11	0x0B	0xEA	qmc_offsetb(12:8)					Unused	Unused	Unused
CONFIG12	0x0C	0x45	qmc_gaina (7:0)							
CONFIG13	0x0D	0x1A	qmc_gainb (7:0)							
CONFIG14	0x0E	0x16	qmc_phase (7:0)							
CONFIG15	0x0F	0xAA	qmc_phase(9:8)		qmc_gaini(10:8)			qmc_gainq(10:8)		
CONFIG16	0x10	0xC6	freq (7:0)							
CONFIG17	0x11	0x24	freq (15:8)							
CONFIG18	0x12	0x02	freq (23:16)							
CONFIG19	0x13	0x00	freq (31:24)							
CONFIG20	0x14	0x00	phase (7:0)							
CONFIG21	0x15	0x00	phase (15:8)							
CONFIG22	0x16	0x00	Reserved							
CONFIG23	0x17	0xXX	Reserved							
CONFIG24	0x18	0xXX	Reserved							
CONFIG25	0x19	0xXX	Reserved							
CONFIG26	0x1A	0xXX	Reserved							
CONFIG27	0x1B	0xXX	Reserved							
CONFIG28	0x1C	0xXX	Reserved							
CONFIG29	0x1D	0xXX	Reserved							
CONFIG30	0x1E	0xXX	Reserved							
CONFIG31	0x1F	0x82	titest_voh	titest_vol	Version(5:0)					

Register name: CONFIG0; Address: 0x00

BIT 7							BIT 0
div2_dacclk_ena	div2_sync_ena	clkio_sel	clkio_out_ena_n	data_clk_sel	data_type	fifo_ena	sync_IorQ
0	0	0	1	0	0	0	0

Table 3. Clock Mode Memory Programming

Mode	div2_dacclk_ena	div2_sync_ena	clkio_sel	clkio_out_ena_n	data_clk_sel
Dual input clock(00)	1	0	1	1	0
Dual output clock (01)	1	1	0	0	0
Single differential DDR clock (10)	0	0	0	1	1
Single differential SDR clock (11)	0	0	1	1	1

div2_dacclk_ena:	When set to 1, this enables the divide-by-2 in the DAC clock path. This must be set to 1 when in dual-input clock mode or dual-output clock mode.
div2_sync_ena:	When set to 1, the divide-by-2 is synchronized with the iq_flag. It is only useful in the dual-clock modes when the divide-by-2 is enabled. Care must be take to ensure the input data and DAC clocks are correctly aligned.
clkio_sel:	This bit is used to determine which clock is used to latch the input data. This should be set according to Table 3.
clkio_out_ena_n:	When set to 0, the clock CLK_IO is an output. Depending on the mode, is should be set according to Table 3.
data_clk_sel:	This bit is used to determine which clock is used to latch the input data. This should be set according to Table 3.
data_type:	When asserted, the phase data is presented at the data interface. The phase data is then updated with each clock. The phase register then holds the value of the I and Q data to be used with the mix operation.
fifo_ena:	When asserted, the FIFO is enabled. Used in dual-input clock mode only. In all other modes, the FIFO is bypassed.
sync_IorQ:	When set to 0, sync is latched on the I phase of the input clock. When set to 1, sync is detected on the Q phase of the clock and is sent to the rest of the chip when the next I data is presented.

Register name: CONFIG1; Address: 0x01

BIT 7							BIT 0
twos	iqswap	trim_clk_rc_fltr		daca_complement	dacb_complement	lvds_clk_div	
0	0	0	1	0	0	X	X

twos:	When asserted, the input to the chip is 2s complement, otherwise offset binary.
iqswap:	When asserted, the DACA data is driven onto DACB and reverse.
trim_clk_rc_fltr:	2 bits to trim the RC filter for LVDS out
daca_complement:	When asserted, the output to DACA is complemented. This allows the user of the chip effectively to change the + and – designations of the PADs.
dacb_complement:	When asserted, the output to DACB is complemented. This allows the user of the chip effectively to change the + and – designations of the PADs.
lvds_clk_div:	

lvds_clk_div	LVDS Clock Division
00	2
01	4
10	1
11	1

Register name: CONFIG2; Address: 0x02

Write-to-clear register bits remain asserted once set. Each bit must be written to 0 before another 1 can be captured.

BIT 7							BIT 0
unused	unused	unused	unused	unused	unused	Alarm_fifo_2away	Alarm_fifo_1away
0	0	0	0	0	0	1	1

Alarm_fifo_2away:	When asserted, the FIFO pointers are 2 away from collision. **(WRITE_TO_CLEAR)**
Alarm_fifo_1away:	When asserted, the FIFO pointers are 1 away from collision. **(WRITE_TO_CLEAR)**

Register name: CONFIG3; Address: 0x03 (INTERFACE SELECTION)

BIT 7							BIT 0
alarm_or_sdo_ena	sif_4pin	SLEEP	TXenable	SYNC	sync_sleep_txenable_sel		msb_out
0	0	0	1	0	0	0	0

alarm_or_sdo_ena:	When asserted, the output of the ALARM_SDO pin is enabled.
sif_4pin:	When asserted, the part is in 4-pin SPI mode. The data-out is output on the ALARM_SDO pin. If this bit is not enabled, the alarm signal is output on the ALARM_SDO pin.
sleep:	When asserted, all blocks programmed to go to sleep in CONFIG4 and CONFIG6 registers labeled pd_***_mask are powered down.
TXenable:	When 0, the data path is zeroed. When 1, the device transmits.
sync:	When written with a 1, the part is synced. To be resynced using the sif register, it must be reset to 0 by writing a 0 then write a 1 to the sif to sync.
sync_sleep_ txenable_sel:	This is used to define the function of the SYNC_SLEEP pin. This pin can be used for multiple functions, but only one at a time. When it is set to control any one of the functions, all other functions are controlled by writing their respective sif register bits.

sync_sleep_txenable_sel	Pin controls
00	All controlled by sif bit
01	TXENABLE
10	SYNC
11	SLEEP

msb_out:	When set, and alarm_sdo_out_ena is also set, the ALARM_SDO pin outputs the value of daca bit 13.

Register name: CONFIG4; Address: 0x04

BIT 7 … BIT 0

fuse_pd	mixer_gain	pd_clkrcvr	pd_clkrcvr_mask	coarse_dac(3:0)			
0	0	0	0	1	1	1	1

fuse_pd:	When set to 1, the fuses are powered down. This saves approximately 50 µA at 1.8 V for every intact fuse. The default value is 0.
mixer_gain:	When asserted, the complex mixer output is multiplied by 2. Only applied when the mixer is enabled (mixer_ena = 1).
pd_clkrcvr:	When asserted, the clock receiver is powered down.
pd_clkrcvr_mask:	When asserted, allows the clock receiver to be powered down with the SYNC_SLEEP pin or sleep register bit.
coarse_dac:	DAC full-scale current control

Register name: CONFIG5; Address: 0x05

BIT 7 … BIT 0

offset_ena	qmc_corr_ena	mixer_ena	filter_tune(4:0)				
0	0	0	0	0	0	0	0

offset_ena:	When asserted, the qmc offset blk is enabled.
qmc_corr_ena:	When asserted, the qmc correction is enabled.
mixer_ena:	When asserted, the complex mix is performed. Otherwise, the mixer is bypassed.
filter_tune(4:0):	Bits used to change the bandwidth of the analog filters

Register name: CONFIG6; Address: 0x06

BIT 7 … BIT 0

pd_lvds	pd_rf_out	pd_dac	pd_analogout	pd_lvds_mask	pd_tf_out_mask	pd_dac_mask	pd_analogout_ mask
0	0	0	1	1	1	0	0

pd_lvds:	When asserted, the LVDS output stage is powered down.
pd_rf_out:	When asserted, the RF output stage is powered down.
pd_dac:	When asserted, DACs are powered down.
pd_analog_out:	When asserted, the entire analog circuit after the DACs (filters, modulator, LO input, RF output stage, LVDS output) is powered down.

The following are used to determine what blocks are powered down when the SYNC_SLEEP pin is used or the sleep register bit is set.

pd_lvds_mask:	When asserted, allows the LVDS to be powered down
pd_rf_out_mask:	When asserted, allows the RF output to be powered down
pd_dac_mask:	When asserted, allows the DACs to be powered down

Register name: CONFIG7; Address: 0x07

BIT 7 BIT 0

mask_2away	mask_1away	fifo_sync_mask	fifo_offset			alarm_2away_ena	alarm_1away_ena
0	0	0	1	0	0	1	1

mask_2away:	When set to 1, the ALARM_SDO pin is not asserted when the FIFO pointers are 2 away from collision. The alarm still shows up in the CONFIG7 bits.
mask_1away:	When set to 1, the ALARM_SDO pin is not asserted when the FIFO pointers are 1 away from collision. The alarm still shows up in the CONFIG7 bits.
fifo_sync_mask:	When set to 1, the sync to the FIFO is masked off. Sync does not then reset the pointers. If the value is 0, when the sync is toggled the FIFO pointers are reset to the offset values.
fifo_offset:	Used to set the offset pointers in the FIFO. Programs the starting location of the output side of the FIFO, allows the output pointer to be shifted from –4 to +3 (2s complement) positions with respect to its default position when synced. The default position for the output side pointer is 2. The input side pointer defaults to 0.
alarm_2away_ena:	When asserted, alarms from the FIFO that represent the pointers being 2 away from collision are enabled.
alarm_1away_ena:	When asserted, alarms from the FIFO that represent the pointers being 1 away from collision are enabled.

Register name: CONFIG8; Address: 0x08

BIT 7 BIT 0

qmc_offseta (7:0)							
0	0	0	0	0	0	0	0

qmc_offseta(7:0):	Bits 7:0 of qmc_offseta. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG9; Address: 0x09

BIT 7 BIT 0

qmc_offsetb (7:0)							
0	1	1	1	1	0	1	0

qmc_offsetb(7:0):	Bits 7:0 of qmc_offsetb. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG10; Address: 0x0A

BIT 7 BIT 0

qmc_offseta(12:8)					Unused	Unused	Unused
1	0	1	1	0	1	1	0

qmc_offsetb(12:8):	Bits 12:8 of qmc_offseta. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG11; Address: 0x0B

BIT 7							BIT 0
qmc_offsetb(12:8)					Unused	Unused	Unused
1	1	1	0	1	0	1	0

qmc_offsetb(12:8): Bits 12:8 of qmc_offsetb. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG12; Address: 0x0C

BIT 7							BIT 0
qmc_gaina (7:0)							
0	1	0	0	0	1	0	1

qmc_gaina(7:0): Bits 7:0 of qmc_gaina. The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG13; Address: 0x0D

BIT 7							BIT 0
qmc_gainb (7:0)							
0	0	0	1	1	0	0	0

qmc_gainb(7:0): Bits 7:0 of qmc_gainb. The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG14; Address: 0x0E

BIT 7							BIT 0
qmc_phase (7:0)							
0	0	0	1	0	1	1	0

qmc_phase(7:0) Bits 7:0 of qmc_phase. The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG15; Address: 0x0F

BIT 7							BIT 0
qmc_phase(9:8)		qmc_gaina(10:8)			qmc_gainb(10:8)		
1	0	1	0	1	0	1	0

qmc_phase(9:8):	Bits 9:8 of qmc_phase value
qmc_gaina(10:8):	Bits 9:8 of qmc_gaina value
qmc_gainb(10:8):	Bits 9:8 of qmc_gainb value

The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG16; Address: 0x10

BIT 7							BIT 0
freq (7:0)							
1	1	0	0	0	1	1	0

freq(7:0): Bits 7:0 of frequency value

Register name: CONFIG17; Address: 0x11

BIT 7							BIT 0
freq (15:8)							
0	0	1	0	0	1	0	0

freq (15:8): Bits 15:8 of frequency value

Register name: CONFIG18; Address: 0x12

BIT 7							BIT 0
freq (23:15)							
0	0	0	0	0	0	1	0

freq (23:15): Bits 23:15 of frequency value

Register name: CONFIG19; Address: 0x13

BIT 7							BIT 0
freq (31:24)							
0	0	0	0	0	0	0	0

freq (31:24): Bits 31:24 of frequency value

Register name: CONFIG20; Address: 0x14

BIT 7							BIT 0
phase (7:0)							
0	0	0	0	0	0	0	0

phase (7:0): Bits 7:0 of phase value

Register name: CONFIG21; Address: 0x15

BIT 7							BIT 0
phase (15:8)							
0	0	0	0	0	0	0	0

phase (15:8): Bits 15:8 of phase value

Register name: CONFIG22; Address: 0x16

BIT 7							BIT 0
nco__sync_sleep(7:0)							
0	0	0	0	0	0	0	0

nco_sync_sleep(7:0): Set to 11110000 to use the SYNC_SLEEP pin to update the NCO frequency value; otherwise, set to 00000000. Note that register sync_sleep_txenable_sel in CONFIG3 must be set to 10 to use the SYNC_SLEEP pin as a SYNC input.

Register name: CONFIG23; Address: 0x17

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG24; Address: 0x18

BIT 7							BIT 0
reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG25; Address: 0x19

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG26; Address: 0x1A

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG27; Address: 0x1B

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG28; Address: 0x1C

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG29; Address: 0x1D

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG30; Address: 0x1E

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG31; Address: 0x1F

BIT 7							BIT 0
titest_voh	titest_vol	Version(5:0)					
1	0	0	0	0	0	1	0

titest_voh:	Bit held high for sif test purposes
titest_voh:	Bit held low for sif test purposes
version:	Version of the chip

PARALLEL DATA INPUT

The AFE7070 can input either complex I and Q data interleaved on D[13:0] at a data rate 2× the internal output sample clock frequency, 16-bit NCO phase data interleaved as 8 MSBs and 8 LSBs on pins D[13:6] at a data rate 2× the internal output sample clock frequency, or 14-bit NCO phase data at a data rate 1× the internal output sample clock frequency. These modes are described in detail in the CLOCK MODES section.

CLOCK MODES

The AFE7070 has four clock modes for providing the DAC sample clock and data latching clocks.

Clock Mode	CLK_IO	FIFO	DataLatch	DACCLKFreqRatio	DataFormat	Progamming Bits
Dual-input clock	Input	Enabled	CLK_IO	1× or 2× internal sample clock	IQ or phase (MSB/LSB)	See Table 3 in CONFIG0 decription.
Dual-output clock	Output	Disabled	CLK_IO	2× internal sample clock	IQ or phase (MSB/LSB)	
Single differential DDR clock	Disabled	Disabled	DACCLK	1× internal sample clock	IQ or phase (MSB/LSB)	
Single differential SDR clock	Disabled	Disables	DACCLK	1× internal sample clock	14-bit phase-only	

DUAL-INPUT CLOCK MODE

In dual-input clock mode, the user provides both a differential DAC clock at pins DACCLKP/N at 2× the internal sample clock frequency and a second single-ended CMOS-level clock at CLK_IO for latching input data. The DACCLK is divided by 2 internally to provide the internal output sample clock, with the phase determined by the IQ_FLAG input. The IQ_FLAG signal can either be a repetitive high/low signal or a single event that is used to reset the clock divider phase and identify the I sample.

CLK_IO is an SDR clock at the input data rate, or 2× the internal sample-clock frequency. The DAC clock and data clock must be frequency locked, and a FIFO is used internally to absorb the phase difference between the two clock domains. The phase relationship of CLK_IO and DACCLK can be any phase at the initial sync of the FIFO, and thereafter can move up to ±4 clock cycles before the FIFO input and output pointers overrun and cause data errors. In dual-input clock mode, the latency from input data to output samples is not controlled because the FIFO can introduce a one-clock cycle variation in latency, depending on the exact phase relationship between DACCLK and CLK_IO.

An external sync must be given on the SYNC_SLEEP pin to reset/initialize internal signal processing blocks. Because the internal processing blocks process I and Q in parallel, the user can provide the sync signal during either the I or Q input times (or both). Note that the internal sync signal must propagate through the input FIFO, and therefore the latency of the sync updates of the signal processing blocks is not controlled.

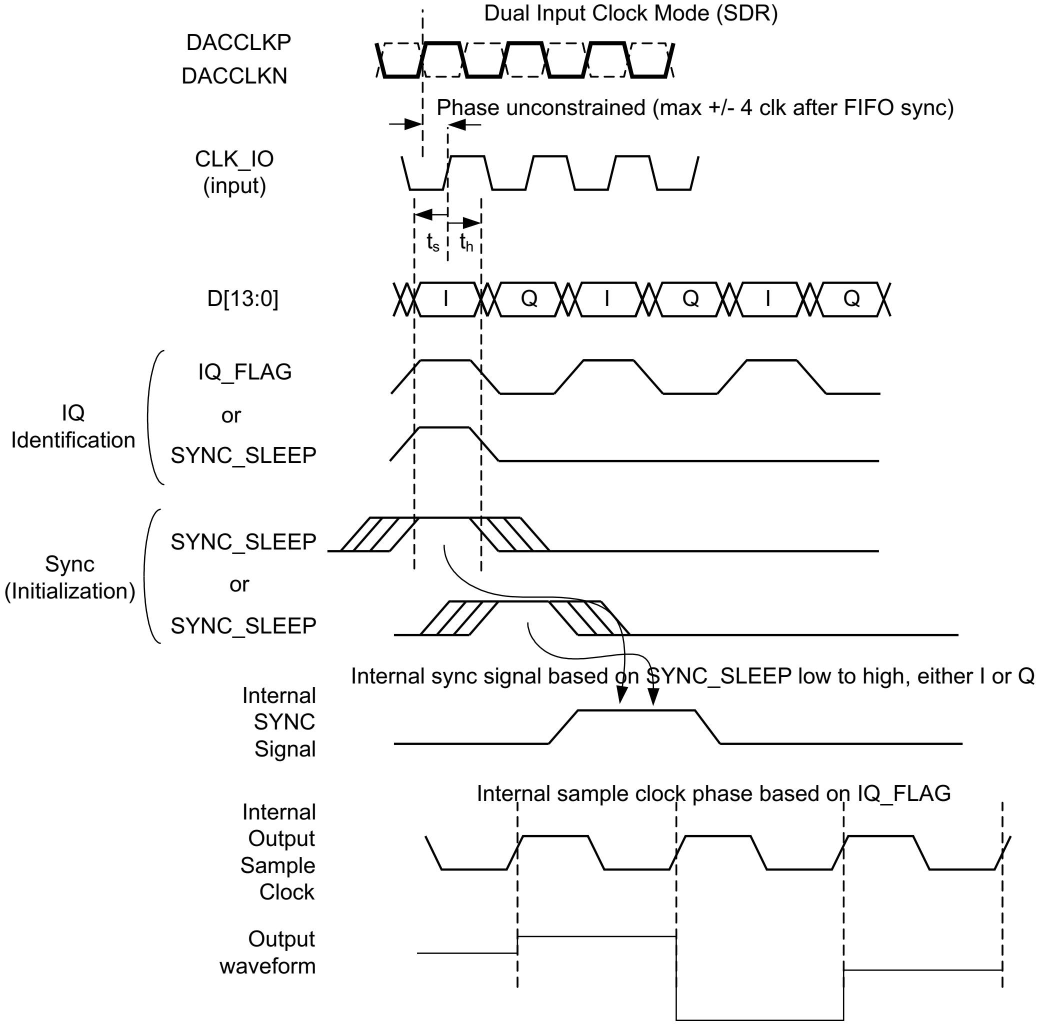


Figure 39. Dual-Input Clock Mode

DUAL-OUTPUT CLOCK MODE

In dual-output clock mode, the user provides a differential DAC clock at pins DACCLKP/N at 2× the internal sample clock frequency. The DACCLK is divided by 2 internally to provide the internal output sample clock, with the phase determined by the IQ_FLAG input. The IQ_FLAG signal can either be a repetitive high/low signal or a single event that is used to reset the clock divider phase and identify the I sample.

The AFE7070 outputs a single-ended CMOS-level clock at CLK_IO for latching input data. CLK_IO is an SDR clock at the input data rate, or 2× the internal sample clock frequency. The CLK_IO clock can be used to drive the input data source (such as digital upconverter) that sends the data to the DAC. Note that the CLK_IO delay relative to the input DACCLK rising edge (t_d) in Figure 40) increases with increasing loads.

An external sync can be given on the SYNC_SLEEP pin to reset/initialize internal signal processing blocks. Because the internal processing blocks process I and Q in parallel, the user can provide the sync signal during either the I or Q input times (or both).

In the dual-output clock mode, the FIFO is bypassed, so the latency from the data input to the DAC output and the time from sync input to update of the signal processing block are deterministic.

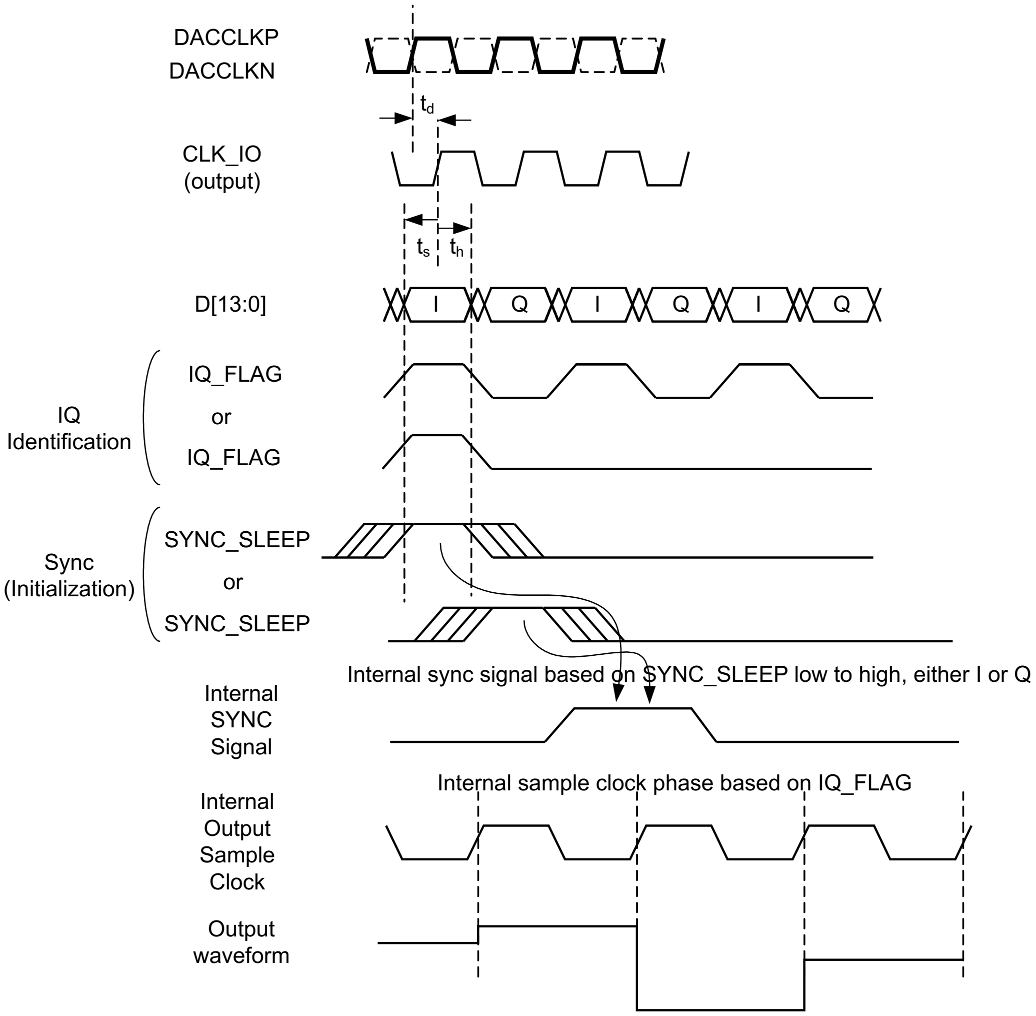


Figure 40. Dual-Output Clock Mode Timing Diagram

SINGLE DIFFERENTIAL DDR CLOCK

In single differential DDR clock mode, the user provides a differential clock to DACCLKP/N at the internal output sample clock frequency. The rising and falling edges of DACCLK are used to latch I and Q data, respectively. The internal output sample clock is derived from DACCLKP/N.

An external sync can be given on the SYNC_SLEEP pin to reset/initialize internal signal processing blocks. Because the internal processing blocks process I and Q in parallel, the user can provide the sync signal during either the I or Q input times (or both).

In the single differential DDR clock mode, the FIFO is bypassed, so the latency from the data input to the DAC output and the time from sync input to update of the signal processing block are deterministic.

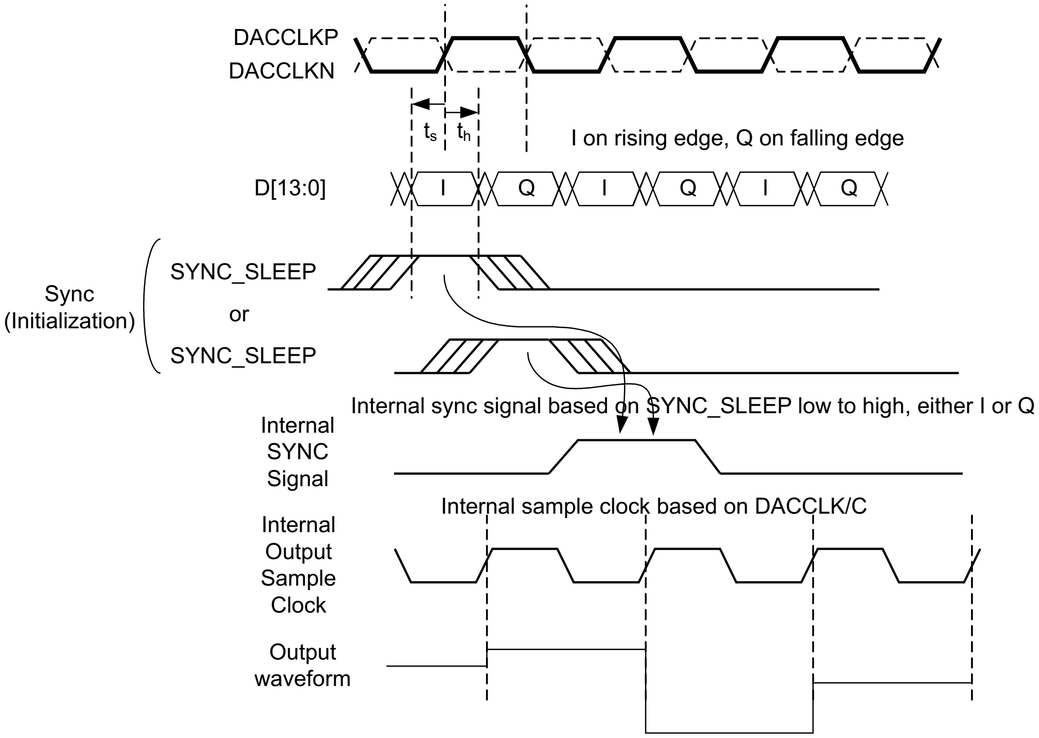


Figure 41. Single Clock Mode Timing Diagram

SINGLE DIFFERENTIAL SDR CLOCK MODE

In single differential SDR clock mode, the user provides a differential clock to DACCLKP/N at 1× the internal output sample clock frequency. This mode is only used for transferring 14-bit phase data, and therefore only requires one data latching per internal output sample clock. The internal output sample clock is derived from DACCLKP/N.

An external sync can be given on the SYNC_SLEEP pin to reset/initialize internal signal processing blocks.

In the single differential SDR clock mode, the FIFO is bypassed, so the latency from the data input to the DAC output and the time from sync input to update of the signal processing block are deterministic.

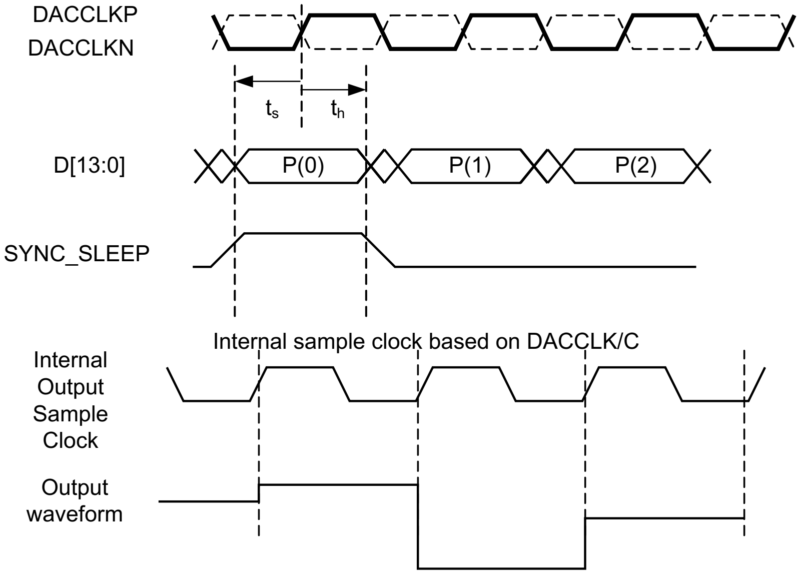


Figure 42. Single Differential SDR Clock Mode

FIFO ALARMS

The FIFO only operates when the write and read pointers are positioned properly. If either pointer over- or under-runs the other, samples are duplicated or skipped. To prevent this, register CONFIG2 can be used to track two FIFO-related alarms:

- alarm_fifo_2away: Occurs when the pointers are within two addresses of each other
- alarm_fifo_1away: Occurs when the pointers are within one address of each other

These two alarm events are generated asynchronously with respect to the clocks and can be accessed through the ALARM_SDO pin by writing a 1 in register alarm_or_sdo_ena (CONFIG3[7]) and 0 in register sif_4pin (CONFIG3[6]).

SYNCHRONIZATON

The AFE7070 has a synchonization input pin, SYNC_SLEEP, that is sampled by the same clock mode as the input data to initialize signal processing blocks and optionally update NCO frequency and phase values. In the case of dual input clock mode, the sync signal must propagate through the input FIFO, which creates an uncertainty of ±1 clock cycle for the synchronization of the signal processing. In all other clock modes, the FIFO is bypassed; therefore the exact time of the SYNC_SLEEP input to sync event is deterministic, and multiple devices can be exactly synchronized.

The function of the pin SYNC_SLEEP is determined by register sync_sleep_txenable_sel in CONFIG3; setting to 10 configures the SYNC_SLEEP pin as a SYNC input.

QUADRATURE MODULATOR CORRECTION (QMC) BLOCK

The quadrature modulator correction (QMC) block provides a means for changing the phase balance of the complex signal to compensate for I and Q imbalance present in an analog quadrature modulator. The block diagram for the QMC block is shown in Figure 43. The QMC block contains three programmable parameters. Registers **qmc_gaina(10:0)** and **qmc_gainb(10:0)** control the I and Q path gains and are 11-bit values with a range of 0 to approximately 2.0. Register **qmc_phase(9:0)** controls the phase imbalance between I and Q and is a 10-bit value with a range of –1/8 to approximately +1/8. LO feedthrough can be minimized by adjusting the DAC offset feature described below.

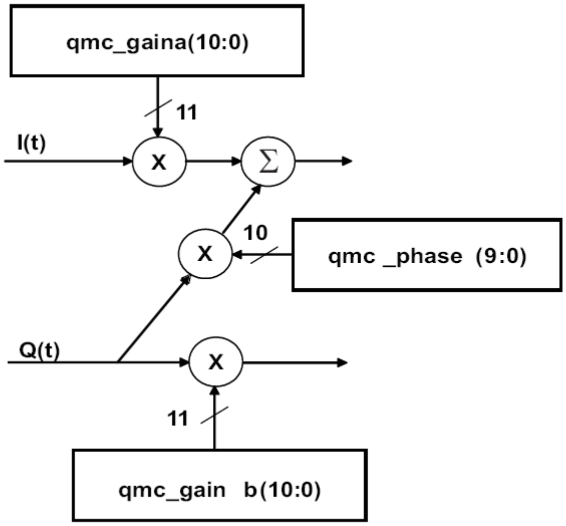


Figure 43. QMC Gain/Phase Block Diagram

The LO feedthrough can be minimized by adjusting the DAC offset. Registers **qmc_offseta(12:0)** and **qmc_offsetb(12:0)** control the I and Q path offsets and are 13-bit values with a range of –4096 to 4095. The DAC offset value adds a digital offset to the digital data before digital-to-analog conversion. The **qmc_gaina** and **qmc_gainb** registers can be used to back off the signal before the offset to prevent saturation when the offset value is added to the digital signal.

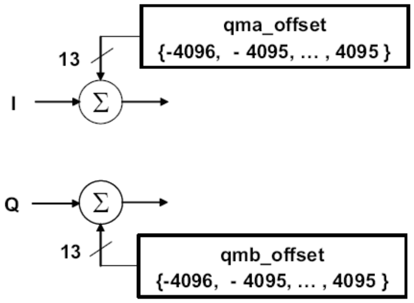


Figure 44. QMC Offset Block Diagram

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

The AFE7070 contains a numerically controlled oscillator that can be used as either a data generation source or to provide sin and cos for fully complex mixing with input data. The NCO has a 32-bit frequency register **freq(31:0)** and a 16-bit phase register **phase(15:0)**. The NCO tuning frequency is programmed in the CONFIG16 through CONFIG19 registers. Phase offset is programmed in the CONFIG20 and CONFIG21 registers. A block diagram of the NCO is shown in Figure 45.

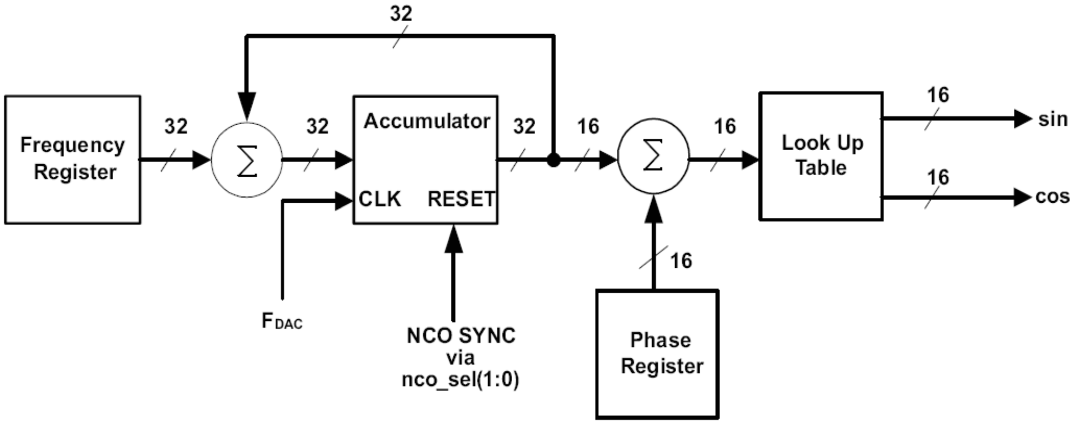


Figure 45. Numerically Controlled Oscillator (NCO)

Synchronization of the NCO occurs by resetting the NCO accumulator to zero, which is described as follows. Frequency word **freq** in the frequency register is added to the accumulator every clock cycle, f_{DAC}. The output frequency of the NCO is

$$f_{NCO} = \frac{freq \times f_{NCO\_CLK}}{2^{32}} \tag{1}$$

With a complex input represented by $I_{IN}(t)$ and $Q_{IN}(t)$, the output of FMIX $I_{OUT}(t)$ and $Q_{OUT}(t)$ is

$$\begin{aligned} I_{OUT}(t) &= \left[I_{IN}(t)\cos(2\pi f_{NCO} t + \delta) - Q_{IN}(t)\sin(2\pi\ f_{NCO} t + \delta) \right] \times 2^{(mixer\_gain\ -\ 1)} \\ Q_{OUT}(t) &= \left[I_{IN}(t)\sin(2\pi f_{NCO} t + \delta) + Q_{IN}(t)\cos(2\pi\ f_{NCO} t + \delta) \right] \times 2^{(mixer\_gain\ -\ 1)} \end{aligned} \tag{2}$$

where t is the time since the last resetting of the NCO accumulator, δ is the phase offset value, and **mixer_gain** is either 0 or 1. δ is given by:

$$\delta = 2\pi \times phase\,(15:0)/2^{16} \tag{3}$$

When register **mixer_gain** is set to 0, the gain through FMIX is sqrt(2)/2 or –3 dB. This loss in signal power is in most cases undesirable, and it is recommended that the gain function of the QMC block be used to increase the signal by 3 dB to compensate. With mixer_gain = 1, the gain through FMIX is sqrt(2) or 3 dB, which can cause clipping of the signal if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously near full-scale amplitude and should therefore be used with caution.

There are two methods to change the frequency and phase values in the NCO block.

1. Synchronous updating: To update the NCO frequency and phase using the SYNC_SLEEP pin, sync_sleep_txenable_sel in the CONFIG3 register must be set to 10 and nco_sync_sleep in the CONFIG22 register must be set to 11110000 should be written to the CONFIG22 register. With these settings, the frequency and phase register values only update the NCO frequency and phase values the pin SYNC_SLEEP is raised, which allows precise control of when the frequency is updated. The accumulator is not reset. There is a six-clock cycle latency from the time when the sync is clocked into the part until the new frequency value is used in the calculation of the accumulator.
2. Non-synchronous updating: If the nco_sync_sleep register in CONFIG22 is set to 00000000, the frequency register value updates the NCO frequency value when the lowest register bits freq(7:0) in CONFIG16 are written. To assure updating with a complete frequency value, register bits freq(32:8) in CONFIG17, CONFIG18, and CONFIG19 should be written before CONFIG16. Likewise, the phase register value updates the NCO phase value when the lowest register bits phase(7:0) in CONFIG20 are written. To assure updating with a complete phase value, register bits phase(15:8) in CONFIG21 should be written before CONFIG20.

ANALOG OUTPUT MODE

The AFE7070 has two output modes. The analog output mode includes an an RF buffer amplifier and covers the full frequency range of output frequency listed in the AC Electrical Characteristics table. The RF output should be AC coupled and is intended to drive a 50-Ω load.

LVDS OUTPUT MODE

The AFE7070 provides an output mode where the modulator output is converted from an analog signal by a comparator to a digital LVDS output signal. The RF output frequency in the LVDS output mode is limited to frequencies below the specification listed in the AC Electrical Characteristics table.

The output includes options for frequency division of ÷1, ÷2 and ÷4 (Figure 46), set in register lvds_clk_div in CONFIG1.

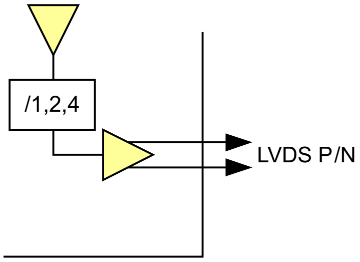


Figure 46. LVDS Output Option

CMOS DIGITAL INPUTS

Figure 47 through Figure 50 show schematics of the equivalent CMOS digital inputs and outputs of the AFE7070. All the CMOS digital inputs and outputs are relative to the IOVDD supply, which can vary from 1.8 V to 3.3 V. This facilitates the I/O interface and eliminates the need of level translation. See the specification table for logic thresholds. The pullup and pulldown circuitry is approximately equivalent to 100 kΩ.

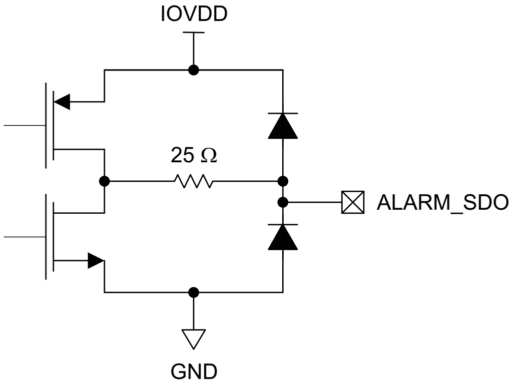


Figure 47. CMOS Digital Equivalent Circuit for ALARM_SDO Output

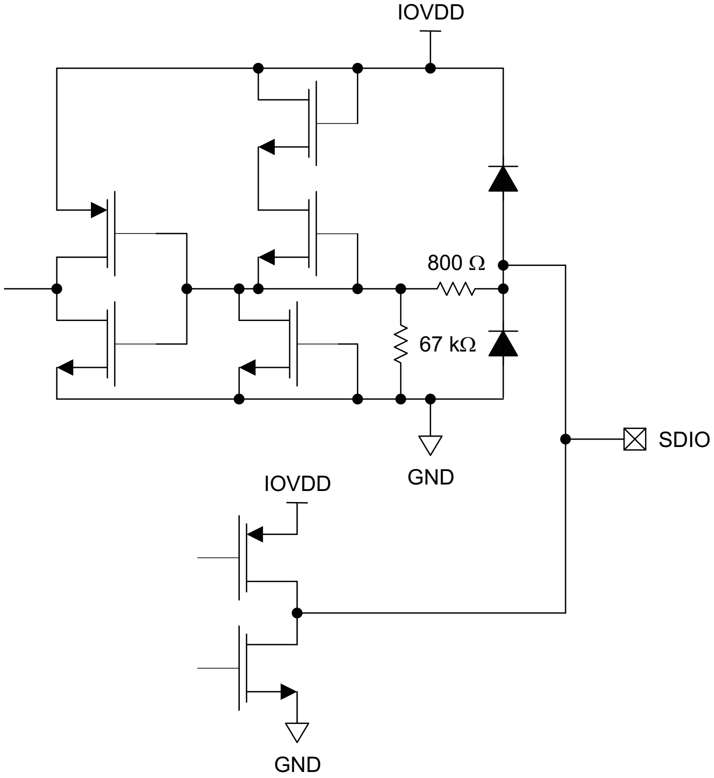


Figure 48. CMOS Digital Equivalent Circuit for SDIO Bidirectional Input/Output

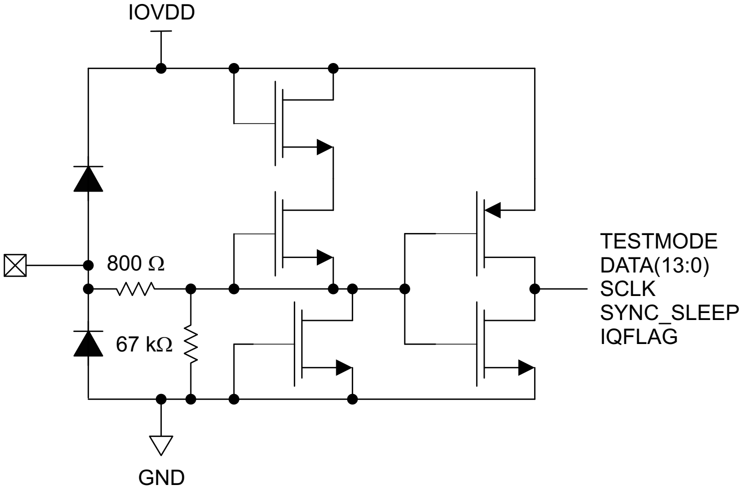


Figure 49. CMOS Digital Equivalent Circuit for TESTMODE, DATA, SCLK, SYNC_SLEEP and IQFLAG Inputs

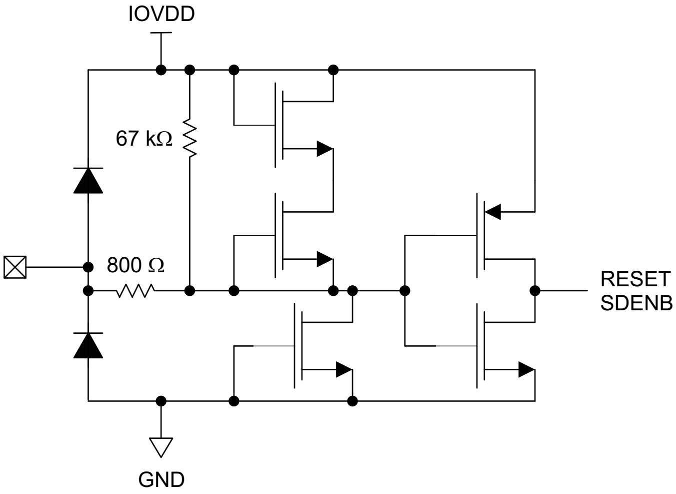


Figure 50. CMOS Digital Equivalent Circuit for RESET and SDENB Inputs

REVISION HISTORY

Changes from Original (February 2012) to Revision A	Page
• Changed the TYPICAL PERFORMANCE PLOTS of the Product Preview data sheet	9
• Changed the SERIAL INTERFACE of the Product Preview data sheet	16

Changes from Revision A (July 2012) to Revision B	Page
• Changed the device status From: Product Preview To: Production	1

Changes from Revision B (August 2012) to Revision C	Page
• Added AFE7070IRGZ25 to AVAILABLE OPTIONS	1

Changes from Revision B (October 2012) to Revision D	Page
• Changed the TYP value of f_{LO} = 450 MHz, Analog Output noise floor From: 156 To: 143	7

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7070IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7070I
AFE7070IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7070I
AFE7070IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7070I
AFE7070IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AFE7070I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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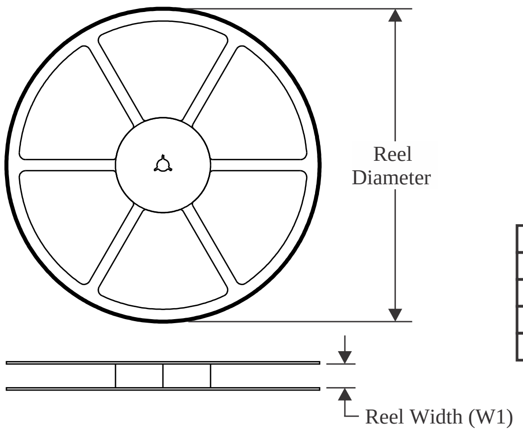
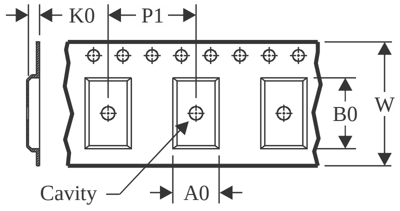
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

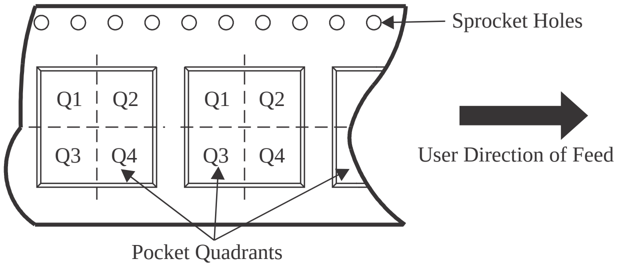


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

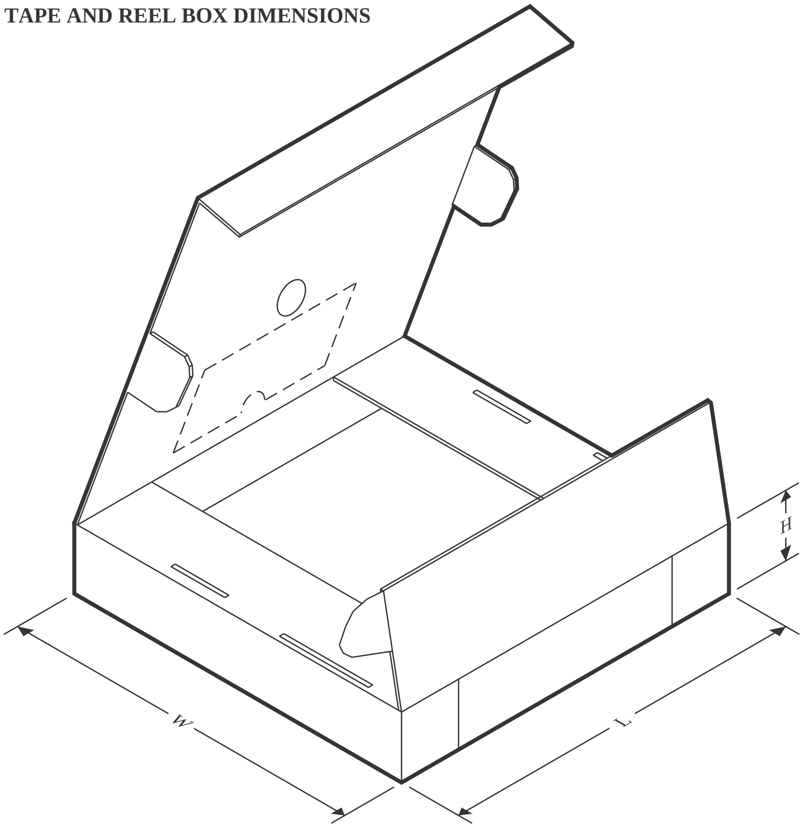


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE7070IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE7070IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

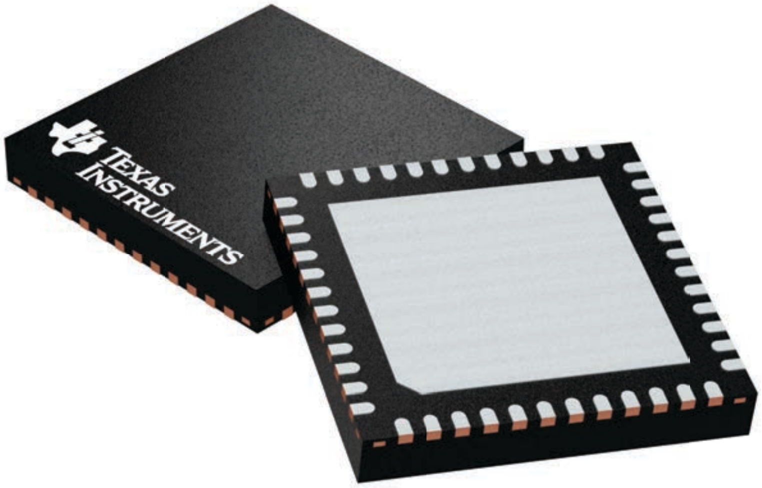
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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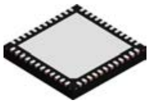
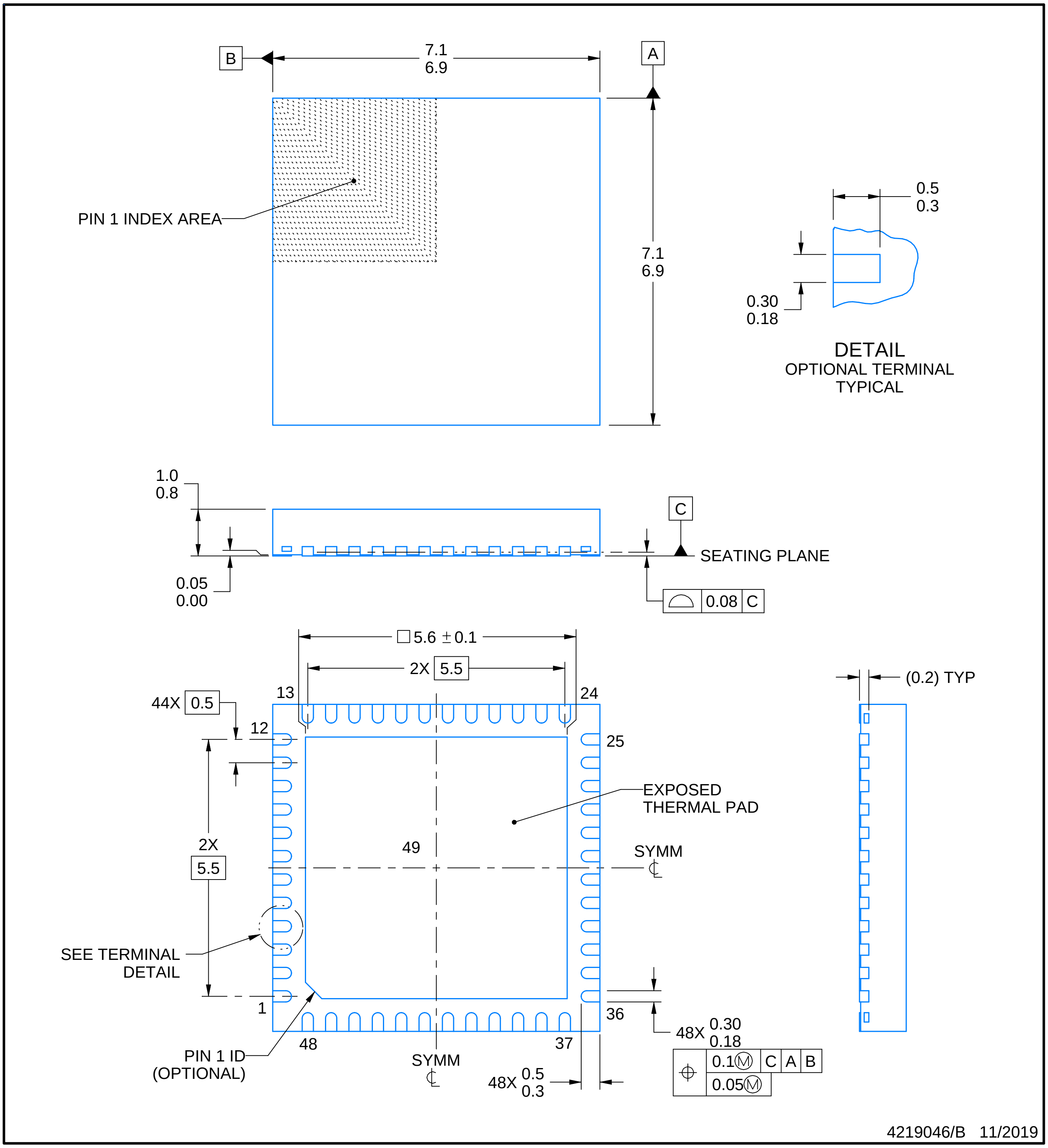


PACKAGE OUTLINE

RGZ0048D

VQFN - 1 mm max height

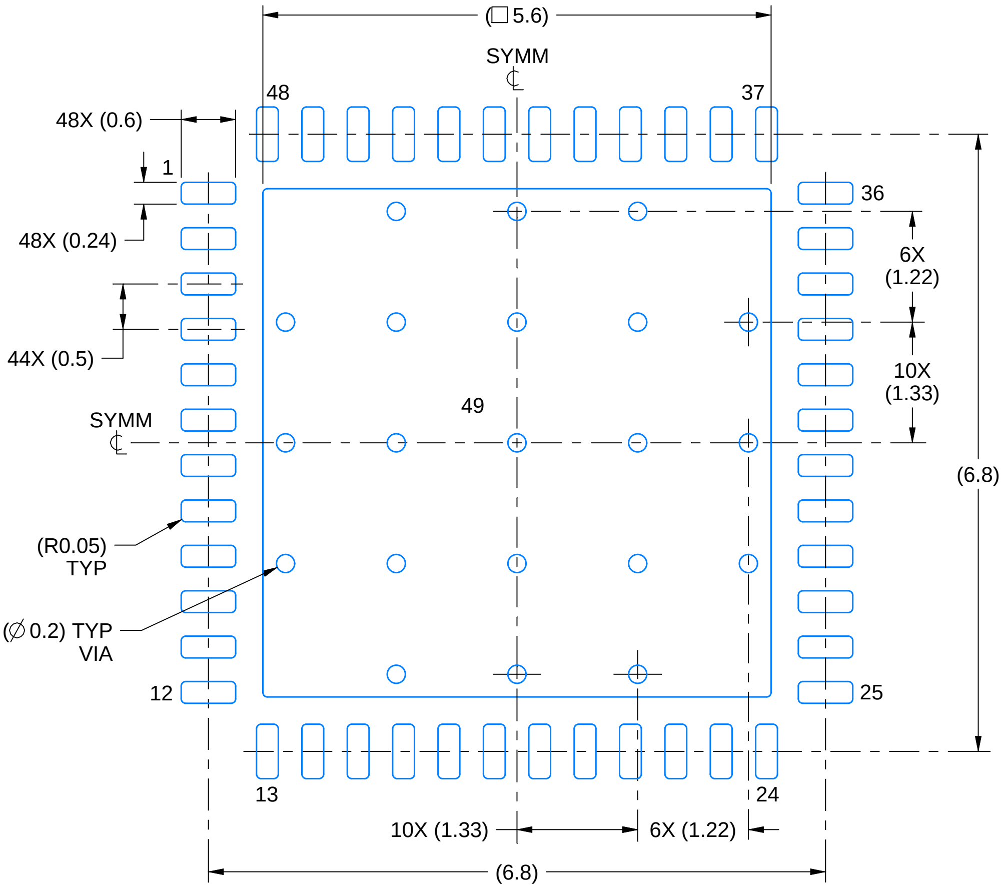
PLASTIC QUAD FLATPACK - NO LEAD



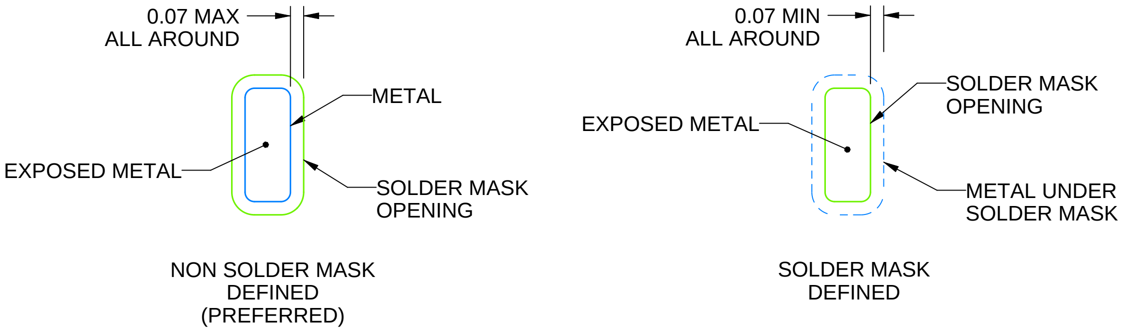
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

NOTES: (continued)

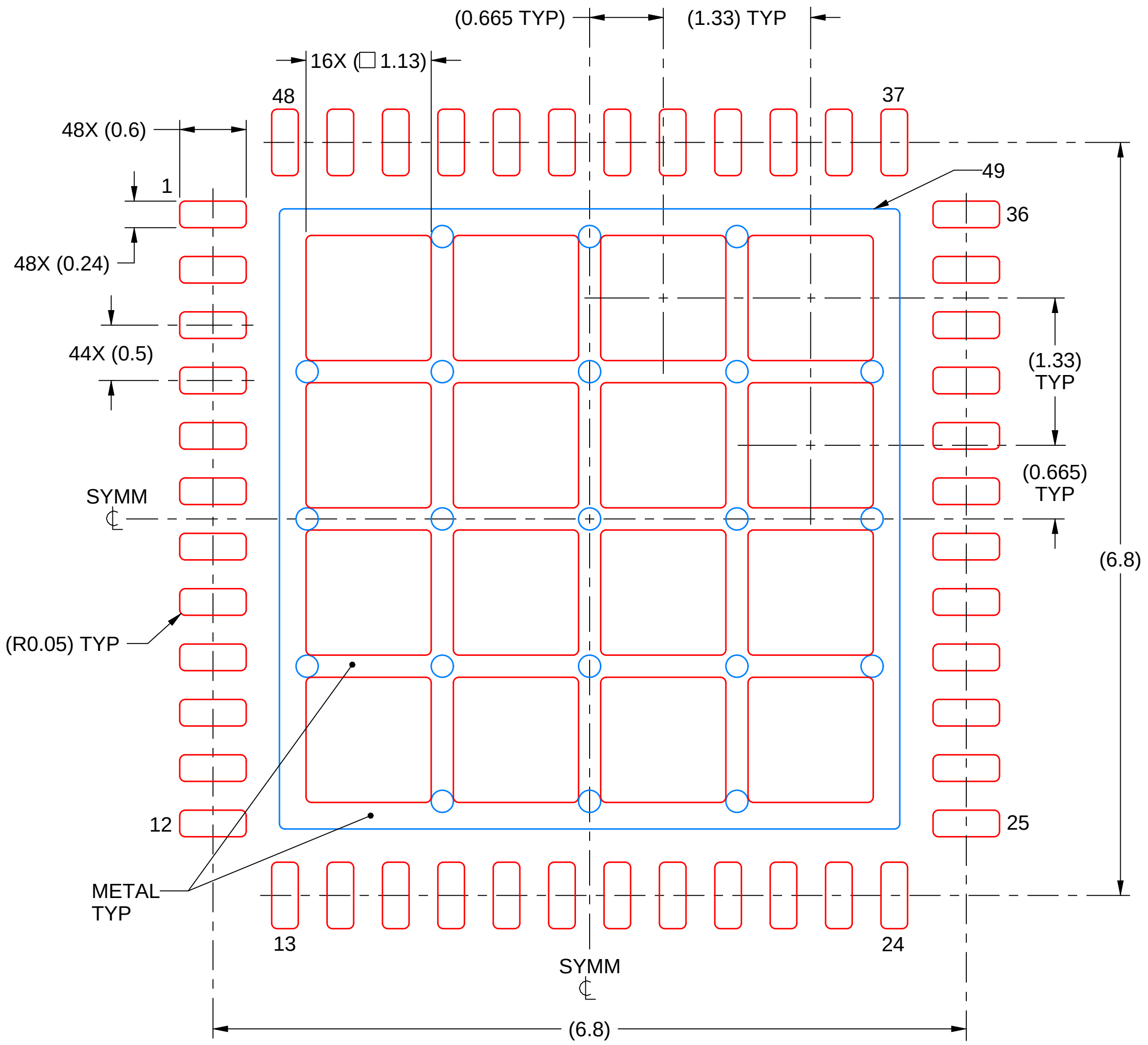
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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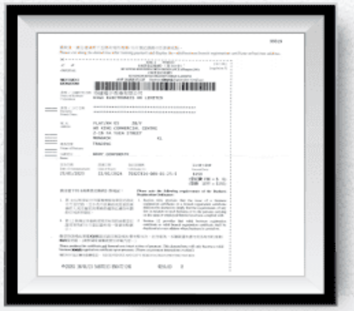

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