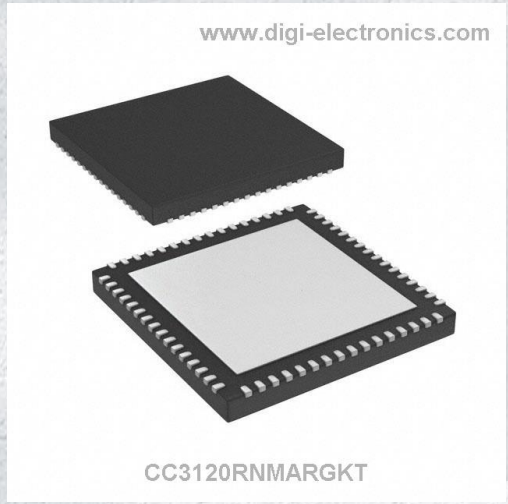
CC3120RNMARGKT Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	CC3120RNMARGKT-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	CC3120RNMARGKT
Description	IC RF TXRX+MCU WIFI 64VFQFN
Detailed Description	IC RF TxRx + MCU WiFi 802.11b/g/n 2.4GHz 64-VFQFN Exposed Pad

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
CC3120RNMARGKT	Texas Instruments
Series:	Product Status:
SimpleLink™	Active
DiGi-Electronics Programmable:	Type:
Not Verified	TxRx + MCU
RF Family/Standard:	Protocol:
WiFi	802.11b/g/n
Modulation:	Frequency:
DSSS, OFDM	2.4GHz
Data Rate (Max):	Power - Output:
54Mbps	18dBm
Sensitivity:	Memory Size:
-96dBm	-
Serial Interfaces:	Voltage - Supply:
SPI, UART	2.1V ~ 3.6V
Current - Receiving:	Current - Transmitting:
59mA	229mA
Operating Temperature:	Mounting Type:
-40°C ~ 85°C	Surface Mount
Package / Case:	Supplier Device Package:
64-VFQFN Exposed Pad	64-VQFN (9x9)
Base Product Number:	
CC3120	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	5A992C
HTSUS:	
8542.31.0001	

CC3120 SimpleLink™ Wi-Fi® Network Processor, Internet-of-Things Solution for MCU Applications

1 Features

- CC3120R SimpleLink™ Wi-Fi® consists of a wireless network processor (NWP) and power-management subsystems
- Featuring a dedicated Wi-Fi Internet-on-a chip™ Wi-Fi NWP that completely offloads Wi-Fi and internet protocols from the application microcontroller unit (MCU)
- Wi-Fi modes:
  - 802.11b/g/n station
  - 802.11b/g/n access point (AP) supports up to four stations
  - Wi-Fi Direct® client/group owner
- WPA2 personal and enterprise security: WEP, WPA™/ WPA2™ PSK, WPA2 Enterprise (802.1x), WPA3™ personal, WPA3™ enterprise
- IPv4 and IPv6 TCP/IP Stack
  - Industry-standard BSD socket application programming interfaces (APIs):
    - 16 simultaneous TCP or UDP sockets
    - 6 simultaneous TLS and SSL sockets
- IP addressing: static IP, LLA, DHCPv4, and DHCPv6 with duplicate address detection (DAD)
- SimpleLink connection manager for autonomous and fast Wi-Fi connections
- Flexible Wi-Fi provisioning with SmartConfig™ technology, AP mode, and WPS2 options:
- RESTful API support using internal HTTP server
- Wide set of security features:
  - Hardware features:
    - Separate execution environments
    - Device identity
  - Networking security:
    - Personal and enterprise Wi-Fi security
    - Secure sockets (SSLv3, TLS1.0/1.1/TLS1.2)
    - HTTPS server
    - Trusted root-certificate catalog
    - TI root-of-trust public key
  - Software IP protection:
    - Secure key storage
    - File system security
    - Software tamper detection
    - Cloning protection
- Embedded network applications running on the dedicated NWP:
  - HTTP/HTTPS web server with dynamic user callbacks
  - mDNS, DNS-SD, DHCP server
  - Ping
- Recovery mechanism—can recover to factory defaults or to a complete factory image
- Wi-Fi TX power:
  - 18.0dBm at 1 DSSS
  - 14.5dBm at 54 OFDM
- Wi-Fi RX sensitivity:
  - –96.0dBm at 1 DSSS
  - –74.5dBm at 54 OFDM
- Application throughput:
  - UDP: 16Mbps
  - TCP: 13Mbps
- Power-management subsystem
  - Integrated DC/DC converters support a wide range of supply voltage:
    - VBAT wide-voltage mode: 2.1V to 3.6V
    - VIO is always tied with VBAT
    - Preregulated 1.85V mode
  - Advanced low-power modes
    - Shutdown: 1µA
    - Hibernate: 4.5µA
    - Low-power deep sleep (LPDS): 115µA
    - RX traffic : 59mA at 54 OFDM
    - TX traffic : 229mA at 54 OFDM, maximum power
    - Idle connected (MCU in LPDS): 690710µA at DTIM = 1
- Clock source
  - 40.0MHz crystal with internal oscillator
  - 32.768kHz crystal or external RTC
- RGK package
  - 64-pin, 9mm × 9mm very thin quad flat nonleaded (VQFN) package, 0.5mm pitch
- Operating temperature
  - Ambient temperature range: –40°C to +85°C
- Device supports SimpleLink MCU Platform Developers' Ecosystem

2 Applications

- For Internet-of-Things (IoT) applications, such as:
  - Cloud connectivity
  - Internet gateway
  - Home and building automation
  - Appliances
  - Access control

- Security systems
- Smart energy
- Industrial control
- Smart plug and metering
- Wireless audio
- IP network sensor nodes
- Asset tracking
- Medical devices

3 Description

The CC3120R device is part of the SimpleLink™ microcontroller (MCU) platform that consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz, and host MCUs. All share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink™ platform enables you to add any combination of the devices from the portfolio into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit *www.ti.com/simplelink*.

Connect any microcontroller (MCU) to the internet-of-things (IoT) cloud with the CC3120R device from Texas Instruments™. The Wi-Fi Alliance®-certified CC3120R device is part of the second generation of the SimpleLink™ Wi-Fi® family that dramatically simplifies the implementation of low-power internet connectivity.

The CC3120R has all of the Wi-Fi and internet protocols implemented in the ROM, which runs from the dedicated on-chip Arm® network processor and significantly offloads the host MCU and simplifies the system integration.

The CC3120R Wi-Fi® Internet-on-a chip™ device contains a dedicated Arm® MCU that offloads many of the networking activities from the host MCU. This subsystem includes an 802.11b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure internet connections with 256-bit encryption. The CC3120R device supports station, AP, and Wi-Fi direct modes. The device also supports WPA2™ personal and enterprise security and WPA3™ personal and enterprise. The device includes embedded TCP/IP and TLS/SSL stacks, an HTTP server, and multiple internet protocols. The CC3120R device supports a variety of Wi-Fi provisioning methods, including HTTP based on AP mode, SmartConfig™ technology, and WPS2.0.

As part of TI's SimpleLink™ Wi-Fi® family second generation, the CC3120R device introduces new features and enhanced capabilities, such as the following:

- IPv6
- Enhanced Wi-Fi provisioning
- Optimized low-power management
- Wi-Fi AP connection with up to four stations
- More concurrently opened BSD sockets; up to 16 BSD sockets, of which six are secure
- HTTPS support
- RESTful API support
- Asymmetric keys crypto library

The CC3120R device is delivered with a slim and user-friendly host driver to simplify the integration and development of networking applications. The host driver can easily be ported to most platforms and operating systems (OS). The driver is written in strict ANSI-C (C99) programming language and requires a minimal platform adaptation layer (porting layer). The driver has a small memory footprint and can run on 8-, 16-, or 32-bit MCUs with any clock speed (no performance or real-time dependency).

The CC3120R device comes in an easy-to-layout VQFN package and is delivered as a complete platform solution, including various tools and software, sample applications, user and programming guides, reference designs, and the TI E2E™ support community. The CC3120R device is part of the SimpleLink MCU Ecosystem.

Device Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE
CC3120RNMARGKT/R	VQFN (64)	9.00mm × 9.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagrams

Figure 4-1 shows the functional block diagram of the CC3120R SimpleLink Wi-Fi solution.

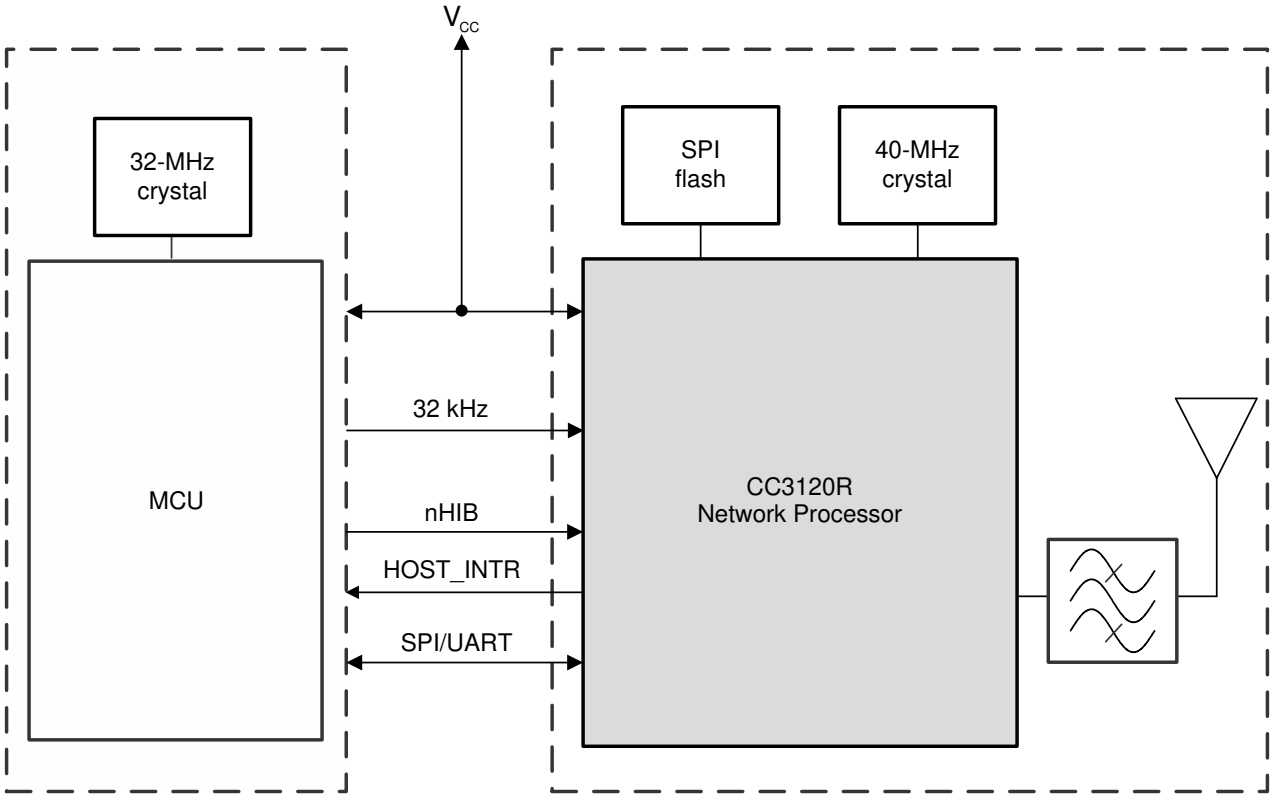


Figure 4-1. Functional Block Diagram

Figure 4-2 shows the CC3120R hardware overview.

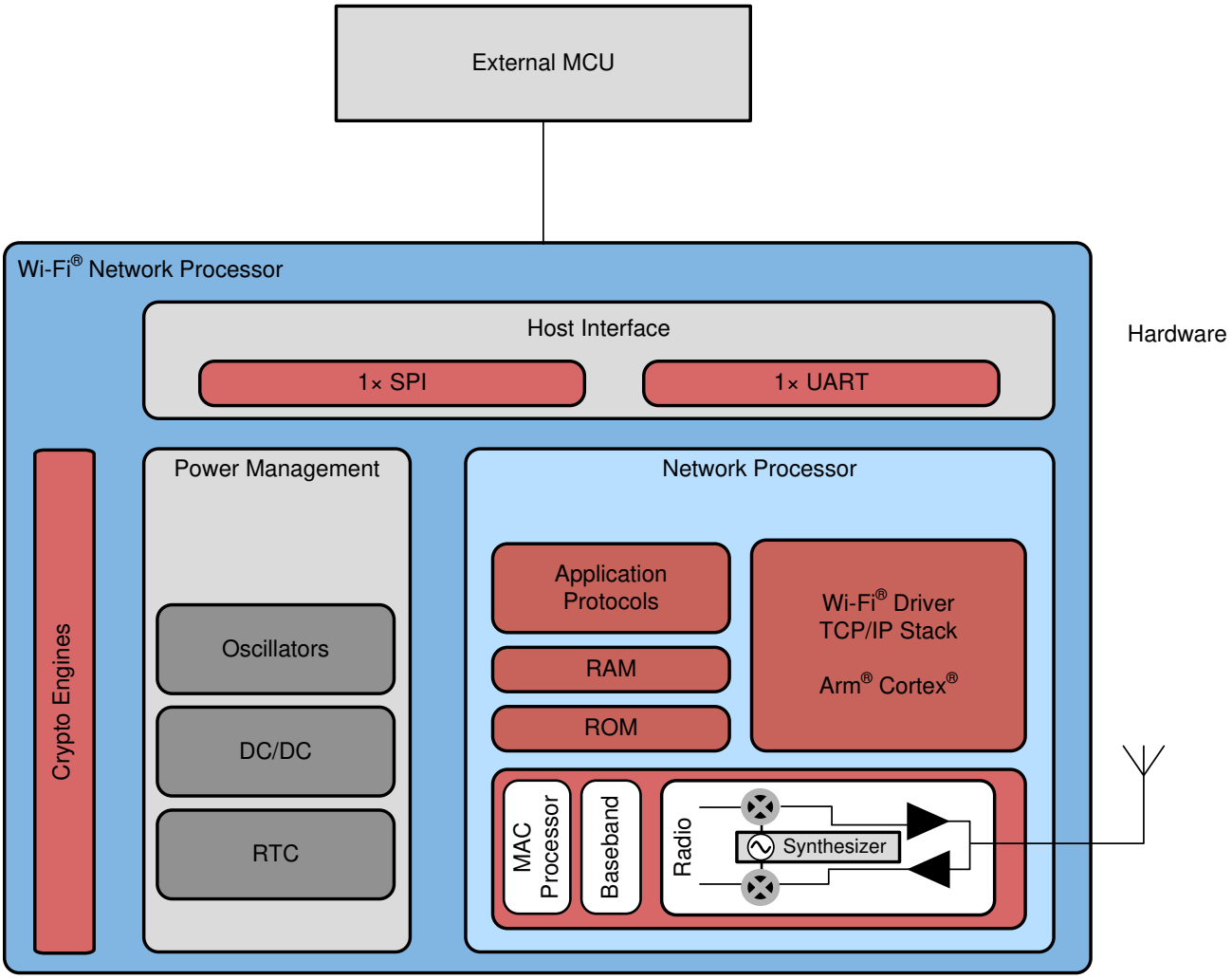


Figure 4-2. CC3120R Hardware Overview

Figure 4-3 shows an overview of the CC3120R embedded software.

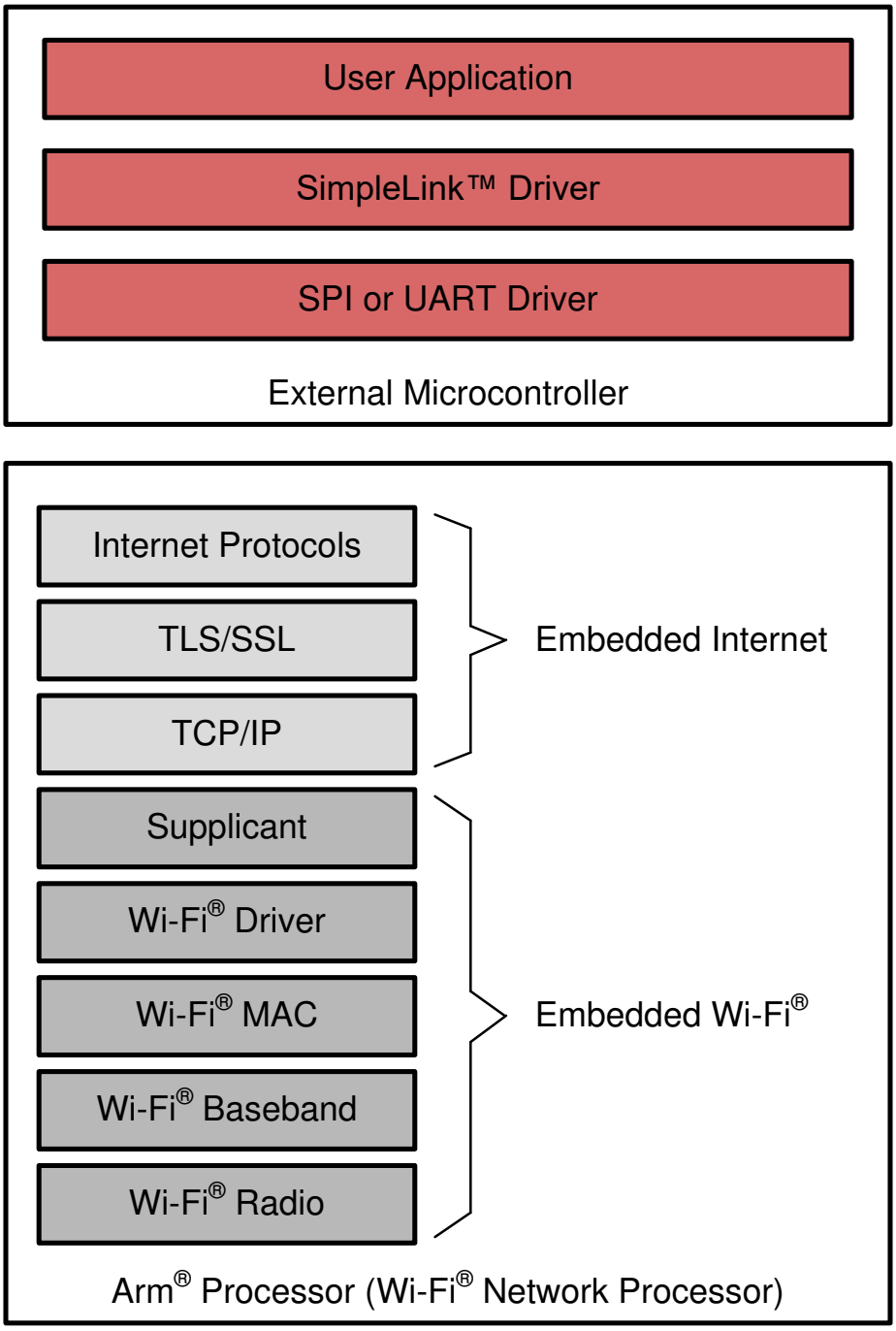


Figure 4-3. CC3120R Software Overview

Table of Contents

5 Device Comparison

Table 5-1 shows the features supported across different CC3220 devices.

Table 5-1. Device Features Comparison

FEATURE	DEVICE		
	CC3220R	CC3220S	CC3220SF
	On-Chip Application Memory		
RAM	256KB	256KB	256KB
Flash	–	–	1MB
	Security Features		
Enhanced Application Level Security	–	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming
Hardware Acceleration	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines
Additional Networking Security	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key
Secure Boot	No	Yes	Yes
	Additional Features		
Standard	802.11 b/g/n		
TCP/IP Stack	IPv4, IPv6		
Package	9 mm × 9 mm VQFN		
Sockets	16		

5.1 Related Products

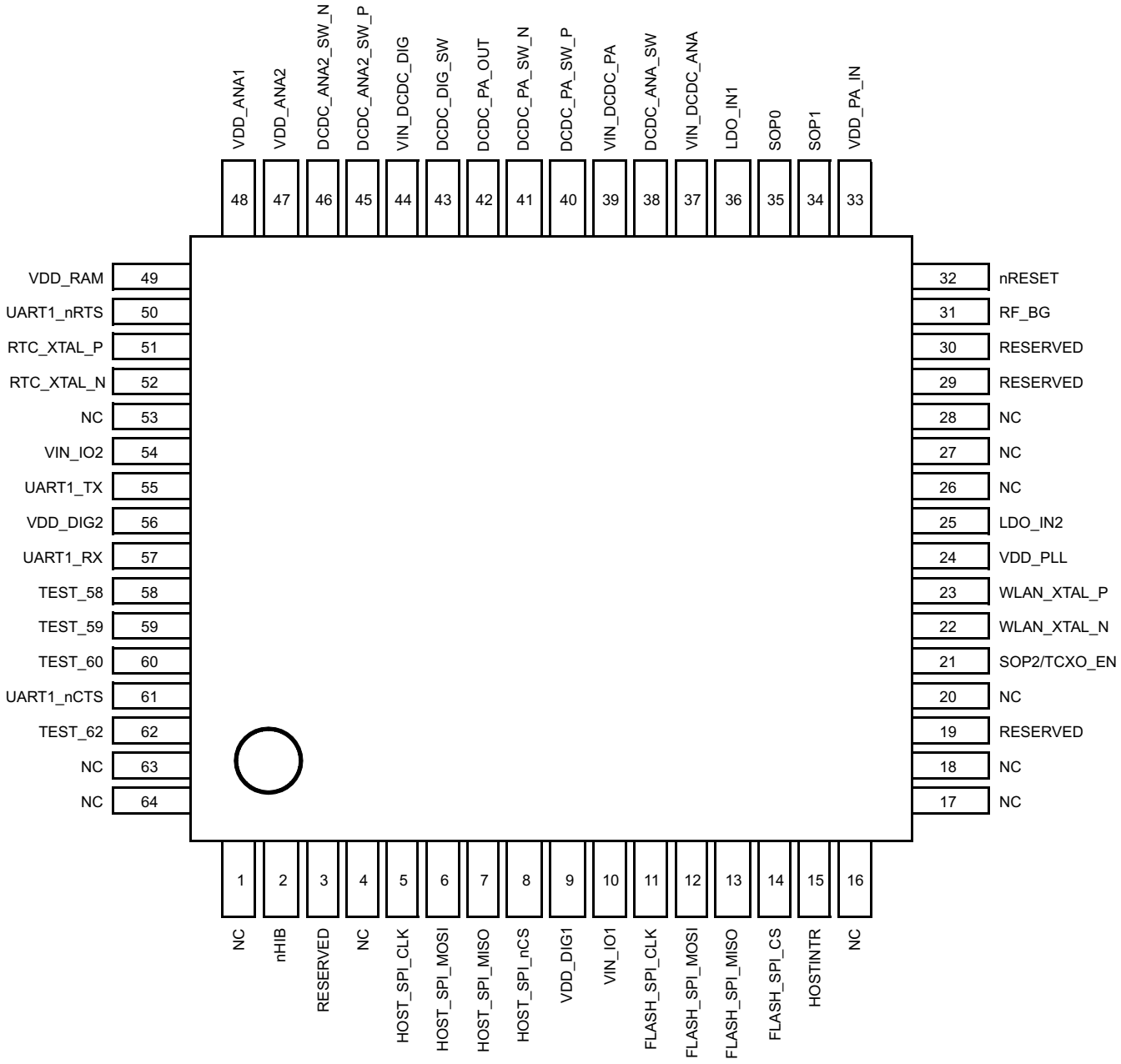
For information about other devices in this family of products or related products, see the following links:

SimpleLink™ MCU Portfolio	This portfolio offers a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. With 100 percent code reuse across host MCUs, Wi-Fi, Bluetooth® low energy, Sub-1 GHz devices and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink software development kit (SDK) allows you to reuse often, opening the door to create unlimited applications.
SimpleLink™ Wi-Fi® Family	This device platform offers several Internet-on-a chip™ solutions, which address the need of battery operated, security enabled products. Texas instruments offers a single chip wireless microcontroller and a wireless network processor which can be paired with any MCU, to allow developers to design new wi-fi products, or upgrade existing products with wi-fi capabilities.
MSP432™ Host MCU	These MCUs feature the Arm® Cortex®-M4 processor that offers ample processing capability with floating point unit and memory footprint for advanced processing algorithm, communication protocols and application needs, while incorporating a 14-bit 1-msps ADC14 that provides a flexible and low-power analog with best-in-class performance to enable developers to add differentiated sensing and measurement capabilities to their Wi-Fi applications.
Reference Designs for CC3100 and CC3120 Devices	TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.
SimpleLink™ Wi-Fi® CC3120 SDK Plug-in	This SDK plug-in contains drivers, sample applications for Wi-Fi features and internet, and documentation required to use the CC3120 solution.

6 Terminal Configuration and Functions

6.1 Pin Diagram

Figure 6-1 shows pin assignments for the 64-pin VQFN package.



NC = No internal connection

Figure 6-1. VQFN 64-Pin Assignments Top View

6.2 Pin Attributes

Table 6-1 describes the CC3120R pins.

Note

If an external device drives a positive voltage to signal pads when the CC3120R device is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3120R device can occur. To prevent current draw, TI recommends one of the following:

- All devices interfaced to the CC3120R device must be powered from the same power rail as the CC3120R device.
- Use level shifters between the CC3120R device and any external devices fed from other independent rails.
- The nRESET pin of the CC3120R device must be held low until the V_{BAT} supply to the device is driven and stable.

Table 6-1. Pin Attributes

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
2	nHIB	Hi-Z	I	Hibernate signal input to the NWP subsystem (active low). This is connected to the MCU GPIO. If the GPIO from the MCU can float while the MCU enters low power, consider adding a pullup resistor on the board to avoid floating.
3	Reserved	Hi-Z	—	Reserved for future use
5	HOST_SPI_CLK	Hi-Z	I	Host interface SPI clock
6	HOST_SPI_MOSI	Hi-Z	I	Host interface SPI data input
7	HOST_SPI_MISO	Hi-Z	O	Host interface SPI data output
8	HOST_SPI_nCS	Hi-Z	I	Host interface SPI chip select (active low)
9	VDD_DIG1	Hi-Z	Power	Digital core supply (1.2 V)
10	VIN_IO1	Hi-Z	Power	I/O supply
11	FLASH_SPI_CLK	Hi-Z	O	Serial Flash interface: SPI clock
12	FLASH_SPI_MOSI	Hi-Z	O	Serial Flash interface: SPI data out
13	FLASH _SPI_MISO	Hi-Z	I	Serial Flash interface: SPI data in (active high)
14	FLASH _SPI_CS	Hi-Z	O	Serial Flash interface: SPI chip select (active low)
15	HOST_INTR	Hi-Z	O	Interrupt output (active high)
19	Reserved	Hi-Z	—	Connect a 100-kΩ pulldown resistor to ground.
21	SOP2/TCXO_EN	Hi-Z	O	Controls restore to default mode. Enable signal for external TCXO. Add a 10-kΩ pulldown resistor to ground.
22	WLAN_XTAL_N	Hi-Z	Analog	Connect the WLAN 40-MHz crystal here.
23	WLAN_XTAL_P	Hi-Z	Analog	Connect the WLAN 40-MHz crystal here.
24	VDD_PLL	Hi-Z	Power	Internal PLL power supply (1.4-V nominal)
25	LDO_IN2	Hi-Z	Power	Input to internal LDO
29	Reserved	Hi-Z	O	Reserved for future use
30				
31	RF_BG	Hi-Z	RF	2.4-GHz RF TX, RX
32	nRESET	Hi-Z	I	RESET input for the device. Active low input. Use RC circuit (100 k || 0.1 µF) for power on reset (POR).
33	VDD_PA_IN	Hi-Z	Power	Power supply for the RF power amplifier (PA)

Table 6-1. Pin Attributes (continued)

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE(1)	DESCRIPTION
34	SOP1	Hi-Z	—	SOP[2:0] used for factory restore. Add 100-kΩ pulldown to ground. See .
35	SOP0	Hi-Z	—	SOP[2:0] used for factory restore. Add 100-kΩ pulldown to ground. See .
36	LDO_IN1	Hi-Z	Power	Input to internal LDO
37	VIN_DCDC_ANA	Hi-Z	Power	Power supply for the DC/DC converter for analog section
38	DCDC_ANA_SW	Hi-Z	Power	Analog DC/DC converter switch output
39	VIN_DCDC_PA	Hi-Z	Power	PA DC/DC converter input supply
40	DCDC_PA_SW_P	Hi-Z	Power	PA DC/DC converter switch output +ve
41	DCDC_PA_SW_N	Hi-Z	Power	PA DC/DC converter switch output –ve
42	DCDC_PA_OUT	Hi-Z	Power	PA DC/DC converter output. Connect the output capacitor for DC/DC here.
43	DCDC_DIG_SW	Hi-Z	Power	Digital DC/DC converter switch output
44	VIN_DCDC_DIG	Hi-Z	Power	Power supply input for the digital DC/DC converter
45	DCDC_ANA2_SW_P	Hi-Z	Power	Analog2 DC/DC converter switch output +ve
46	DCDC_ANA2_SW_N	Hi-Z	Power	Analog2 DC/DC converter switch output –ve
47	VDD_ANA2	Hi-Z	Power	Analog2 power supply input
48	VDD_ANA1	Hi-Z	Power	Analog1 power supply input
49	VDD_RAM	Hi-Z	Power	Power supply for the internal RAM
50	UART1_nRTS	Hi-Z	O	UART host interface (active low)
51	RTC_XTAL_P	Hi-Z	Analog	32.768-kHz XTAL_P or external CMOS level clock input
52	RTC_XTAL_N	Hi-Z	Analog	32.768-kHz XTAL_N or 100-kΩ external pullup for external clock
54	VIN_IO2	Hi-Z	Power	I/O power supply. Same as battery voltage.
55	UART1_TX	Hi-Z	O	UART host interface. Connect to test point on prototype for Flash programming.
56	VDD_DIG2	Hi-Z	Power	Digital power supply (1.2 V)
57	UART1_RX	Hi-Z	I	UART host interface; connect to test point on prototype for Flash programming.
60	TEST_60	Hi-Z	O	Test signal; connect to an external test point.
61	UART1_nCTS	Hi-Z	I	UART host interface (active low)
62	TEST_62	Hi-Z	O	Test signal; connect to an external test point.
—	GND	—	Power	Ground tab used as thermal and electrical ground

(1) I = Input
O = Output
RF = radio frequency
I/O = bidirectional

6.3 Connections for Unused Pins

All unused pins must be left as no connect (NC) pins. Table 6-2 provides a list of NC pins.

Table 6-2. Connections for Unused Pins

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE	DESCRIPTION
1	NC	WLAN analog	—	Unused; leave unconnected.
4	NC	WLAN analog	—	Unused; leave unconnected.
16	NC	WLAN analog	—	Unused; leave unconnected.
17	NC	WLAN analog	—	Unused; leave unconnected.
18	NC	WLAN analog	—	Unused; leave unconnected.
20	NC	WLAN analog	—	Unused; leave unconnected.
26	NC	WLAN analog	—	Unused; leave unconnected.
27	NC	WLAN analog	—	Unused; leave unconnected.
28	NC	WLAN analog	—	Unused; leave unconnected.
53	NC	WLAN analog	—	Unused; leave unconnected.
58	NC	WLAN analog	—	TEST_58 Unused; leave unconnected.
59	NC	WLAN analog	—	TEST_59 Unused; leave unconnected.
63	NC	WLAN analog	—	TEST_60 Unused; leave unconnected.
64	NC	WLAN analog	—	Unused; leave unconnected.

7 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

7.1 Absolute Maximum Ratings

These specifications indicate levels where permanent damage to the device can occur. Functional operation is not ensured under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device. (1) (2)

		MIN	MAX	UNIT
V_{BAT} and V_{IO}	Pins: 37, 39, 44	–0.5	3.8	V
V_{IO} – V_{BAT} (differential)	Pins: 10, 54		0.0	V
Digital inputs		–0.5	V_{IO} + 0.5	V
RF pins		–0.5	2.1	V
Analog pins, crystal	Pins: 22, 23, 51, 52	–0.5	2.1	V
Operating temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Power-On Hours (POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

OPERATING CONDITION	POWER-ON HOURS [POH] (hours)
T_A up to 85°C(1)	87,600

(1) The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	TYP	MAX	UNIT
V_{BAT}, V_{IO} (shorted to V_{BAT})	Pins: 10, 37, 39, 44, 54	Direct battery connection(3)	2.1(6)	3.3	3.6	V
		Preregulated 1.85 V(4) (5)				
Ambient thermal slew			–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(3) To ensure WLAN performance, ripple on the 2.1- to 3.3-V supply must be less than ±300 mV.
(4) To ensure WLAN performance, ripple on the 1.85-V supply must be less than 2% (±40 mV).
(5) TI recommends keeping V_{BAT} above 1.85 V. For lower voltages, use a boost converter.
(6) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.

7.5 Current Consumption Summary

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER	TEST CONDITIONS(1) (4)		MIN	TYP	MAX	UNIT
TX	1 DSSS	TX power level = 0		272		mA
		TX power level = 4		188		
	6 OFDM	TX power level = 0		248		
		TX power level = 4		179		
	54 OFDM	TX power level = 0		223		
		TX power level = 4		160		
RX(6)	1 DSSS			53		mA
	54 OFDM			53		
Idle connected(2)				690		µA
LPDS				115		µA
Hibernate(5)				4.5		µA
Shutdown				1		µA
Peak calibration current(3) (6)	V_{BAT} = 3.6 V			420		mA
	V_{BAT} = 3.3 V			450		
	V_{BAT} = 2.1 V			670		
	V_{BAT} = 1.85 V			700		

(1) TX power level = 0 implies maximum power (see Figure 7-1, Figure 7-2, and Figure 7-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) DTIM = 1
(3) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see *CC3120, CC3220 SimpleLink™ Wi-Fi® and IoT Network Processor Programmer's Guide*.
(4) The CC3120R system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(5) For the 1.85-V mode, the hibernate current is higher by 50 µA across all operating modes because of leakage into the PA and analog power inputs.
(6) The RX current is measured with a 1-Mbps throughput rate.

7.6 TX Power and IBAT versus TX Power Level Settings

Figure 7-1, Figure 7-2, and Figure 7-3 show TX Power and IBAT versus TX power level settings for modulations of 1 DSSS, 6 OFDM, and 54 OFDM, respectively.

In Figure 7-1, the area enclosed in the circle represents a significant reduction in current during transition from TX power level 3 to level 4. In the case of lower range requirements (14-dBm output power), TI recommends using TX power level 4 to reduce the current.

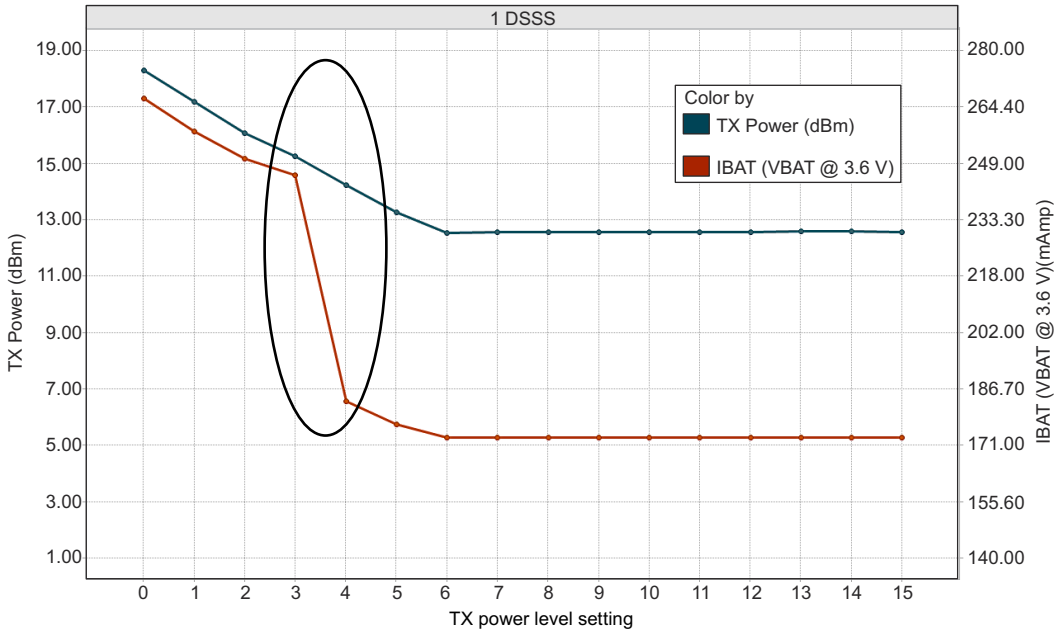


Figure 7-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

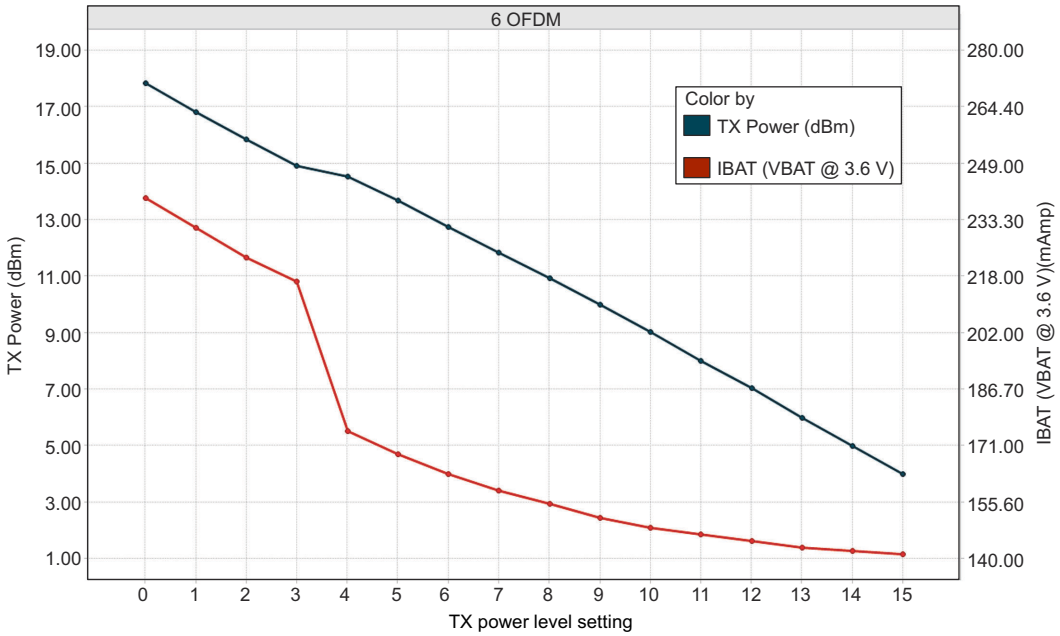


Figure 7-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

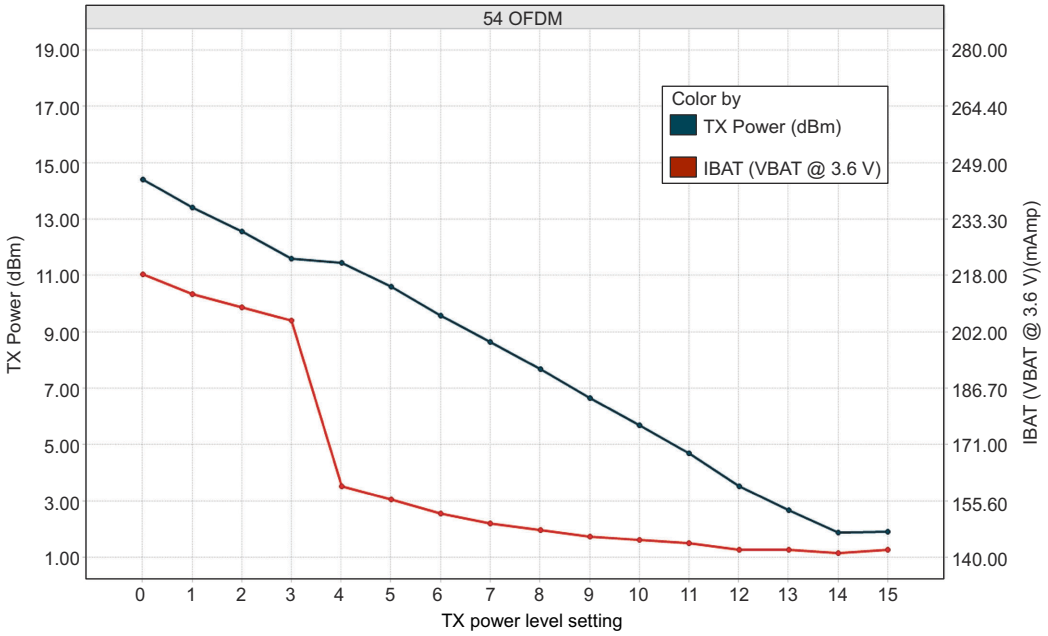


Figure 7-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

7.7 Brownout and Blackout Conditions

The device enters a brownout condition when the input voltage drops below $V_{brownout}$ (see Figure 7-4 and Figure 7-5). This condition must be considered during design of the power supply routing, especially when operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout condition. The resistance includes the internal resistance of the battery, the contact resistance of the battery holder (four contacts for 2× AA batteries), and the wiring and PCB routing resistance.

Note

When the device is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

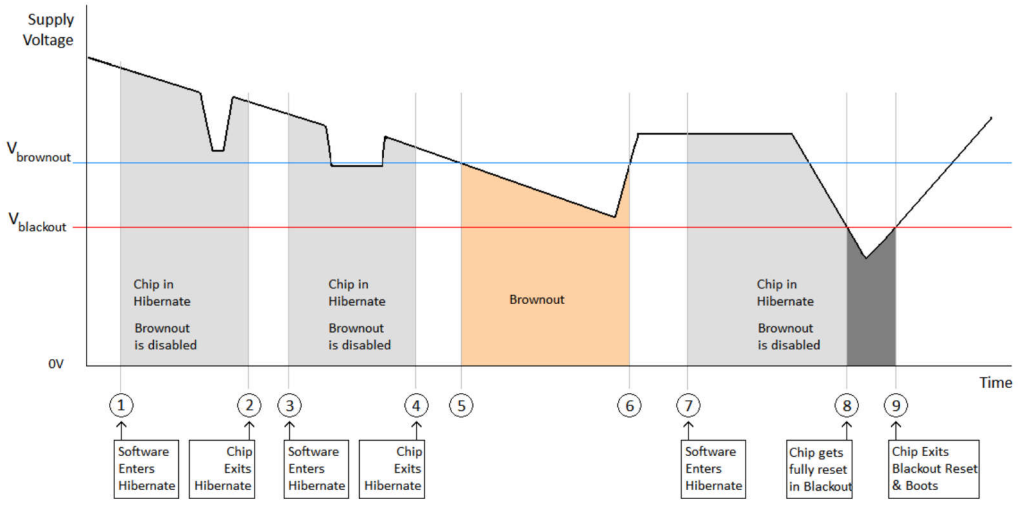


Figure 7-4. Brownout and Blackout Levels (1 of 2)

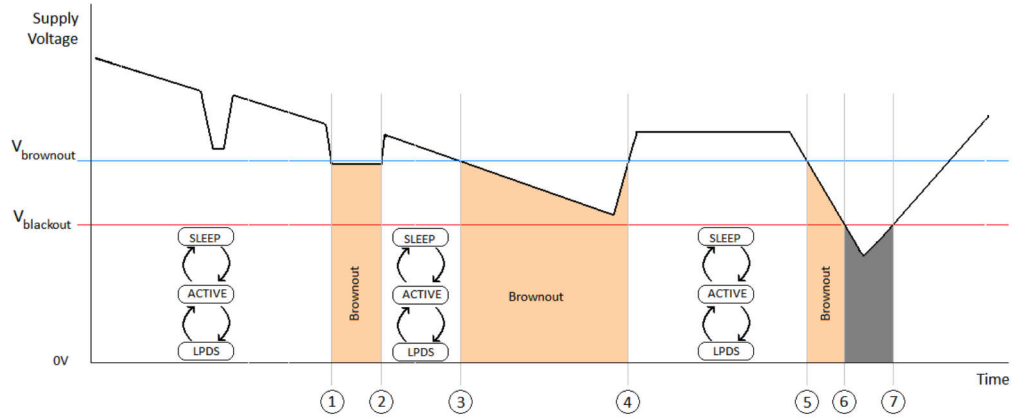


Figure 7-5. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the device (including the 32-kHz RTC) shut down except for the Hibernate module, which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost.

Table 7-1 lists the brownout and blackout voltage levels.

Table 7-1. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

7.8 Electrical Characteristics (3.3 V, 25°C)

GPIO Pins Except 29, 30, 50, 52, and 53 (25°C)[1]							
PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 8 mA; configured I/O drive strength = 8 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V			V_{DD} × 0.75	
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V			V_{DD} × 0.7	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 8 mA; configured I/O drive strength = 8 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V	V_{DD} × 0.25			
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V	V_{DD} × 0.35			
I_{OH}	High-level source current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			

GPIO Pins Except 29, 30, 50, 52, and 53 (25°C)[1]						
PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{OL}	Low-level sink current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			
V_{IL}	nRESET[2]			0.6			V

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.
(2) The nRESET pin must be held below 0.6 V for the device to register a reset.

7.9 WLAN Receiver Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters are measured at the SoC pin on channel 6 (2437 MHz).

PARAMETER	TEST CONDITIONS (Mbps)	MIN	TYP[1]	MAX	UNIT
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates) (10% PER)[3]	1 DSSS		–96.0		dBm
	2 DSSS		–94.0		
	11 CCK		–88.0		
	6 OFDM		–90.5		
	9 OFDM		–90.0		
	18 OFDM		–86.5		
	36 OFDM		–80.5		
	54 OFDM		–74.5		
	MCS7 (GF)[2]		–71.5		
	MCS7 (MM)[2]		–70.5		
Maximum input level (10% PER)	802.11b		–4.0		dBm
	802.11g		–10.0		

(1) In preregulated 1.85-V mode, RX sensitivity is 0.25- to 1-dB lower.
(2) Sensitivity for mixed mode is 1-dB worse.
(3) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

7.10 WLAN Transmitter Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters measured at SoC pin on channel 7 (2442 MHz).[1] [2] [3]

PARAMETER	TEST CONDITIONS[3]	MIN	TYP	MAX	UNIT
Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		18.0		dBm
	2 DSSS		18.0		
	11 CCK		18.3		
	6 OFDM		17.3		
	9 OFDM		17.3		
	18 OFDM		17.0		
	36 OFDM		16.0		
	54 OFDM		14.5		
	MCS7 (MM)		13.0		
Transmit center frequency accuracy		–25		25	ppm

(1) The edge channels (2412 and 2472 MHz) have reduced TX power to meet FCC emission limits.
(2) Power of 802.11b rates are reduced to meet ETSI requirements.
(3) In preregulated 1.85-V mode, maximum TX power is 0.25- to 0.75-dB lower for modulations higher than 18 OFDM.

7.11 WLAN Filter Requirements

The device requires an external band-pass filter to meet the various emission standards, including FCC. Section 7.11.1 presents the attenuation requirements for the band-pass filter. TI recommends using the same filter used in the reference design to ease the process of certification.

7.11.1 WLAN Filter Requirements

PARAMETER	FREQUENCY (MHz)	MIN	TYP	MAX	UNIT
Return loss	2412 to 2484	10			dB
Insertion loss(1)	2412 to 2484		1	1.5	dB
Attenuation	800 to 830	30	45		dB
	1600 to 1670	20	25		
	3200 to 3300	30	48		
	4000 to 4150	45	50		
	4800 to 5000	20	25		
	5600 to 5800	20	25		
	6400 to 6600	20	35		
	7200 to 7500	35	45		
	7500 to 10000	20	25		
Reference impendence	2412 to 2484		50		Ω
Filter type	Bandpass				

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

7.12 Thermal Resistance Characteristics

7.12.1 Thermal Resistance Characteristics for RGK Package

AIR FLOW				
PARAMETER	0 lfm (C/W)	150 lfm (C/W)	250 lfm (C/W)	500 lfm (C/W)
θ_{ja}	23	14.6	12.4	10.8
Ψ_{jt}	0.2	0.2	0.3	0.1
Ψ_{jb}	2.3	2.3	2.2	2.4
θ_{jc}	6.3			
θ_{jb}	2.4			

7.13 Reset Requirement

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	Operation mode level		0.65 × V_{BAT}		V
V_{IL}	Shutdown mode level(1)	0	0.6		V
	Minimum time for nReset low for resetting the module	5			ms
T_r and T_f	Rise and fall times		20		µs

(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

7.14 Timing and Switching Characteristics

7.14.1 Power Supply Sequencing

For proper operation of the CC3120R device, perform the recommended power-up sequencing as follows:

1. Tie V_{BAT} (pins 37, 39, 44) and V_{IO} (pins 54 and 10) together on the board.
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100 K ||, 1 µF, RC = 100 ms).
3. For an external RTC, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see Section 7.14.3.

7.14.2 Device Reset

When a device restart is required, the user may either issue a negative pulse on the nHIB pin (pin 2) or on the nRESET pin (pin 32), keeping the other pulled high, depending on the configuration of the platform. In case the nRESET pin is used, the user must follow one of the two alternatives to ensure the reset is properly applied:

- A high-to-low reset pulse (on pin 32) of at least 200-ms duration
- If the above cannot be ensured, a pulldown resistor of 2 MΩ should be connected to pin 52 (RTC_XTAL_N). If implemented, a shorter pulse of at least 100 µs can be used.

To ensure a proper reset sequence, the user has to call the sl_stop function prior to toggling the reset.

7.14.3 Reset Timing

7.14.3.1 nRESET (32-kHz Crystal)

Figure 7-6 shows the reset timing diagram for the 32-kHz crystal first-time power-up and reset removal.

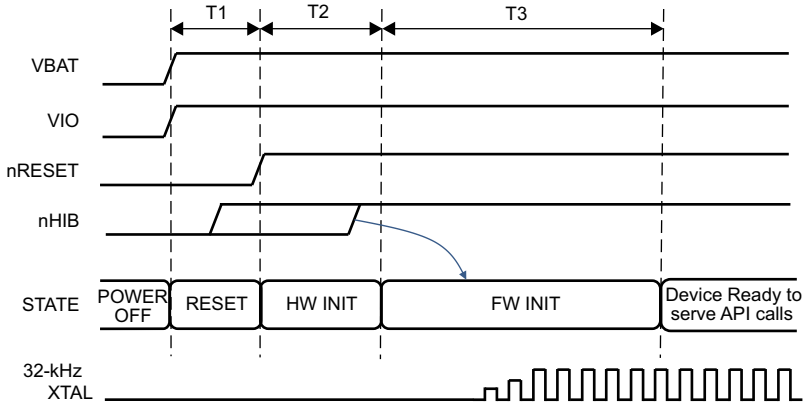


Figure 7-6. First-Time Power-Up and Reset Removal Timing Diagram (32-kHz Crystal)

Section 7.14.3.2 describes the timing requirements for the crystal first-time power-up and reset removal.

7.14.3.2 First-Time Power-Up and Reset Removal Timing Requirements (32-kHz Crystal)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	Depends on application board power supply, decoupling capacitor, and so on		3		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	32-kHz crystal settling plus firmware initialization time plus radio calibration		1.35		s

7.14.3.3 nRESET (External 32-kHz)

Figure 7-7 shows the reset timing diagram for the external 32-kHz first-time power-up and reset removal.

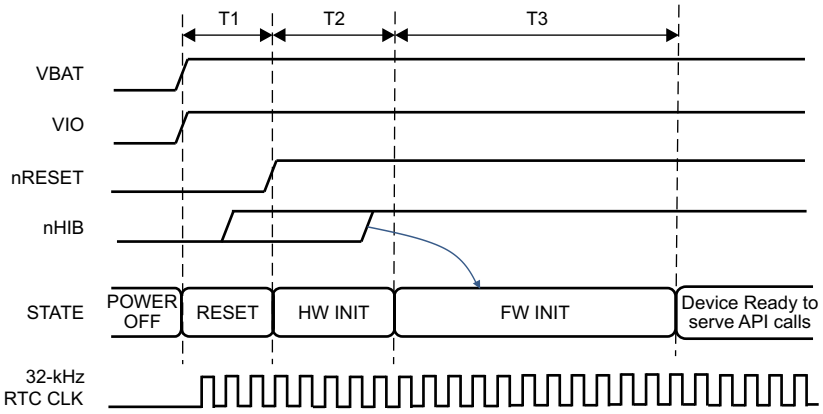


Figure 7-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32-kHz)

Section 7.14.3.3.1 describes the timing requirements for the external first-time power-up and reset removal.

7.14.3.3.1 First-Time Power-Up and Reset Removal Timing Requirements (External 32-kHz)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	Depends on application board power supply, decoupling capacitor, and so on		3		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	Firmware initialization time plus radio calibration		250		ms

7.14.4 Wakeup From HIBERNATE Mode

Figure 7-8 shows the timing diagram for wakeup from HIBERNATE mode.

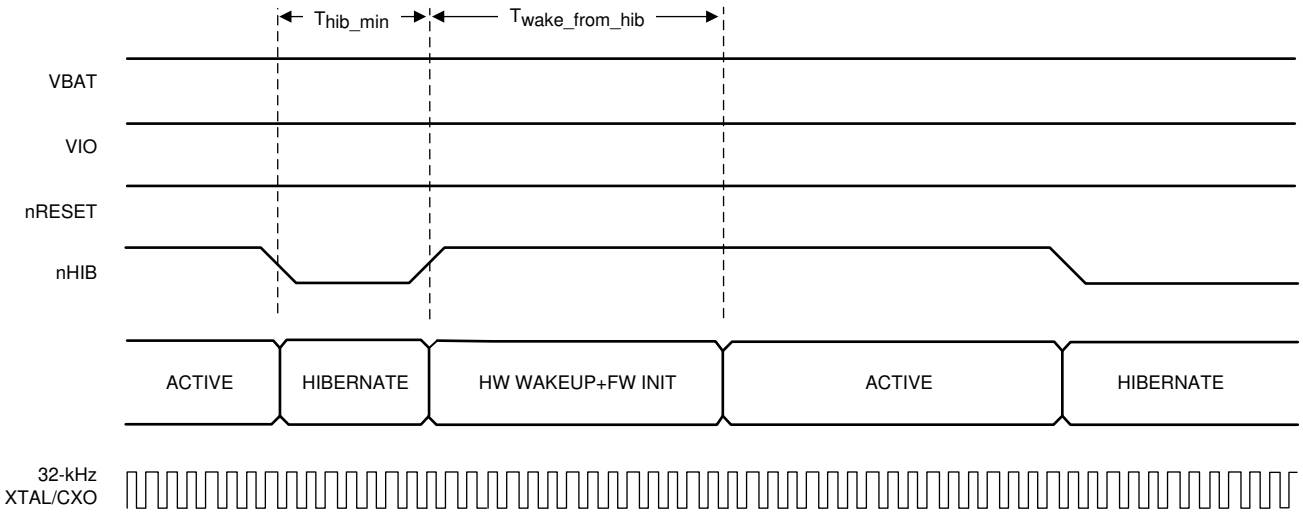


Figure 7-8. nHIB Timing Diagram

Note

The 32.768-kHz crystal is kept enabled by default when the chip goes into HIBERNATE mode in response to nHIB being pulled low.

Section 7.14.4.1 Section 7.14.4.1 describes the timing requirements for nHIB.

7.14.4.1 nHIB Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{hib_min}	Minimum hibernate time	Minimum pulse width of nHIB being low(2)	10			ms
$T_{wake\_from\_hib}$	Hardware wakeup time plus firmware initialization time	See(1)		50		ms

(1) If temperature changes by more than 20°C, initialization time from HIB can increase by 200 ms due to radio calibration.
(2) Ensure that the nHIB pulse width is kept above the minimum requirement under all conditions (such as power up, MCU reset, and so on).

7.14.5 Clock Specifications

The CC3120R device requires two separate clocks for its operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of less-expensive crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and to reduce overall cost.

7.14.5.1 Slow Clock Using Internal Oscillator

The RTC crystal connected on the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768 kHz ±150 ppm. In this mode of operation, the crystal is tied between RTC_XTAL_P (pin 51) and RTC_XTAL_N (pin 52) with a suitable load capacitance to meet the ppm requirement.

Figure 7-9 shows the crystal connections for the slow clock.

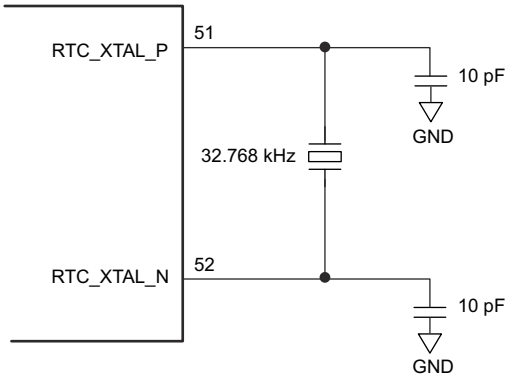


Figure 7-9. RTC Crystal Connections

Section 7.14.5.1.1 lists the RTC crystal requirements.

7.14.5.1.1 RTC Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			32.768		kHz
Frequency accuracy	Initial plus temperature plus aging			±150	ppm
Crystal ESR	32.768 kHz			70	kΩ

7.14.5.2 Slow Clock Using an External Clock

When an RTC oscillator is present in the system, the CC3120R device can accept this clock directly as an input. The clock is fed on the RTC_XTAL_P line, and the RTC_XTAL_N line is held to V_{IO}. The clock must be a CMOS-level clock compatible with V_{IO} fed to the device.

Figure 7-10 shows the external RTC input connection.

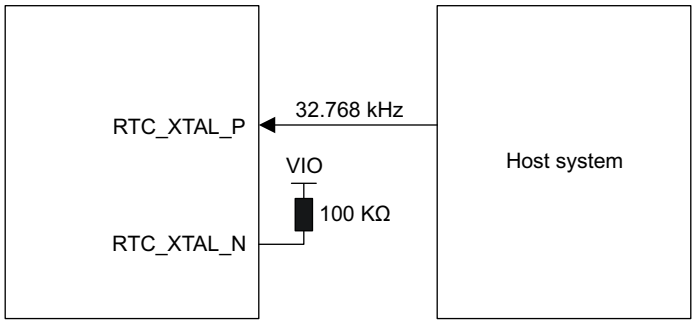


Figure 7-10. External RTC Input

Section 7.14.5.2.1 lists the external RTC digital clock requirements.

7.14.5.2.1 External RTC Digital Clock Requirements

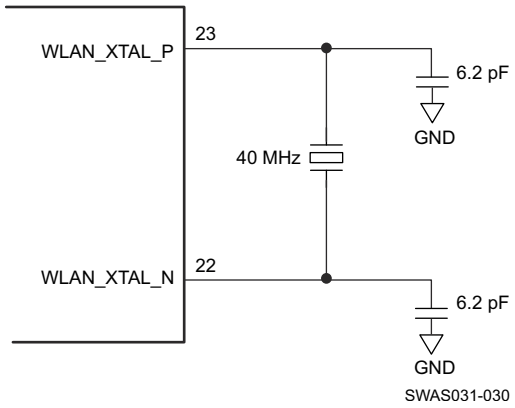
CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency			32768		Hz
	Frequency accuracy (Initial plus temperature plus aging)			±150		ppm
t_r, t_f	Input transition time t_r, t_f (10% to 90%)				100	ns

CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency input duty cycle			20%	50%	80%	
V_{ih}	Slow clock input voltage limits	Square wave, DC coupled	0.65 × V_{IO}		V_{IO}	V
V_{il}			0		0.35 × V_{IO}	V_{peak}
Input impedance			1			MΩ
					5	pF

7.14.5.3 Fast Clock (F_{ref}) Using an External Crystal

The CC3120R device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The crystal is fed directly between WLAN_XTAL_P (pin 23) and WLAN_XTAL_N (pin 22) with suitable loading capacitors.

Figure 7-11 shows the crystal connections for the fast clock.



A. The crystal capacitance must be tuned to ensure that the PPM requirement is met. See *CC31xx & CC32xx Frequency Tuning* for information on frequency tuning.

Figure 7-11. Fast Clock Crystal Connections

Section 7.14.5.3.1 lists the WLAN fast-clock crystal requirements.

7.14.5.3.1 WLAN Fast-Clock Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			40		MHz
Frequency accuracy	Initial plus temperature plus aging			±25	ppm
Crystal ESR	40 MHz			60	Ω

7.14.5.4 Fast Clock (F_{ref}) Using an External Oscillator

The CC3120R device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to WLAN_XTAL_P (pin 23). WLAN_XTAL_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 7-12 shows the connection.

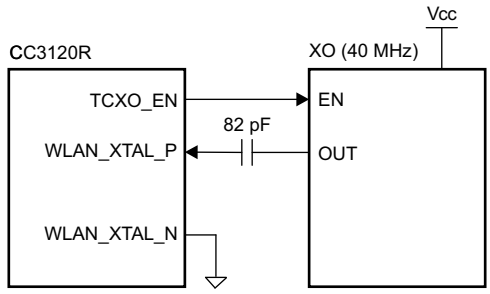


Figure 7-12. External TCXO Input

Section 7.14.5.4.1 lists the external F_{ref} clock requirements.

7.14.5.4.1 External F_{ref} Clock Requirements (–40°C to +85°C)

CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency				40.00		MHz
Frequency accuracy (Initial plus temperature plus aging)					±25	ppm
Frequency input duty cycle			45%	50%	55%	
V_{pp} Clock voltage limits		Sine or clipped sine wave, AC coupled	0.7		1.2	V_{pp}
Phase noise at 40 MHz		at 1 kHz			–125	dBc/Hz
		at 10 kHz			–138.5	
		at 100 kHz			–143	
Input impedance	Resistance		12			kΩ
	Capacitance				7	pF

7.14.6 Interfaces

This section describes the interfaces that are supported by the CC3120R device:

- Host SPI
- Flash SPI

7.14.6.1 Host SPI Interface Timing

Figure 7-13 shows the Host SPI interface timing diagram.

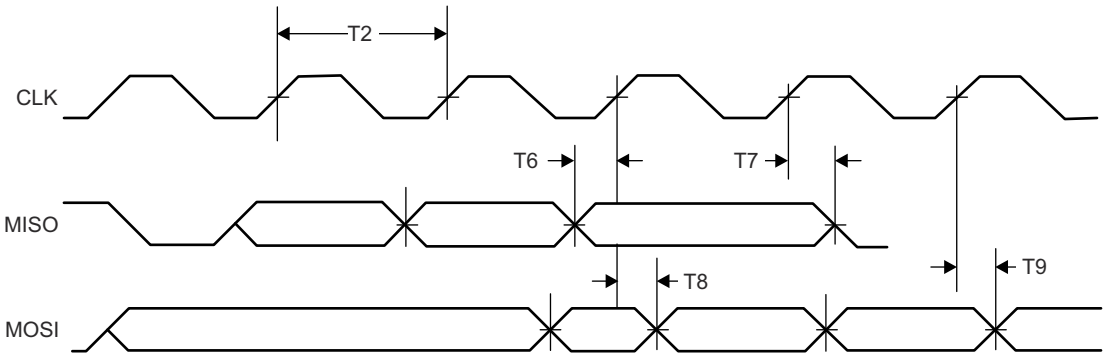


Figure 7-13. Host SPI Interface Timing

Section 7.14.6.1.1 lists the Host SPI interface timing parameters.

7.14.6.1.1 Host SPI Interface Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	F(1)	Clock frequency at V_{BAT} = 3.3 V		20	MHz
		Clock frequency at V_{BAT} ≤ 2.1 V		12	
T2	t_{clk} (1) (2)	Clock period	50		ns
T3	t_{LP} (1)	Clock low period		25	ns
T4	t_{HT} (1)	Clock high period		25	ns
T5	D(1)	Duty cycle	45%	55%	
T6	t_{IS} (1)	RX data setup time	4		ns
T7	t_{IH} (1)	RX data hold time	4		ns
T8	t_{OD} (1)	TX data output delay		20	ns
T9	t_{OH} (1)	TX data hold time		24	ns

(1) The timing parameter has a maximum load of 20 pF at 3.3 V.
(2) Ensure that nCS (active-low signal) is asserted 10 ns before the clock is toggled. The nCS can be deasserted 10 ns after the clock edge.

7.14.6.2 Flash SPI Interface Timing

Figure 7-14 shows the Flash SPI interface timing diagram.

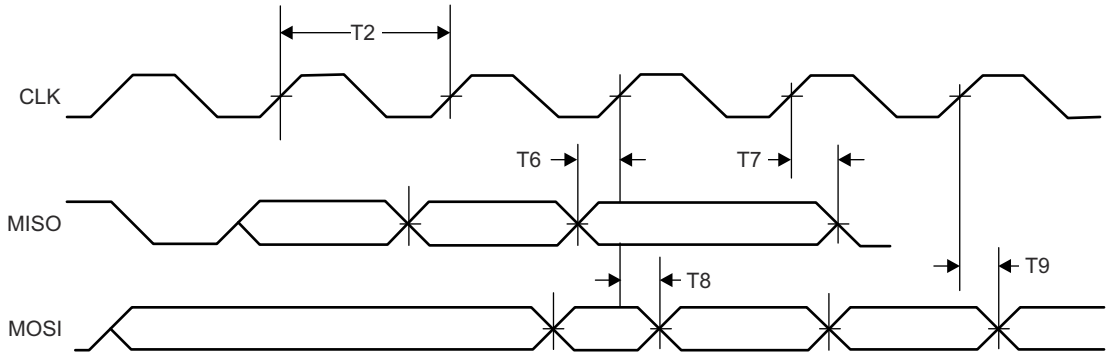


Figure 7-14. Flash SPI Interface Timing

Section 7.14.6.2.1 lists the Flash SPI interface timing parameters.

7.14.6.2.1 Flash SPI Interface Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	F	Clock frequency		20	MHz
T2	t_{clk}	Clock period	50		ns
T3	t_{LP}	Clock low period		25	ns
T4	t_{HT}	Clock high period		25	ns
T5	D	Duty cycle	45%	55%	
T6	t_{IS}	RX data setup time	1		ns
T7	t_{IH}	RX data hold time	2		ns
T8	t_{OD}	TX data output delay		8.5	ns
T9	t_{OH}	TX data hold time		8	ns

7.15 External Interfaces

7.15.1 SPI Flash Interface

The external serial Flash stores the user profiles and firmware patch updates. The CC3120R device acts as a master in this case; the SPI serial Flash acts as the slave device. This interface can work up to a speed of 20 MHz.

Figure 7-15 shows the SPI Flash interface.

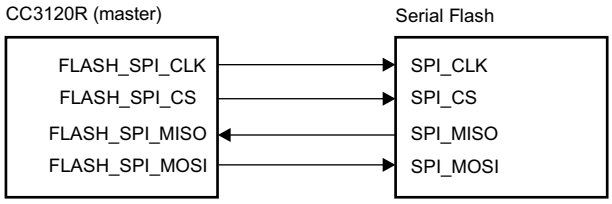


Figure 7-15. SPI Flash Interface

Section 7.15.1.1 lists the SPI Flash interface pins.

7.15.1.1 SPI Flash Interface

PIN NAME	DESCRIPTION
FLASH_SPI_CLK	Clock (up to 20 MHz) CC3120R device to serial Flash
FLASH_SPI_CS	CS signal from CC3120R device to serial Flash
FLASH_SPI_MISO	Data from serial Flash to CC3120R device
FLASH_SPI_MOSI	Data from CC3120R device to serial Flash

7.15.2 SPI Host Interface

The device interfaces to an external host using the SPI interface. The CC3120R device can interrupt the host using the HOST_INTR line to initiate the data transfer over the interface. The SPI host interface can work up to a speed of 20 MHz.

Figure 7-16 shows the SPI host interface.

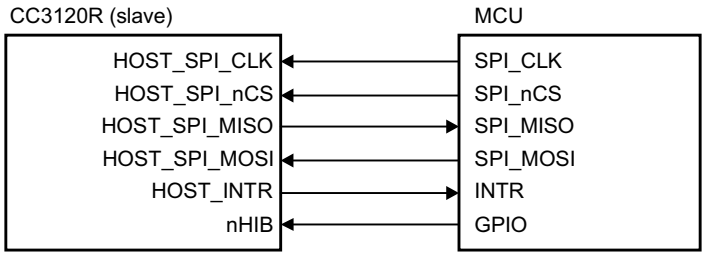


Figure 7-16. SPI Host Interface

Section 7.15.2.1 lists the SPI host interface pins.

7.15.2.1 SPI Host Interface

PIN NAME	DESCRIPTION
HOST_SPI_CLK	Clock (up to 20 MHz) from MCU host to CC3120R device
HOST_SPI_nCS	CS (active low) signal from MCU host to CC3120R device
HOST_SPI_MOSI	Data from MCU host to CC3120R device
HOST_INTR	Interrupt from CC3120R device to MCU host
HOST_SPI_MISO	Data from CC3120R device to MCU host
nHIB	Active-low signal that commands the CC3120R device to enter hibernate mode (lowest power state)

7.15.3 Host UART Interface

The SimpleLink device requires the UART configuration described in Section 7.15.3.1.

7.15.3.1 SimpleLink™ UART Configuration

PROPERTY	SUPPORTED CC3120R CONFIGURATION
Baud rate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first
Host interrupt polarity	Active high
Host interrupt mode	Rising edge or level 1
Endianness	Little-endian only(1)

(1) The SimpleLink device does not support automatic detection of the host length while using the UART interface.

7.15.3.2 5-Wire UART Topology

Figure 7-17 shows the typical 5-wire UART topology comprised of four standard UART lines plus one IRQ line from the device to the host controller to allow efficient low-power mode.

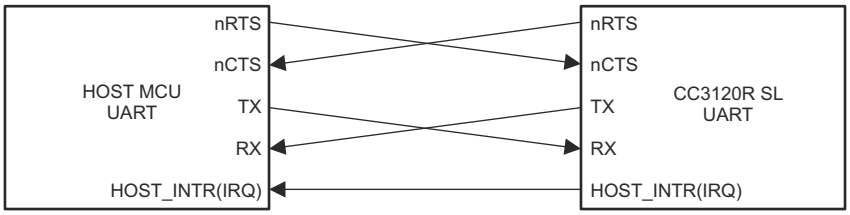


Figure 7-17. Typical 5-Wire UART Topology

This topology is recommended because the configuration offers the maximum communication reliability and flexibility between the host and the SimpleLink device.

7.15.3.3 4-Wire UART Topology

The 4-wire UART topology eliminates the host IRQ line (see Figure 7-18). Using this topology requires meeting one of the following conditions:

- The host is always awake or active.
- The host goes to sleep, but the UART module has receiver start-edge detection for auto wakeup and does not lose data.

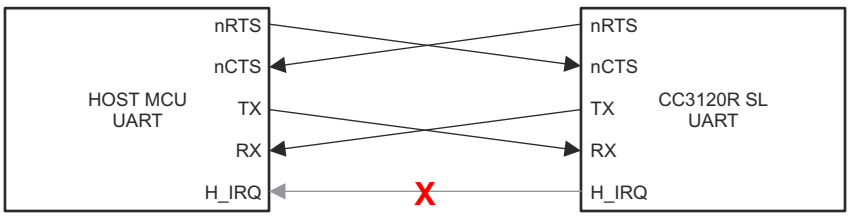


Figure 7-18. 4-Wire UART Configuration

7.15.3.4 3-Wire UART Topology

The 3-wire UART topology requires only the following lines (see Figure 7-19):

- RX
- TX
- CTS

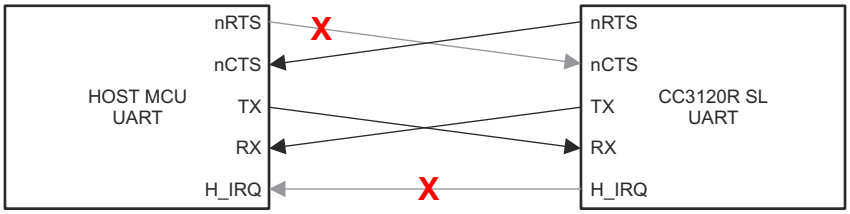


Figure 7-19. 3-Wire UART Topology

Using this topology requires meeting one of the following conditions:

- The host always stays awake or active.
- The host goes to sleep but the UART module has receiver start-edge detection for auto-wake-up and does not lose data.
- The host can always receive any amount of data transmitted by the SimpleLink device because there is no flow control in this direction.

Because there is no full flow control, the host cannot stop the SimpleLink device to send its data; thus, the following parameters must be carefully considered:

- Maximum baud rate
- RX character interrupt latency and low-level driver jitter buffer
- Time consumed by the user's application

8 Detailed Description

The CC3120R Wi-Fi Internet-on-a-chip contains a dedicated Arm MCU that offloads many of the networking activities from the host MCU. The device includes an 802.11b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3120R device supports station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security, WPS 2.0, and WPA3 personal and enterprise security. The Wi-Fi network processor includes an embedded IPv6 and IPv4 TCP/IP stack.

8.1 Device Features

8.1.1 WLAN

The WLAN features are as follows:

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct client and group owner with CCK and OFDM rates in the 2.4GHz ISM band, channels 1 to 13.

Note

802.11n is supported only in Wi-Fi station, Wi-Fi direct, and P2P client mode.

- Autocalibrated radio with a single-ended 50Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial Flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x), WPA3 Personal, and WPA3 Enterprise.

Note

When using WPA Enterprise security modes, the TLS socket used to communicate with the Radius server is limited to TLSv1.0.

- Smart provisioning options deeply integrated within the device providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point using HTTPS
  - SmartConfig Technology: a 1-step, 1-time process to connect a CC3120R-enabled device to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, it is usable by deeply embedded applications
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket without adding MAC or PHY headers. The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.

8.1.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD (BSD adjacent) socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

Note

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, or RAW sockets
- Support of 6 simultaneous SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet

- Built-in network application and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial Flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks
  - Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3120R device provides critical information, such as device name, IP, vendor, and port number.
  - DHCP server
  - Ping

Table 8-1 summarizes the NWP features.

Table 8-1. NWP Features

Feature	Description
Wi-Fi standards	802.11b/g/n station 802.11b/g AP supporting up to four stations Wi-Fi Direct client and group owner
Wi-Fi	Channels 1 to 13
Wi-Fi security	WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x), WPA3 personal and enterprise
Wi-Fi provisioning	SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP/HTTPS web server
IP protocols	IPv4/IPv6
IP addressing	Static IP, LLA, DHCPv4, DHCPv6 (Stateful) with DAD and stateless auto configuration
Cross layer	ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP
Transport	UDP, TCP SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2 RAW IP
Network applications and utilities	Ping HTTP/HTTPS web server mDNS DNS-SD DHCP server
Host interface	UART/SPI
Security	Device identity Trusted root-certificate catalog TI root-of-trust public key
Power management	Enhanced power policy management uses 802.11 power save and deep sleep power modes
Other	RF Transceiver Programmable RX Filters with Events trigger mechanism including WoWLAN Recovery mechanism – Restore to factory default

8.1.3 Security

The SimpleLink Wi-Fi CC3120R Internet-on-a-chip device enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0 MSCHAPv2
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2
- Secure sockets
  - Protocol versions: SSL v3/TLS 1.0/TLS 1.1/TLS 1.2
  - On-chip powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256

  - Server authentication
  - Client authentication
  - Domain name verification
  - Socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- The Trusted root-certificate catalog verifies that the CA used by the application is trusted and known secure content delivery
- The TI root-of-trust public key is a hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery allows file transfer to the system in a secure way on any unsecured tunnel

Code and Data Security:

- Secured network information: Network passwords and certificates are encrypted
- Secured and authenticated service pack: SP is signed based on TI certificate

8.1.4 Host Interface and Driver

- Interfaces over a 4-wire serial peripheral interface (SPI) with any MCU or a processor at a clock speed of 20 MHz.
- Interfaces over UART with any MCU with a baud rate up to 3 Mbps. A low footprint driver is provided for TI MCUs and is easily ported to any processor or ASIC.
- Simple APIs enable easy integration with any single-threaded or multithreaded application.

8.1.5 System

- Works from a single preregulated power supply or connects directly to a battery
- Ultra-low leakage when disabled (hibernate mode) with a current of less than 4 µA with the RTC running
- Integrated clock sources

8.2 Power-Management Subsystem

The CC3120R power-management subsystem contains DC/DC converters to accommodate the different voltage or current requirements of the system.

- Digital DC/DC (Pin 44)
  - Input: V_{BAT} wide voltage (2.1 to 3.6 V) or preregulated 1.85 V
- ANA1 DC/DC (Pin 38)
  - Input: V_{BAT} wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the ANA1 DC/DC converter is bypassed.
- PA DC/DC (Pin 39)
  - Input: V_{BAT} wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the PA DC/DC converter is bypassed.

The CC3120R device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources. For maximum flexibility, the device can operate in the modes described in Section 8.2.1 and Section 8.2.2.

8.2.1 V_{BAT} Wide-Voltage Connection

In the wide-voltage battery connection, the device is powered directly by the battery or preregulated 3.3-V supply . All other voltages required to operate the device are generated internally by the DC/DC converters. This scheme supports wide-voltage operation from 2.1 to 3.6 V and is thus the most common mode for the device.

8.2.2 Preregulated 1.85V

The preregulated 1.85-V mode of operation applies an external regulated 1.85 V directly at pins 10, 25, 33, 36, 37, 39, 44, 48, and 54 of the device. The V_{BAT} and the V_{IO} are also connected to the 1.85-V supply. This mode provides the lowest BOM count version in which inductors used for PA DC/DC and ANA1 DC/DC (2.2 and 1 µH) and a capacitor (22 µF) can be avoided.

In the preregulated 1.85-V mode, the regulator providing the 1.85 V must have the following characteristics:

- Load current capacity ≥900 mA
- Line and load regulation with <2% ripple with 500-mA step current and settling time of < 4 µs with the load step

Note

The regulator must be placed as close as possible to the device so that the IR drop to the device is very low.

8.3 Low-Power Operating Modes

This section describes the low-power modes supported by the device to optimize battery life.

8.3.1 Low-Power Deep Sleep

The low-power deep-sleep (LPDS) mode is an energy-efficient and transparent sleep mode that is entered automatically during periods of inactivity based on internal power optimization algorithms. The device can wake up in less than 3 ms from the internal timer or from any incoming host command. Typical battery drain in this mode is 115 µA. During LPDS mode, the device retains the software state and certain configuration information. The operation is transparent to the external host; thus, no additional handshake is required to enter or exit LPDS mode.

8.3.2 Hibernate

The hibernate mode is the lowest power mode in which all of the digital logic is power-gated. Only a small section of the logic powered directly by the main input supply is retained. The RTC is kept running and the device wakes up once the nHIB line is asserted by the host driver. The wake-up time is longer than LPDS mode at approximately 50 ms. The typical battery drain in this mode is 4.5 µA.

Note

Wake-up time can be extended depending on the service-pack size.

8.3.3 Shutdown

The shutdown mode is the lowest power-mode system-wise. All device logics are off, including the real-time clock (RTC). The wake-up time in this mode is longer than hibernate at approximately 1.1 s. The typical battery drain in this mode is 1 µA.

8.4 Memory

8.4.1 External Memory Requirements

The CC3120R device maintains a proprietary file system on the serial flash. The CC3120R file system stores the service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always at the beginning of the serial flash. The applications microcontroller must access the serial flash memory area allocated to the file system directly through the CC3120R file system. The applications microcontroller must not access the serial flash memory area directly.

The file system manages the allocation of serial flash blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on serial flash using human-readable filenames rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system.

All file types can have a maximum of 100 supported files in the file system. All files are stored in 4-KB blocks and thus use a minimum of 4KB of Flash space. Fail-safe files require twice the original size and use a minimum of 8KB. Encrypted files are counted as fail-safe in terms of space. The maximum file size is 1MB.

Table 8-2 lists the minimum required memory consumption under the following assumptions:

- System files in use consume 64 blocks (256KB).
- Vendor files are not taken into account.
- Gang image:
  - Storage for the gang image is rounded up to 32 blocks (meaning 128KB resolution).
  - Gang image size depends on the actual content size of all components. Additionally, the image should be 128KB aligned so unaligned memory is considered lost. Service pack, system files, and the 128KB aligned memory are assumed to occupy 256KB.
- All calculations consider that the restore-to-default is enabled.

Table 8-2. Recommended Flash Size

ITEM	CC3120 [KB]
File system allocation table	20
System and configuration files	256
Service Pack	264
Gang image size	256
Total	796
Minimal Flash size	8MBit
Recommended Flash size	16MBit

Note

The maximum supported serial flash size is 32MB (256Mb). See the *Using Serial Flash on CC3120/CC3220 SimpleLink™ Wi-Fi® and Internet-of-Things Devices* application report.

8.5 Restoring Factory Default Configuration

The device has an internal recovery mechanism that allows rolling back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the serial flash in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None—no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by pulling or forcing SOP[2:0] = 110 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial Flash vendor.

9 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Typical Application—CC3120R Wide-Voltage Mode

Figure 9-1 shows the typical application schematic using the CC3120R device in the wide-voltage mode of operation. For a full operation reference design, refer to the BoosterPack that uses the CC3120R device (see *CC3120 SimpleLink™ and Internet of Things Hardware Design Files*).

Table 9-1 lists the bill of materials for an application using the CC3120R device in wide-voltage mode.

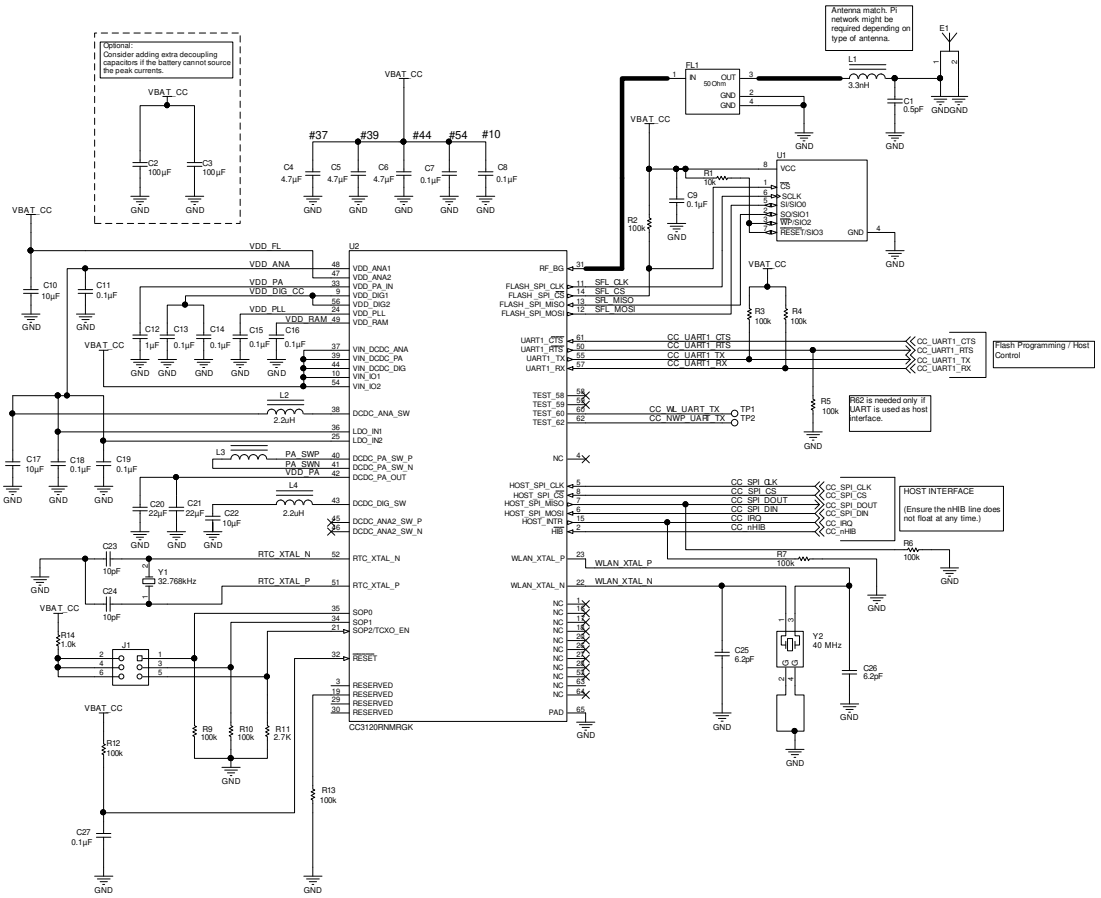


Figure 9-1. CC3120R Wide-Voltage Mode Application Circuit

Table 9-1. Bill of Materials for CC3120R in Wide-Voltage Mode

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C1	0.5 pF	Murata	GRM1555C1HR50BA01D	Capacitor, Ceramic, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402
2	C2, C3	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	Capacitor, Ceramic, 100 µF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210
3	C4, C5, C6	4.7 µF	TDK	C1005X5R0J475M050BC	Capacitor, Ceramic, 4.7 µF, 6.3 V, ±20%, X5R, 0402
11	C7, C8, C9, C11, C13, C14, C15, C16, C18, C19, C27	0.1 µF	TDK	C1005X5R1A104K050BA	Capacitor, Ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402
3	C10, C17, C22	10 µF	Murata	GRM188R60J106ME47D	Capacitor, Ceramic, 10 µF, 6.3 V, ±20%, X5R, 0603
1	C12	1 µF	TDK	C1005X5R1A105K050BB	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
2	C20, C21	22 µF	TDK	C1608X5R0G226M080AA	Capacitor, Ceramic, 22 µF, 4 V, ±20%, X5R, 0603
2	C23, C24	10 pF	Johanson Technology	500R07S100JV4T	Capacitor, Ceramic, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C25, C26	6.2 pF	Murata	GRM1555C1H6R2CA01D	Capacitor, Ceramic, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
1	E1	2.45-GHz Antenna	Taiyo Yuden	AH316M245001-T	ANT Bluetooth W-LAN Zigbee® WiMAX™, SMD
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4GHz W-LAN/Bluetooth, SMD
1	L1	3.3 nH	Murata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 ohm, SMD
2	L2, L4	2.2 µH	Murata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	L3	1 µH	Murata	LQM2HPN1R0MG0L	Inductor, Multilayer, Ferrite, 1 µH, 1.6 A, 0.055 ohm, SMD
1	R1	10 k	Vishay-Dale	CRCW040210K0JNED	RES, 10 k, 5%, 0.063 W, 0402
1	R11	2.7 k	Vishay-Dale	CRCW04022K70JNED	RES, 2.7 k, 5%, 0.063 W, 0402
10	R2, R3, R4, R5, R6, R7, R9, R10, R12, R13	100 k	Vishay-Dale	CRCW0402100KJNED	RES, 100 k, 5%, 0.063 W, 0402
1	R14	1.0 k	Vishay-Dale	CRCW04021K00JNED	RES, 1.0 k, 5%, 0.063 W, 0402
1	U1	MX25R	Macronix International Co., LTD	MX25R1635FM1IL0	Ultra-Low Power, 16-Mbit [x 1/x 2/x 4] CMOS MXSMIO (Serial Multi I/O) Flash Memory, SOP-8
1	U2	CC3120	Texas Instruments	CC3120RNMRGK	SimpleLink™ Wi-Fi® Network Processor, internet-of-things Solution for MCU Applications, RGK0064B
1	Y1	Crystal	Abracon Corporation	ABS07-32.768KHZ-9-T	CRYSTAL, 32.768 kHz, 9 pF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40 MHz, 8 pF, SMD

9.1.2 Typical Application Schematic—CC3120R Preregulated, 1.85-V Mode

Figure 9-2 shows the typical application schematic using the CC3120R in preregulated, 1.85-V mode of operation. For addition information on this mode of operation please contact your TI representative.

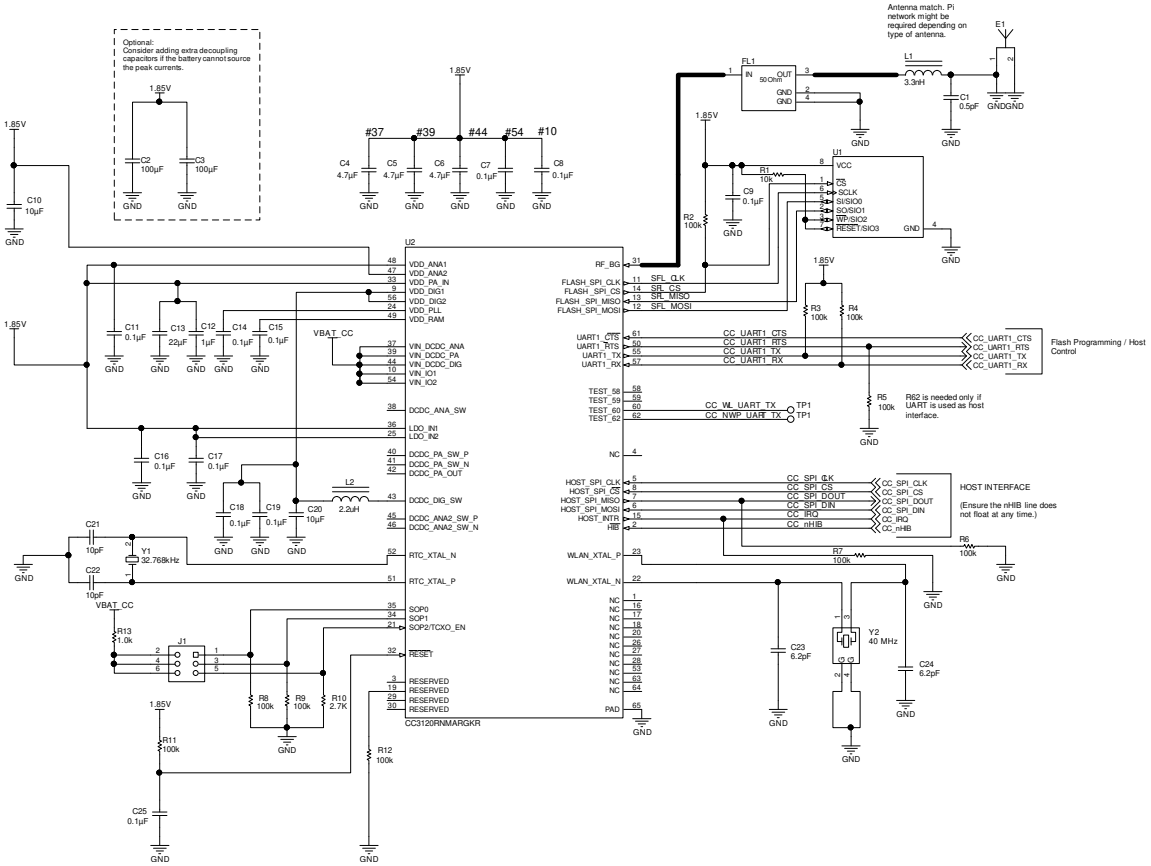


Figure 9-2. CC3120R Preregulated 1.85-V Mode Application Circuit

Table 9-2 lists the bill of materials for an application using the CC3120R device in preregulated 1.85-V mode.

Table 9-2. Bill of Materials for CC3120R in Preregulated, 1.85-V Mode

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C1	0.5 pF	MuRata	GRM1555C1HR50BA01D	Capacitor, Ceramic, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402
2	C2, C3	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	Capacitor, Ceramic, 100 µF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210
3	C4, C5, C6	4.7 µF	TDK	C1005X5R0J475M050BC	Capacitor, Ceramic, 4.7 µF, 6.3 V, ±20%, X5R, 0402
11	C7, C8, C9, C11, C14, C15, C16, C17, C18, C19, C25	0.1 µF	TDK	C1005X5R1A104K050BA	Capacitor, Ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402
2	C10, C20	10 µF	MuRata	GRM188R60J106ME47D	Capacitor, Ceramic, 10 µF, 6.3 V, ±20%, X5R, 0603
1	C12	1 µF	TDK	C1005X5R1A105K050BB	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
1	C13	22 µF	TDK	C1608X5R0G226M080AA	Capacitor, Ceramic, 22 µF, 4 V, ±20%, X5R, 0603
2	C21, C22	10 pF	Johanson Technology	500R07S100JV4T	Capacitor, Ceramic, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C23, C24	6.2 pF	MuRata	GRM1555C1H6R2CA01D	Capacitor, Ceramic, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
1	E1	2.45-GHz Antenna	Taiyo Yuden	AH316M245001-T	ANT Bluetooth W-LAN Zigbee® WiMAX™, SMD
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4-GHz W-LAN/Bluetooth, SMD
1	L1	3.3 nH	MuRata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 ohm, SMD
1	L2	2.2 µH	MuRata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	R1	10 k	Vishay-Dale	CRCW040210K0JNED	Resistor, 10 k, 5%, 0.063 W, 0402
10	R2, R3, R4, R5, R6, R7, R8, R9, R11, R12	100 k	Vishay-Dale	CRCW0402100KJNED	Resistor, 100 k, 5%, 0.063 W, 0402
1	R10	2.7 k	Vishay-Dale	CRCW04022K70JNED	Resistor, 2.7 k, 5%, 0.063 W, 0402
1	R13	1.0 k	Vishay-Dale	CRCW04021K00JNED	Resistor, 1.0 k, 5%, 0.063 W, 0402
1	U1	MX25R	Macronix International Co., LTD	MX25R1635FM1IL0	Ultra-Low Power, 16M-BIT [x 1/x 2/x 4] CMOS MXSMIO (Serial Multi I/O) Flash Memory, SOP-8
1	U2	CC3120	Texas Instruments	CC3120RNMRGK	SimpleLink™ Wi-Fi®Network Processor, internet-of-things Solution for MCU Applications, RGK0064B
1	Y1	Crystal	Abracon Corportation	ABS07-32.768KHZ-9-T	Crystal, 32.768 kHz, 9 pF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40 MHz, 8 pF, SMD

9.2 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC3120R VQFN device. Follow these guidelines ensures that the design will minimize the risk with regulatory certifications including FCC, ETSI, and CE. For more information, see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.

9.2.1 General PCB Guidelines

Use the following PCB guidelines:

- Verify the recommended PCB stackup in the PCB design guidelines, as well as the recommended layers for signals and ground.
- Ensure that the PCB footprint of the VQFN follows the information in .
- Ensure that the GND and solder paste of the VQFN PCB follow the recommendations provided in *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.
- Decoupling capacitors must be as close as possible to the VQFN device.

9.2.2 Power Layout and Routing

Three critical DC/DC converters must be considered for the CC3120R device.

- Analog DC/DC converter
- PA DC/DC converter
- Digital DC/DC converter

Each converter requires an external inductor and capacitor that must be laid out with care. DC current loops are formed when laying out the power components.

9.2.2.1 Design Considerations

The following design guidelines must be followed when laying out the CC3120R device:

- Route all of the input decoupling capacitors (C11, C13, and C18) on L2 using thick traces, to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pins 33, 40, 41, and 42), and all input supply pins (pins 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close to the respective pins as possible.
- Power budget: The CC3120R device can consume up to 450 mA for 3.3 V, 670 mA for 2.1 V, and 700 mA for 1.85 V, for 24 ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.
- The CC3120R device contains many high-current input pins. Ensure the trace feeding these pins is capable of handling the following currents:
  - VIN_DCDC_PA input (pin 39) maximum is 1 A
  - VIN_DCDC_ANA input (pin 37) maximum is 600 mA
  - VIN_DCDC_DIG input (pin 44) maximum is 500 mA
  - DCDC_PA_SW_P (pin 40) and DCDC_PA_SW_N (pin 41) switching nodes maximum is 1 A
  - DCDC_PA_OUT output node (pin 42) maximum 1 A
  - DCDC_ANA_SW switching node (pin 38) maximum is 600 mA
  - DCDC_DIG_SW switching node (pin 43) maximum is 500 mA
  - VDD_PA_IN supply (pin 33) maximum is 500 mA

Figure 9-3 shows the ground routing for the input decoupling capacitors.

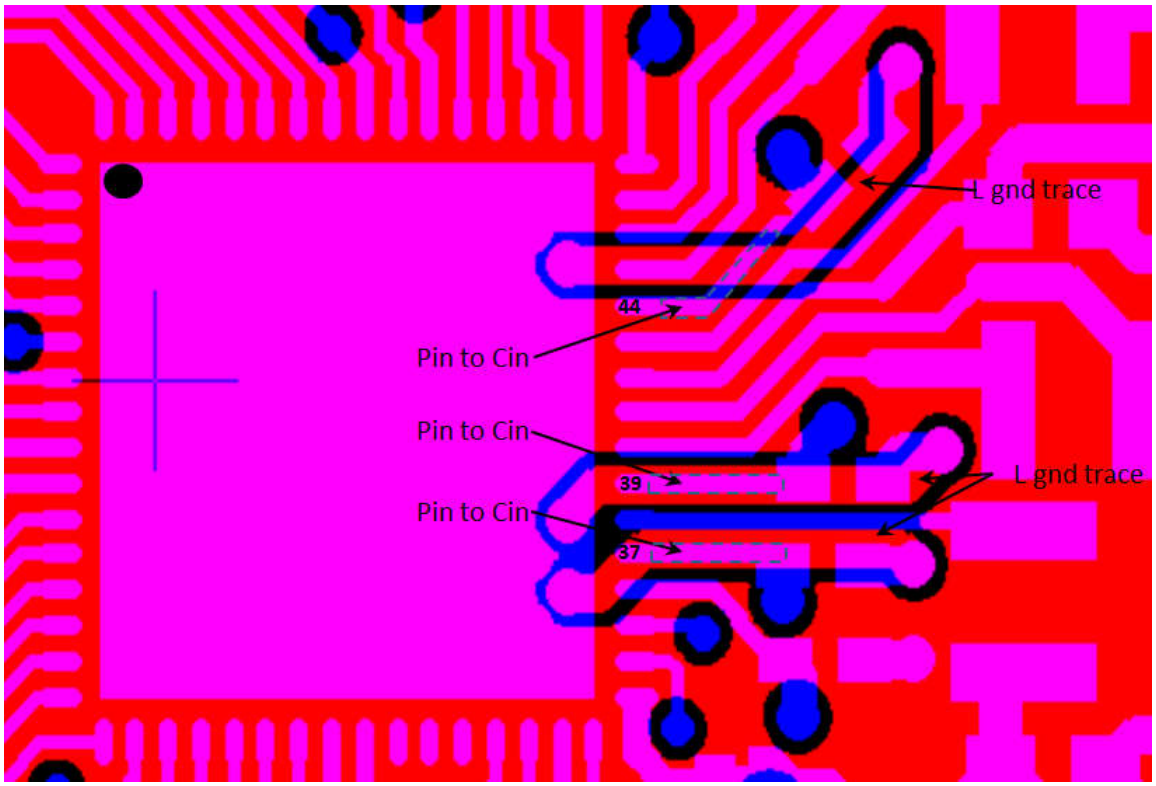


Figure 9-3. Ground Routing for the Input Decoupling Capacitors

The ground return for the input capacitors are routed on L2 to reduce the EMI and improve the spectral mask. This routing must be strictly followed because it is critical for the overall performance of the device.

9.2.3 Clock Interfaces

The following guidelines are for the slow clock.

- The 32.768-kHz crystal must be placed close to the VQFN package.
- Ensure that the load capacitance is tuned according to the board parasitics to the frequency tolerance is within ±150 ppm.
- The ground plane on layer two is solid below the trace lanes and there is ground around these traces on the top layer.

The following guidelines are for the fast clock.

- The 40-MHz crystal must be placed close to the VQFN package.
- Ensure that he load capacitance is tuned according to the board parasitics to the frequency tolerance is within ±100 ppm at room temperature. The total frequency across parts, temperature, and with aging, must be ±25 ppm to meet the WLAN specification.
- Ensure that no high-frequency lines are routed close to the crystal routing to avoid noise degradation.
- Ensure that crystal tuning capacitors are close to the crystal pads.
- Make both traces (XTAL_N and XTAL_P) as close to parallel as possible and approximately the same length.
- The ground plane on layer two is solid below the trace lines and that there is ground around these traces on the top layer.
- See *CC31xx & CC32xx Frequency Tuning* for frequency tuning.

9.2.4 Digital Input and Output

The following guidelines are for the digital I/O.

- Route SPI and UART lines away from any RF traces.
- Keep the length of the high-speed lines as short as possible to avoid transmission line effects.
- Keep the line lower than 1/10 of the rise time of the signal to ignore transmission line effects. This is required if the traces cannot be kept short. Place the resistor at the source end, closer to the device that is driving the signal.
- Add a series-terminating resistor for each high-speed line (such as SPI_CLK or SPI_DATA) to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.
- Route high-speed lines with a ground reference plane continuously below it to offer good impedance throughout. This routing also helps shield the trace against EMI.
- Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.
- If the lines are longer compared to the rise time, add series-terminating resistors near the driver for each high-speed line to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.

9.2.5 RF Interface

The following guidelines are for the RF interface. Follow guidelines specified in the vendor-specific antenna design guides (including placement of the antenna). Also see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines* for general antenna guidelines.

- Ensure that the antenna is matched for 50-Ω. TI recommends using a Pi-matching network.
- Ensure that the area underneath the BPF pads is grounded on layer one and layer two, and ensure that the minimum filter requirements are met.
- Verify that the Wi-Fi RF trace is a 50-Ω, impedance-controlled trace with a reference to solid ground.
- The RF trace bends must be made with gradual curves. Avoid using 90-degree bends.
- The RF traces must not have sharp corners.
- Do not place traces or ground under the antenna section.
- The RF traces must have via stitching on the ground plane beside the RF trace on both sides.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

10.1 Development Tools and Software

For the most up-to-date list of development tools and software, see the *CC3120 Tools & Software* product page. Users can also click the "Alert Me" button on the top right corner of the *CC3120 Tools & Software* page to stay informed about updates related to the CC3120MOD device.

Development Tools

SimpleLink™ Wi-Fi® Starter Pro	The supported devices are: CC3100, CC3200, CC3120R, and CC3220x. The SimpleLink™ Wi-Fi® Starter Pro mobile App is a new mobile application for SimpleLink provisioning. The app goes along with the embedded provisioning library and example that runs on the device side (see *SimpleLink™ Wi-Fi® CC3120 SDK plugin* and *TI SimpleLink™ Wi-Fi® CC3220 Software Development Kit (SDK)*). The new provisioning release is a TI recommendation for Wi-Fi provisioning using SimpleLink Wi-Fi products. The provisioning release implements advanced AP mode and SmartConfig™ technology provisioning with feedback and fallback options to ensure successful process has been accomplished. Customers can use both embedded library and the mobile library for integration to their end products.
SimpleLink™ Wi-Fi® CC3120 SDK plugin	The CC3120R device is supported. The CC3120 SDK contains drivers, many sample applications for Wi-Fi features and internet, and documentation needed to use the CC3120 Internet-on-a chip™ solution. This SDK can be used with TI's MSP432P401R LaunchPad, or SimpleLink Studio, a PC tool that allows MCU development with CC3120. You can also use the SDK as example code for any platform. All sample applications in the SDK are supported on TI's MSP432P401R ultra-low power MCUs with Code Composer Studio IDE and TI RTOS. In addition, many of the applications support IAR.
SimpleLink™ Studio for CC31xx	The CC3120R device is supported. SimpleLink Studio for CC31xx is a Windows®-based software tool used to aid in the development of embedded networking applications and software for microcontrollers. Using SimpleLink Studio for CC31xx, embedded software developers can develop and test applications using any desktop IDE, such as Visual Studio or Eclipse, and connect their applications to the cloud using the CC31xx BoosterPack™ Plug-in Module. The application can then be easily ported to any microcontroller. With the SimpleLink Wi-Fi CC31xx solution, customers now have the flexibility to add Wi-Fi to any microcontroller (MCU). This Internet-on-a-chip solution contains all you need to easily create IoT solutions: security, quick connection, cloud support, and more. For more information on CC31xx, visit SimpleLink™ Wi-Fi® Solutions.
SimpleLink™ Wi-Fi® Radio Testing Tool	The supported devices are: CC3100, CC3200, and CC3220x. The SimpleLink™ Wi-Fi® Radio Testing Tool is a Windows-based software tool for RF evaluation and testing of SimpleLink Wi-Fi CC3120 and CC3220 designs during development and certification. The tool enables low-level radio testing capabilities by manually setting the radio into transmit or receive modes. Using the tool requires familiarity and knowledge of radio circuit theory and radio test methods. Created for the Internet of Things (IoT), the SimpleLink Wi-Fi CC31xx and CC32xx family of devices include on-chip Wi-Fi, Internet, and robust security protocols with no

prior Wi-Fi experience needed for faster development. For more information on these devices, visit SimpleLink™ Wi-Fi® family, Internet-on-a chip™ solutions.

CC3220 Software Development Kit (SDK)	The CC3120R device is supported. The SimpleLink Wi-Fi CC3220 SDK contains drivers for the CC3220 programmable MCU, 30+ sample applications, and documentation needed to use the solution. The SDK also contains the Flash programmer, a command line tool for flashing software, configuring network and software parameters (SSID, access point channel, network profile, and so on), system files, and user files (certificates, web pages, and so on). This SDK can be used with TI's SimpleLInk Wi-Fi CC3220 LaunchPad™ development kit. The SDK has a variety of support offerings. All sample applications in the SDK are supported on the integrated Cortex-M4 processor with CCS IDE and no RTOS. In addition, a few of the applications support IAR, Free RTOS, and TI-RTOS.
Uniflash Standalone Flash Tool for TI Microcontrollers (MCU), Sitara Processors & SimpleLink Devices	CCS Uniflash is a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara processors. Uniflash has a GUI, command line, and scripting interface. CCS Uniflash is available free of charge.

TI Designs and Reference Designs

The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jumpstart your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

10.2 Firmware Updates

TI updates features in the service pack for this module with no published schedule. Due to the ongoing changes, TI recommends that the user has the latest service pack in their module for production.

To stay informed, click the SDK "Alert me" button the top right corner of the product page, or visit *SimpleLink™ Wi-Fi® CC3120 SDK plugin*.

10.3 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3120R device and support tools (see Figure 10-1).

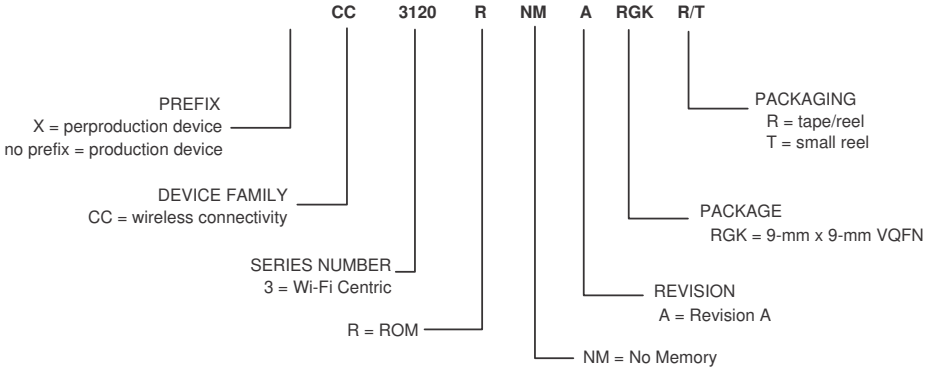


Figure 10-1. CC3120R Device Nomenclature

10.4 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (CC3120). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document. The current documentation that describes the processor, related peripherals, and other technical collateral follows.

The following documents provide support for the CC3120 device.

Application Reports

CC3120 and CC3220 SimpleLink™ Wi-Fi® Embedded Programming	CC3120 and CC3220 SimpleLink™ Wi-Fi® Embedded Programming
SimpleLink™ CC3120, CC3220 Wi-Fi® Internet-on-a chip™ Networking Sub-System Power Management	This application report describes the best practices for power management and extended battery life for embedded low-power Wi-Fi devices such as the SimpleLink™ Wi-Fi® Internet-on-a chip™ solution from Texas Instruments™.
SimpleLink™ CC3120, CC3220 Wi-Fi® Internet-on-a chip™ Solution Built-In Security Features	The SimpleLink™ Wi-Fi® CC3120 and CC3220 Internet-on-a chip™ family of devices from Texas Instruments™ offer a wide range of built-in security features to help developers address a variety of security needs, which is achieved without any processing burden on the main microcontroller (MCU). This document describes these security-related features and provides recommendations for leveraging each in the context of practical system implementation.
SimpleLink™ CC3120, CC3220 Wi-Fi® and Internet of Things Over-the-Air Update	This document describes the OTA library for the SimpleLink™ Wi-Fi® CC3x20 family of devices from Texas Instruments™ and explains how to prepare a new cloud-ready update to be downloaded by the OTA library.
SimpleLink™ CC3120, CC3220 Wi-Fi® Internet-on-a chip™ Solution Device Provisioning	This guide describes the provisioning process, which provides the SimpleLink™ Wi-Fi® device with the information (network name, password, and so forth) needed to connect to a wireless network.
Transfer of TI's Wi-Fi® Alliance Certifications to Products Based on SimpleLink™	This document explains how to employ the Wi-Fi® Alliance (WFA) derivative certification transfer policy to transfer a WFA certification, already obtained by Texas Instruments, to a system you have developed.
Using Serial Flash on SimpleLink™ CC3120 and CC3220 Wi-Fi® and Internet-of-Things Devices	This application note is divided into two parts. The first part provides important guidelines and best- practice design techniques to consider when choosing and embedding a serial Flash paired with the CC3120 and CC3220 (CC3x20) devices. The second part describes the file system, along with guidelines and considerations for system designers working with the CC3x20 devices.

User's Guides

SimpleLink™ Wi-Fi® and Internet of Things CC3120 and CC3220 Network Processor	This document provides software (SW) programmers with all of the required knowledge for working with the networking subsystem of the SimpleLink™ Wi-Fi® devices. This guide provides basic guidelines for writing robust, optimized networking host applications, and describes the capabilities of the networking subsystem. The guide contains some example code snapshots, to give users an idea of how to work with the host driver. More comprehensive code examples can be found in the formal software development kit (SDK). This guide does not provide a detailed description of the host driver APIs.
SimpleLink™ Wi-Fi® CC3120 BoosterPack™ Plug-In Module and IoT Solution	The SimpleLink™ Wi-Fi® CC3120 wireless network processor from Texas Instruments™ provides users the flexibility to add Wi-Fi to any MCU. This user's guide explains the various configurations of the CC3120 BoosterPack™ Plug-In Module.
SimpleLink™ Wi-Fi® CC3120 and CC3220 and IoT Solution Layout Guidelines	This document provides the design guidelines of the 4-layer PCB used for the CC3120 and CC3220 SimpleLink™ Wi-Fi® family of devices from Texas Instruments™. The CC3120 and CC3220 devices are easy to lay out and are available in quad flat no-leads (QFNS) packages. When designing the board, follow the suggestions in this document to optimize performance of the board.
SimpleLink™ Wi-Fi® CC3120 Internet-on-a-chip™ Solution SDK	This guide is intended to help users in the initial setup and demonstration of the different demos in the CC3120 SDK. The guide lists the software and hardware components required to get started, and explains how to install the supported integrated development environment (IDE), SimpleLink CC3120 SDK, and the various other tools required.
SimpleLink™ Wi-Fi® and Internet-on-a-chip™ CC3120 and CC3220 Solution Radio Tool	The Radio Tool serves as a control panel for direct access to the radio, and can be used for both the radio frequency (RF) evaluation and for certification purposes. This guide describes how to have the tool work seamlessly on Texas Instruments™ evaluation platforms such as the BoosterPack™ plus FTDI emulation board for CC3120 devices, and the LaunchPad™ for CC3220 devices.
SimpleLink™ Wi-Fi® CC3120 and CC3220 Provisioning for Mobile Applications	This guide describes TI's SimpleLink™ Wi-Fi® provisioning solution for mobile applications, specifically on the usage of the Android™ and iOS® building blocks for UI requirements, networking, and provisioning APIs required for building the mobile application.

UniFlash CC3120 and CC3220 SimpleLink™ Wi-Fi® and Internet-on-a chip™ Solution ImageCreator and Programming Tool	This document describes the installation, operation, and usage of the SimpleLink ImageCreator tool as part of the UniFlash.

More Literature

RemoTI Manifest	
CC3120 SimpleLink™ WI-Fi® and Internet of Things	CC3120 hardware design files.
CC3120, CC3220 SimpleLink™ Wi-Fi® and Internet of Things Design Checklist	

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

SimpleLink™, Internet-on-a chip™, SmartConfig™, Texas Instruments™, BoosterPack™, LaunchPad™, and TI E2E™ are trademarks of Texas Instruments.
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Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
Zigbee® is a registered trademark of Zigbee Alliance.
Windows® is a registered trademark of Microsoft Inc.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

10.9 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2021) to Revision B (July 2024)	Page
• Updated WLAN	33

Changes from February 7, 2018 to May 13, 2021 (from Revision * (Feb 2017) to Revision A (May 2021))	Page
• Updated formatting and organization to reflect current TI standards	0
• Added WPA3 Personal and WPA3 Enterprise to Section 1	1
• Changed *Features* section	1
• Added WPA3 Personal and WPA3 Enterprise to *Description*	2
• Changed *Description* section	2
• Added *Functional Block Diagram* to the *Functional Block Diagrams* section	3
• Added *CC3120R Hardware Overview* block diagram	3
• Added *Device Comparison* section	7
• Changed *Device Features Comparison* table	7
• Changed *CC3120 SDK Plug-In* link	8
• Added *NC = No internal connection* note to the pinout diagram	9
• Changed *Pin Attributes* table	10
• Deleted the pin number for GND_TAB	10
• Changed *Connections for Unused Pins* table	12
• Changed the typical value for Hibernate from "4 µA" to "4.5 µA"	14
• Deleted the + sign from the typical values in the *WLAN Transmitter Characteristics* table	19
• Added the table note "Power of 802.11b rates are reduced to meet ETSI requirements" to the *WLAN Transmitter Characteristics* table	19
• Added *Reset Requirement* table	20
• Changed from "200-mS" to 200-ms" in the *Device Reset* section	21
• Changed from "pin 32" to "pin 52" in the second list item of the *Device Reset* section	21
• Changed the *Host SPI Interface Timing* diagram	27
• Changed the parameter numbers in the *Host SPI Interface Timing Parameters* table	27
• Changed *Flash SPI Interface Timing* diagram	28
• Changed the parameter numbers in the *Flash SPI Interface Timing Parameters* table	28
• Added WPA3 Personal and WPA3 Enterprise to Section 8	33
• Added WPA3 Personal and WPA3 Enterprise to WLAN	33
• Added WPA3 personal and enterprise to Table 8-1	33
• Added "The typical battery drain in this mode is 4.5 µA" to the *Hibernate* section	37
• Added "The typical battery drain in this mode is 1 µA" to the *Shutdown* section	37
• Changed the table title from "Title" to "Recommended Flash Size"	38
• Changed the *CC3120R Wide-Voltage Mode Application Circuit* diagram	40
• Added R14 information to the *Bill of Materials for CC3120R in Wide-Voltage Mode* table	40
• Changed the *CC3120R Preregulated 1.85-V Mode Application Circuit* diagram	42
• Added R13 information to the *Bill of Materials for CC3120R in Preregulated, 1.85-V Mode* table	42
• Changed from "XTALM" to "XTAL_N" in the *Clock Interfaces* section	45
• Changed *Tools and Software* section	47
• Changed *CC3120R Device Nomenclature*figure	49
• Changed *Documentation Support* section	50

12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC3120RNMARGKR	Active	Production	VQFN (RGK) | 64	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3120R NMA
CC3120RNMARGKR.B	Active	Production	VQFN (RGK) | 64	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC3120R NMA
CC3120RNMARGKT	Active	Production	VQFN (RGK) | 64	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3120R NMA
CC3120RNMARGKT.B	Active	Production	VQFN (RGK) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC3120R NMA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OPTION ADDENDUM

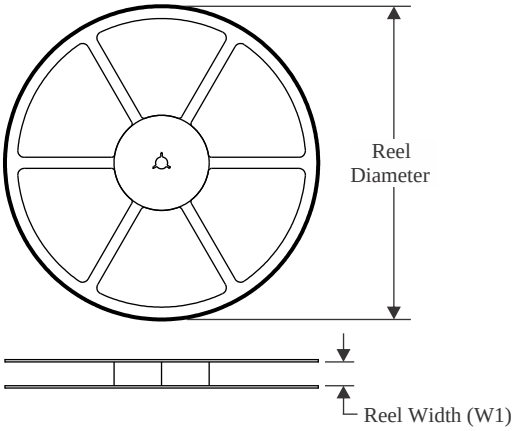
PACKAGE MATERIALS INFORMATION

www.ti.com

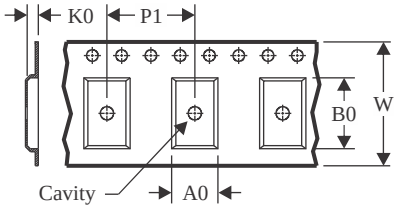
25-Sep-2024

TAPE AND REEL INFORMATION

REEL DIMENSIONS

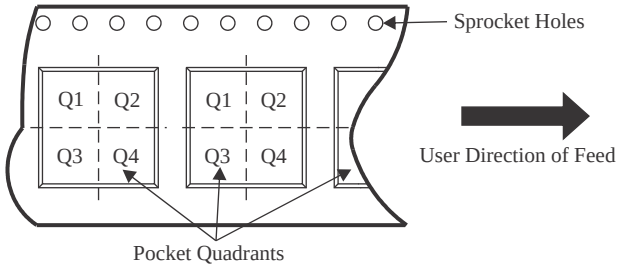


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

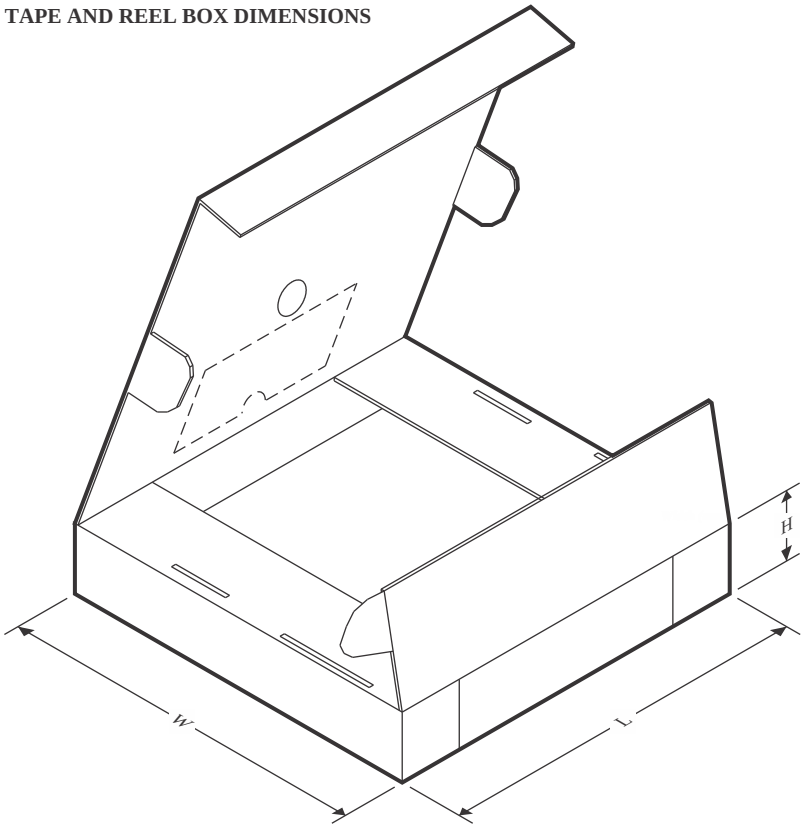


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3120RNMARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3120RNMARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

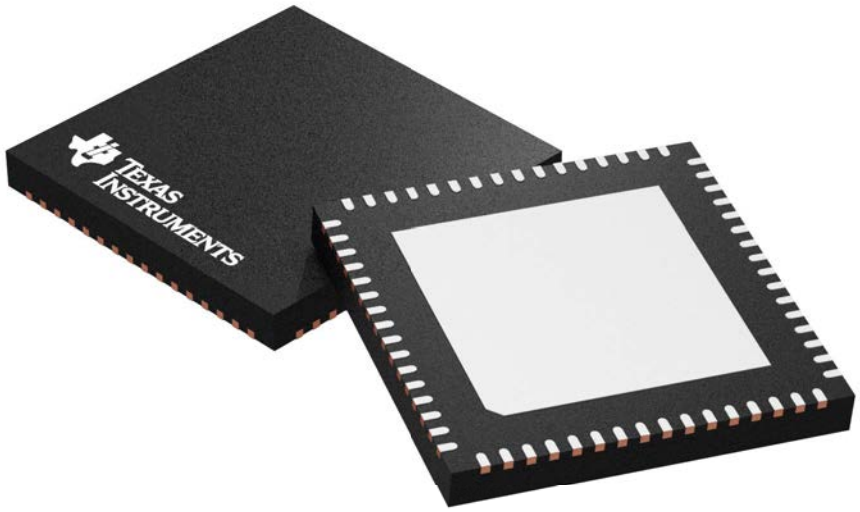
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3120RNMARGKR	VQFN	RGK	64	2500	367.0	367.0	38.0
CC3120RNMARGKT	VQFN	RGK	64	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGK 64

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

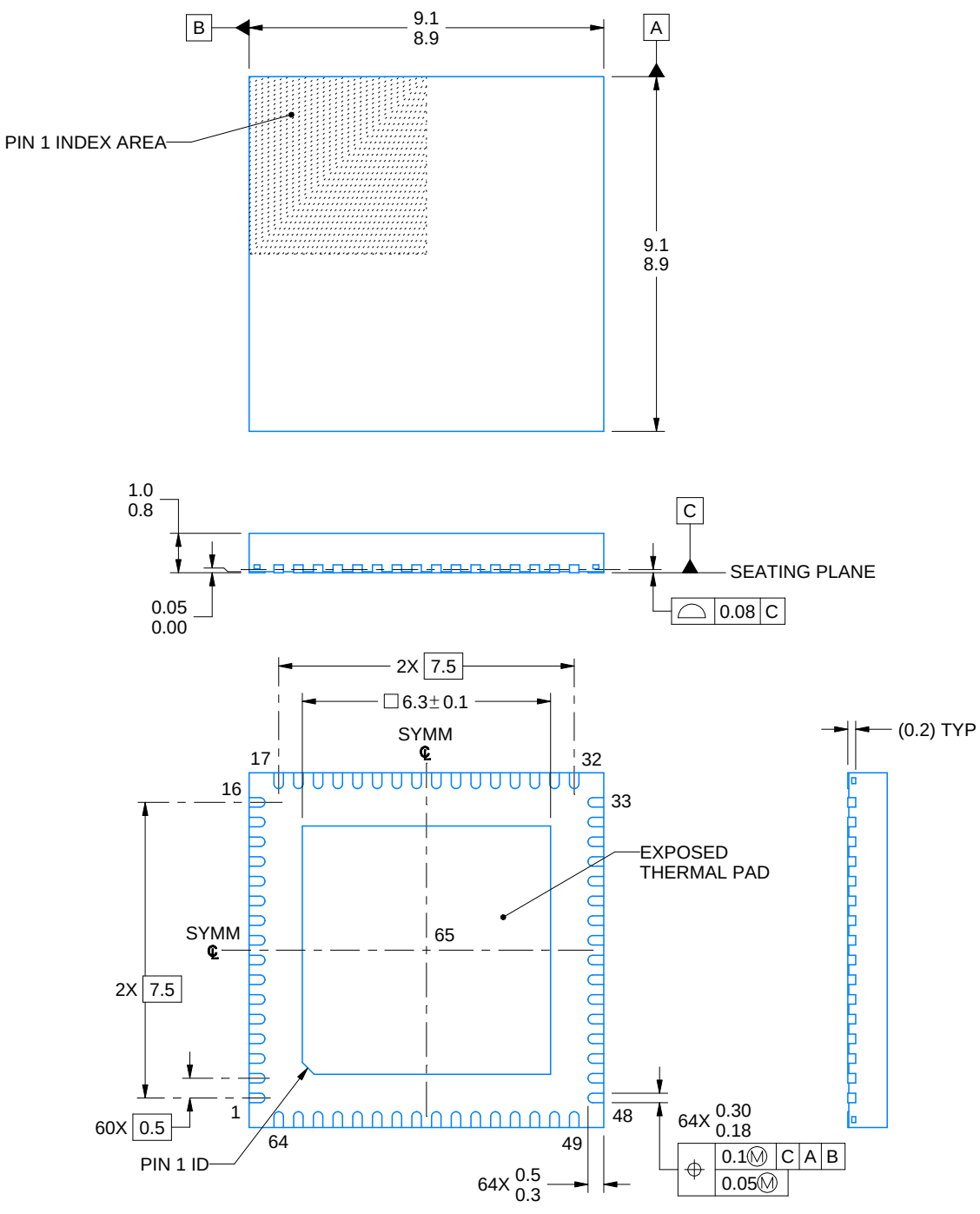
4211520/D

PACKAGE OUTLINE

RGK0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

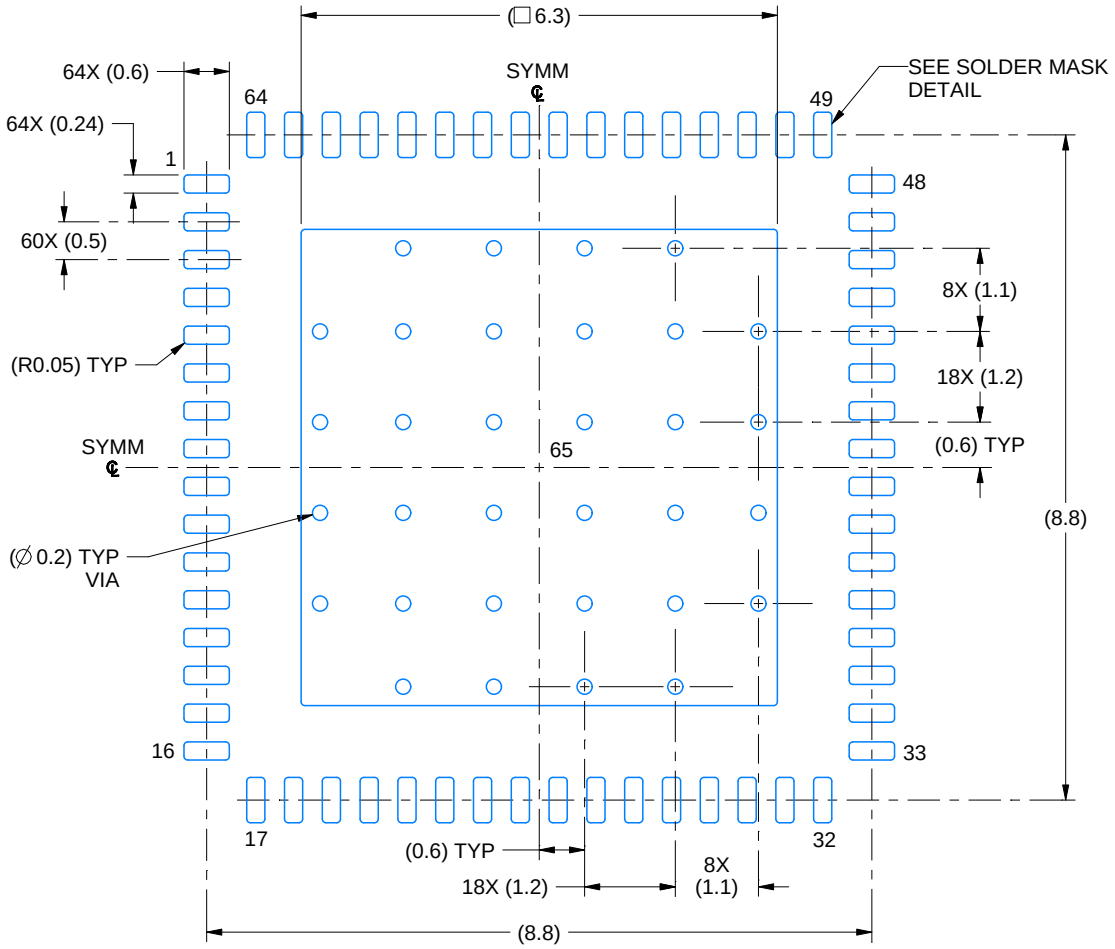
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

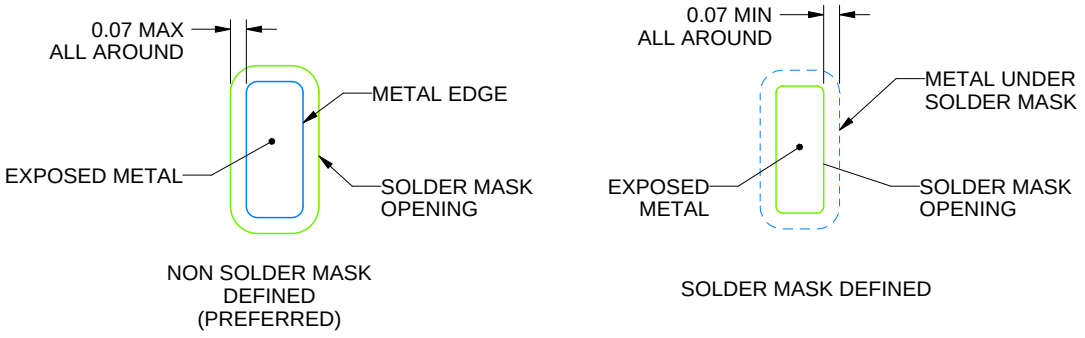
RGK0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4222201/B 03/2018

NOTES: (continued)

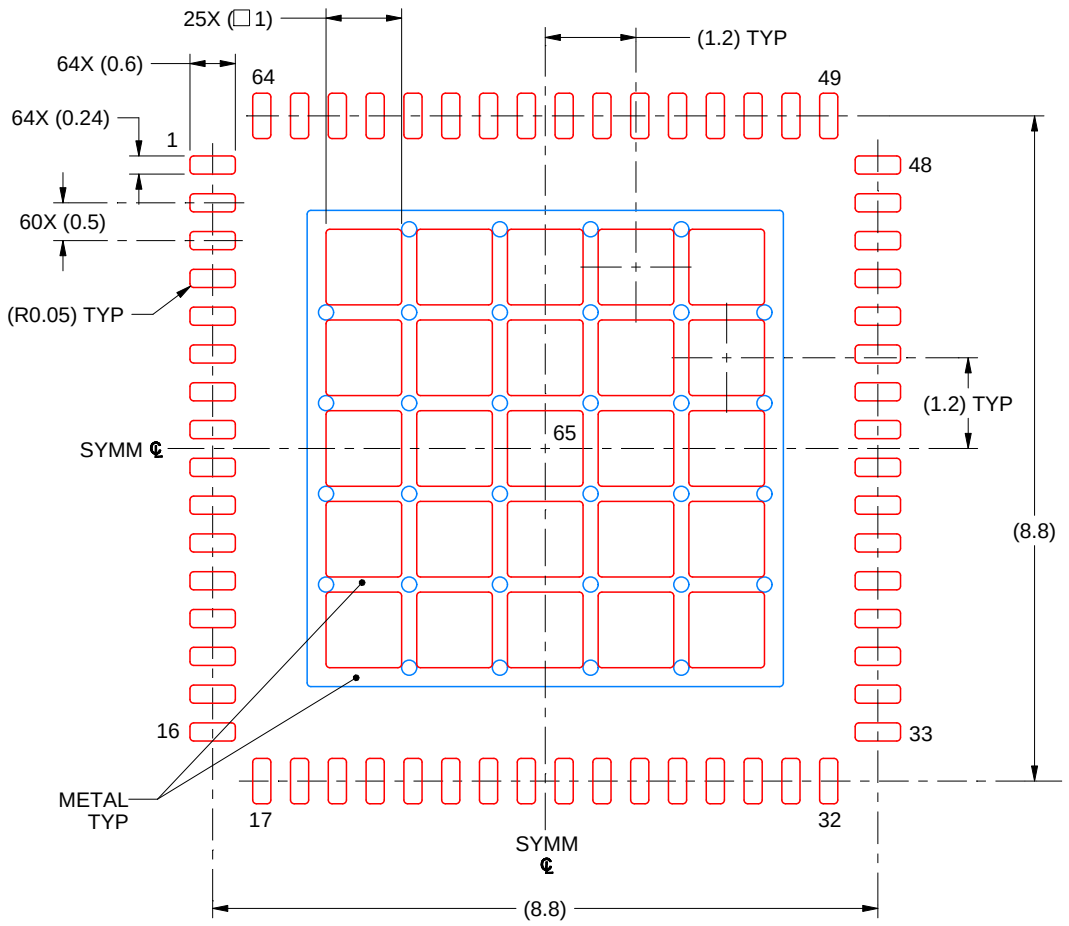
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGK0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4222201/B 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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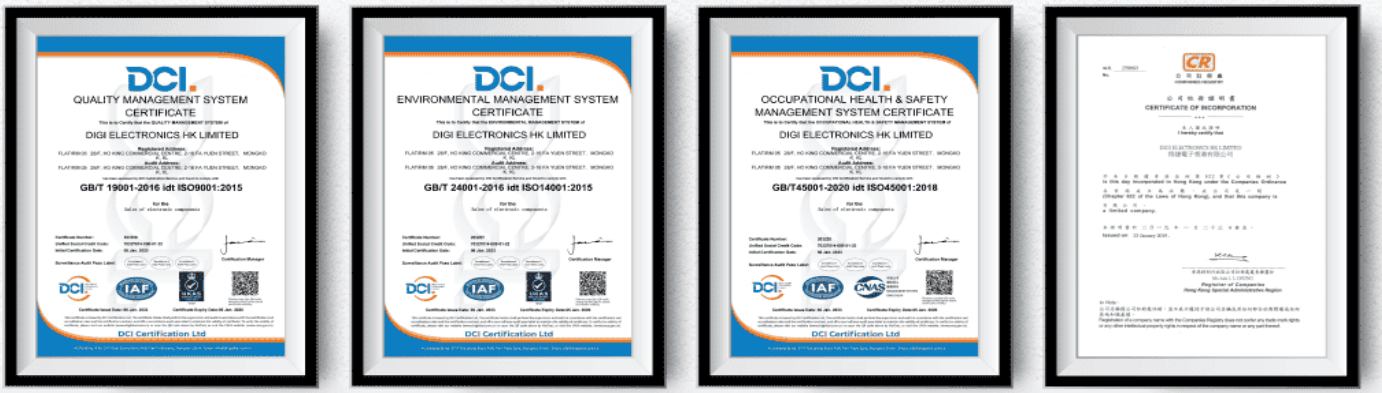

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