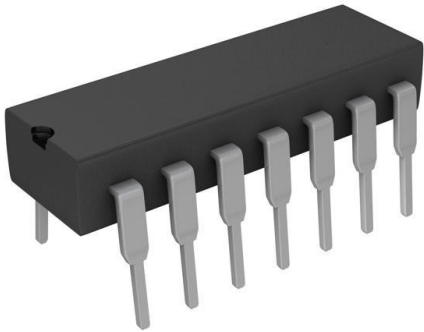


# CD4011BE Datasheet

[www.digi-electronics.com](http://www.digi-electronics.com)



CD4011BE

<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	CD4011BE-DG
Manufacturer	<a href="#">Texas Instruments</a>
Manufacturer Product Number	CD4011BE
Description	IC GATE NAND 4CH 2-INP 14DIP
Detailed Description	NAND Gate IC 4 Channel 14-PDIP



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

CD4011BE

Series:

4000B

Logic Type:

NAND Gate

Number of Inputs:

2

Voltage - Supply:

3V ~ 18V

Current - Output High, Low:

3.4mA, 3.4mA

Input Logic Level - High:

3.5V ~ 11V

Operating Temperature:

-55°C ~ 125°C

Supplier Device Package:

14-PDIP

Base Product Number:

CD4011

Manufacturer:

Texas Instruments

Product Status:

Active

Number of Circuits:

4

Features:

-

Current - Quiescent (Max):

1  $\mu$ A

Input Logic Level - Low:

1.5V ~ 4V

Max Propagation Delay @ V, Max CL:

90ns @ 15V, 50pF

Mounting Type:

Through Hole

Package / Case:

14-DIP (0.300", 7.62mm)

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

Not Applicable

ECCN:

EAR99



Data sheet acquired from Harris Semiconductor  
SCHS021D – Revised September 2003

# CD4011B, CD4012B, CD4023B Types

## CMOS NAND GATES

High-Voltage Types (20-Volt Rating)

- Quad 2 Input – CD4011B
- Dual 4 Input – CD4012B
- Triple 3 Input – CD4023B

■ CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PWR suffix). The CD4011B and CD4023B types also are supplied in 14-lead thin shrink small-outline packages (PW suffix).

**MAXIMUM RATINGS, Absolute-Maximum Values:**

**DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)**

Voltages referenced to V<sub>SS</sub> Terminal ..... -0.5V to +20V

**INPUT VOLTAGE RANGE, ALL INPUTS** ..... -0.5V to V<sub>DD</sub>+0.5V

**DC INPUT CURRENT, ANY ONE INPUT** ..... ±10mA

**POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):**

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW

**DEVICE DISSIPATION PER OUTPUT TRANSISTOR**

FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

**OPERATING-TEMPERATURE RANGE (T<sub>A</sub>)** ..... -55°C to +125°C

**STORAGE TEMPERATURE RANGE (T<sub>stg</sub>)** ..... -65°C to +150°C

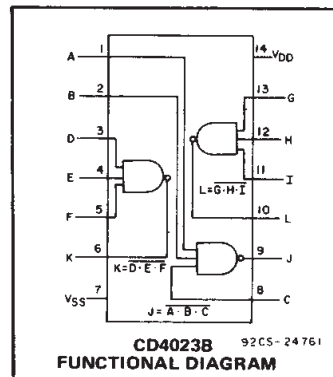
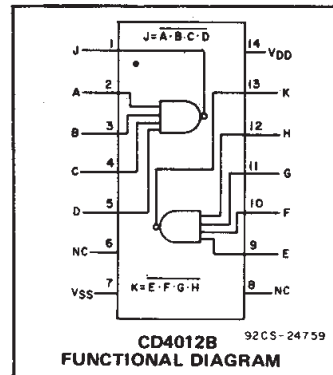
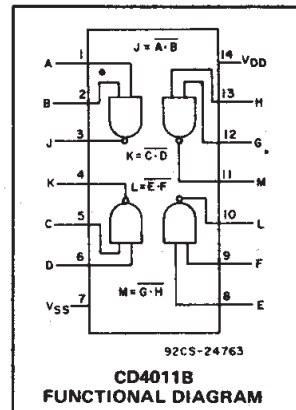
**LEAD TEMPERATURE (DURING SOLDERING):**

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

**Features:**

- Propagation delay time = 60 ns (typ.) at C<sub>L</sub> = 50 pF, V<sub>DD</sub> = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
  - 1 V at V<sub>DD</sub> = 5 V
  - 2 V at V<sub>DD</sub> = 10 V
  - 2.5 V at V<sub>DD</sub> = 15 V

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

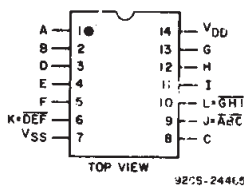
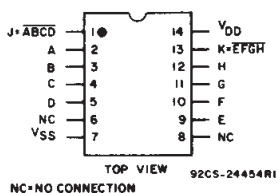
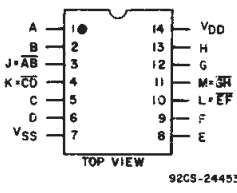


**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package Temperature Range)	3	18	V

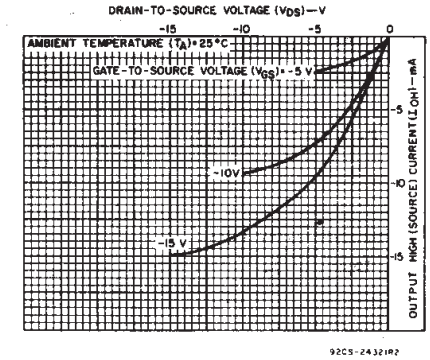
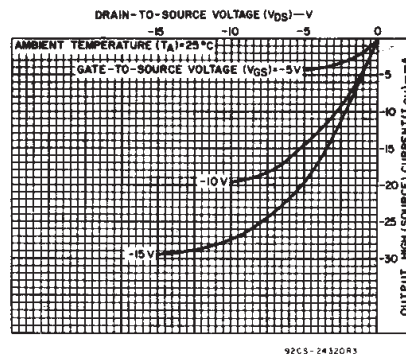
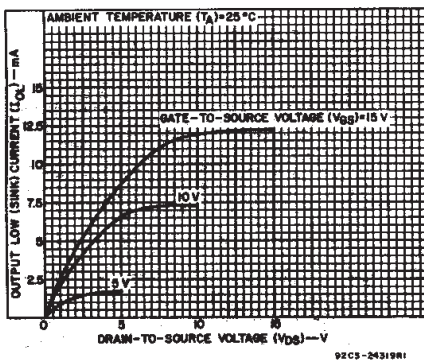
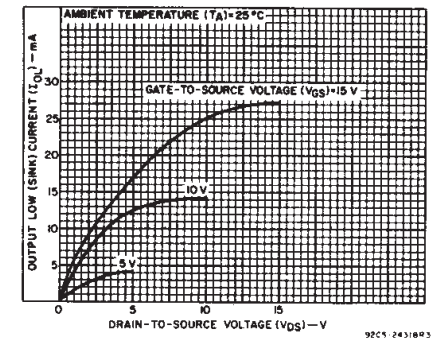
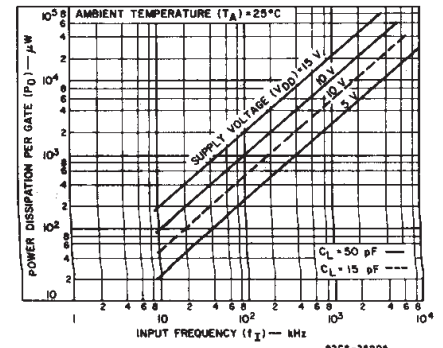
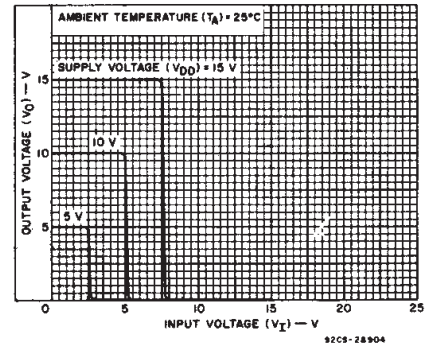
**TERMINAL ASSIGNMENTS**



### CD4011B, CD4012B, CD4023B Types

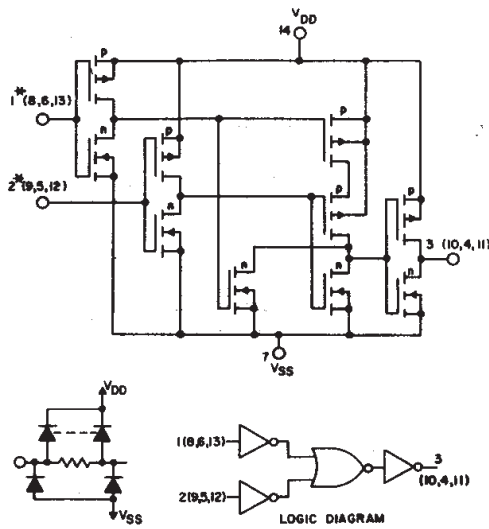
#### STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0,5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0,10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0,15	15	1	1	30	30	-	0.01	1	
	-	0,20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	-	0,5	5	4.95				4.95	5	-	V
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V <sub>IL</sub> Max.	4.5	-	5	1.5				-	-	1.5	V
	9	-	10	3				-	-	3	
	13.5	-	15	4				-	-	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	-	5	3.5				3.5	-	-	V
	1,9	-	10	7				7	-	-	
Input Current I <sub>IN</sub> Max.		0,18	18	±0.1	±0.1	±1	±1	-	±10 <sup>-5</sup>	±0.1	μA



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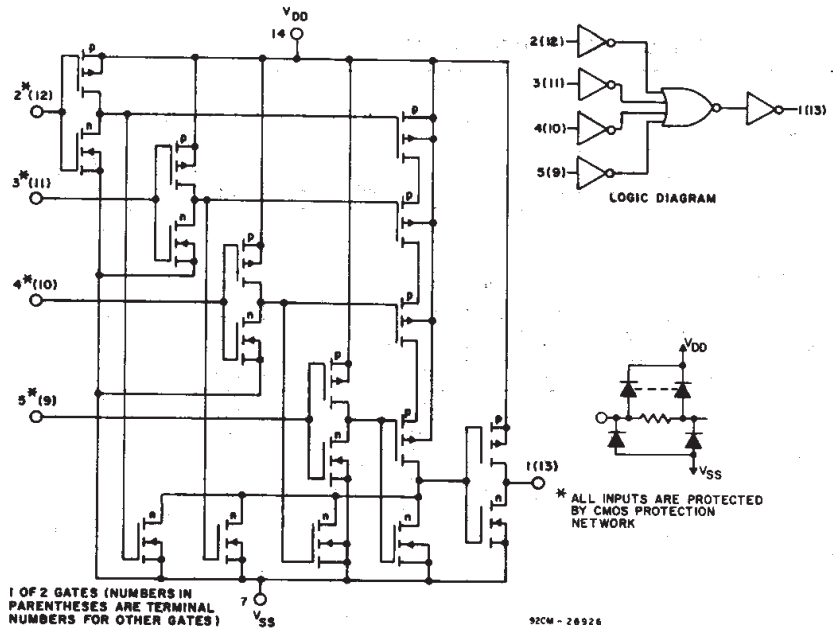
### CD4011B, CD4012B, CD4023B Types



\* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

1 OF 4 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

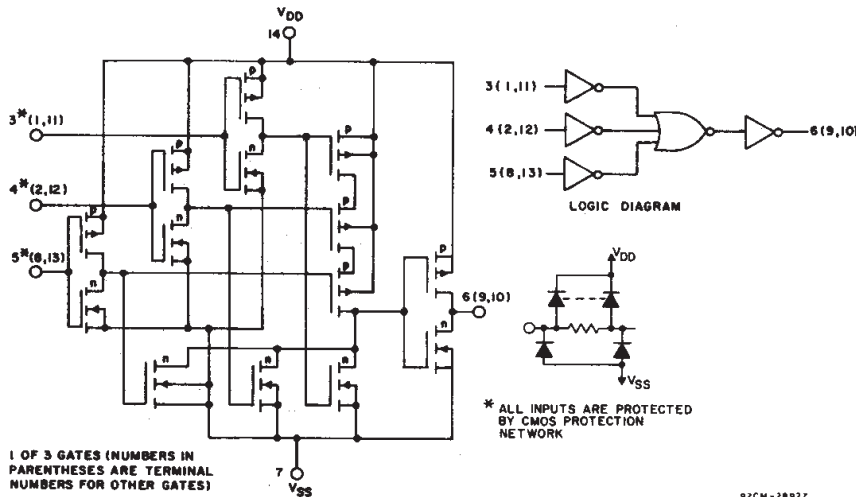
Fig.7 - Schematic and logic diagrams for CD4011B.



1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

92CM - 28926

Fig.8 - Schematic and logic diagrams for CD4012B.



1 OF 3 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

\* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

92CM - 28927

Fig. 9 - Schematic and logic diagrams for CD4023B.

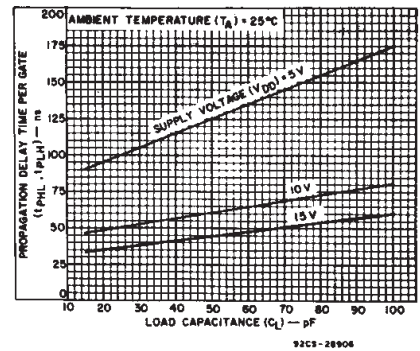


Fig.10 - Typical propagation delay time per gate as a function of load capacitance.

#### DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ C$ ; Input  $t_r, t_f = 20 ns$ ,  $C_L = 50 pF$ ,  $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		VDD VOLTS	TYP.		MAX.
Propagation Delay Time, $t_{PHL}, t_{PLH}$		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, $t_{THL}, t_{TLH}$		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, $C_{IN}$	Any Input		5	7.5	pF

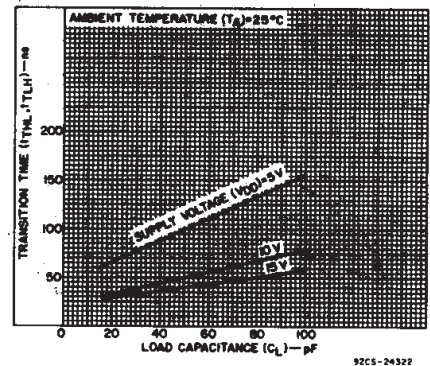


Fig.11 - Typical transition time as a function of load capacitance.

**CD4011B, CD4012B, CD4023B Types**

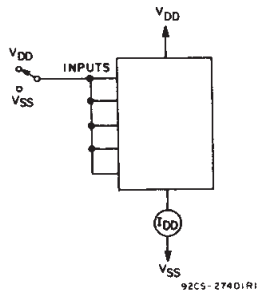


Fig. 12 - Quiescent-device-current test circuit.

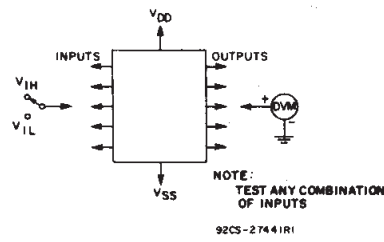


Fig. 13 - Input-voltage test circuit.

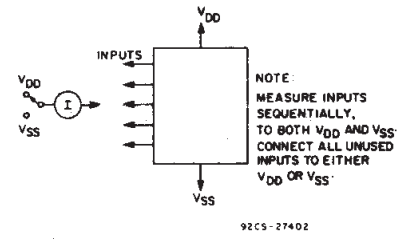
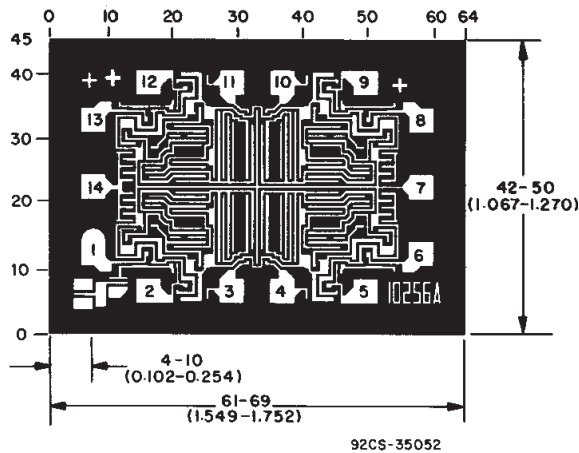
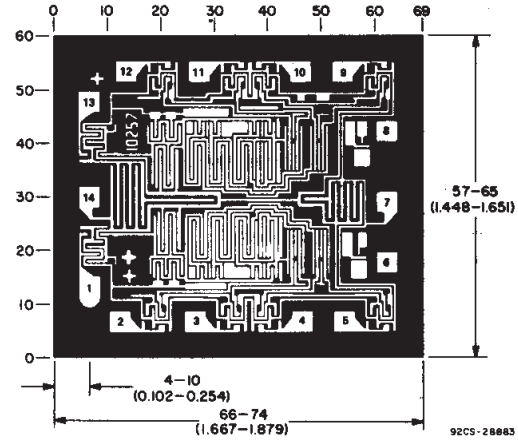


Fig. 14 - Input-current test circuit.

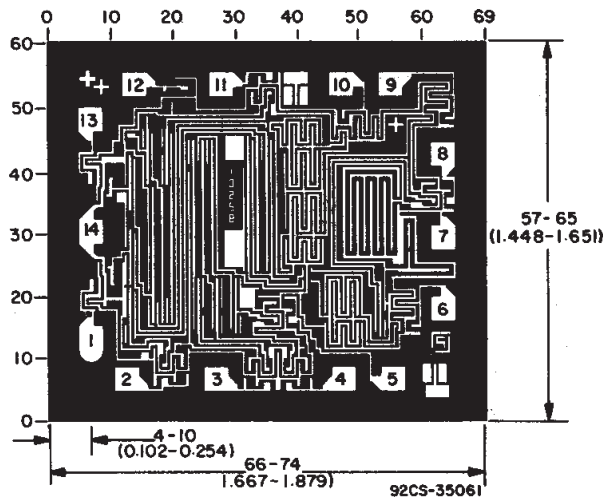
**Chip Dimensions and Pad Layouts**



CD4011BH



CD4012BH



CD4023BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD4011BE</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4011BE
CD4011BE.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4011BE
CD4011BEE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4011BE
<a href="#">CD4011BF</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4011BF
CD4011BF.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4011BF
<a href="#">CD4011BF3A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4011BF3A
CD4011BF3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4011BF3A
<a href="#">CD4011BM</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011BM
CD4011BM.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011BM
<a href="#">CD4011BM96</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011BM
CD4011BM96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011BM
CD4011BM96E4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011BM
CD4011BME4	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011BM
<a href="#">CD4011BMT</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	CD4011BM
<a href="#">CD4011BNSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011B
CD4011BNSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4011B
<a href="#">CD4011BPW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-55 to 125	CM011B
<a href="#">CD4011BPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM011B
CD4011BPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM011B
CD4011BPWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM011B
<a href="#">CD4012BE</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4012BE
CD4012BE.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4012BE
CD4012BEE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4012BE
<a href="#">CD4012BF3A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4012BF3A
CD4012BF3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4012BF3A
<a href="#">CD4012BM</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	CD4012BM
<a href="#">CD4012BM96</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4012BM
CD4012BM96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4012BM
CD4012BM96E4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4012BM

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4012BM96G4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4012BM
<a href="#">CD4012BNSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4012B
CD4012BNSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4012B
<a href="#">CD4012BPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM012B
CD4012BPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM012B
<a href="#">CD4023BE</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4023BE
CD4023BE.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4023BE
CD4023BEE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4023BE
<a href="#">CD4023BF</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4023BF
CD4023BF.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4023BF
<a href="#">CD4023BF3A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4023BF3A
CD4023BF3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4023BF3A
<a href="#">CD4023BM</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	CD4023BM
<a href="#">CD4023BM96</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4023BM
CD4023BM96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4023BM
<a href="#">CD4023BMT</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	CD4023BM
<a href="#">CD4023BNSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4023B
CD4023BNSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4023B
<a href="#">CD4023BPW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-55 to 125	CM023B
<a href="#">CD4023BPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	CM023B
CD4023BPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM023B
<a href="#">JM38510/05051BCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05051BCA
JM38510/05051BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05051BCA
<a href="#">JM38510/05052BCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05052BCA
JM38510/05052BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05052BCA
<a href="#">JM38510/05053BCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05053BCA

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/05053BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05053BCA
<a href="#">M38510/05051BCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05051BCA
<a href="#">M38510/05052BCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05052BCA
<a href="#">M38510/05053BCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05053BCA

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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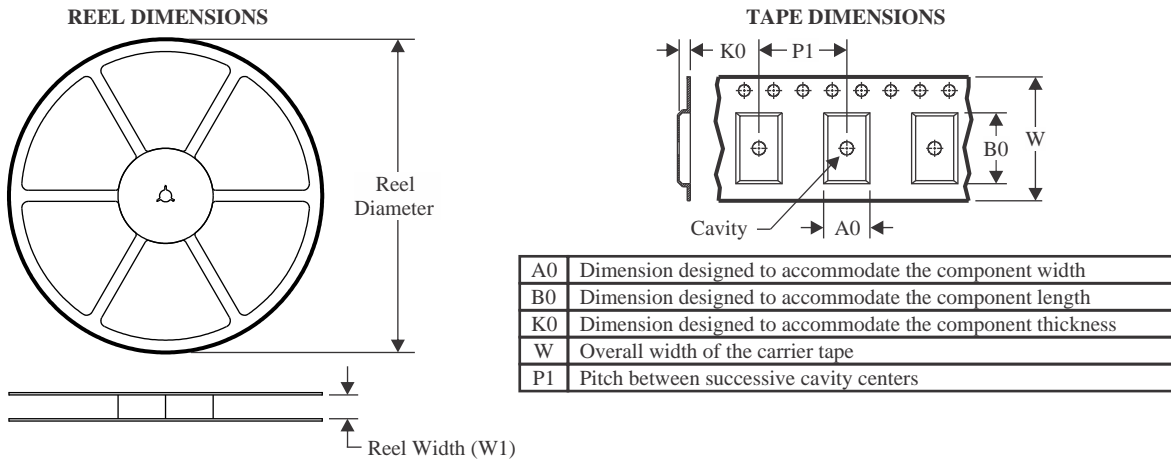
**OTHER QUALIFIED VERSIONS OF CD4011B, CD4011B-MIL, CD4012B, CD4012B-MIL, CD4023B, CD4023B-MIL :**

- Catalog : [CD4011B](#), [CD4012B](#), [CD4023B](#)
- Military : [CD4011B-MIL](#), [CD4012B-MIL](#), [CD4023B-MIL](#)

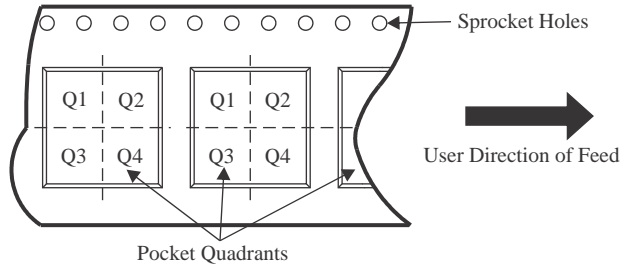
## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



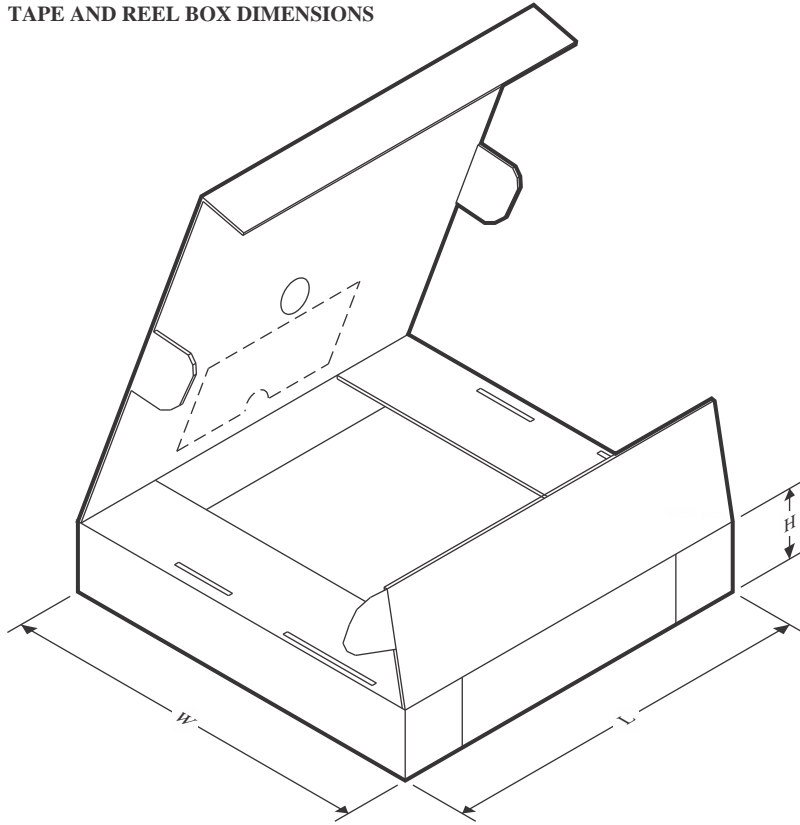
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

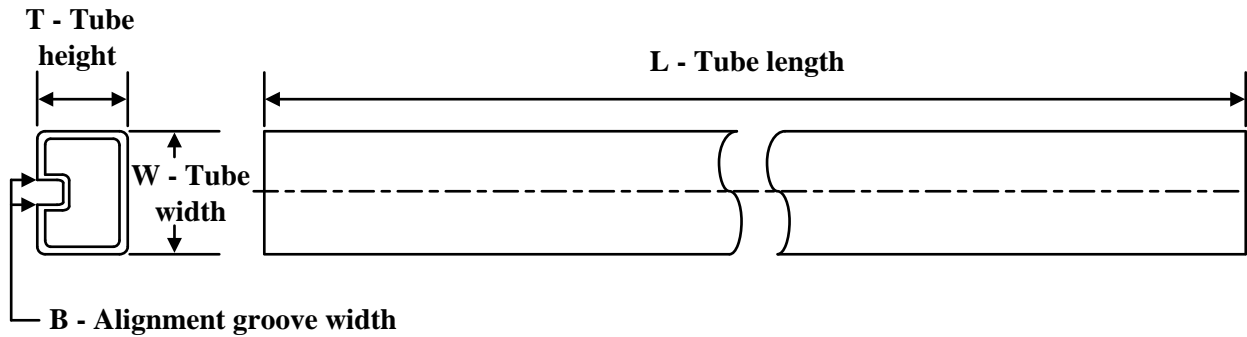
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4011BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4011BNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD4011BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4012BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4012BNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4012BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4023BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4023BNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD4023BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



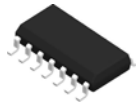
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4011BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4011BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4011BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
CD4012BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4012BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4012BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
CD4023BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4023BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4023BPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4011BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4011BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4011BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4011BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4011BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4011BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4011BM	D	SOIC	14	50	506.6	8	3940	4.32
CD4011BM.A	D	SOIC	14	50	506.6	8	3940	4.32
CD4011BME4	D	SOIC	14	50	506.6	8	3940	4.32
CD4012BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4012BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4012BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4012BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4012BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4012BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4023BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4023BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4023BEE4	N	PDIP	14	25	506	13.97	11230	4.32

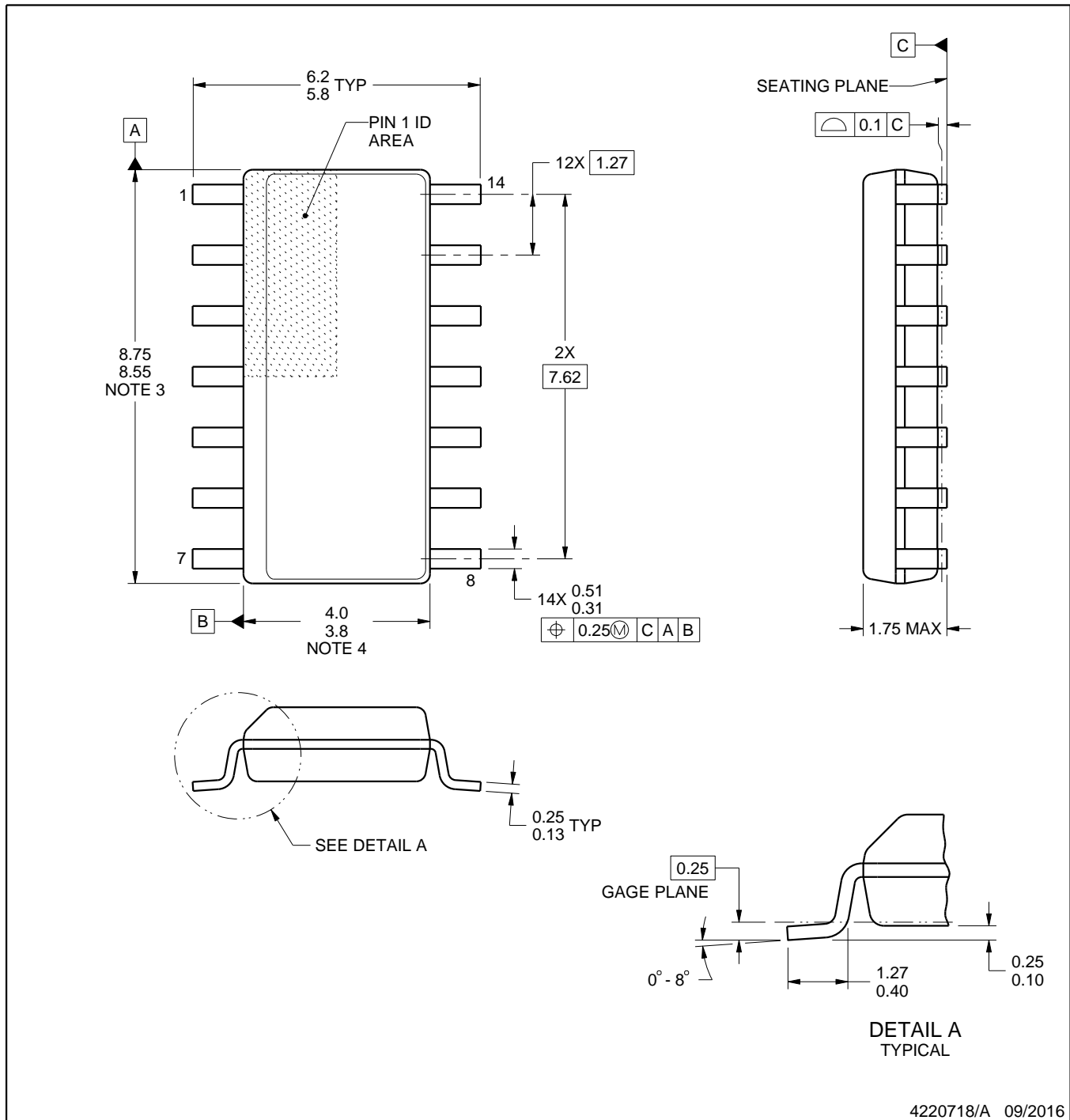


D0014A

## PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

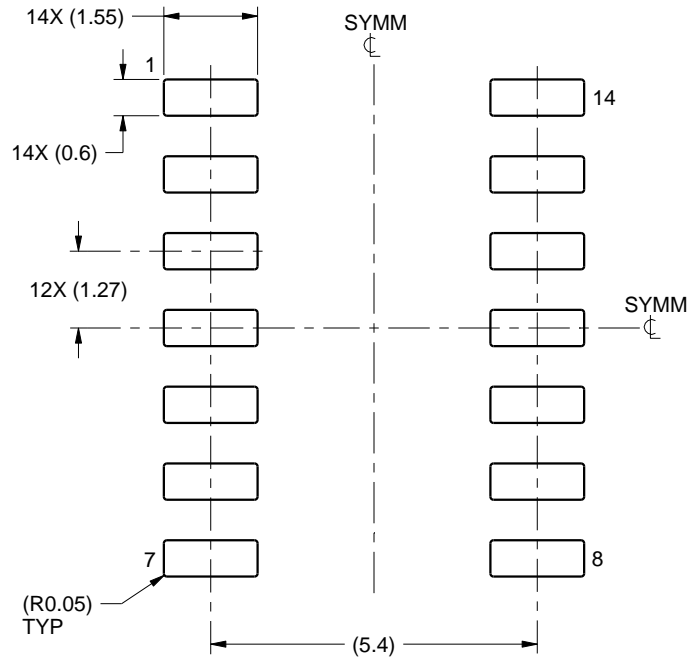
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

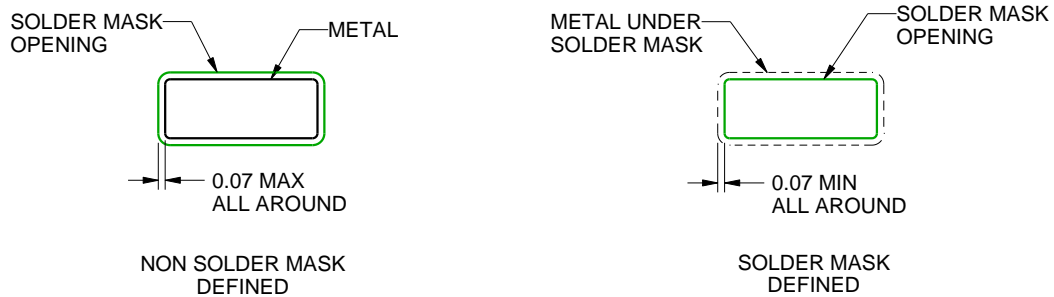
**D0014A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

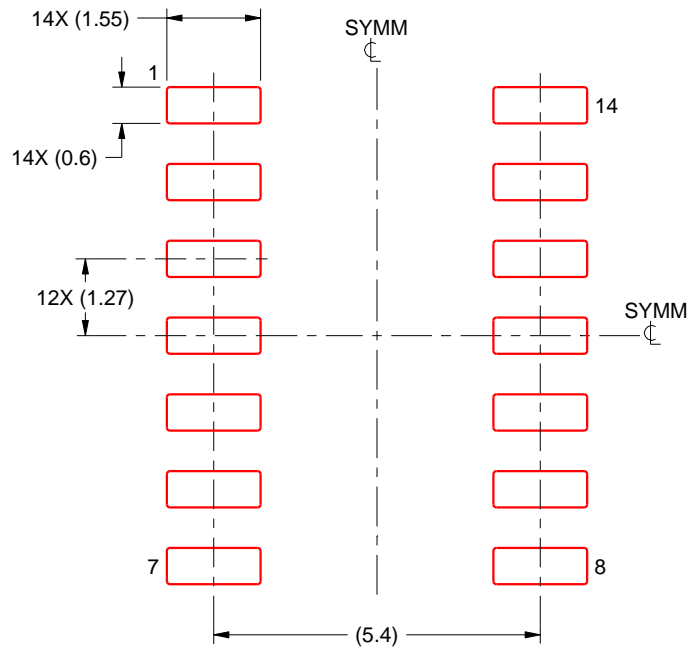
4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****D0014A****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:8X

4220718/A 09/2016

NOTES: (continued)

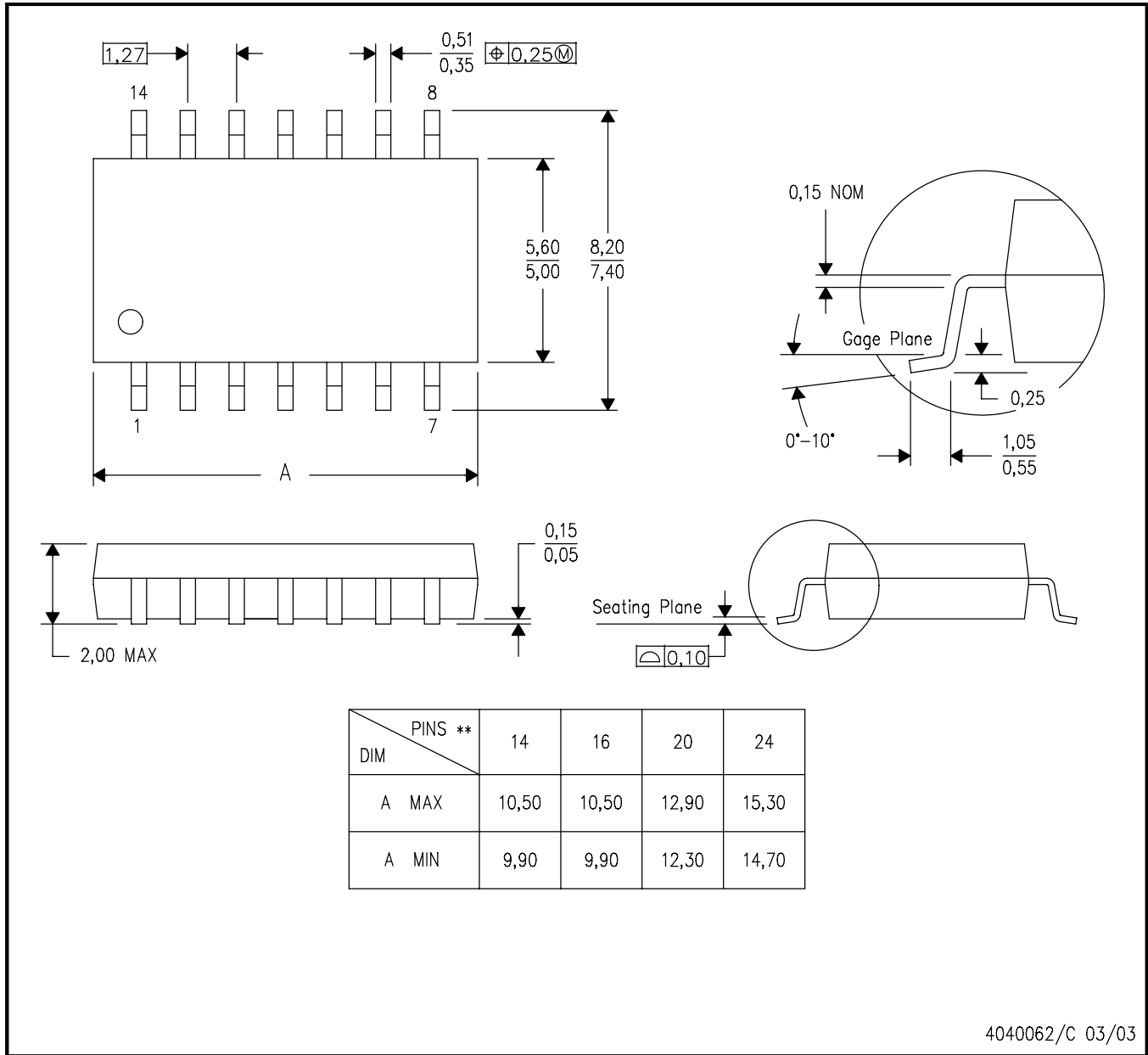
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**MECHANICAL DATA**

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



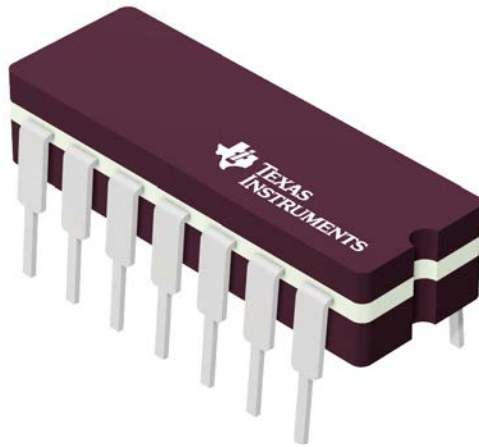
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

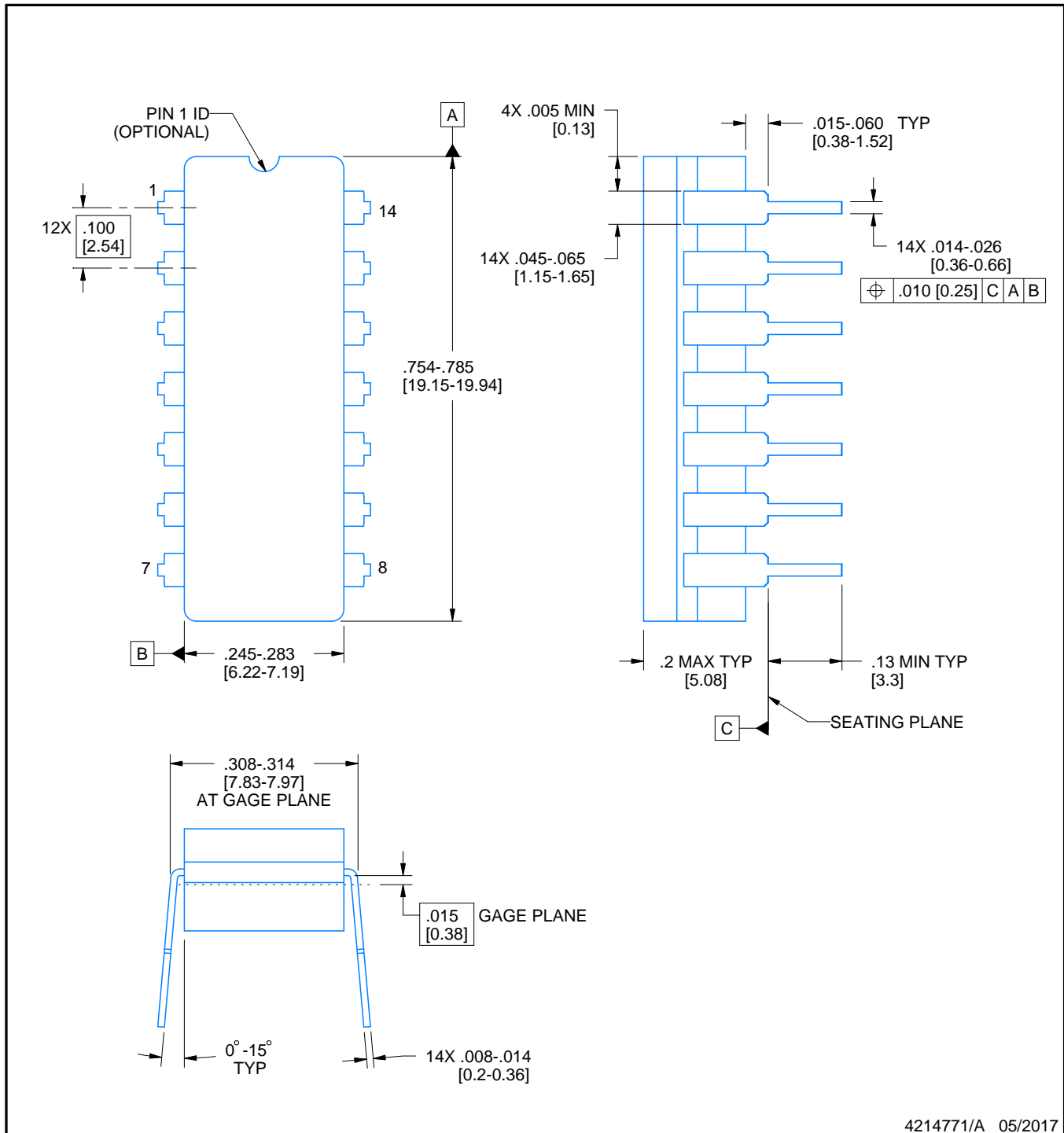


J0014A

## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



## NOTES:

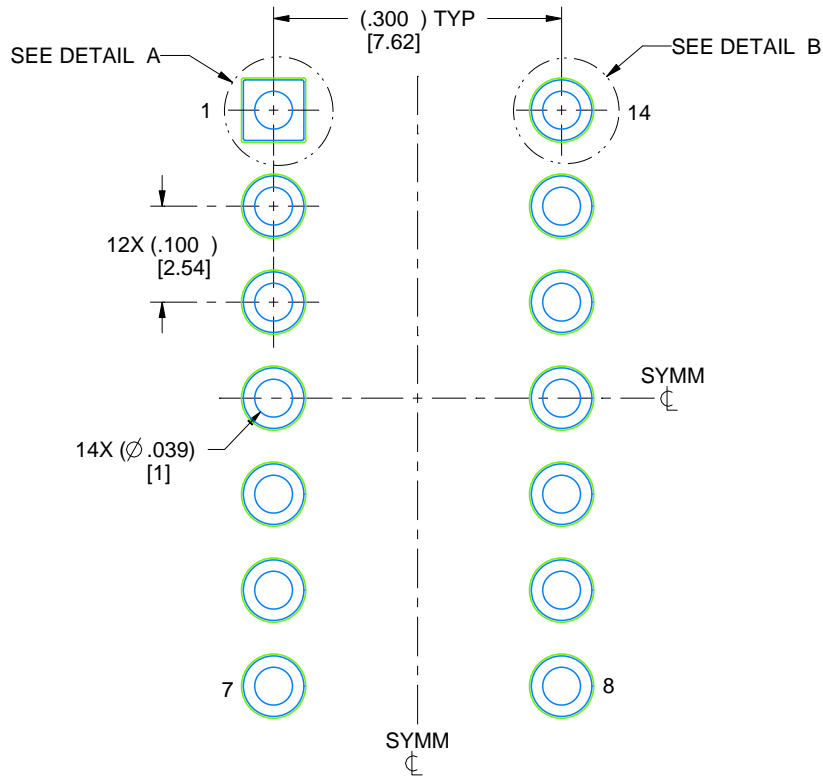
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

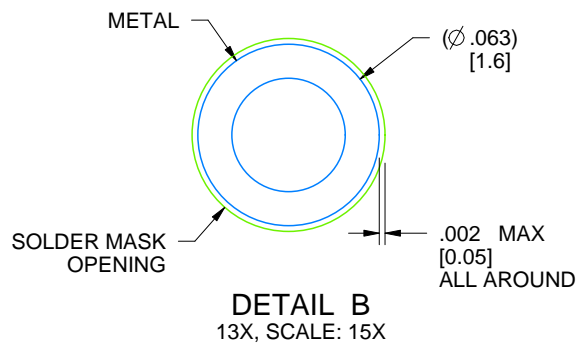
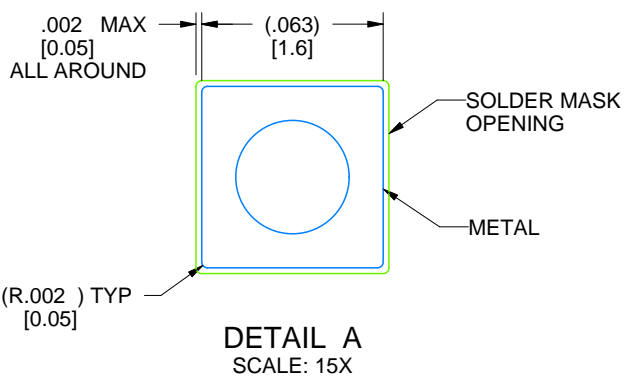
**J0014A**

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



**LAND PATTERN EXAMPLE**  
NON-SOLDER MASK DEFINED  
SCALE: 5X



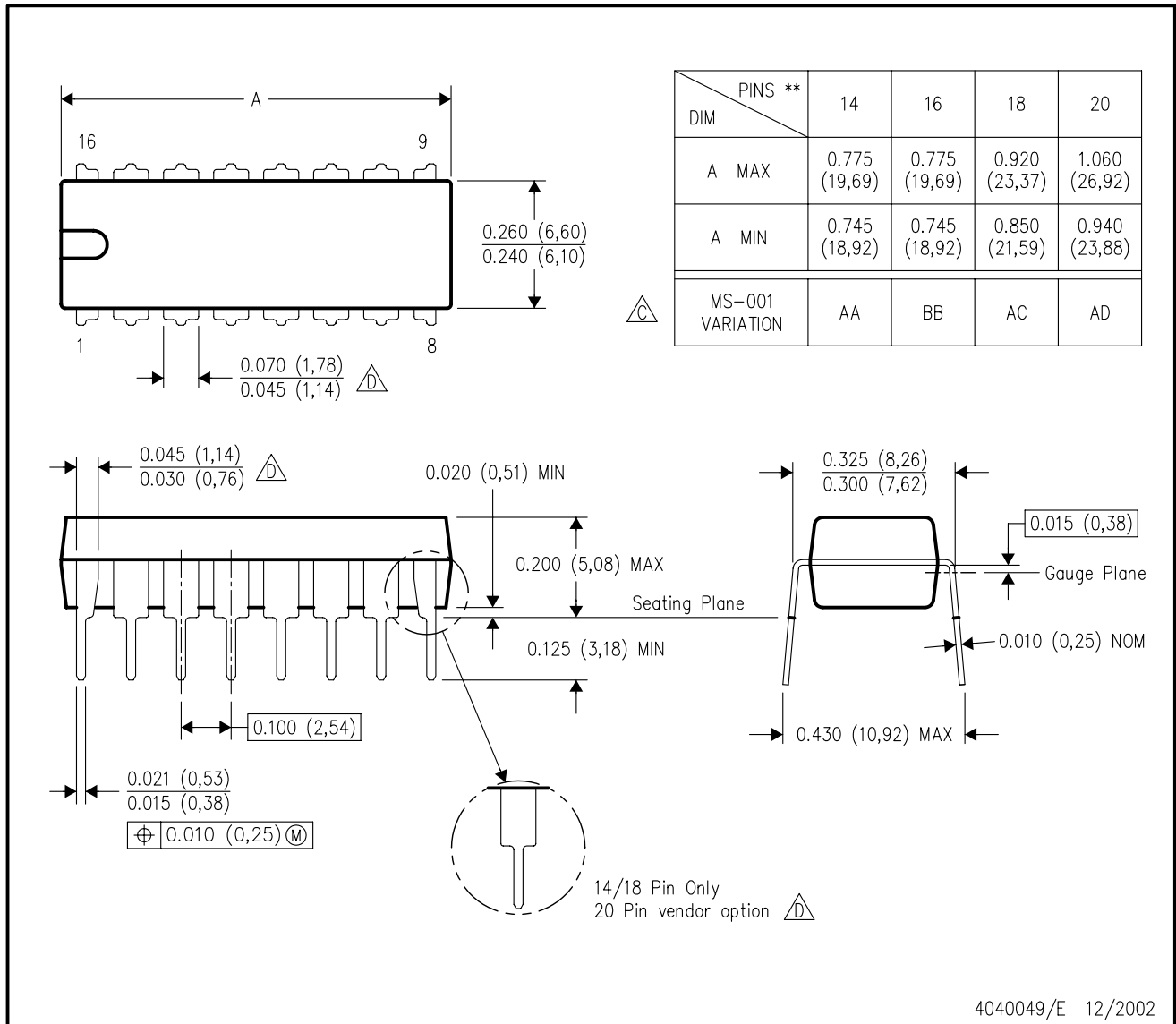
4214771/A 05/2017

**MECHANICAL DATA**

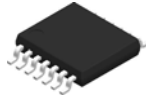
**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

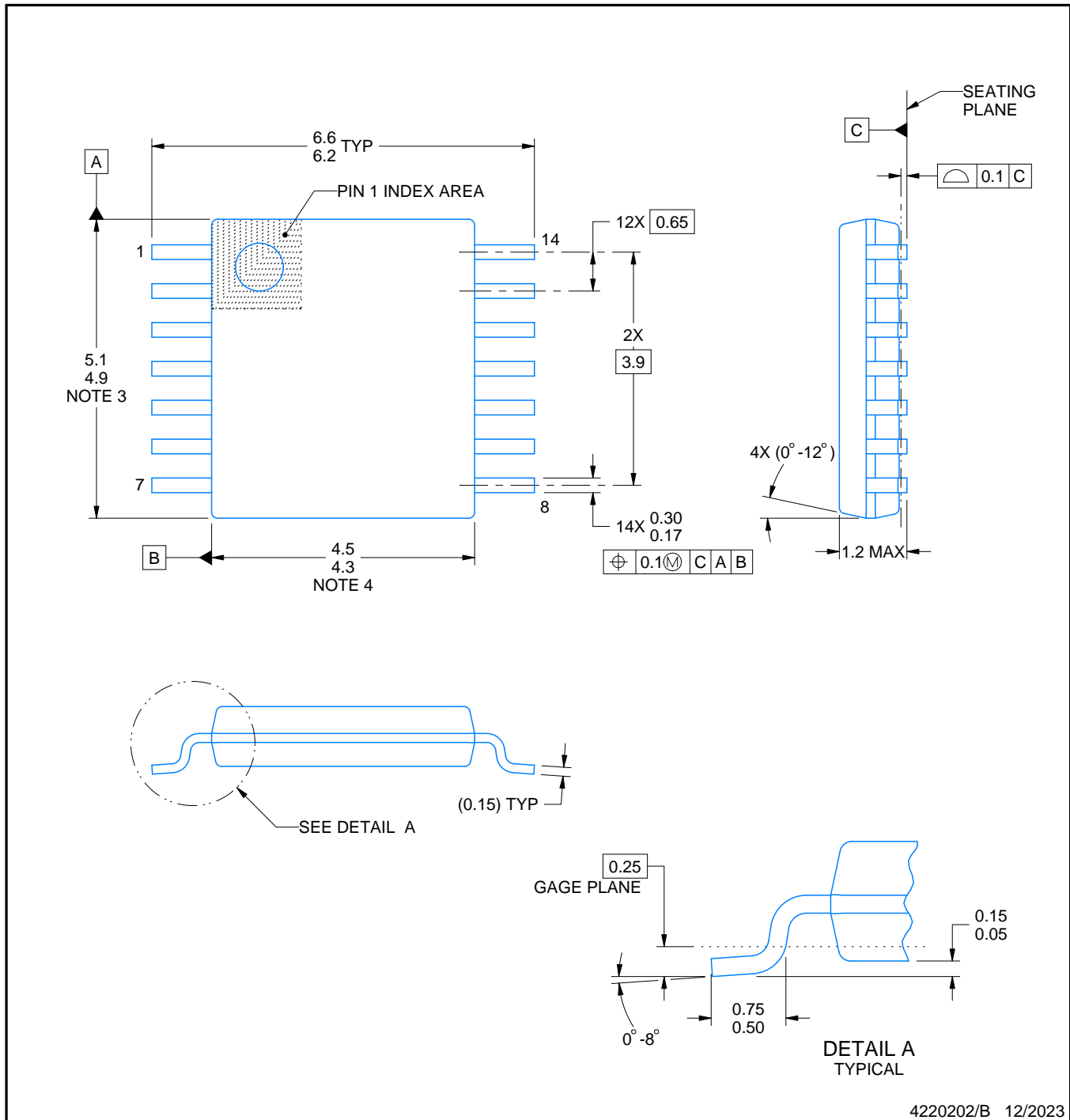


PW0014A

## PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

## NOTES:

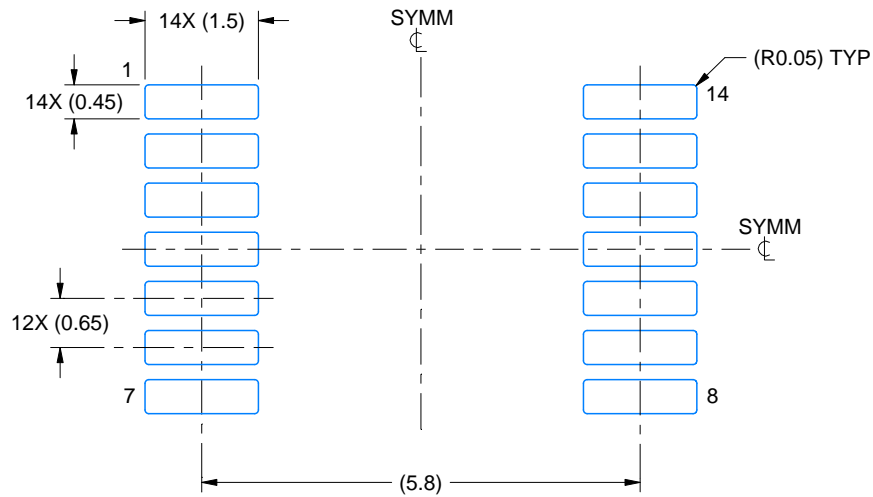
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

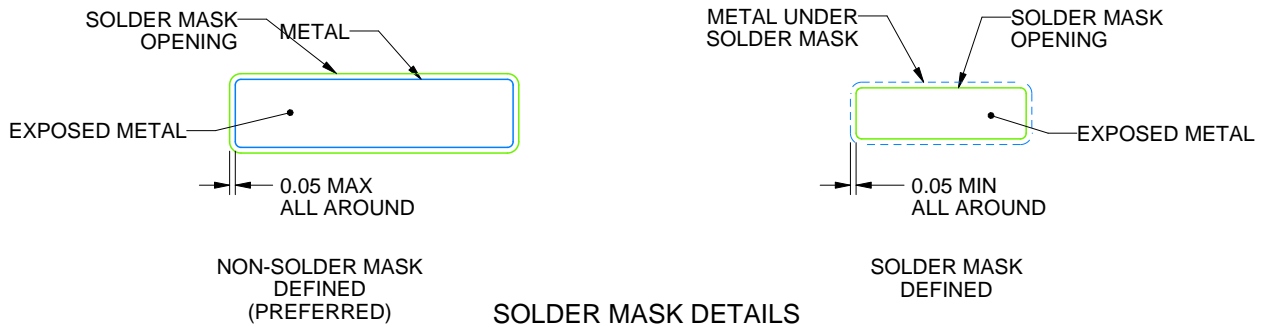
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



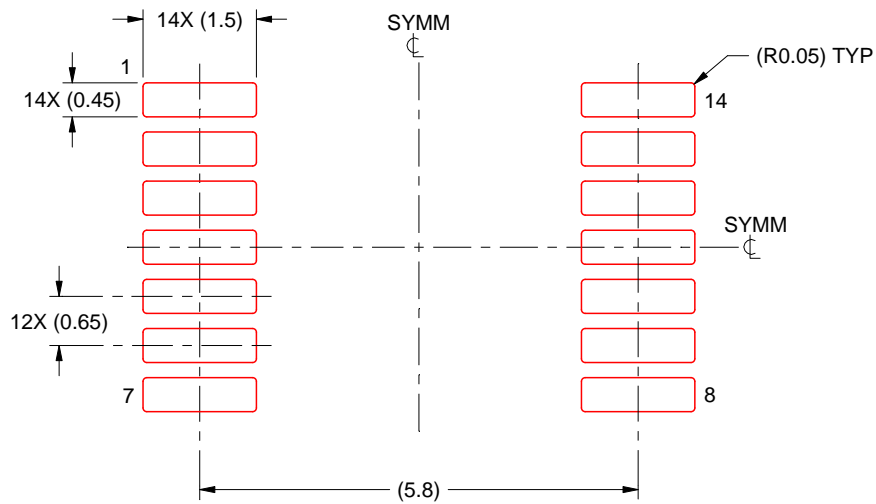
4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****PW0014A****TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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