CD74HC4538QPWRG4Q1 Datasheet

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DiGi Electronics Part Number	CD74HC4538QPWRG4Q1-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	CD74HC4538QPWRG4Q1
Description	IC MULTIVIBRATOR 21NS 16TSSOP
Detailed Description	Monostable Multivibrator 21 ns 16-TSSOP

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
CD74HC4538QPWRG4Q1	Texas Instruments
Series:	Product Status:
74HC	Active
Logic Type:	Independent Circuits:
Monostable	2
Schmitt Trigger Input:	Propagation Delay:
Yes	21 ns
Current - Output High, Low:	Voltage - Supply:
5.2mA, 5.2mA	2 V ~ 6 V
Operating Temperature:	Grade:
-40°C ~ 125°C	Automotive
Qualification:	Mounting Type:
AEC-Q100	Surface Mount
Package / Case:	Supplier Device Package:
16-TSSOP (0.173", 4.40mm Width)	16-TSSOP
Base Product Number:	
74HC4538	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

CD74HC4538-Q1 Automotive High-Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrator

1 Features

- Qualified for automotive applications
- Qualified for automotive applications retriggerable/ resettable capability
- Trigger and reset propagation delays independent of R_X, C_X
- Triggering from the leading or trailing edge
- Q and $\overline{Q}$ buffered outputs available
- Separate resets
- Wide range of output pulse widths
- Schmitt-Trigger input on A and $\overline{B}$ inputs
- Retrigger time is independent of C_X
- Fanout (over temperature range)
  - Standard outputs 10 LSTTL loads
  - Bus driver outputs 15 LSTTL loads
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- V_{CC} voltage = 2V to 6V
- High noise immunity N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5V

2 Description

The CD74HC4538 is a dual retriggerable/resettable precision monostable multivibrator for fixed-voltage timing applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE
CD74HC4538-Q1	D (SOIC, 16)	9.9mm × 6mm	9.9mm x 3.90mm
	PW (TSSOP, 16)	5mm × 6.4mm	5.00mm x 4.40mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.

Table of Contents

3 Pin Configuration and Functions

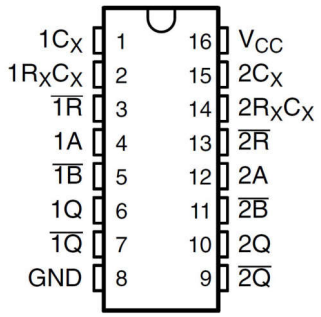


Figure 3-1. D or PW Package; 16-Pin SOIC or TSSOP (Top View)

Table 3-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$1C_X$	1	—	Connects to external capacitor
$1R_XC_X$	2	—	Connects to external capacitor and resistor
1 $\overline{1R}$	3	—	Connects to external resistor
1A	4	I	Ch1 Rising edge input
1B	5	I	Ch1 Falling edge input
1Q	6	O	Ch1 Output
$\overline{1Q}$	7	O	Ch1 Inverted Output
GND	8	—	Ground
$\overline{2Q}$	9	O	Ch2 Inverted Output
2Q	10	O	Ch2 Output
$\overline{2B}$	11	I	Ch2 Falling edge input
2A	12	I	Ch2 Rising edge input
2R	13	—	Connects to external resistor
$2R_XC_X$	14	—	Connects to external capacitor and resistor
$2C_X$	15	—	Connects to external capacitor
V_{CC}	16	—	Power Pin

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	7	V
I_{IK}	Input clamp current	(V_I < −0.5V or V_I > V_{CC} + 0.5V)		±20	mA
I_{OK}	Output clamp current	(V_O < −0.5V or V_O > V_{CC} + 0.5V)		±20	mA
I_O	Switch current per output pin	(V_O > −0.5V or V_O < V_{CC} + 0.5V)		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to GND, unless otherwise specified.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±1500	V
		Charged device model (CDM), per AEC Q100-011	±250	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2	6	V
V_{IH}	High-level input voltage		V_{CC} = 2V	1.5		V
			V_{CC} = 4.5V	3.15		
			V_{CC} = 6V	4.2		
V_{IL}	Low-level input voltage		V_{CC} = 2V		0.5	V
			V_{CC} = 4.5V		1.35	
			V_{CC} = 6V		1.8	
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
t_t	Input transition (rise and fall) time	Reset input	V_{CC} = 2V	0	1000	ns
			V_{CC} = 4.5V	0	500	
			V_{CC} = 6V	0	400	
		Trigger inputs A or $\overline{B}$	V_{CC} = 2V	0	Unlimited	
			V_{CC} = 4.5V	0	Unlimited	
			V_{CC} = 6V	0	Unlimited	
R_X	External timing resistor(1)			5		kΩ
C_X	External timing capacitor(1)			0		F
T_A	Operating free-air temperature			–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC(1)		CD74HC4538-Q1		UNIT
		D	PW	
		16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_OmA	V_{CC}	T_A = 25°C		T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	CMOS loads	−0.02	2 V	1.9		1.9		1.9		V
				4.5 V	4.4		4.4		4.4		
				6 V	5.9		5.9		5.9		
		TTL loads	− 4	4.5 V	3.98		3.84		3.7		
			−5.2	6 V	5.48		5.34		5.2		
V_{OL}	V_I = V_{IH} or V_{IL}	CMOS loads	0.02	2 V		0.1		0.1		0.1	V
				4.5 V		0.1		0.1		0.1	
				6 V		0.1		0.1		0.1	
		TTL loads	4	4.5 V		0.26		0.33		0.4	
			5.2	6 V		0.26		0.33		0.4	
I_I	V_I = V_{CC} or GND	A, $\overline{B}$, R		6 V		±1		±1		±1	µA
		R_XC_X (1)		6 V		±0.05		±0.05		±0.05	
I_{CC}	V_I = V_{CC} or GND	Quiescent	0	6 V		8		80		160	µA
		Active, Q = high, Pins 2 and 14 at V_{CC}/4	0	6 V		0.6		0.8		1	mA
C_{IN}	C_L = 50 pF					10		10		10	pF

(1) When testing I_{IL}, the Q output must be high. If Q is low (device not triggered), the pullup P device is ON and the low-resistance path from V_{DD} to the test pin causes a current far exceeding the specification.

4.6 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER		V_{CC}	T_A = 25°C			T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Input pulse width	2 V	80			100		120		ns
		4.5 V	16			20		24		
		6 V	14			17		20		
t_{su}	Reset setup time	2 V	5			5		5		ns
		4.5 V	5			5		5		
		6 V	5			5		5		
t_{rr}	Retrigger time	5 V		175						ns
	Output pulse-width match, same package			± 1						%

4.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, $\overline{B}$	Q or $\overline{Q}$	C_L = 50 pF	2 V			250		315		375	ns
				4.5 V			50		63		75	
				6 V			43		54		64	
			C_L = 15 pF	5 V		21						
	$\overline{R}$	Q or $\overline{Q}$	C_L = 50 pF	2 V			250		315		375	ns
				4.5 V			50		63		75	
				6 V			43		54		64	
			C_L = 15 pF	5 V		21						
t_t			C_L = 50 pF	2 V			75		95		110	ns
				4.5 V			15		19		22	
				6 V			13		16		19	
τ(1)			C_L = 50 pF	3 V	0.64		0.78	0.612	0.812	0.605	0.819	ms
				5 V	0.63		0.77	0.602	0.798	0.595	0.805	

(1) Output pulse width with R_X = 10 kΩ and C_X = 0.1 µF

4.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns, C_L = 15 pF

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	136	pF

Note

- C_{pd} is used to determine the dynamic power consumption, per one shot.
- $P_D = (C_{pd} + C_X) V_{CC} 2 f_I \Sigma(C_L V_{CC} 2 f_O)$
- f_I = input frequency
- f_O = output frequency
- C_L = output load capacitance
- C_X = external capacitance
- V_{CC} = supply voltage, assuming f_I I/τ

4.9 Typical Characteristics

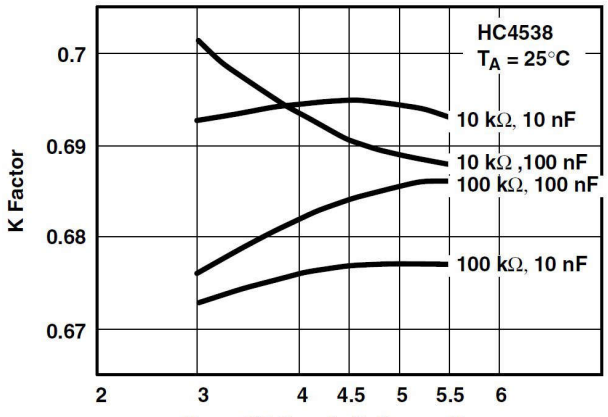


Figure 4-1. K Factor vs DC Supply Voltage

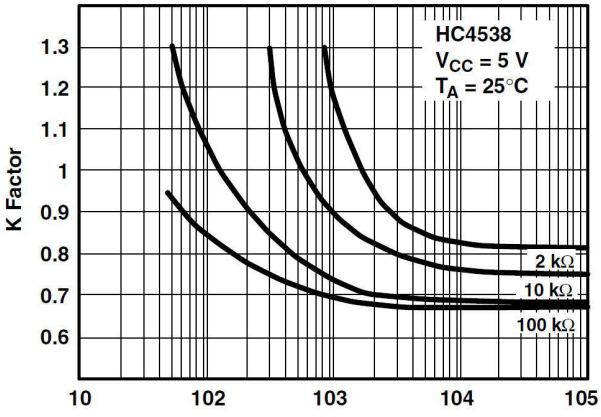


Figure 4-2. K Factor vs C_X

4.9 Typical Characteristics (continued)

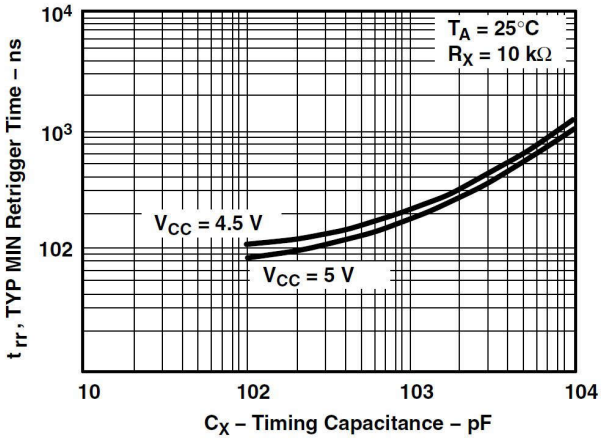


Figure 4-3. Minimum Retrigger Time vs Timing Capacitance

5 Parameter Measurement Information

Load Circuit and Voltage Waveforms

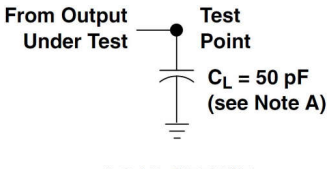


Figure 5-1. Load Circuit

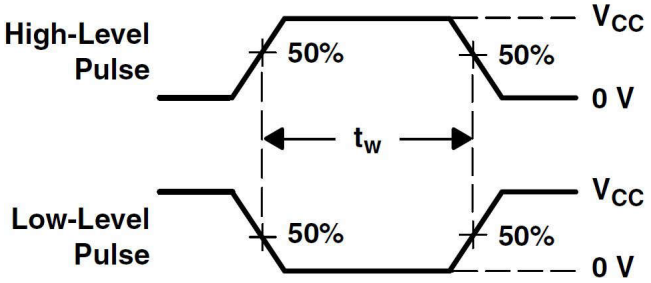


Figure 5-2. Voltage Waveforms Pulse Durations

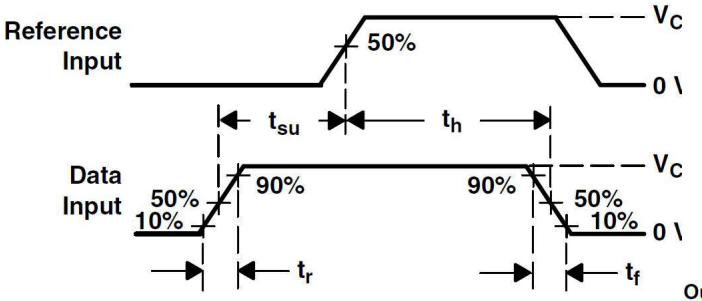


Figure 5-3. Voltage Waveforms Setup and Hold and Input Rise and Fall Times

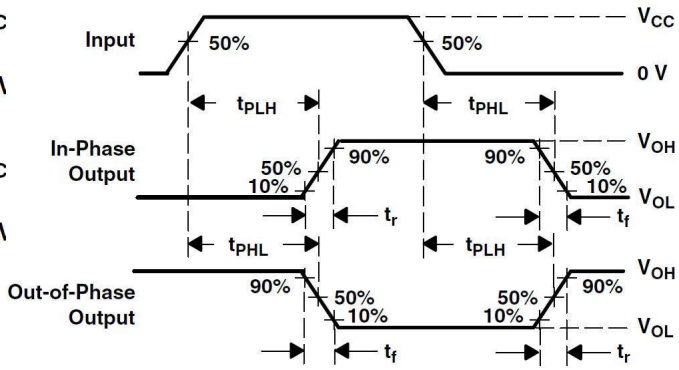


Figure 5-4. Voltage Waveforms Propagation Delay and Output Transition Times

Note

- C_L includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
- For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- The outputs are measured one at a time, with one input transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd}.

6 Detailed Description

6.1 Overview

An external resistor (R_X) and external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of R_X and C_X.

Leading-edge triggering (A) and trailing-edge triggering ($\overline{B}$) inputs are provided for triggering from either edge of the input pulse. An unused A input should be tied to GND and an unused $\overline{B}$ input should be tied to V_{CC}. On power up, the IC is reset. Unused resets and sections must be terminated. In normal operation, the circuit retriggers on the application of each new trigger pulse. To operate in the nontriggerable mode, $\overline{Q}$ is connected to $\overline{B}$ when leading-edge triggering (A) is used, or Q is connected to A when trailing-edge triggering ($\overline{B}$) is used. The period (τ) can be calculated from $\tau = (0.7)\ R_X, C_X$; R_{MIN} is 5 kΩ. C_{MIN} is 0 pF.

6.2 Functional Block Diagram

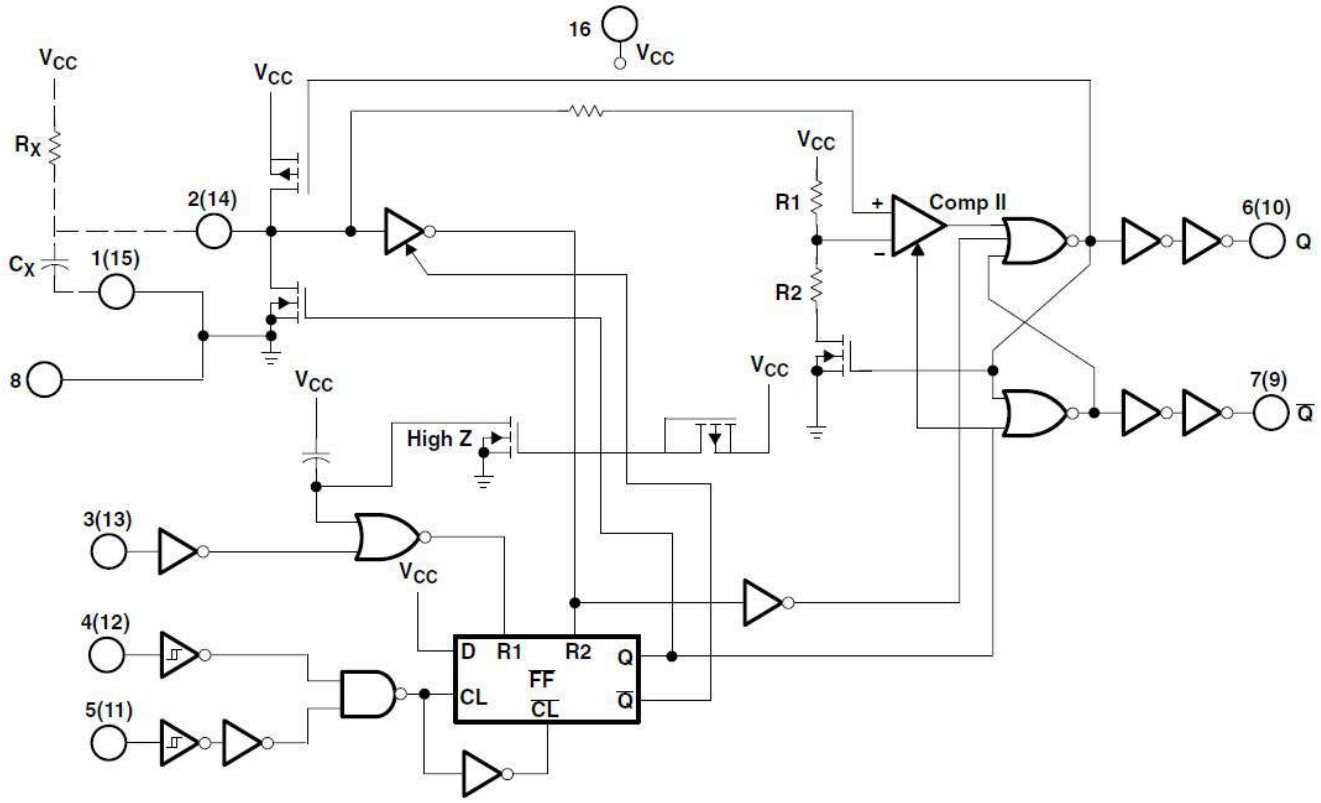


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table

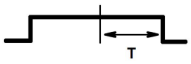
INPUTS			OUTPUTS	
$\overline{R}$	A	$\overline{B}$	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎍
H	↑	H	⎍	⎍

Table 6-2. Functional Terminal Connections

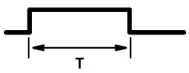
FUNCTION	V_{CC} TO TERMINAL NUMBER		GND TO TERMINAL NUMBER		INPUT PULSE TO TERMINAL NUMBER		OTHER CONNECTIONS	
	MONO(1)	MONO(2)	MONO(1)	MONO(2)	MONO(1)	MONO(2)	MONO(1)	MONO(2)
Leading-edge trigger/ retriggerable	3, 5	11, 13			4	12		
Leading-edge trigger/ nonretriggerable	3	13			4	12	5−7	11−9
Trailing-edge trigger/ retriggerable	3	13	4	12	5	11		
Trailing-edge trigger/ nonretriggerable	3	13			5	11	4−6	12−10

(1) A retriggerable one-shot multivibrator has an output pulse width that is extended one full time period (T) after application of the last trigger pulse.
(2) A nontriggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.

Input Pulse Train



Retriggerable Mode Pulse Width (A Mode)



Nonretriggerable Mode Pulse Width (A Mode)

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

Power-Down Mode

During a rapid power-down condition (as would occur with a power-supply short circuit with a poorly filtered power supply), the energy stored in C_X could discharge into pin 2 or pin 14. To avoid possible device damage in this mode when C_X is \u0001 0.5 µF, a protection diode with a 1-A rating or higher (1N5395 or equivalent) and a separate ground return for C_X should be provided. Rapid-Power-Down Protection Circuit

An alternate protection method is shown in Alternative Rapid-Power-Down Protection Circuit, where a 51-Ω current-limiting resistor is inserted in series with C_X . Note that a small pulse-duration decrease occurs, however, and R_X must be increased appropriately to obtain the originally desired pulse duration.

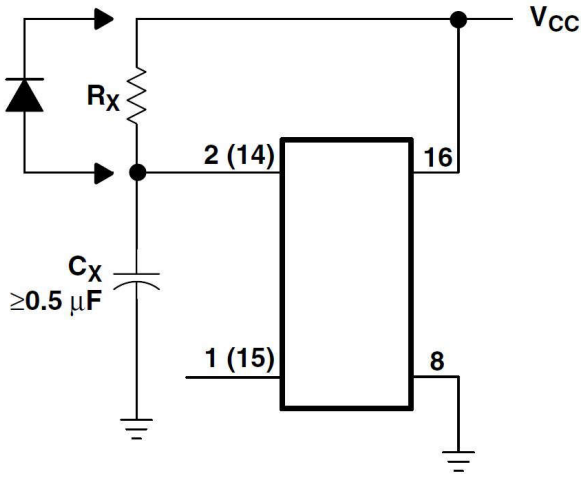


Figure 7-1. Rapid-Power-Down Protection Circuit

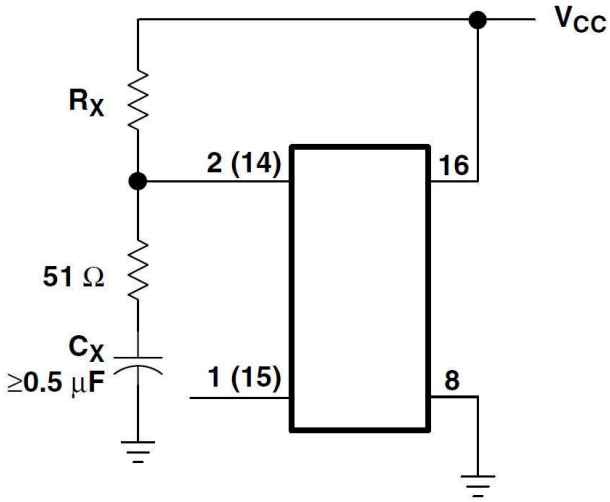


Figure 7-2. Alternative Rapid-Power-Down Protection Circuit

7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

7.3 Layout

7.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used,

or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74HC4538-Q1	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision A (April 2008) to Revision B (August 2024)	Page
• Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4538QM96G4Q1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M
CD74HC4538QM96G4Q1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M
CD74HC4538QPWRG4Q1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M
CD74HC4538QPWRG4Q1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M
CD74HC4538QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M
CD74HC4538QPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD74HC4538-Q1 :

- Catalog : CD74HC4538
- Military : CD54HC4538

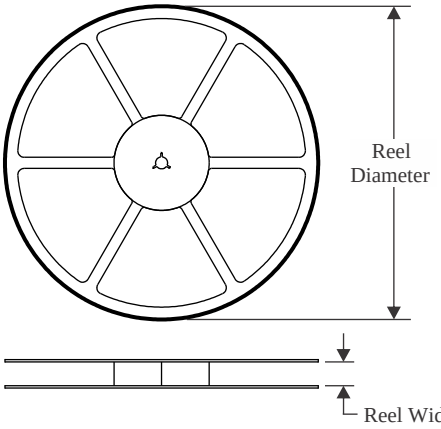
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

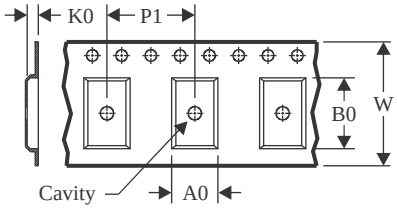
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

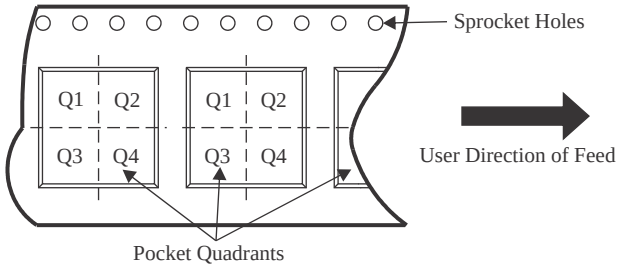


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4538QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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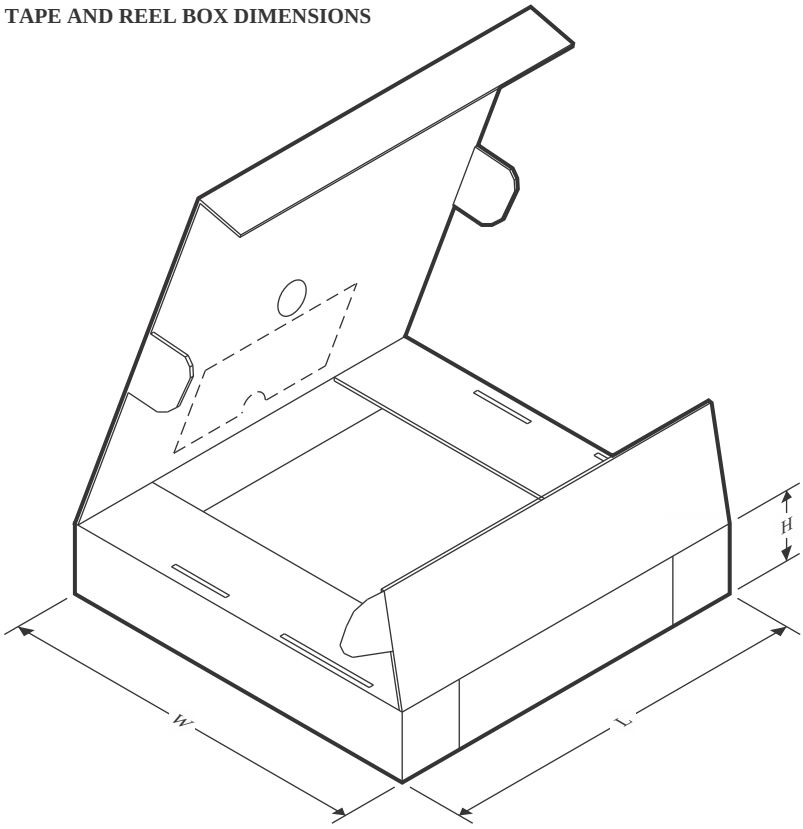
24-Jul-2025

TAPE AND REEL BOX DIMENSIONS

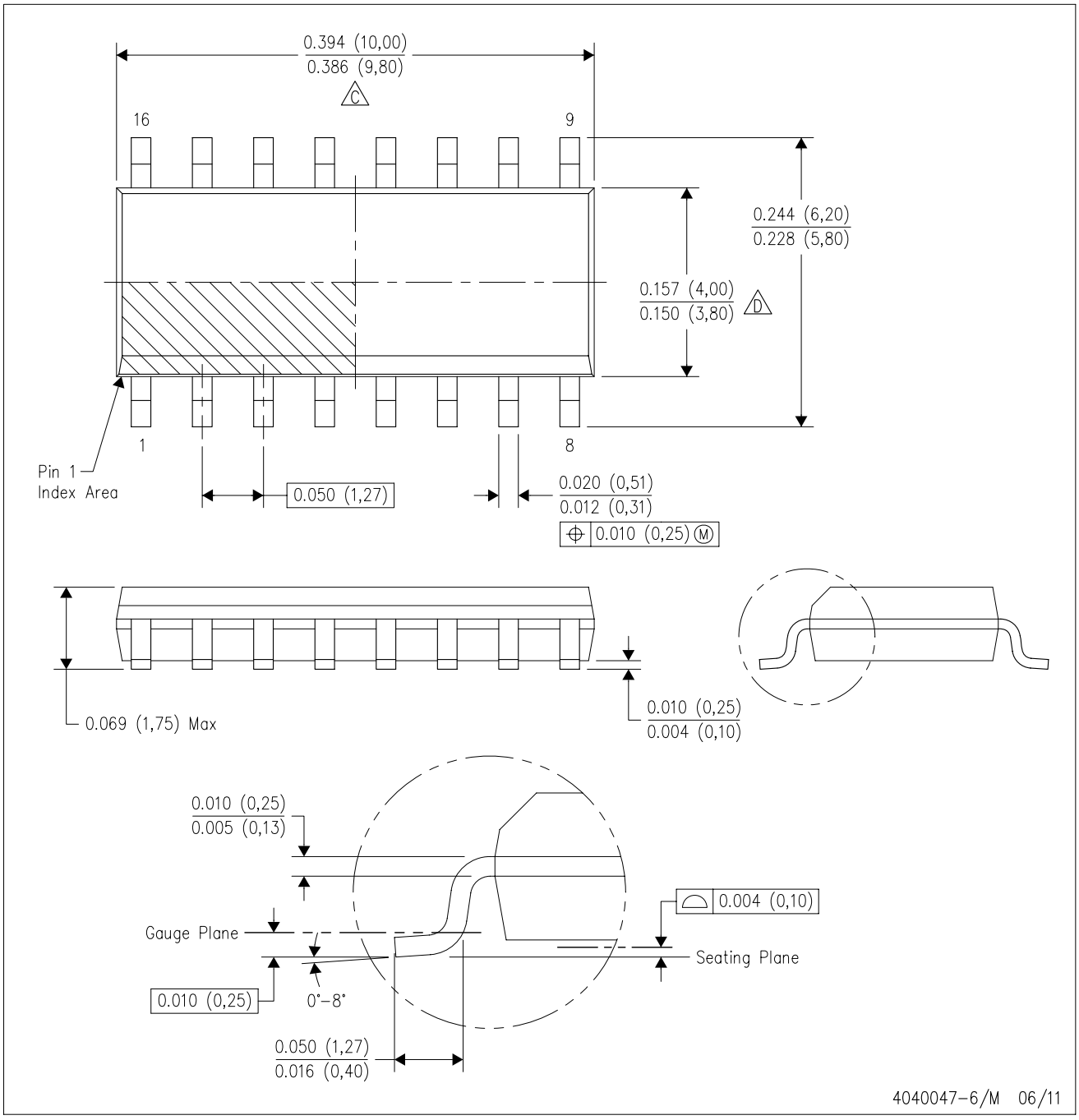


*All dimensions are nominal

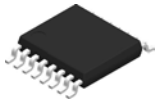
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4538QPWRG4Q1	TSSOP	PW	16	2000	353.0	353.0	32.0

MECHANICAL DATA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

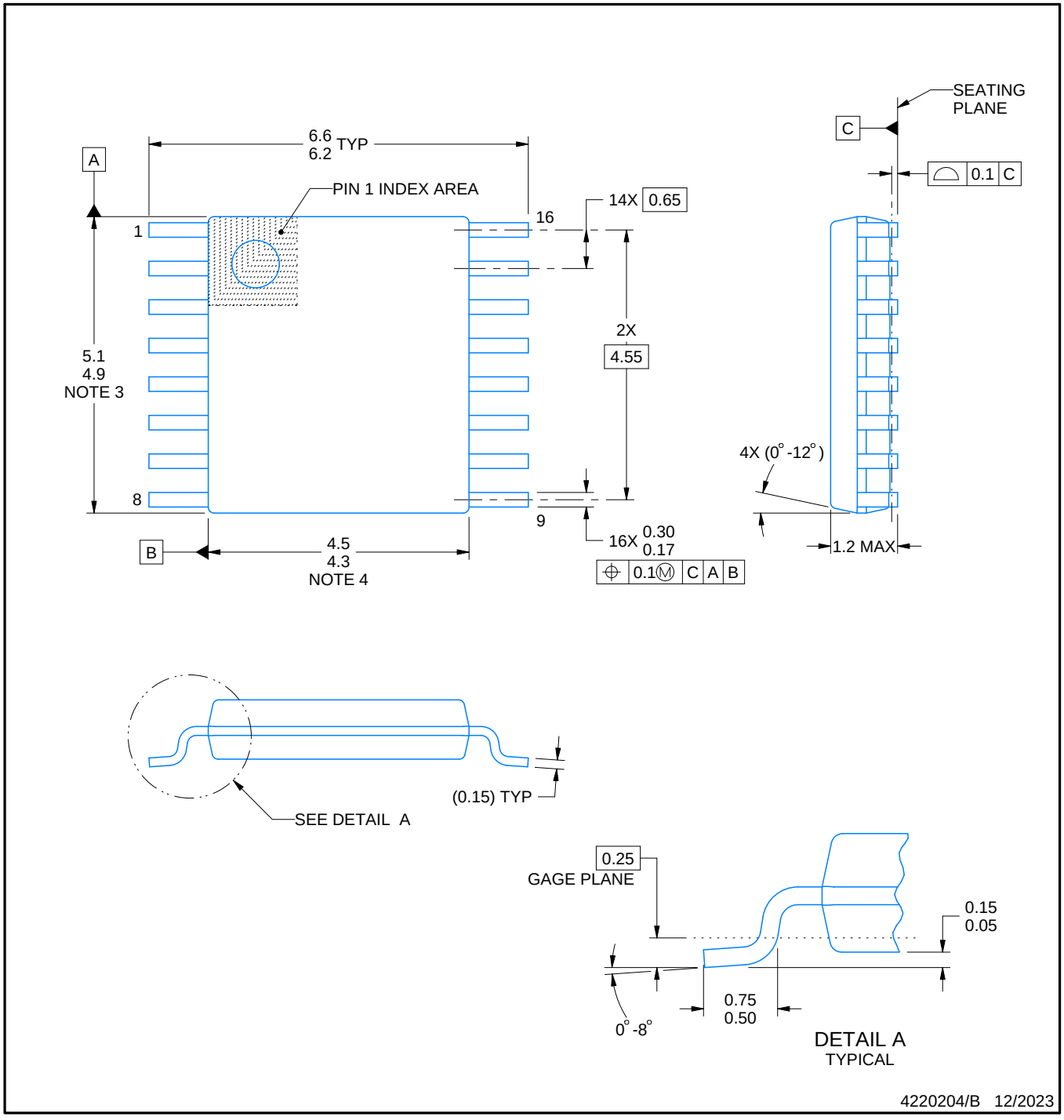


PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

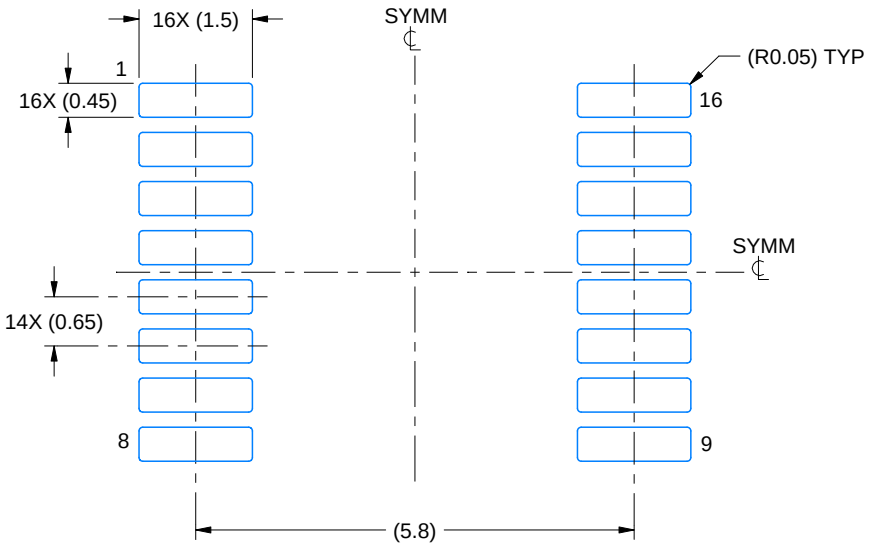
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

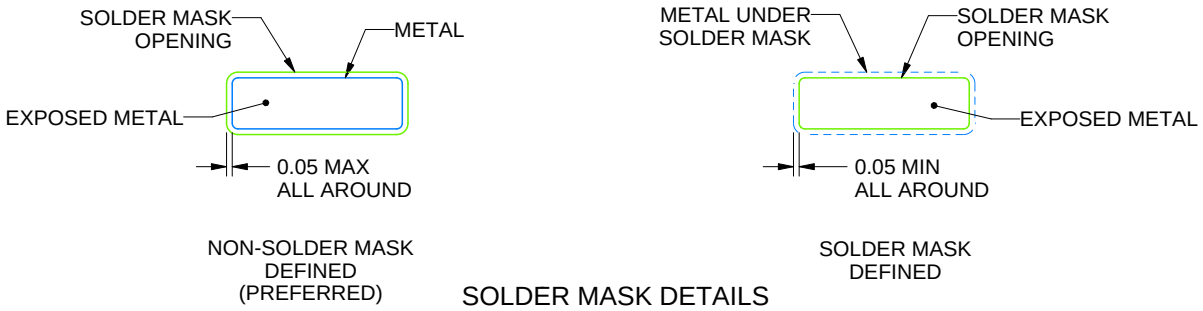
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

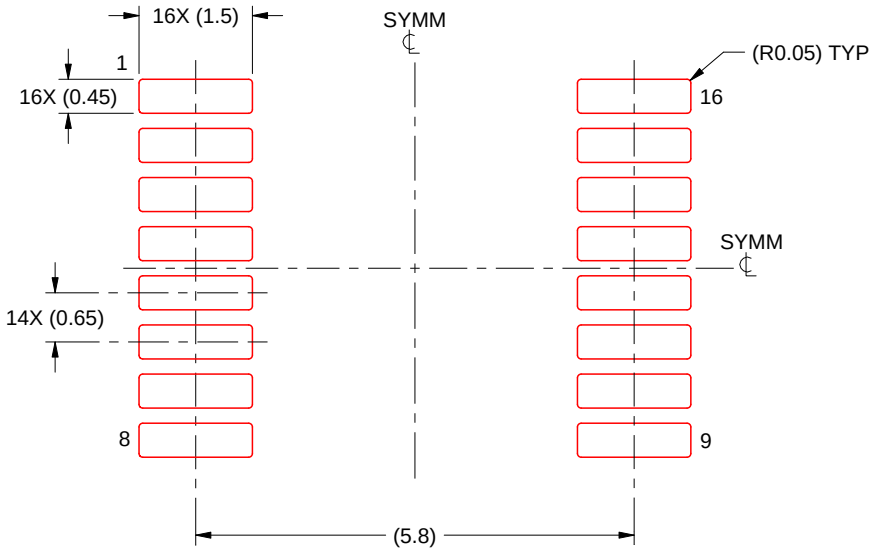
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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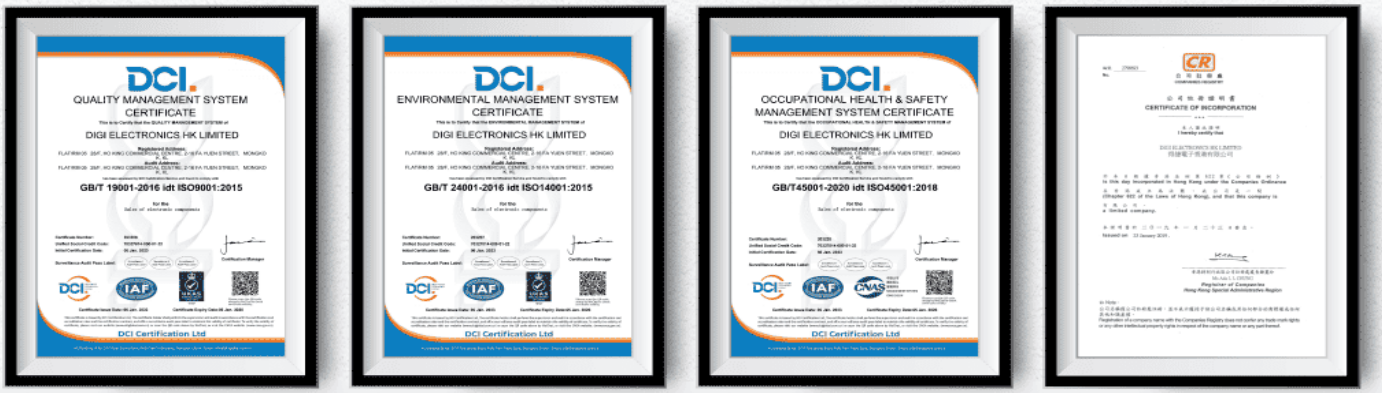

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