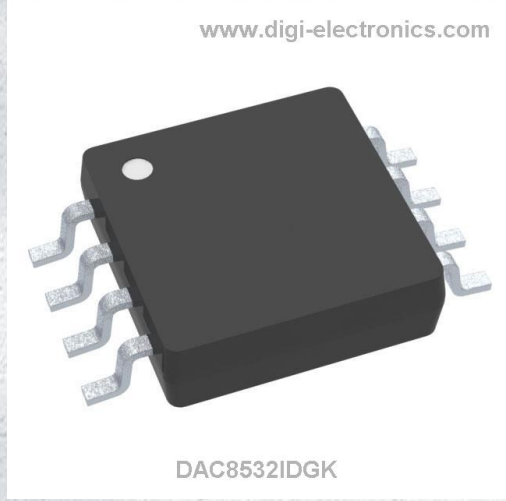
# DAC8532IDGK Datasheet




https://www.DiGi-Electronics.com

| | |
|---|---|
| DiGi Electronics Part Number | DAC8532IDGK-DG |
| Manufacturer | Texas Instruments |
| Manufacturer Product Number | DAC8532IDGK |
| Description | IC DAC 16BIT V-OUT 8VSSOP |
| Detailed Description | 16 Bit Digital to Analog Converter 2 8-VSSOP |

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RFQ Email: Info@DiGi-Electronics.com

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| DAC8532IDGK | Texas Instruments |
| Series: | Product Status: |
| - | Active |
| DiGi-Electronics Programmable: | Number of Bits: |
| Not Verified | 16 |
| Number of D/A Converters: | Settling Time: |
| 2 | 10µs |
| Output Type: | Differential Output: |
| Voltage - Buffered | No |
| Data Interface: | Reference Type: |
| SPI, DSP | External |
| Voltage - Supply, Analog: | Voltage - Supply, Digital: |
| 2.7V ~ 5.5V | 2.7V ~ 5.5V |
| INL/DNL (LSB): | Architecture: |
| -, ±1 (Max) | String DAC |
| Operating Temperature: | Package / Case: |
| -40°C ~ 105°C | 8-TSSOP, 8-MSOP (0.118", 3.00mm Width) |
| Supplier Device Package: | Mounting Type: |
| 8-VSSOP | Surface Mount |
| Base Product Number: | |
| DAC8532 | |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| ROHS3 Compliant | 2 (1 Year) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

# DAC8532 Dual Channel, 16-Bit, Low Power, Serial Input Digital-To-Analog Converter

## 1 Features

- 16-Bit Monotonic Over Temperature
- *Micro*Power Operation: 500 µA at 5 V
- Power-On Reset to Zero-Scale
- Power Supply: 2.7 V to 5.5 V
- Settling Time: 10 µs to ±0.003% FSR
- Ultra-Low AC Crosstalk: –100 dB Typ
- Low-Power Serial Interface With Schmitt-Triggered Inputs
- On-Chip Output Buffer Amplifier With Rail-to-Rail Operation
- Double-Buffered Input Architecture
- Simultaneous or Sequential Output Update and Powerdown
- Available in a Tiny VSSOP-8 Package

## 2 Applications

- Portable Instrumentation
- Closed-Loop Servo Control
- Process Control
- Data Acquisition Systems
- Programmable Attenuation
- PC Peripherals

## 3 Description

The DAC8532 is a dual channel, 16-bit digital-to-analog converter (DAC) offering low power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7 V to 5.5 V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30 MHz for $V_{DD}$ = 5 V.

The DAC8532 requires an external reference voltage to set the output range of each DAC channel. The device incorporates a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place. The DAC8532 provides a flexible power-down feature, accessible over the serial interface, that reduces the current consumption of the device to 200 nA at 5 V.

The low-power consumption of the device in normal operation makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 2.5 mW at 5 V, reducing to 1 µW in power-down mode.

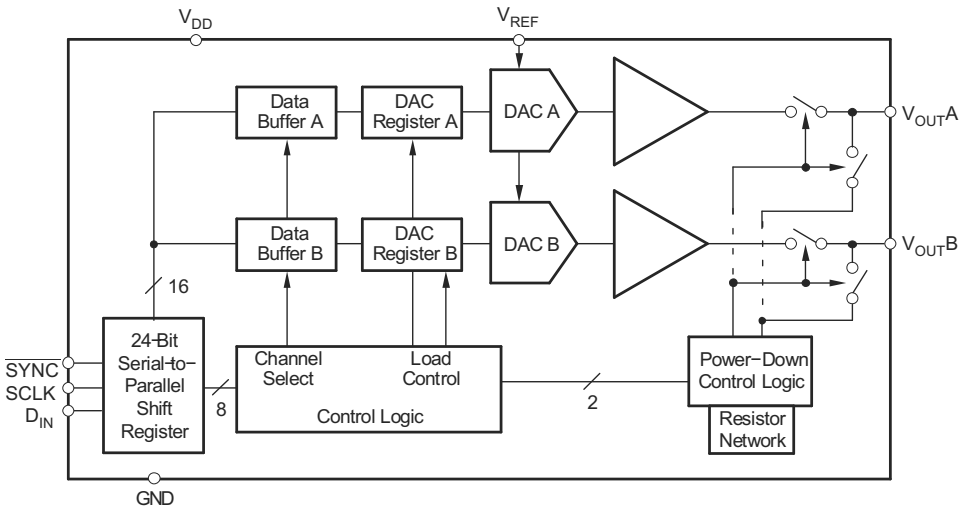
The DAC8532 is available in a VSSOP-8 package with a specified operating temperature range of –40°C to 105°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DAC8532 | VSSOP (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Diagram



## Table of Contents



## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (May 2003) to Revision B** **Page**

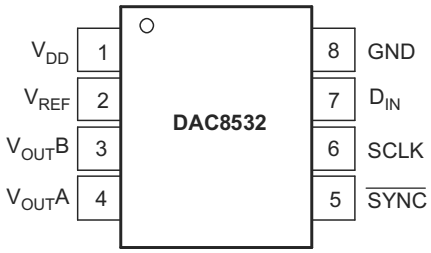
- Added Device Information and Handling Rating tables, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ... 1

**Changes from Original (December 2001) to Revision A** **Page**

- Added text string "No device pin should be brought high before power is applied to the device." to the Power-On Reset Description. ... 14

# 6 Pin Configuration and Functions

**VSSOP (DGK) Package**
**8 Pins**
**Top View**




**Pin Functions**

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{DD}$ | Power supply input, 2.7 V to 5.5 V |
| 2 | $V_{REF}$ | Reference voltage input |
| 3 | $V_{OUT}B$ | Analog output voltage from DAC B |
| 4 | $V_{OUT}A$ | Analog output voltage from DAC A |
| 5 | $\overline{SYNC}$ | Level triggered $\overline{SYNC}$ input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred on the falling edges of SCLK. The action specified by the 8-bit control byte and 16-bit data word is executed following the 24th falling SCLK clock edge (unless $\overline{SYNC}$ is taken HIGH before this edge in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8532). |
| 6 | SCLK | Serial Clock Input. Data can be transferred at rates up to 30 MHz at 5 V. |
| 7 | $D_{IN}$ | Serial Data Input. Data is clocked into the 24-bit input shift register on the falling edge of the serial clock input. |
| 8 | GND | Ground reference point for all circuitry on the part. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{DD}$ to GND | –0.3 | 6 | V |
| Digital input voltage to GND | –0.3 | $V_{DD}$+0.3 | V |
| $V_{OUTA}$ or $V_{OUTB}$ to GND | –0.3 | $V_{DD}$+0.3 | V |
| Operating temperature range | –40 | 105 | °C |
| $T_J$ | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1) | | 1000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2) | | 500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

all specifications –40°C to 105°C (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ to GND | 0 | | 5.5 | V |
| Digital input voltage to GND | 0 | | $V_{DD}$ | |
| $V_{OUTA}$ or $V_{OUTB}$ to GND | 0 | | $V_{DD}$ | |
| Operating temperature range | –40 | | 105 | °C |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | DAC8532 DGK 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 164.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 59.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 84.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 83.3 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

$V_{DD}$ = 2.7 V to 5.5 V, all specifications –40°C to 105°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **STATIC PERFORMANCE[1]** | | | | | |
| Resolution | | 16 | | | Bits |
| Relative accuracy | | | | ±0.0987 | % of FSR |
| Differential nonlinearity | 16-bit monotonic | | | ±1 | LSB |
| Zero code error | | | 5 | 25 | mV |
| Full-scale error | | | –0.15 | –1 | % of FSR |
| Gain error | | | | ±1 | % of FSR |
| Zero code error drift | | | ±20 | | µV/°C |
| Gain temperature coefficient | | | ±5 | | ppm of FSR/°C |
| Channel-to-channel matching PSRR | $R_L$ = 2 kΩ, $C_L$ = 200 pF | | 15 | | mV |
| | | | 0.75 | | mV/V |
| **OUTPUT CHARACTERISTICS[2]** | | | | | |
| Output voltage range | | 0 | | $V_{REF}$ | V |
| Output voltage settling time | To ±0.003% FSR $0200_H$ to $FD00_H$, $R_L$ = 2 kΩ; 0 pF < $C_L$ < 200 pF, $R_L$ = 2 kΩ; $C_L$ = 500 pF | | 8 | 10 | µs |
| | | | 12 | | |
| Slew rate | | | 1 | | V/µs |
| Capacitive load stability | $R_L$ = ∞ | | 470 | | pF |
| | $R_L$ = 2 kΩ | | 1000 | | |
| Code change glitch impulse | 1 LSB change around major carry | | 20 | | nV-s |
| Digital feedthrough | | | 0.5 | | nV-s |
| DC crosstalk | | | 0.25 | | LSB |
| AC crosstalk | | | –100 | –96 | dB |
| DC output impedance | | | 1 | | Ω |
| Short circuit current | $V_{DD}$ = 5 V | | 50 | | mA |
| | $V_{DD}$ = 3 V | | 20 | | |

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.
(2) Ensured by design and characterization, not production tested.

## Electrical Characteristics (continued)

$V_{DD}$ = 2.7 V to 5.5 V, all specifications –40°C to 105°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Power-up time | Coming out of power-down mode $V_{DD}$ = 5 V | | 2.5 | | µs |
| | Coming out of power-down mode $V_{DD}$ = 3 V | | 5 | | µs |
| **AC PERFORMANCE** | | | | | |
| SNR | BW = 20 kHz, $V_{DD}$ = 5 V, $F_{OUT}$ = 1 kHz, 1st 19 harmonics removed | | 94 | | dB |
| THD | | | 67 | | |
| SFDR | | | 69 | | |
| SINAD | | | 65 | | |
| **REFERENCE INPUT** | | | | | |
| Reference current | $V_{REF}$ = $V_{DD}$ = 5 V | | 67 | 90 | µA |
| | $V_{REF}$ = $V_{DD}$ = 3 V | | 40 | 54 | |
| Reference input range | | 0 | | $V_{DD}$ | V |
| Reference input impedance | | | 75 | | kΩ |
| **LOGIC INPUTS** (2) | | | | | |
| Input current | | | | ±1 | µA |
| $V_{IN}$L, Input LOW voltage | $V_{DD}$ = 5 V | | | 0.8 | V |
| | $V_{DD}$ = 3 V | | | 0.6 | |
| $V_{IN}$H, Input HIGH voltage | $V_{DD}$ = 5 V | 2.4 | | | V |
| | $V_{DD}$ = 3 V | 2.1 | | | |
| Pin capacitance | | | | 3 | pF |
| **POWER REQUIREMENTS** | | | | | |
| $V_{DD}$ | | 2.7 | | 5.5 | V |
| $I_{DD}$ (normal mode) | DAC active and excluding load current | | | | µA |
| $V_{DD}$ = 3.6 V to 5.5 V | $V_{IH}$ = $V_{DD}$ and $V_{IL}$ = GND | | 500 | 800 | |
| $V_{DD}$ = 2.7 V to 3.6 V | | | 450 | 750 | |
| $I_{DD}$ (all power-down modes) | $V_{IH}$ = $V_{DD}$ and $V_{IL}$ = GND | | | | µA |
| $V_{DD}$ = 3.6 V to 5.5 V | | | 0.2 | 1 | |
| $V_{DD}$ = 2.7 V to 3.6 V | | | 0.05 | 1 | |
| **POWER EFFICIENCY** | | | | | |
| $I_{OUT}/I_{DD}$ | $I_{LOAD}$ = 2 mA, $V_{DD}$ = 5 V | | 89% | | |
| **TEMPERATURE RANGE** | | | | | |
| Specified performance | | –40 | | 105 | °C |

## 7.6 Timing Requirements (1)(2)

$V_{DD}$ = 2.7 V to 5.5 V, all specifications –40°C to 105°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ (3) | SCLK cycle time | $V_{DD}$ = 2.7 V to 3.6 V | 50 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 33 | | | |
| $t_2$ | SCLK HIGH time | $V_{DD}$ = 2.7 V to 3.6 V | 13 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 13 | | | |
| $t_3$ | SCLK LOW time | $V_{DD}$ = 2.7 V to 3.6 V | 22.5 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 13 | | | |
| $t_4$ | $\overline{SYNC}$ to SCLK rising edge setup time | $V_{DD}$ = 2.7 V to 3.6 V | 0 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 0 | | | |
| $t_5$ | Data setup time | $V_{DD}$ = 2.7 V to 3.6 V | 5 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 5 | | | |
| $t_6$ | Data hold time | $V_{DD}$ = 2.7 V to 3.6 V | 4.5 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 4.5 | | | |
| $t_7$ | 24th $\overline{SCLK}$ falling edge to SYNC rising edge | $V_{DD}$ = 2.7 V to 3.6 V | 0 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 0 | | | |
| $t_8$ | Minimum $\overline{SYNC}$ HIGH time | $V_{DD}$ = 2.7 V to 3.6 V | 50 | | | ns |
| | | $V_{DD}$ = 3.6 V to 5.5 V | 33 | | | |
| $t_9$ | 24th SCLK falling edge to $\overline{SYNC}$ falling edge | $V_{DD}$ = 2.7 V to 5.5 V | 100 | | | ns |

(1) All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See Serial Write Operation timing diagram Figure 1.
(3) Maximum SCLK frequency is 30 MHz at $V_{DD}$ = 3.6 V to 5.5 V and 20 MHz at $V_{DD}$ = 2.7 V to 3.6 V.

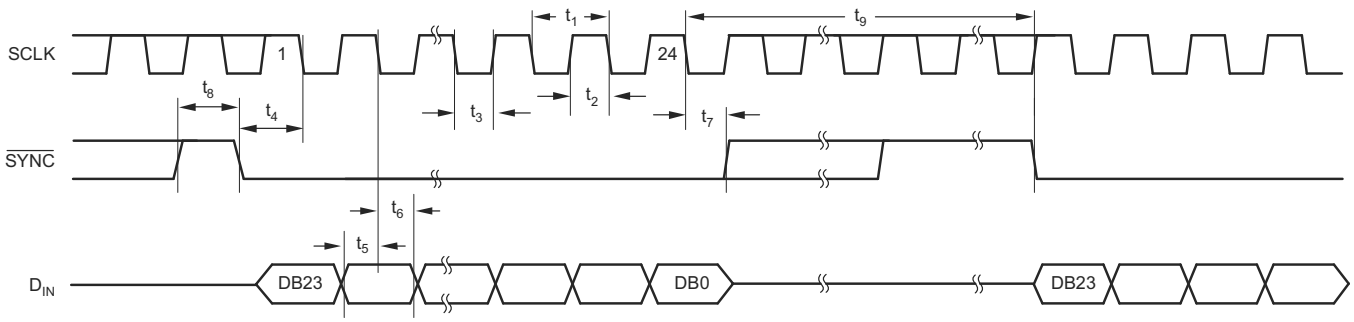



**Figure 1. Serial Write Operation**

## 7.7 Typical Characteristics

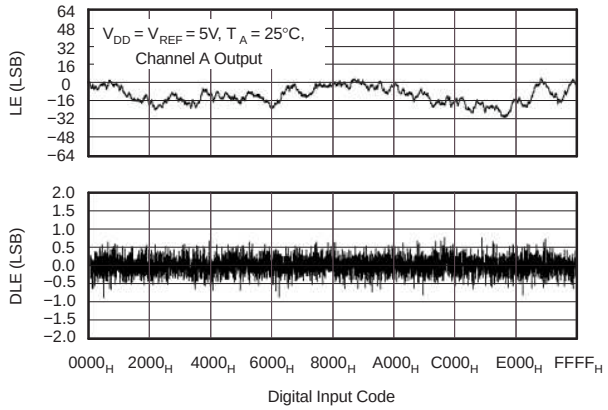



**Figure 2. Linearity Error and Differential Linearity Error vs Code**

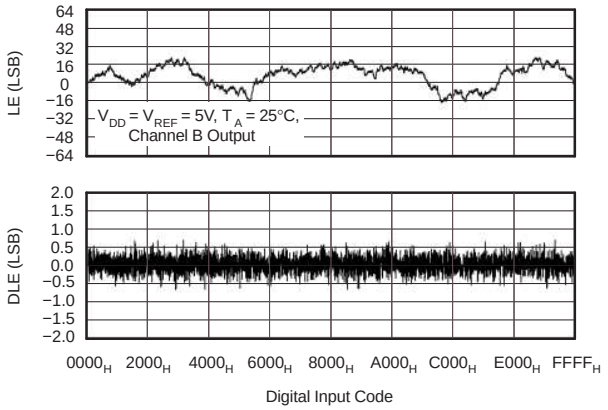



**Figure 3. Linearity Error and Differential Linearity Error vs Code**

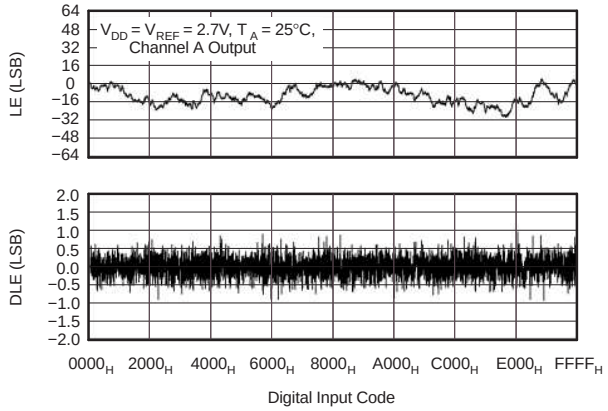



**Figure 4. Linearity Error and Differential Linearity Error vs Code**

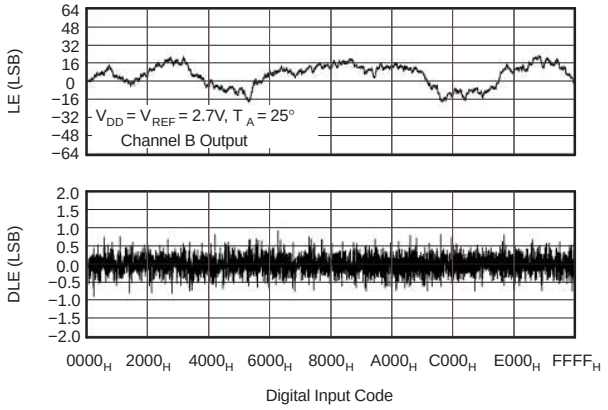



**Figure 5. Linearity Error and Differential Linearity Error vs Code**

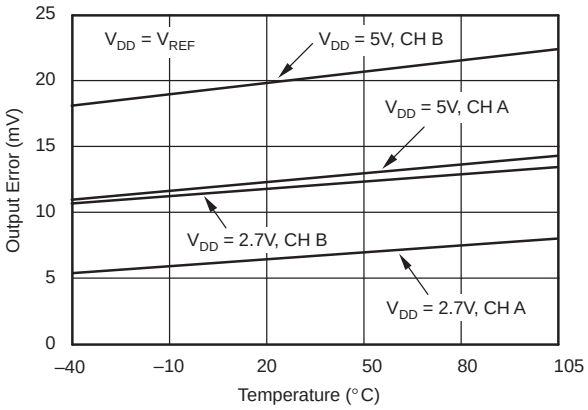



**Figure 6. Zero-Scale Error vs Temperature**

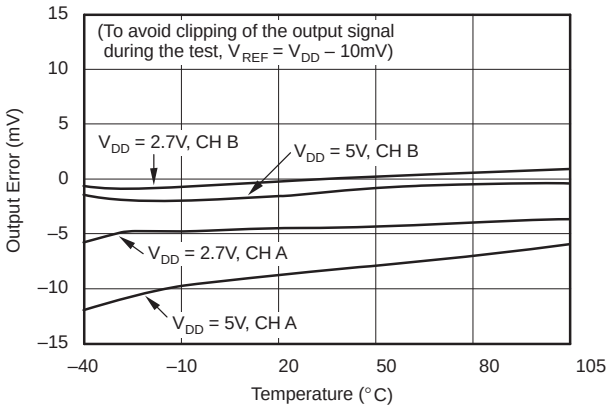



**Figure 7. Full-Scale Error vs Temperature**

## Typical Characteristics (continued)

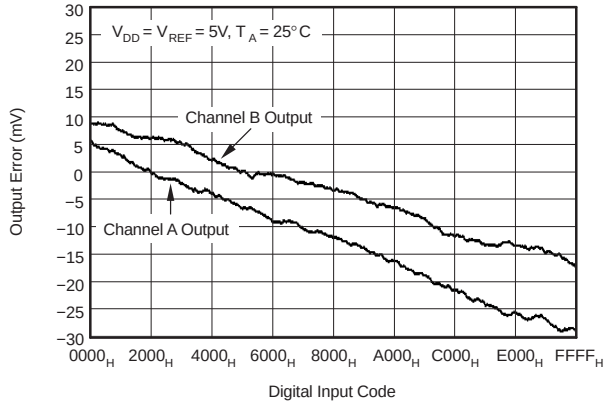



**Figure 8. Absolute Error**

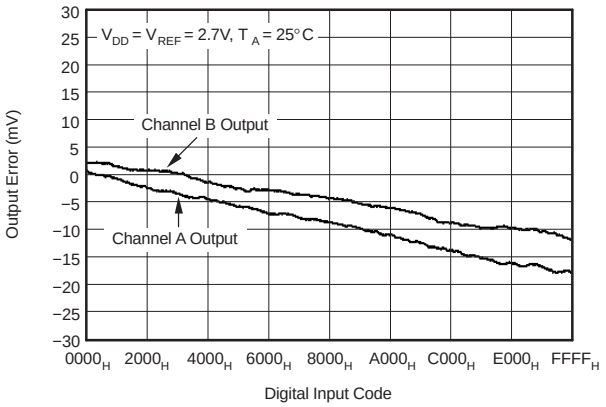



**Figure 9. Absolute Error**

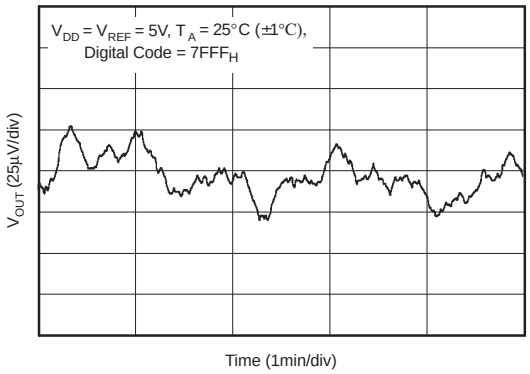



**Figure 10. Output Voltage Drift**

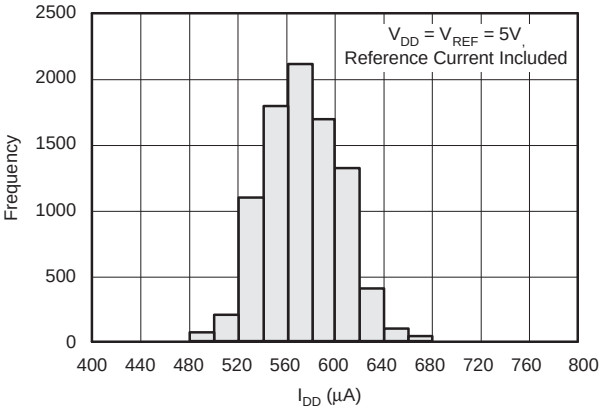



**Figure 11. Histogram of Current Consumption**

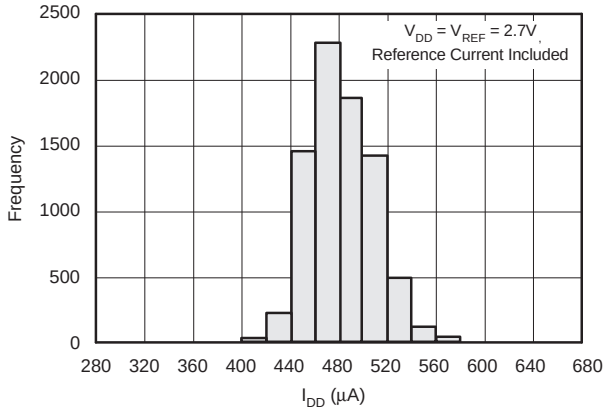



**Figure 12. Histogram of Current Consumption**

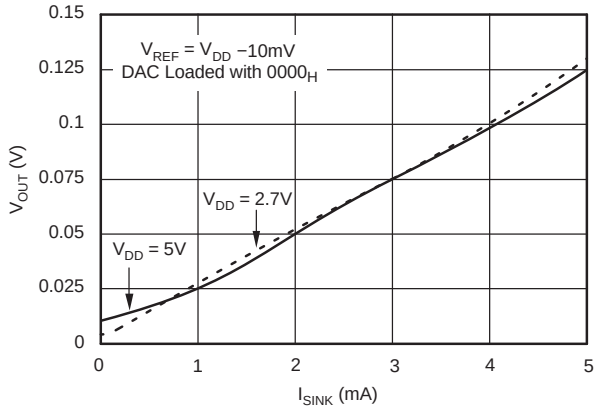



**Figure 13. Sink Current Capability**

## Typical Characteristics (continued)

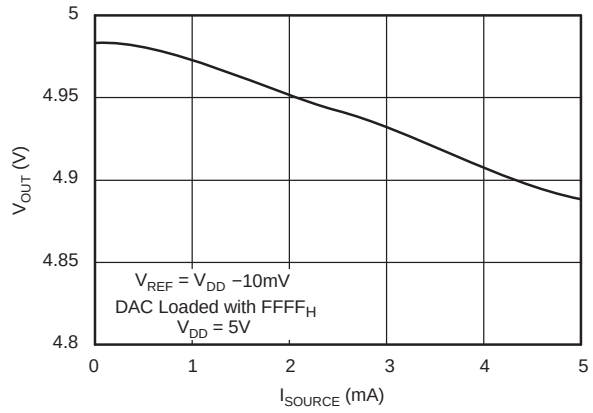



**Figure 14. Source Current Capability**

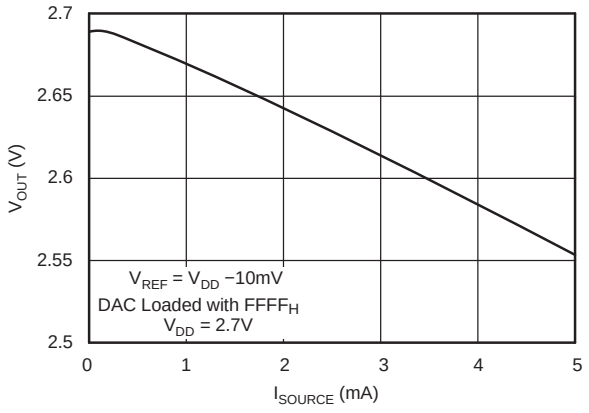



**Figure 15. Source Current Capability**

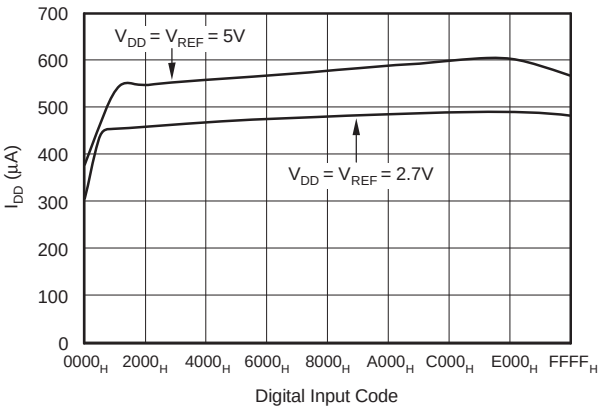



**Figure 16. Supply Current vs Digital Input Code**

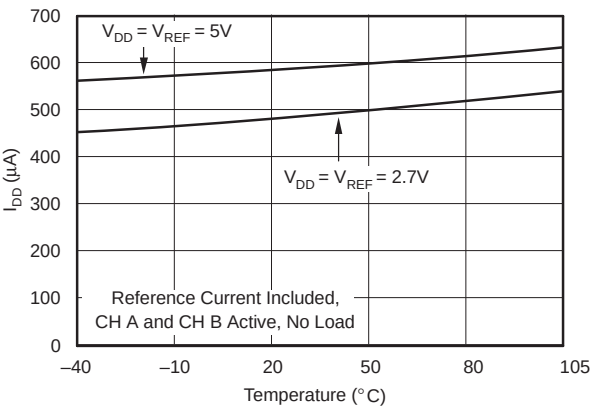



**Figure 17. Supply Current vs Temperature**

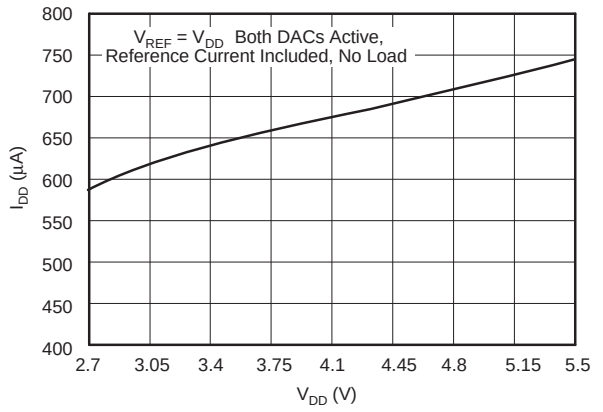



**Figure 18. Supply Current vs Supply Voltage**

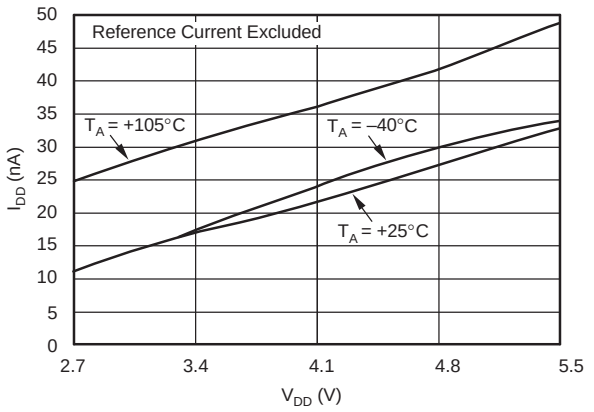



**Figure 19. Power-Down Current vs Supply Voltage**

## Typical Characteristics (continued)

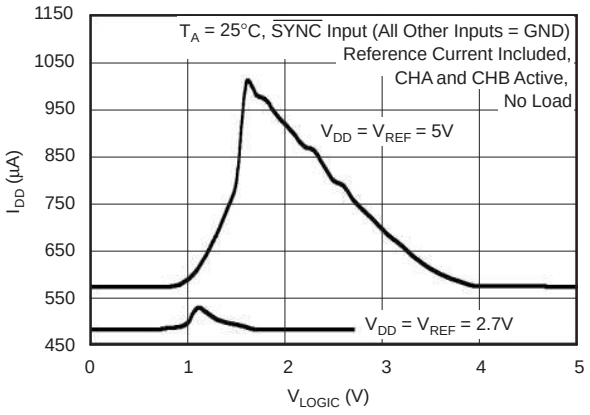



**Figure 20. Supply Current vs Logic Input Voltage**

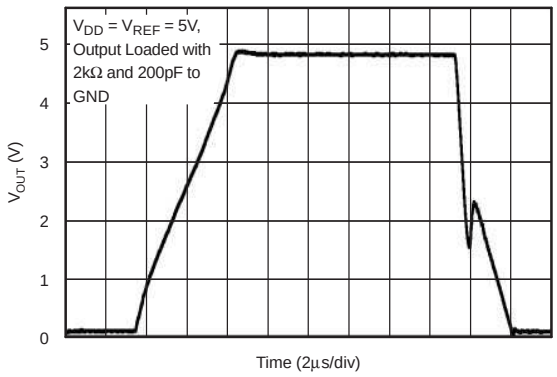



**Figure 21. Full-Scale Settling Time (Large Signal)**

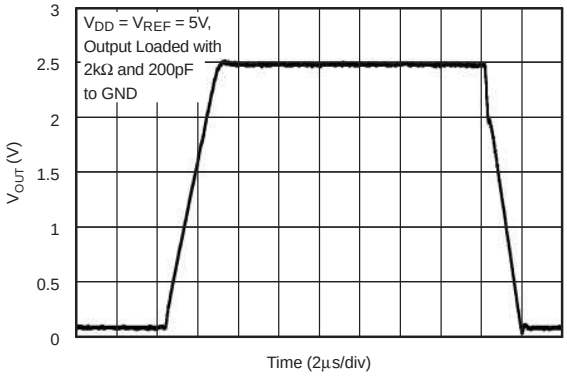



**Figure 22. Half-Scale Settling Time (Large Signal)**

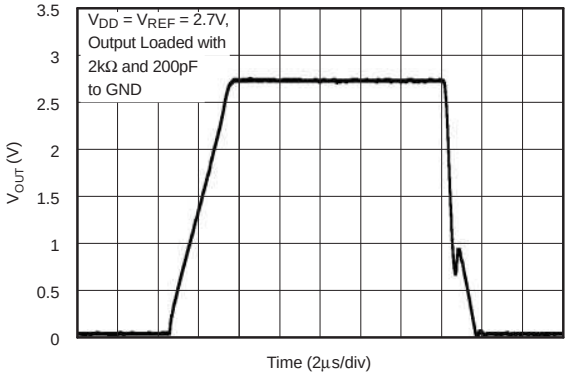



**Figure 23. Full-Scale Settling Time (Large Signal)**

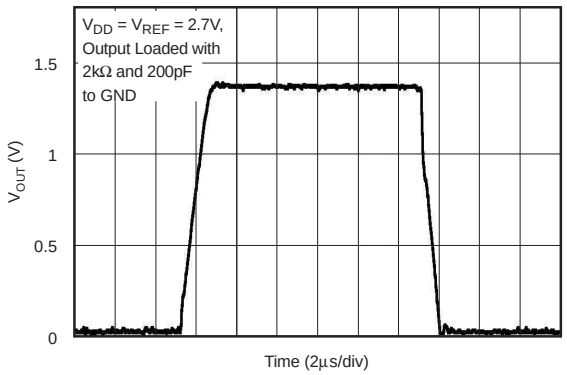



**Figure 24. Half-Scale Settling Time (Large Signal)**

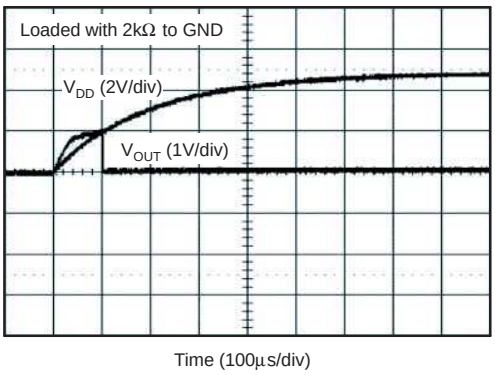



**Figure 25. Power-On Reset to Zero-Scale**

## Typical Characteristics (continued)

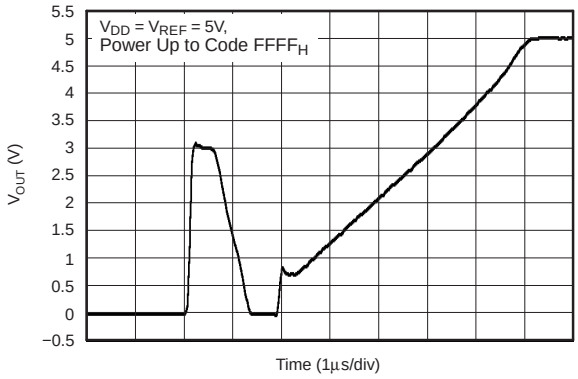



**Figure 26. Exiting Power-Down Mode**

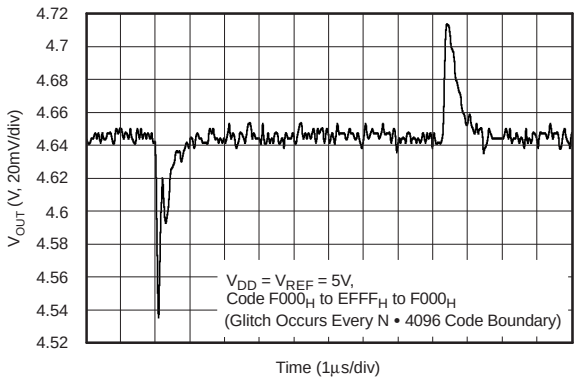



**Figure 27. Output Glitch (Worst Case)**

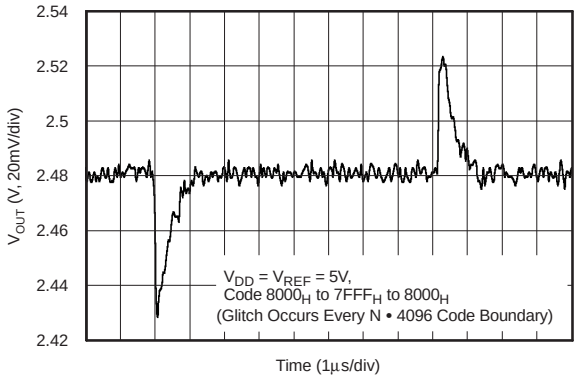



**Figure 28. Output Glitch (Mid-Scale)**

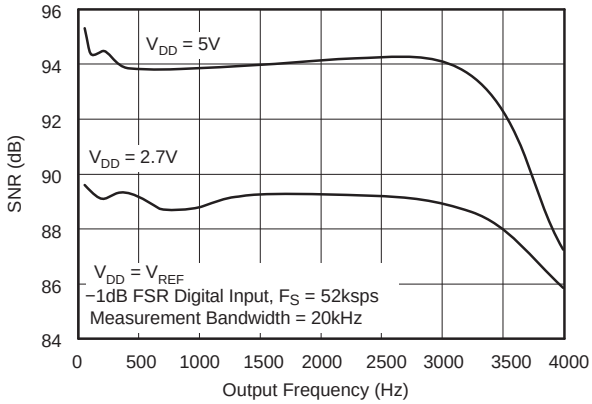



**Figure 29. Signal-to-Noise Ratio vs Output Frequency**

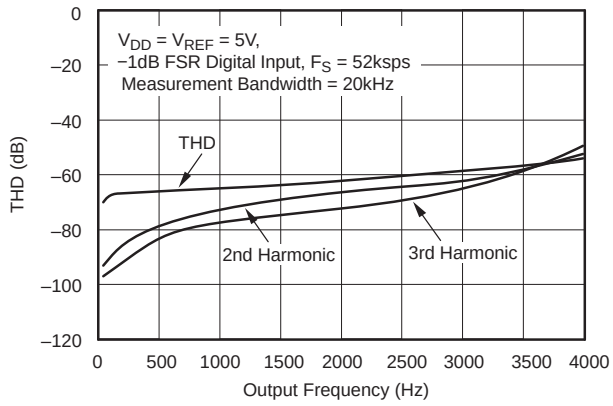


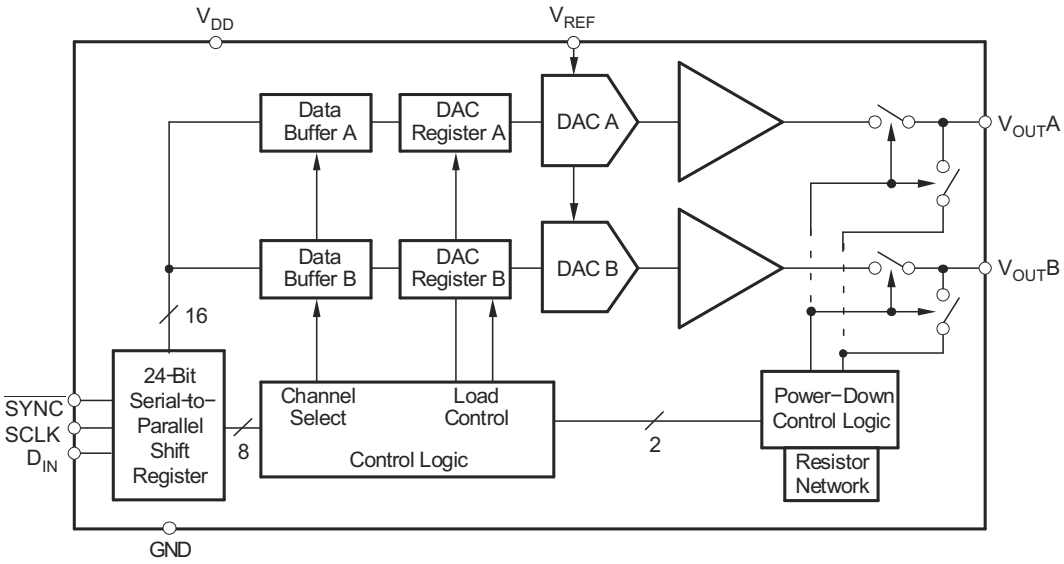

**Figure 30. Total Harmonic Distortion vs Output Frequency**

# 8 Detailed Description

## 8.1 Overview

The DAC8532 is a dual channel, 16-bit digital-to-analog converter (DAC) offering low power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7 V to 5.5 V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30 MHz for $V_{DD}$ = 5 V.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 DAC Section

The architecture of each channel of the DAC8532 consists of a resistor string DAC followed by an output buffer amplifier. Figure 31 shows a simplified block diagram of the DAC architecture.

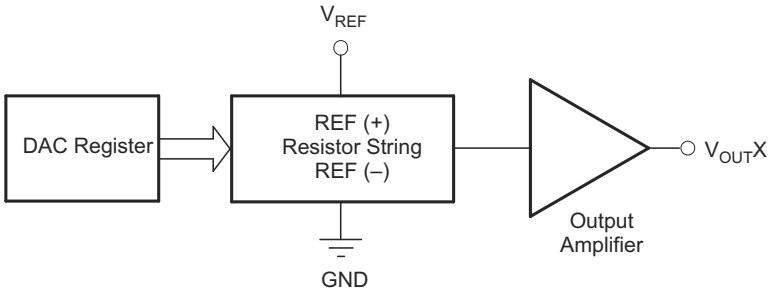



**Figure 31. DAC8532 Architecture**

The input coding for each device is unipolar straight binary, so the ideal output voltage is given by:

$$V_{OUT}X = V_{REF} \times \frac{D}{65536} \quad (1)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535. $V_{OUT}X$ refers to channel A or B.

## Feature Description (continued)

### 8.3.2 Resistor String

The resistor string section is shown in Figure 32. It is simply a divide-by-2 resistor followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. This voltage is then applied to the output amplifier by closing one of the switches connecting the string to the amplifier.

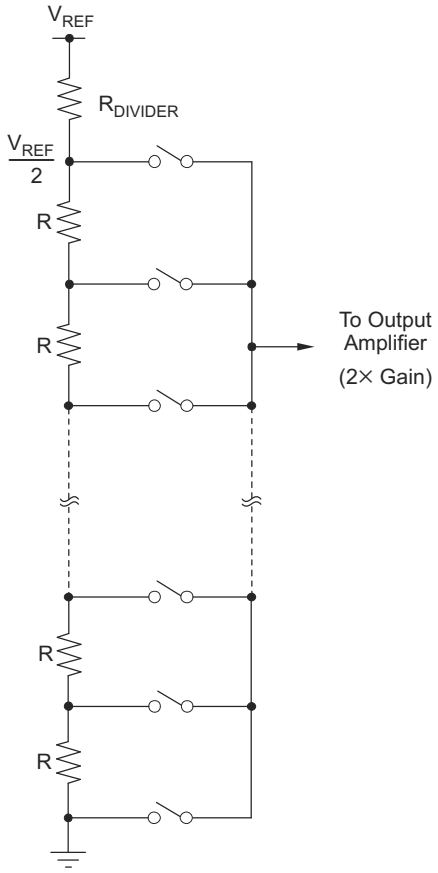



**Figure 32. Resistor String**

### 8.3.3 Output Amplifier

Each output buffer amplifier is capable of generating rail-to-rail voltages on its output which approaches an output range of 0 V to $V_{DD}$ (gain and offset errors must be taken into account). Each buffer is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics.

### 8.3.4 Serial Interface

The DAC8532 uses a 3-wire serial interface ($\overline{SYNC}$, SCLK, and $D_{IN}$), which is compatible with SPI™ and QSP™, and Microwire™ interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the $D_{IN}$ line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the DAC8532 compatible with high speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the programmed function is executed (i.e., a change in Data Buffer contents, DAC register contents, and/or a change in the power-down mode of a specified channel or channels).

## Feature Description (continued)

At this point, the $\overline{\text{SYNC}}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{\text{SYNC}}$ edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the digital input levels are as close to each rail as possible. (See the *Typical Characteristics* section for the *Supply Current vs Logic Input Voltage* transfer characteristic curve).

### 8.3.5 Power-On Reset

The DAC8532 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain there until a valid write sequence and load command is made to the respective DAC channel. This is useful in applications where it is important to know the state of the output of each DAC output while the device is in the process of powering up.

No device pin should be brought high before power is applied to the device.

## 8.4 Device Functional Modes

### 8.4.1 Input Shift Register

The input shift register of the DAC8532 is 24 bits wide (see Figure 33) and is made up of 8 control bits (DB16–DB23) and 16 data bits (DB0–DB15). The first two control bits (DB22 and DB23) are reserved and must be *0* for proper operation. LD A (DB20) and LD B (DB21) control the updating of each analog output with the specified 16-bit data value or power- down command. Bit DB19 is a *Don't Care* bit which does not affect the operation of the DAC8532 and can be 1 or 0. The following control bit, Buffer Select (DB18), controls the destination of the data (or power-down command) between DAC A and DAC B. The final two control bits, PD0 (DB16) and PD1 (DB17), select the power-down mode of one or both of the DAC channels. The four modes are normal mode or any one of three power-down modes. A more complete description of the operational modes of the DAC8532 can be found in the Power-Down Modes section. The remaining sixteen bits of the 24-bit input word make up the data bits. These are transferred to the specified Data Buffer or DAC Register, depending on the command issued by the control byte, on the 24th falling edge of SCLK. See Table 2 and Table 3 for more information.

| **DB23** | | | | | | | | | | | **DB12** |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | LDB | LDA | X | Buffer Select | PD1 | PD0 | D15 | D14 | D13 | D12 |
| **DB11** | | | | | | | | | | | **DB0** |
| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D5 | D3 | D2 | D1 | D0 |

**Figure 33. DAC8532 Data Input Register Format**

### 8.4.2 $\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the addressed DAC register is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register is reset and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents or a change in the operating mode occurs (see Figure 34).

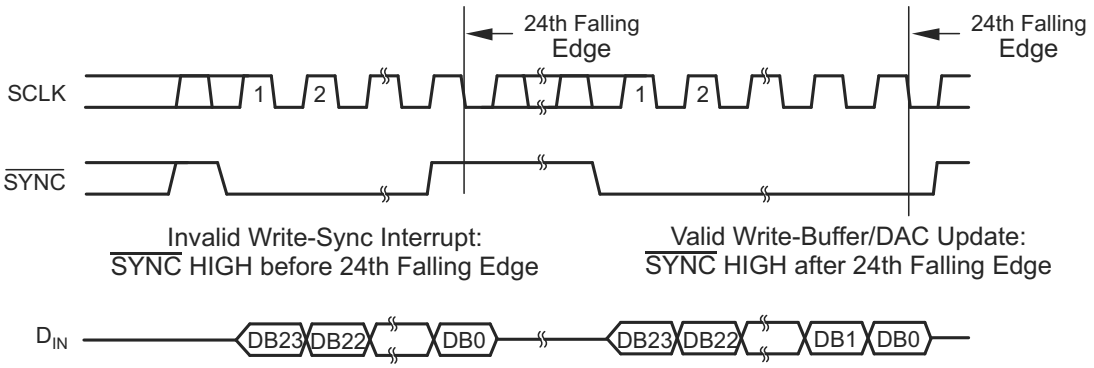



**Figure 34. Interrupt and Valid SYNC Timing**

### 8.4.3 Power-Down Modes

The DAC8532 utilizes four modes of operation. These modes are accessed by setting two bits (PD1 and PD0) in the control *Load* action to one or both DACs. Table 1 shows how the state of the bits correspond to the register and performing a mode of operation of each channel of the device. (Each DAC channel can be powered down simultaneously or independently of each other. Power-down occurs after proper data is written into PD0 and PD1 and a *Load* command occurs.) See the *Operation Examples* section for additional information.

**Table 1. Modes of Operation for the DAC8532**

| PD1 (DB17) | PD0 (DB16) | OPERATING MODE |
|---|---|---|
| 0 | 0 | Normal Operation |
| — | — | Power-down modes |
| 0 | 1 | Output typically 1 kΩ to GND |
| 1 | 0 | Output typically 100 kΩ to GND |
| 1 | 1 | High impedance |

When both bits are set to 0, the device works normally with a typical power consumption of 500 µA at 5 V. For the three power-down modes, however, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options for power-down: The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor, or it is left open-circuited (High-Impedance). The output stage is illustrated in Figure 35.

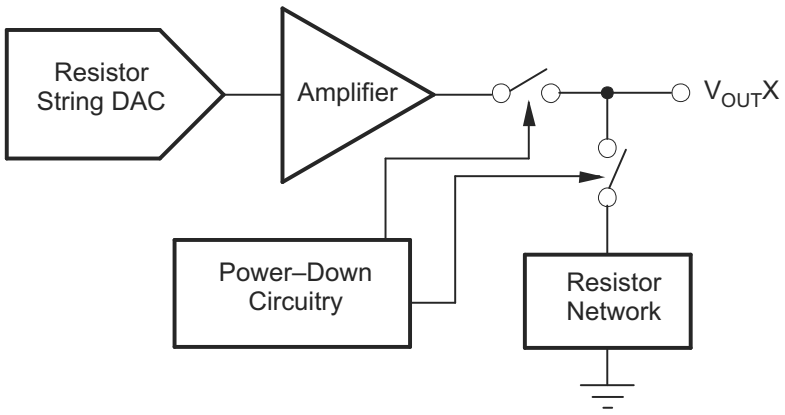



**Figure 35. Output Stage During Power-Down (High Impedance)**

All analog circuitry is shut down when the power-down mode is activated. Each DAC will exit power-down when PD0 and PD1 are set to 0, new data is written to the Data Buffer, and the DAC channel receives a *Load* command. The time to exit power-down is typically 2.5 µs for $V_{DD}$ = 5 V and 5 µs for $V_{DD}$ = 3 V (see the *Typical Characteristics* section.

## 8.5 Register Maps

**Table 2. Control Matrix**

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13–D0 | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Load B | Load A | Don't Care | Buffer Select | PD1 | PD0 | MSB | MSB-1 | MSB-2... LSB | |
| (Always Write 0) | | | | | 0 = A, 1 = B | | | | | | |
| 0 | 0 | 0 | 0 | X | # | 0 | 0 | Data | | | WR Buffer # w/Data |
| 0 | 0 | 0 | 0 | X | # | See Table 3 | | X | | | WR Buffer # w/Power-down Command |
| 0 | 0 | 0 | 1 | X | # | 0 | 0 | Data | | | WR Buffer # w/Data and Load DAC A |
| 0 | 0 | 0 | 1 | X | 0 | See Table 3 | | X | | | WR Buffer A w/Power-Down Command and LOAD DAC A (DAC A Powered Down) |
| 0 | 0 | 0 | 1 | X | 1 | See Table 3 | | X | | | WR Buffer B w/Power-Down Command and LOAD DAC A |
| 0 | 0 | 1 | 0 | X | # | 0 | 0 | Data | | | WR Buffer # w/Data and Load DAC B |
| 0 | 0 | 1 | 0 | X | 0 | See Table 3 | | X | | | WR Buffer A w/Power-Down Command and LOAD DAC B |
| 0 | 0 | 1 | 0 | X | 1 | See Table 3 | | X | | | WR Buffer B w/Power-Down Command and LOAD DAC B (DAC B Powered Down) |
| 0 | 0 | 1 | 1 | X | # | 0 | 0 | Data | | | WR Buffer # w/Data and Load DACs A and B |
| 0 | 0 | 1 | 1 | X | 0 | See Table 3 | | X | | | WR Buffer A w/Power-Down Command and Load DACs A and B (DAC A Powered Down) |
| 0 | 0 | 1 | 1 | X | 1 | See Table 3 | | X | | | WR Buffer B w/Power-Down Command and Load DACs A and B (DAC B Powered Down) |

**Table 3. Power-Down Commands**

| D17 | D16 | OUTPUT IMPEDANCE POWER DOWN COMMANDS |
|---|---|---|
| PD1 | PD0 | |
| 0 | 1 | 1 kΩ |
| 1 | 0 | 100 kΩ |
| 1 | 1 | High Impedance |

### 8.5.1 Operation Examples

**Example 1: Write to Data Buffer A; Through Buffer B; Load DACA Through DACB Simultaneously**

- 1st — Write to DataBuffer A:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | D15 | — | D1 | D0 |

- 2nd — Write to Data Buffer B and Load DAC A and DAC B simultaneously:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | X | 1 | 0 | 0 | D15 | — | D1 | D0 |

The DACA and DACB analog outputs simultaneously settle to the specified values upon completion of the 2nd write sequence. (The *Load* command moves the digital data from the data buffer to the DAC register at which time the conversion takes place and the analog output is updated. *Completion* occurs on the 24th falling SCLK edge after $\overline{\text{SYNC}}$ LOW.)

**Example 2: Load New Data to DACA and DACB Sequentially**

- 1st — Write to Data Buffer A and Load DAC A: DACA output settles to specified value upon completion:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | X | 0 | 0 | 0 | D15 | — | D1 | D0 |

- 2nd — Write to Data Buffer B and Load DAC B: DACB output settles to specified value upon completion:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | X | 1 | 0 | 0 | D15 | — | D1 | D0 |

After completion of the 1st write cycle, the DACA analog output settles to the voltage specified; upon completion of write cycle 2, the DACB analog output settles.

**Example 3: Power-Down DACA to 1 kΩ and Power-Down DACB to 100 kΩ Simultaneously**

- 1st — Write power-down command to Data Buffer A:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | 0 | 0 | 1 | Don't Care | | | |

- 2nd — Write power-down command to Data Buffer B and Load DACA and DACB simultaneously:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | X | 1 | 1 | 0 | Don't Care | | | |

The DACA and DACB analog outputs simultaneously power-down to each respective specified mode upon completion of the 2nd write sequence.

**Example 4: Power-Down DACA and DACB to High-Impedance Sequentially:**

- 1st — Write power-down command to Data Buffer A and Load DAC A: DAC A output = Hi-Z:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | X | 0 | 1 | 1 | Don't Care | | | |

- 2nd — Write power-down command to Data Buffer B and Load DAC B: DAC B output = Hi-Z:

| Reserved | Reserved | LDB | LDA | DC | Buffer Select | PD1 | PD0 | DB15 | — | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | X | 1 | 1 | 1 | Don't Care | | | |

The DACA and DACB analog outputs sequentially power-down to high-impedance upon completion of the 1st and 2nd write sequences, respectively.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Current Consumption

The DAC8532 typically consumes 250 µA at $V_{DD}$ = 5 V and 225 µA at $V_{DD}$ = 3 V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if $V_{IH}$<<$V_{DD}$. For most efficient power operation, CMOS logic levels are recommended at the digital input to the DAC.

In power-down mode, typical current consumption is 200 nA. A delay time of 10 to 20 ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10 µA.

### 9.1.2 Driving Resistive and Capacitive Loads

The DAC8532 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC8532 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2 kΩ can be driven by the DAC8532 while achieving a typical load regulation of 1%. As the load resistance drops below 2 kΩ, the load regulation error increases. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20 mV of the DAC's digital input-to-voltage output transfer characteristic. The reference voltage applied to the DAC8532 may be reduced below the supply voltage applied to $V_{DD}$ in order to eliminate this condition if good linearity is a requirement at full scale (under resistive loading conditions).

### 9.1.3 Crosstalk and AC Performance

The DAC8532 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.5LSBs. The AC crosstalk measured (for a full-scale, 1 kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under –100 dB, In addition, the DAC8532 can achieve typical AC performance of 96 dB signal-to-noise ratio (SNR) and 65 dB total harmonic distortion (THD), making the DAC8532 a solid choice for applications requiring low SNR at output frequencies at or below 4 kHz.

### 9.1.4 Output Voltage Stability

The DAC8532 exhibits excellent temperature stability of 5 ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a ±25 µV window for a ±1°C ambient temperature change. Good power-supply rejection ratio (PSRR) performance reduces supply noise present on $V_{DD}$ from appearing at the outputs to well below 10 µV-s. Combined with good DC noise performance and true 16-bit differential linearity, the DAC8532 becomes a perfect choice for closed-loop control applications.

### 9.1.5 Settling Time and Output Glitch Performance

Settling time to within the 16-bit accurate range of the DAC8532 is achievable within 10 µs for a full-scale code change at the input. Worst case settling times between consecutive code changes is typically less than 2 µs, enabling update rates up to 500 ksps for digital input signals changing code-to-code. The high-speed serial interface of the DAC8532 is designed in order to support these high update rates.

## Application Information (continued)

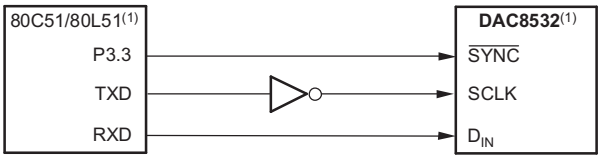
For full-scale output swings, the output stage of each DAC8532 channel typically exhibits less than 100 mV of overshoot and undershoot when driving a 200 pF capacitive load. Code-to-code change glitches are extremely low (~10 µV) given that the code-to-code transition does not cross an Nx4096 code boundary. Due to internal segmentation of the DAC8532, code-to-code glitches occur at each crossing of an Nx4096 code boundary. These glitches can approach 100 mVs for N = 15, but settle out within ~2 µs.

### 9.1.6 Microprocessor Interfacing

The following sections describe interfacing the DAC8532 with various microprocessors.

#### *9.1.6.1 DAC8532 to 8051 Interface*

Figure 36 shows a serial interface between the DAC8532 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8532, while RXD drives the serial data line of the device. The $\overline{SYNC}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8532, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second and third write cycle is initiated to transmit the remaining data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which presents the LSB first, while the DAC8532 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed

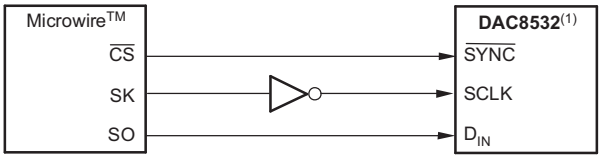



NOTE: (1) Additional pins omitted for clarity.

**Figure 36. DAC8532 to 80C51/80L51 Interface**

#### *9.1.6.2 DAC8532 to Microwire Interface*

Figure 37 shows an interface between the DAC8532 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8532 on the rising edge of the SK signal.




NOTE: (1) Additional pins omitted for clarity.

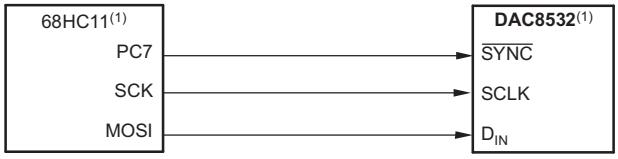
Microwire is a trademark of Texas Instruments

**Figure 37. DAC8532 to Microwire Interface**

#### *9.1.6.3 DAC8532 to 68HC11 Interface*

Figure 38 shows a serial interface between the DAC8532 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8532, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7), similar to the 8051 diagram.

## Application Information (continued)




NOTE: (1) Additional pins omitted for clarity.

**Figure 38. DAC8532 to 68HC11 Interface**

The 68HC11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data is being transmitted to the DAC, the SYNC line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8532, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.

### 9.1.7 DAC8532 to TMS320 DSP Interface

Figure 39 shows the connections between the DAC8532 and a TMS320 digital signal processor. By decoding the FSX signal, multiple DAC8532s can be connected to a single serial port of the DSP.

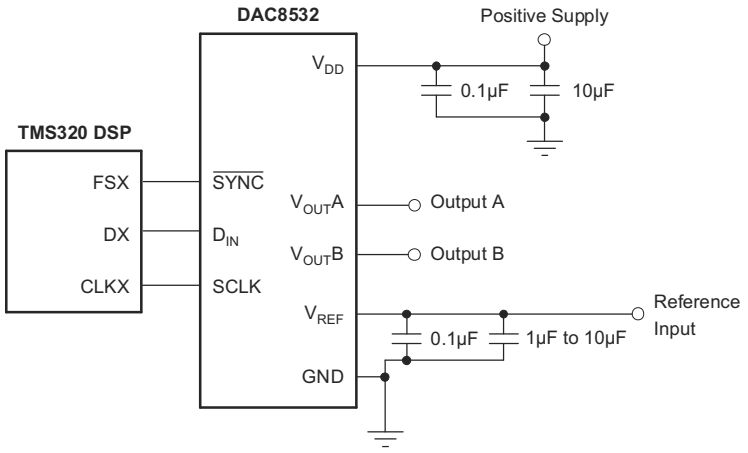
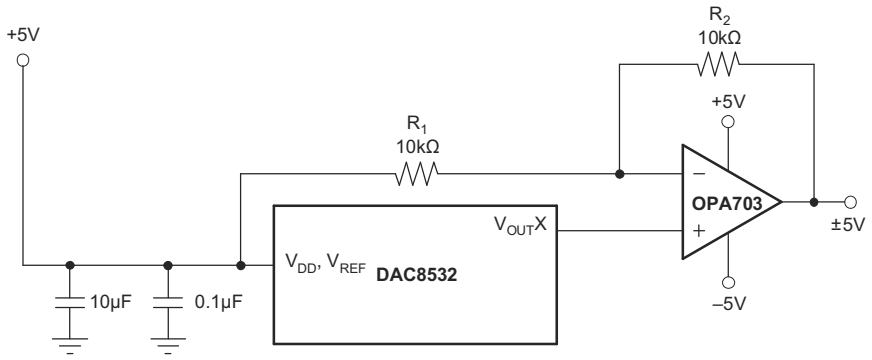



**Figure 39. DAC8532 to TMS320 DSP**

### 9.1.8 Bipolar Operation Using the DAC8532




(Other pins omitted for clarity)

**Figure 40. Bipolar Operation with the DAC8532**

## Application Information (continued)

The DAC8532 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 40. The circuit shown will give an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an amplifier such as the OPA703, see Figure 40.

The output voltage for any input code can be calculated as follows:

$$V_{OUT}X = \left[ V_{REF} \times \left( \frac{D}{65536} \right) \times \left( \frac{R1+R2}{R1} \right) - V_{REF} \times \left( \frac{R2}{R1} \right) \right] \quad (2)$$

where D represents the input code in decimal (0–65535).

With $V_{REF}$ = 5 V, R1 - R2 = 10 kΩ.

$$V_{OUT}X = \left( \frac{10 \times D}{65536} \right) - 5\ V \quad (3)$$

This is an output voltage range of ±5 V with $0000_H$ corresponding to a –5 V output and $FFFF_H$ corresponding to a 5 V output. Similarly, using $V_{REF}$ = 2.5 V, a ±2.5 V output voltage range can be achieved.

## 9.2 Typical Application

### 9.2.1 Using REF5050 as a Power Supply for DAC8532

Due to the extremely low supply current required by the DAC8532, a possible configuration is to use the REF5050, a 5 V precision voltage reference, as the power supply and the reference for the DAC8532 . This configuration is shown in Figure 41. This is especially useful if the power supply is noisy or if 5 V is not readily available as the system supply. This configuration has the drawback of not being able to reach full scale voltage. The output buffer of the DAC requires headroom between the power supply and the reference to generate an output voltage near the reference voltage without distortion or clipping.

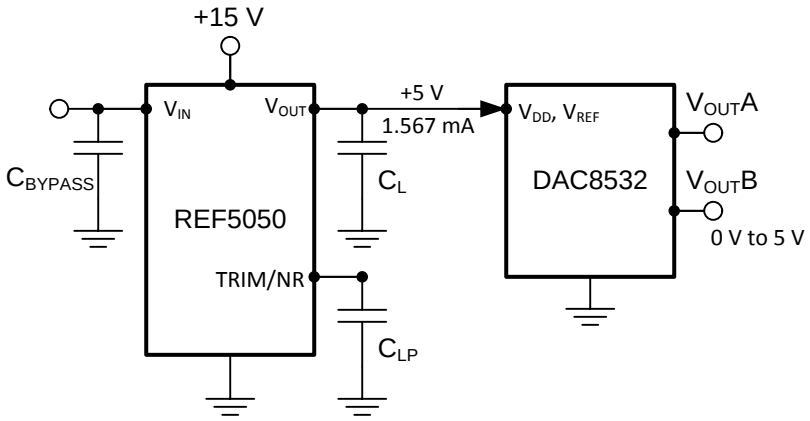



**Figure 41. REF5050 as a Power Supply to the DAC8532**

#### *9.2.1.1 Design Requirements*

The REF5050 requires three capacitors for operation:

1. A supply bypass capacitor ($C_{BYPASS}$) ranging between 1 µF and 10 µF must be connected between the REF5050 $V_{IN}$ and GND pins.
2. A 1 µF to 50 µF output load capacitor ($C_L$) must be connected between the REF5050 $V_{OUT}$ and GND pins. The ESR of $C_L$ must be less than or equal to 1.5Ω to ensure output stability and to minimize noise.
3. A 1µF filter capacitor ($C_{LP}$) must be connected between TRIM/NR and GND pins. $C_{LP}$ forms a low pass filter with a cut-off frequency between 10 Hz and 20 Hz. This filter reduces the noise injected by the reference. Note that the use of this capacitor will increase the startup time.

## Typical Application (continued)

The REF5050 outputs a steady supply voltage for the DAC8532. If the REF5050 is used, the current supplied to the DAC8532 is 567 µA typical and 890 µA max for $V_{DD}$ = 5 V. When a DAC output is loaded, the REF5050 also needs to supply the current to the load. The total typical current required (with a 5 kΩ load on a given DAC output) is:

567 µA + (5 V ÷ 5 kΩ) = 1.567 mA (4)

The load regulation of the REF5050 is typically 0.005 %/mA, which results in an error of 392 µV for the 1.5 mA current drawn from it. This corresponds to a 5.13 LSB error for a 0 V to 5 V output range.

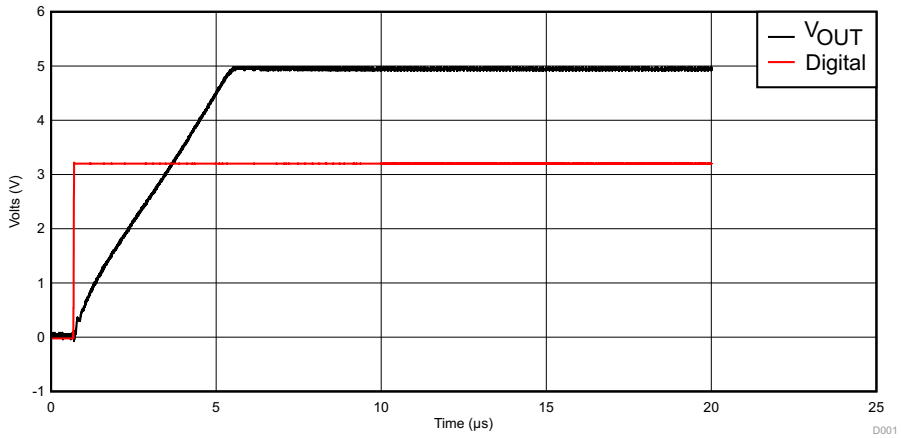
### *9.2.1.2 Detailed Design Procedure*

The REF5050 outputs a steady supply voltage for the DAC8532. The max current consumption of DAC8532 without a resistive load on the output pin is 890 µA. If the DAC outputs are loaded, the reference must also supply the current to the DAC loads. For example, the total max current required (with a 2 kΩ load on each DAC output) is:

Imax = 890 µA + 2 × (5 V ÷ 2 kΩ) = 5.89 mA (5)

The REF5050 output voltage change at room temperature with a 6 mA load is 100 µV. This causes a 0.002 %FSR change on the supply; this is sufficiently small to not affect the performance of the DAC.

### *9.2.1.3 Application Curves*




Input Reference Voltage = 4.991250 V
Full Scale Voltage = 4.996820 V @ 0xFFFF
Zero Scale Voltage = 0.014349 V @ 0x0000
Full Scale Settling time = 4.86 µs

**Figure 42. Settling Time**

# 10 Power Supply Recommendations

The DAC8532 is designed to operate with a unipolar analog power supply ranging from 2.7 V to 5.5 V on pin VDD. This pin supplies power to digital and analog circuits inside the DAC8532. The current consumption of this pin is specified in the *Electrical Characteristics* table. A 1 µF to 10 µF capacitor in parallel with a 0.1 µF bypass capacitor is strongly recommended on this pin to remove high frequency noise.

# 11 Layout

## 11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

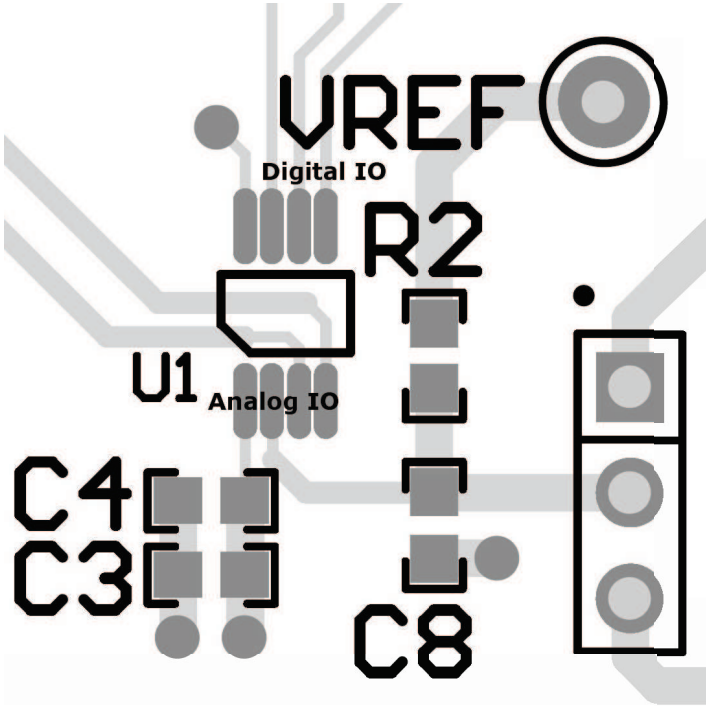
The DAC8532 offers single-supply operation, and it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8532, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to $V_{DD}$ should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, $V_{DD}$ should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, a 1 µF to 10 µF capacitor in parallel with a 0.1 µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100 µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to low-pass filter the supply, removing the high-frequency noise.

### 11.2 Layout Example




Fast moving transients common in digital IO can cause digital feed-through on the analog outputs. Route analog IO traces away from any digital IO traces in order to minimize digital feed-through.

**Figure 43. Layout Example**

## 12 Device and Documentation Support

### 12.1 Trademarks

Microwire is a trademark of Texas Instruments.
SPI, QSP are trademarks of Motorola.
All other trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DAC8532IDGK | Active | Production | VSSOP (DGK) \| 8 | 80 \| TUBE | Yes | Call TI \| Nipdauag | Level-2-260C-1 YEAR | -40 to 105 | D32E |
| DAC8532IDGK.B | Active | Production | VSSOP (DGK) \| 8 | 80 \| TUBE | Yes | Call TI | Level-2-260C-1 YEAR | -40 to 105 | D32E |
| DAC8532IDGKG4 | Active | Production | VSSOP (DGK) \| 8 | 80 \| TUBE | Yes | Call TI | Level-2-260C-1 YEAR | -40 to 105 | D32E |
| DAC8532IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | Call TI \| Nipdauag | Level-2-260C-1 YEAR | -40 to 105 | D32E |
| DAC8532IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | Call TI | Level-2-260C-1 YEAR | -40 to 105 | D32E |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

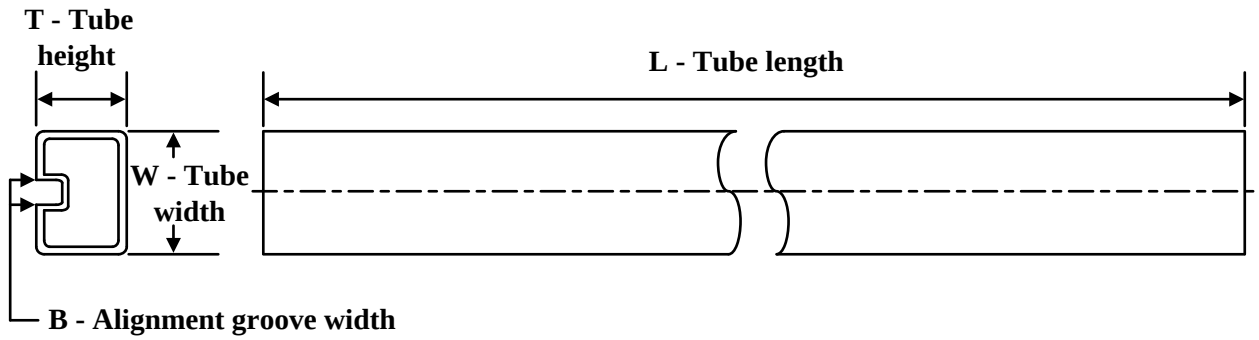
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# PACKAGE MATERIALS INFORMATION

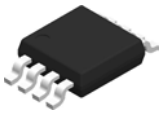


## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| DAC8532IDGK | DGK | VSSOP | 8 | 80 | 331.47 | 6.55 | 3000 | 2.88 |
| DAC8532IDGK.B | DGK | VSSOP | 8 | 80 | 331.47 | 6.55 | 3000 | 2.88 |
| DAC8532IDGKG4 | DGK | VSSOP | 8 | 80 | 331.47 | 6.55 | 3000 | 2.88 |

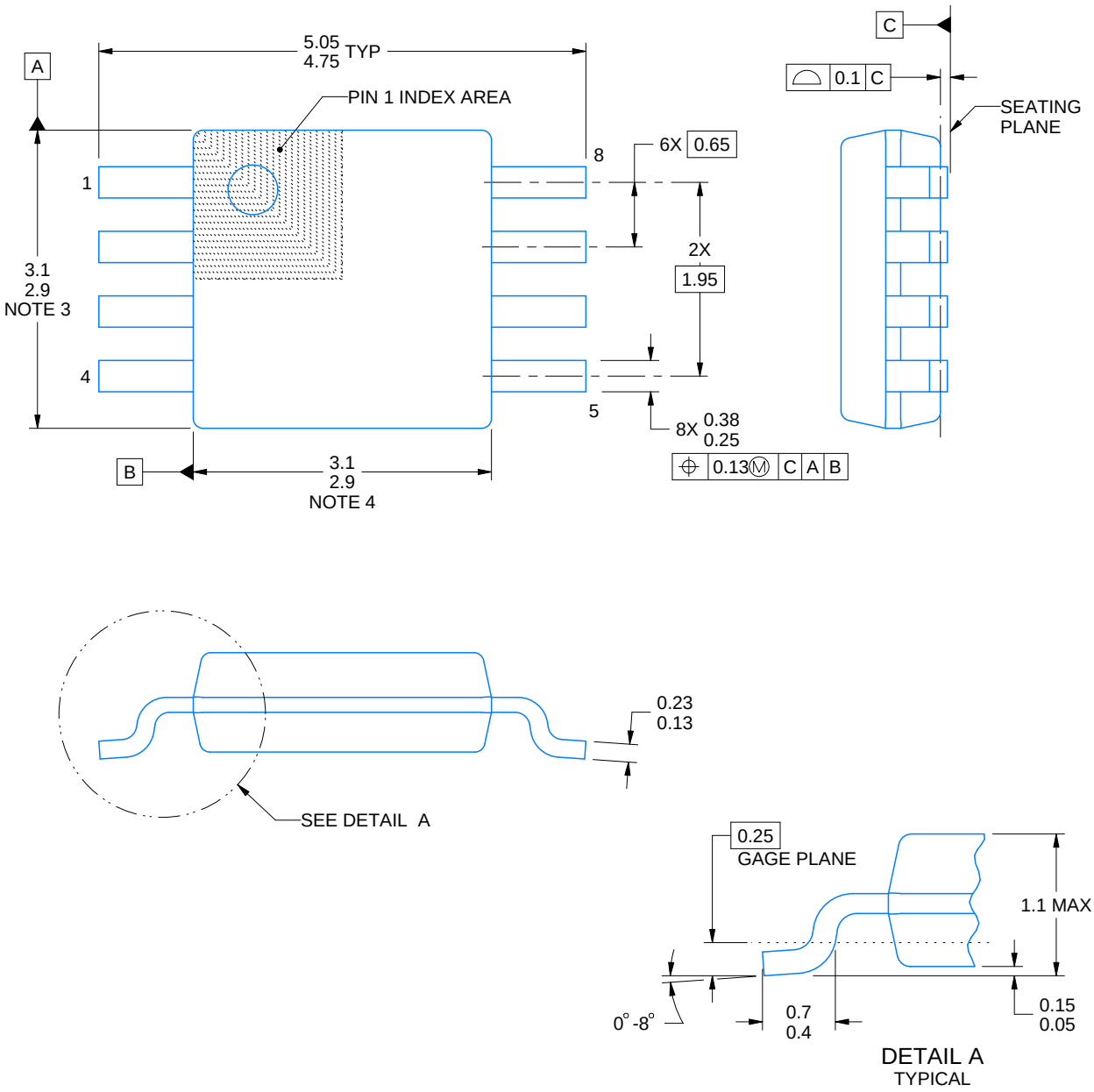


# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




PowerPAD is a trademark of Texas Instruments.

NOTES:

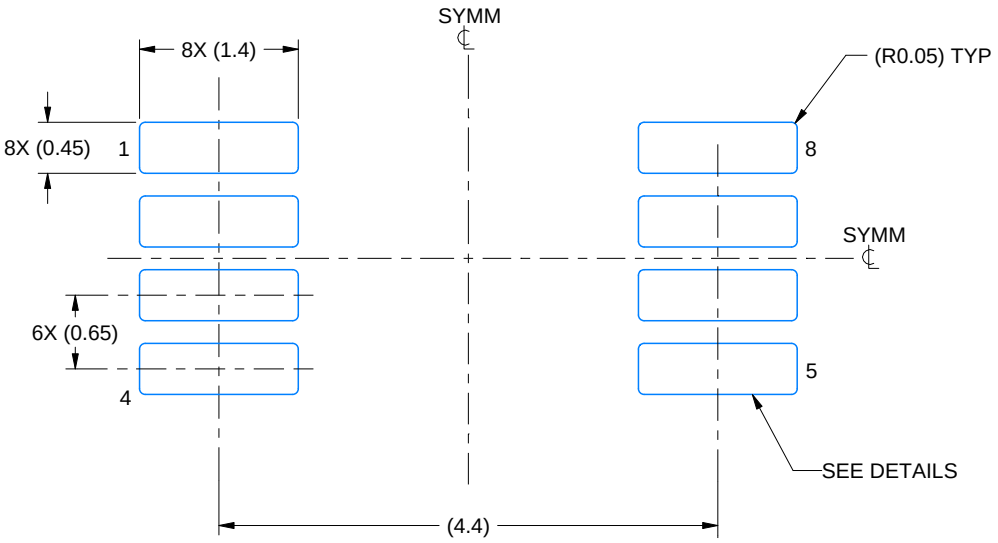
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

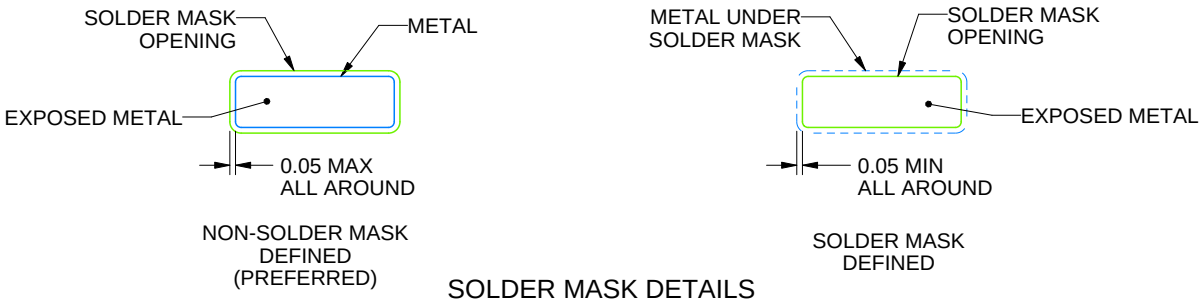
## DGK0008A

## ™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

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NOTES: (continued)

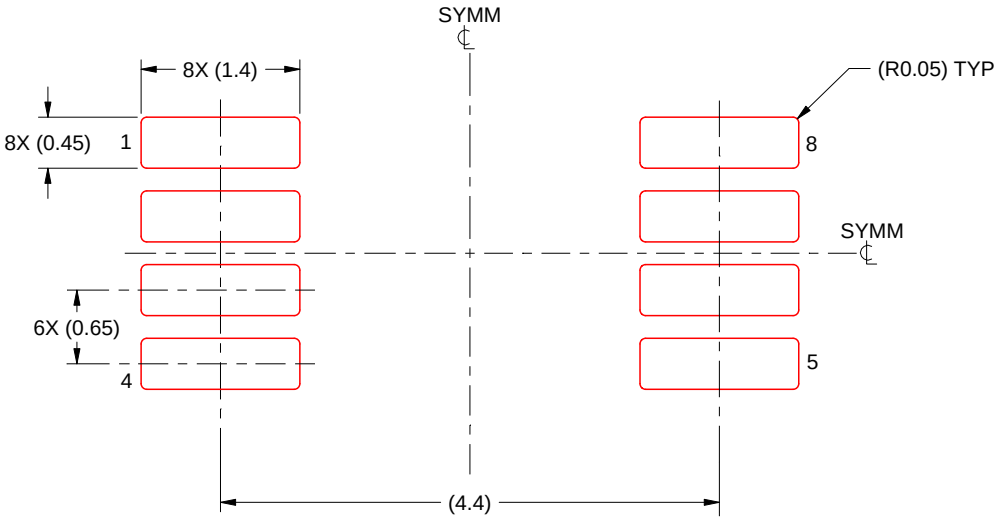
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

## DGK0008A

## ™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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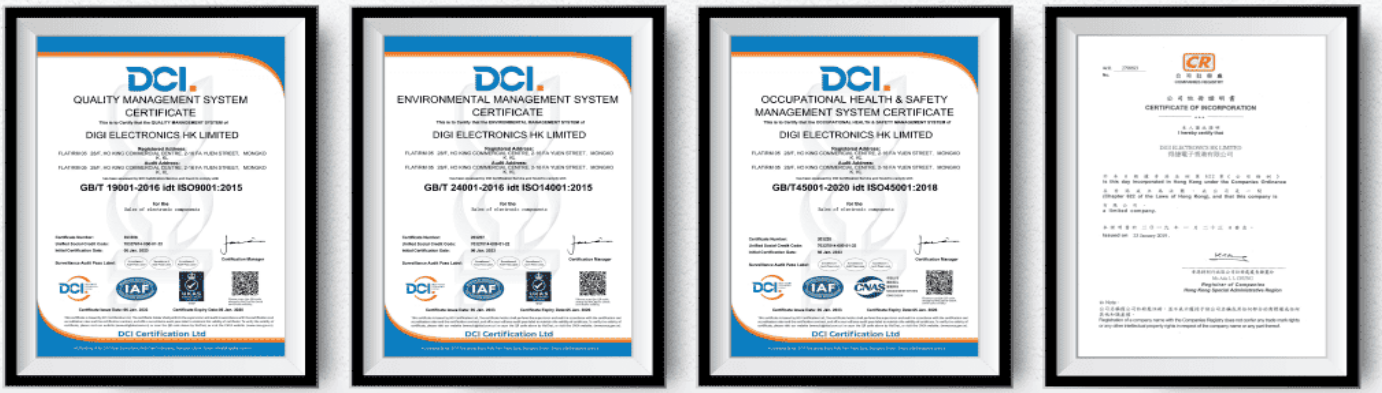



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