

DS1776E/883 Datasheet



DiGi Electronics Part Number	DS1776E/883-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	DS1776E/883
Description	IC TRANSCEIVER HALF 8/8 28LCCC
Detailed Description	8/8 Transceiver Half 28-LCCC (11.43x11.43)

<https://www.DiGi-Electronics.com>



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

DS1776E/883

Series:

DS1776QML

Type:

Transceiver

Number of Drivers/Receivers:

8/8

Data Rate:

-

Operating Temperature:

-55°C ~ 125°C (TA)

Package / Case:

28-CLCC

Manufacturer:

Texas Instruments

Product Status:

Active

Protocol:

-

Duplex:

Half

Voltage - Supply:

4.5V ~ 5.5V

Mounting Type:

Surface Mount

Supplier Device Package:

28-LCCC (11.43x11.43)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

Moisture Sensitivity Level (MSL):

1 (Unlimited)

DS1776QML Pi-Bus Transceiver

1 Features

- Similar to BTL
- Low Power $I_{CCL} = 41 \text{ mA max}$
- B Output Controlled Ramp Rate
- B Input Noise Immunity, Typically 4 ns
- Pin and Function Compatible with Signetics 54F776

2 Description

The DS1776 is an octal PI-bus Transceiver. The A to B path is latched. B outputs are open collector with series Schottky diode, ensuring minimum B output loading. B outputs also have ramped rise and fall times (2.5 ns typical), ensuring minimum PI-bus ringing. B inputs have glitch rejection circuitry, 4 ns typical.

Designed using Texas Instruments's Bi-CMOS process for both low operating and disabled power. AC performance is optimized for the PI-Bus interoperability requirements.

The DS1776 is an octal latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. This bus has a loaded characteristic impedance range of 20Ω to 50Ω and is terminated on each end with a 30Ω to 40Ω resistor.

The DS1776 is an octal bidirectional transceiver with open collector B and TRI-STATE A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2V and features a controlled linear ramp to minimize crosstalk and ringing on the bus.

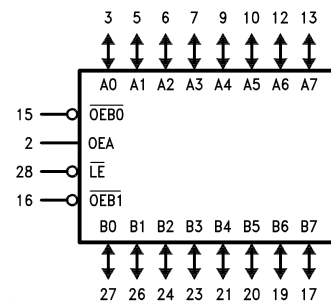
A separate high level control voltage (V_X) is provided to prevent the A side output high level from exceeding future high density processor supply voltage levels. For 5V systems, V_X is tied to V_{CC} .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS1776QML	LCCC (FK)	11.43 mm x 11.43 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Symbol



DS1776QML

SNOSC82B –AUGUST 2012–REVISED JUNE 2015

www.ti.com**Table of Contents**

1 Features	1	5.8 Pi Bus Transceiver DS1776 AC Parameters: A To B Path	7
2 Description	1	5.9 Pi Bus Transceiver DS1776 AC Parameters: Setup / Hold / Pulse Width Specifications	7
3 Revision History	2	5.10 Test Circuit And Waveforms	8
4 Pin Configuration and Functions	3	6 Detailed Description	10
5 Specifications	4	6.1 Controller Power Sequencing Operation	11
5.1 Absolute Maximum Ratings	4	7 Device and Documentation Support	12
5.2 ESD Ratings	4	7.1 Community Resources.....	12
5.3 Recommend Operating Conditions.....	4	7.2 Trademarks	12
5.4 Thermal Information	4	7.3 Electrostatic Discharge Caution.....	12
5.5 Quality Conformance Inspection.....	5	7.4 Glossary.....	12
5.6 Pi Bus Transceiver DS1776 DC Parameters.....	5	8 Mechanical, Packaging, and Orderable Information	12
5.7 Pi Bus Transceiver DS1776 AC Parameters: B To A Path	6		

3 Revision History

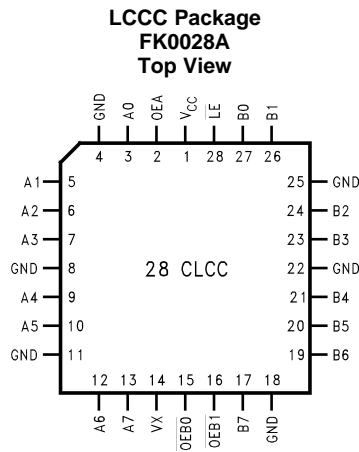
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B**Page**

• Deleted product preview	1
• Changed moved to new TI format	1

Released	Revision	Section	Changes
30-Jul-2012	A1	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. MNDS1776-X Rev 2A0. will be archived.
12-Apr-2013	A	All	Changed layout of National Data Sheet to TI format.

4 Pin Configuration and Functions



Pin Descriptions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	3	I/O	TTL Level, latched input/TRI-STATE output (with V_X control option)
A1	5	I/O	
A2	6	I/O	
A3	7	I/O	
A4	9	I/O	
A5	10	I/O	
A6	12	I/O	
A7	13	I/O	Data input with special threshold circuitry to reject noise/Open Collector output, High current drive
B0	27	I/O	
B1	26	I/O	
B2	24	I/O	
B3	23	I/O	
B4	21	I/O	
B5	20	I/O	
B6	19	I/O	Enables the B outputs when both pins are low
$\overline{OE}0$	15	I	
$\overline{OE}1$	16	I	Enables the A outputs when High
OEA	2	I	
\overline{LE}	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

DS1776QML

SNOSC82B –AUGUST 2012–REVISED JUNE 2015

www.ti.com

5 Specifications**5.1 Absolute Maximum Ratings⁽¹⁾**

	MIN	MAX	UNIT	
Supply Voltage (V_{CC})	-0.5	7.0	V	
V_X , V_{OH} Output Level Control Voltage (A Outputs)	-0.5	7.0	V	
\overline{OEBn} , OEA, \overline{LE} Input Voltage (V_I)	-0.5	7.0	V	
A0–A7, B0–B7 Input Voltage (V_I)	-0.5	5.5	V	
Input Current (I_I)	-40	5	mA	
Voltage Applied to Output in High Output State (V_O)	-0.5V	+ V_{CC}		
A0–A7 Current Applied to Output in Low Output State (I_O)	40	40	mA	
B0–B7 Current Applied to Output in Low Output State (I_O)	200	200	mA	
Lead Temperature (Soldering 10 Sec.)		260	°C	
Power Dissipation ⁽²⁾		740	mW	
Storage temperature	T_{stg}	-65	+150	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specified specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

5.2 ESD Ratings

	MIN	MAX	UNIT
$V_{(ESD)}$ Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ^{(1) (2)}	500		V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) $C_{Zap} = 120$ pF, $R_{Zap} = 1500\Omega$

5.3 Recommend Operating Conditions

	MIN	MAX	UNIT
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Temp. Range (T_A)	-55	+125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DS1776QML	UNIT
		FK0028A	
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	+67.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	See MIL-STD-1835	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

5.6 Pi Bus Transceiver DS1776 DC Parameters

The following conditions apply, unless otherwise specified. $V_{CC} = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
V_{IL2}	Low Level In Voltage Bn	$V_{CC} = 4.5$	See ⁽¹⁾	1.45		V	1, 2, 3
V_{IL1}	All Other Inputs	$V_{CC} = 4.5$.8		V	1, 2, 3
V_{IH1}	Hi Level Input Voltage \overline{OEBn} , OEA, An, LE		See ⁽¹⁾	2.0		V	1, 2, 3
V_{IH2}	High Level In Voltage B0-B7			1.6		V	1, 2, 3
I_{OH1}	High Level Output Current An	$V_{CC} = 4.5, V_{IN} = V_{IH}$ or V_{IL} , $V_{OH} = 2.5V$	See ⁽²⁾		-3.0	mA	1, 2, 3
I_{OH2}	High Level Output Current Bn	$V_{CC} = 5.5, V_{IL} = 0.8V$, $V_{IH} = 2.0V, V_{OH} = 2.1V$		100		μA	1, 2, 3
I_{OL1}	Low Level Output Current An	$V_{CC} = 4.5, V_{IN} = V_{IH}$ or V_{IL} , $V_{OL} = 0.5V$	See ⁽³⁾	20		mA	1, 2, 3
I_{OL2}	Low Level Output Current Bn	$V_{CC} = 4.5, V_{IN} = V_{IH}$ or V_{IL} , $V_{OL} = 1.15V$		100		mA	1, 2, 3
V_{OH}	High Level Output Voltage An	$V_{CC} = 4.5, V_{IN} = V_{IL}$ or V_{IH} , $I_{OH} = -3$ mA, $V_X = 4.5V$		2.5	4.5	V	1, 2, 3
		$V_{CC} = 4.5, V_{IN} = V_{IL}$ or V_{IH} , $I_{OH} = -0.4$ mA, $V_X = 3.13$ to $3.47V$		2.5	V_X	V	1, 2, 3
V_{OL}	Low Level Output Voltage An	$V_{CC} = 4.5, V_{IL} = \text{Max}$, $V_{IH} = \text{Min}, I_{OL} = 20\text{mA}$, $V_X = V_{CC}$		0.5		V	1, 2, 3
V_{OLB}	Low Level Output Voltage Bn	$V_{CC} = 4.5, V_{IL} = \text{Max}$, $V_{IH} = \text{Min}, I_{OL} = 100\text{mA}$		1.15		V	1, 2, 3
		$V_{CC} = 4.5, V_{IL} = \text{Max}$, $V_{IH} = \text{Min}, I_{OL} = 4\text{mA}$		0.4		V	1, 2, 3
V_{IK}	Input Clamp Voltage An	$V_{CC} = 4.5, I_I = -40\text{mA}$			-0.5	V	1, 2, 3
V_{IK}	Input Clamp Voltage Other Inputs	$V_{CC} = 4.5, I_I = -18\text{mA}$			-1.2	V	1, 2, 3

(1) Tested Go-No-Go

(2) Same as V_{OH} test.

(3) Same as V_{OL} test.

DS1776QML

SNOSC82B – AUGUST 2012 – REVISED JUNE 2015

www.ti.com

Pi Bus Transceiver DS1776 DC Parameters (continued)The following conditions apply, unless otherwise specified. $V_{CC} = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS	
I_{IH1}	Input Current Max Input Voltage $\overline{OE}Bn$, OEA, \overline{LE}	$V_{CC} = 5.5, V_I = 7.0V$			100	μA	1, 2, 3	
I_{IH2}	Input Current Max Input Voltage An, Bn	$V_{CC} = 5.5, V_I = 5.5V$			1.0	mA	1, 2, 3	
I_{IH3}	High Level Input Current $\overline{OE}Bn$, OEA, \overline{LE}	$V_{CC} = 5.5, V_I = 2.7V$			20	μA	1, 2, 3	
I_{IH4}	High Level Input Current Bn	$V_{CC} = 5.5, V_I = 2.1V$			100	μA	1, 2, 3	
I_{IL1}	Low Level Input Current $\overline{OE}Bn$, OEA, Except $\overline{OE}Bn$ or OEA	$V_{CC} = 5.5, V_I = 0.5V$			-20	μA	1, 2, 3	
I_{IL2}	Low Level Input Current \overline{LE}	$V_{CC} = 5.5, V_I = 0.5V$			-20	μA	1	
					-40	μA	2, 3	
I_{IL3}	Low Level Input Current Bn	$V_{CC} = 5.5, V_I = 0.3V$			-100	μA	1, 2, 3	
$I_{OZH} + I_{IH}$	TRI-STATE Output Current, High Level Voltage Applied An	$V_{CC} = 5.5, V_O = 2.7V$			70	μA	1, 2, 3	
$I_{OZL} + I_{IL}$	TRI-STATE Output Current, Low Level Voltage Applied An	$V_{CC} = 5.5, V_O = 0.5V$			-70	μA	1, 2, 3	
I_X	High Level Control Current	$V_{CC} = 5.5, V_X = 5.5V,$ $\overline{LE} = OEA = \overline{OE}Bn = 2.7V,$ $A0-A7 = 2.7, B0-B7 = 2V$			-100	100	μA	1, 2, 3
					-10	10	mA	1, 2, 3
I_{OS}	Short Circuit Output Current A0-A7 only	$V_{CC} = 5.5, Bn = 1.9V,$ $OEA = 2.0V, \overline{OE}Bn = 2.7V,$ $V_O = 0V$	See ⁽⁴⁾	-60	-150	mA	1, 2, 3	
I_{CCH}	Supply Current (Total) I_{CCH}	$V_{CC} = 5.5, V_{IN} (An) = 5.0V$			37	mA	1, 2	
					41	mA	3	
I_{CCL}	Supply Current (Total) I_{CCL}	$V_{CC} = 5.5, V_{IN} (An) = 0.5V$			38	mA	1, 3	
					34	mA	2	
I_{CCZ}	Supply Current (Total) I_{CCZ}	$V_{CC} = 5.5, V_{IN} (An) = 0.5V$			35	mA	1, 2, 3	
I_{Off}	Power Off Output Current B0-B7	$V_{CC} = 0, Bn = 2.1V, V_{IL} = Max,$ $V_{IH} = Min$			100	μA	1, 2, 3	

(4) Not more than one output should be shorted at a time. For testing I_{OS} , the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

5.7 Pi Bus Transceiver DS1776 AC Parameters: B To A PathThe following conditions apply, unless otherwise specified. $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
t_{PLH}	Propagation Delay B to A	Waveform 1, 2		4.5	17	ns	9, 10, 11
t_{PHL}	Propagation Delay B to A	Waveform 1, 2		6.0	17	ns	9, 10, 11
t_{PZH}	Output Enable OEA To A	Waveform 3, 4		4.0	17	ns	9, 10, 11
t_{PZL}	Output Enable OEA To A	Waveform 3, 4		4.0	21	ns	9, 10, 11
t_{PHZ}	Output Disable OEA to A	Waveform 3, 4		2.0	12	ns	9, 10, 11
t_{PLZ}	Output Disable OEA to A	Waveform 3, 4		2.0	13	ns	9, 10, 11

5.8 Pi Bus Transceiver DS1776 AC Parameters: A To B Path

The following conditions apply, unless otherwise specified. $V_{CC} = 5V \pm 10\%$, $C_L = 30pF$, $R_L = 9\Omega$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
t_{PLH}	Propagation Delay A to B	Waveform 1, 2		2.0	13	ns	9, 11
				2.0	17	ns	10
t_{PHL}	Propagation Delay A to B	Waveform 1, 2		2.5	13	ns	9, 10, 11
t_{PLH}	Propagation Delay \overline{LE} to B	Waveform 1, 2		2.0	16	ns	9, 11
				2.0	22	ns	10
t_{PHL}	Propagation Delay \overline{LE} to B	Waveform 1, 2		2.0	16	ns	9, 10, 11
t_{PLH}	Enable / Disable Time \overline{OEBn} to B	Waveform 1, 2		2.0	13	ns	9, 11
				2.0	16	ns	10
t_{PHL}	Enable / Disable Time \overline{OEBn} to B	Waveform 1, 2		3.5	14	ns	9
				3.5	13	ns	10
				3.5	16	ns	11

5.9 Pi Bus Transceiver DS1776 AC Parameters: Setup / Hold / Pulse Width Specifications

The following conditions apply, unless otherwise specified. $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
t_S	A to \overline{LE} Setup	Waveform 5		7.0		ns	9, 10, 11
t_H	A to \overline{LE} Hold	Waveform 5		0.0		ns	9, 10, 11
t_W	\overline{LE} Pulse Width Low	Waveform 5		12		ns	9, 10, 11

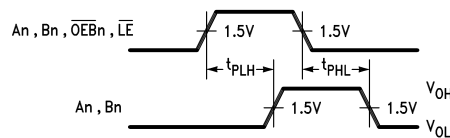


Figure 1. Propagation Delay For Data To Output

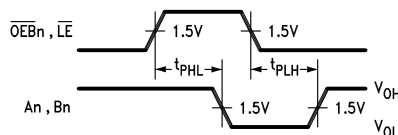


Figure 2. Propagation Delay For Data To Output

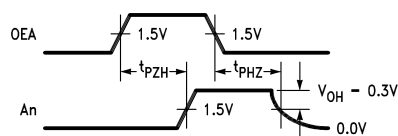


Figure 3. TRI-STATE Output Enable Time To High Level And Output Disable Time From High Level

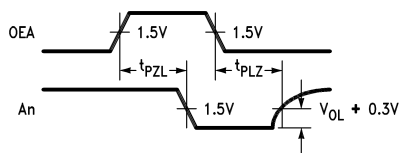
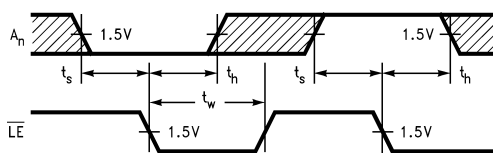


Figure 4. TRI-STATE Output Enable Time To Low Level And Output Disable Time From Low Level



The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5. Data Setup And Hold Times And Le Pulse Widths

5.10 Test Circuit And Waveforms

Figure 6. Test Circuit For TRI-STATE Outputs On A Side

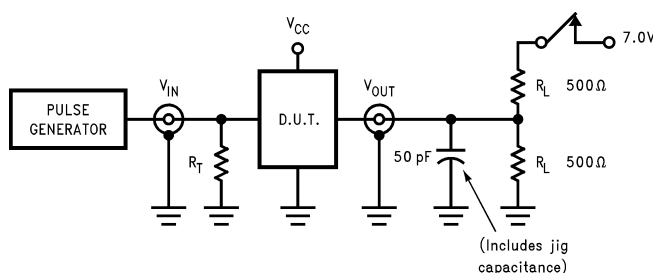
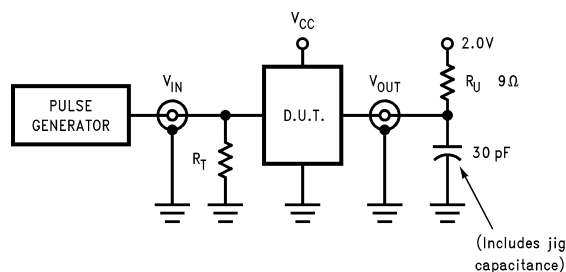


Table 2. Switch Position

Test	Switch
t_{PLZ} , t_{PZL}	Closed
All Other	Open

Figure 7. Test Circuit For TRI-STATE Outputs On B Side



DEFINITIONS

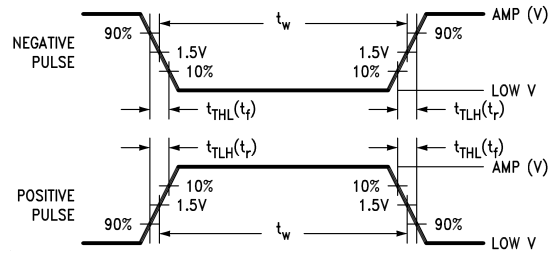
R_L = Load resistor 500 Ω

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_O of pulse generators.

R_U = Pull up resistor

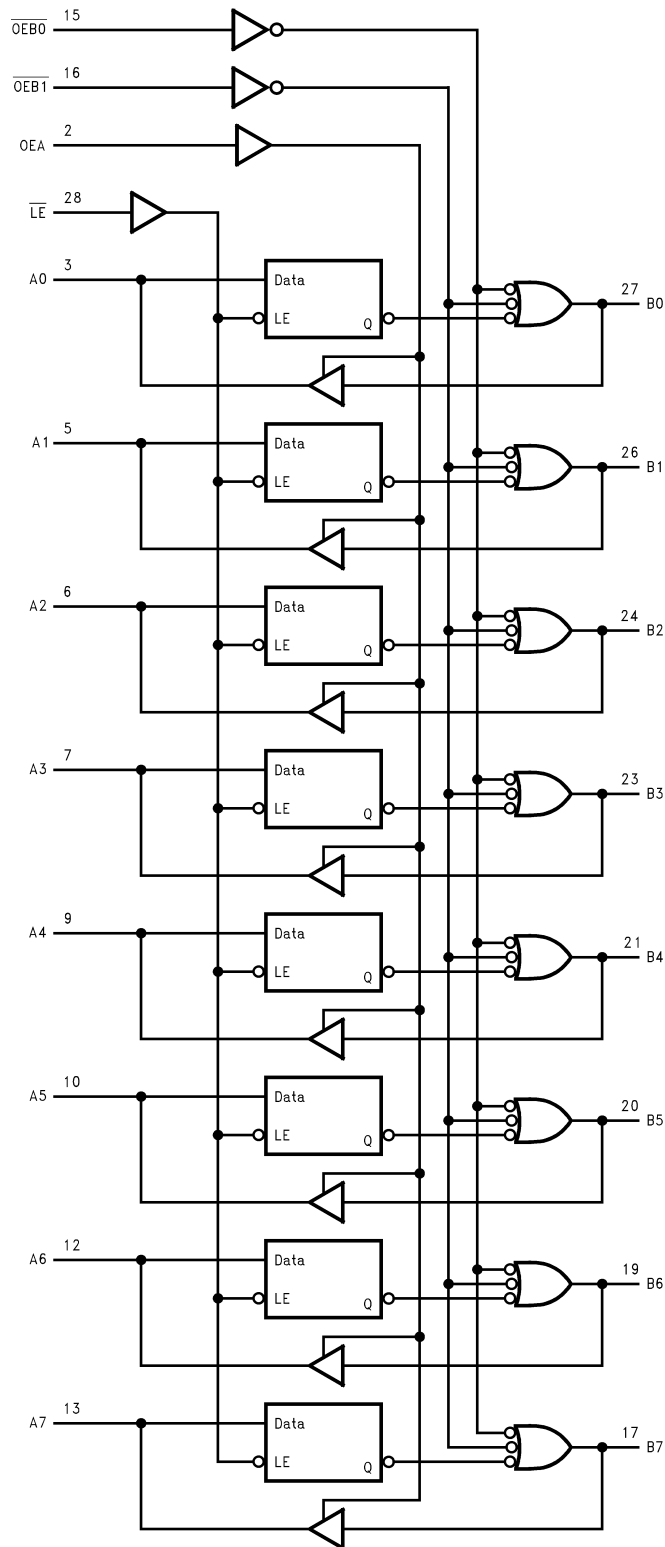
Figure 8. Input Pulse Definition



Input Pulse Characteristics						
	Amplitude	Low V	Rep. Rate	t_w	t_{TLH}	t_{THL}
A Side	3.0V	0.0V	1 MHz	500 ns	2 ns	2 ns
B Side	2.0V	1.0V	1 MHz	500 ns	2 ns	2 ns

DS1776QML

SNOSC82B –AUGUST 2012–REVISED JUNE 2015

www.ti.com**6 Detailed Description**

V_{CC} = Pin 1
 V_X = Pin 14
 Gnd = Pins 4, 8, 11, 18, 22, 25

Figure 9. Functional Logic Diagram

Table 3. Function Table⁽¹⁾

Inputs						Latch	Outputs		Mode
An	Bn ⁽²⁾	\overline{LE}	OEA	$\overline{OEB\ 0}$	$\overline{OEB\ 1}$	State	An	Bn	
H	X	L	L	L	L	H	Z	H	A TRI-STATE, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A TRI-STATE, Latched Data to B
—	—	L	H	L	L	See ⁽³⁾	See ⁽²⁾	See ⁽²⁾	Feedback: A to B, B to A
—	H	H	H	L	L	H ⁽⁴⁾	H	off ⁽⁴⁾	Preconditioned Latch Enabling
—	L	H	H	L	L	H ⁽⁴⁾	L	off ⁽⁴⁾	Data Transfer from B to A
—	—	H	H	L	L	Qn	Qn	Qn	Latch State to A and B
H	X	L	L	H	X	H	Z	off	
L	X	L	L	H	X	L	Z	off	B off and A TRI-STATE
X	X	H	L	H	X	Qn	Z	off	
—	H	L	H	H	X	H	H	off	
—	L	L	H	H	X	L	L	off	
—	H	H	H	H	X	Qn	H	off	B off, Data from B to A
—	L	H	H	H	X	Qn	L	off	
H	X	L	L	X	H	H	Z	off	
L	X	L	L	X	H	L	Z	off	B off and A TRI-STATE
X	X	H	L	X	H	Qn	Z	off	
—	H	L	H	X	H	H	H	off	
—	L	L	H	X	H	L	L	off	B off, Data from B to A
—	H	H	H	X	H	Qn	H	off	
—	L	H	H	X	H	Qn	L	off	

- (1) H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 — = Input not externally driven
 Z = High Impedance (off) state
 Qn = High or Low voltage level one setup time prior to the Low-to-High \overline{LE} transition
- (2) Condition will cause a feedback loop path; A to B and B to A.
- (3) Precaution should be taken to ensure that the B inputs do not float. If they do, they are equal to a Low state.
- (4) The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB\ 0}$ and $\overline{OEB\ 1}$, are Low and \overline{LE} is high.

6.1 Controller Power Sequencing Operation

The DS1776 has a design feature which controls the output transitions during power up (or down). There are two possible conditions that occur.

- When $\overline{LE} = \text{Low}$ and $\overline{OEBn} = \text{Low}$, the B outputs are disabled until the \overline{LE} circuit can take control. This feature ensures that the B outputs will follow the A inputs and allow only one transition during power up (or down).
- If $\overline{LE} = \text{High}$ or $\overline{OEBn} = \text{High}$, then the B outputs still remain disabled during power up (or down).

7 Device and Documentation Support

7.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9231701M3A	LIFEBUY	LCCC	FK	28	25	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS1776E /883 Q 5962-92317 01M3A ACO 01M3A >T	
DS1776E/883	LIFEBUY	LCCC	FK	28	25	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS1776E /883 Q 5962-92317 01M3A ACO 01M3A >T	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

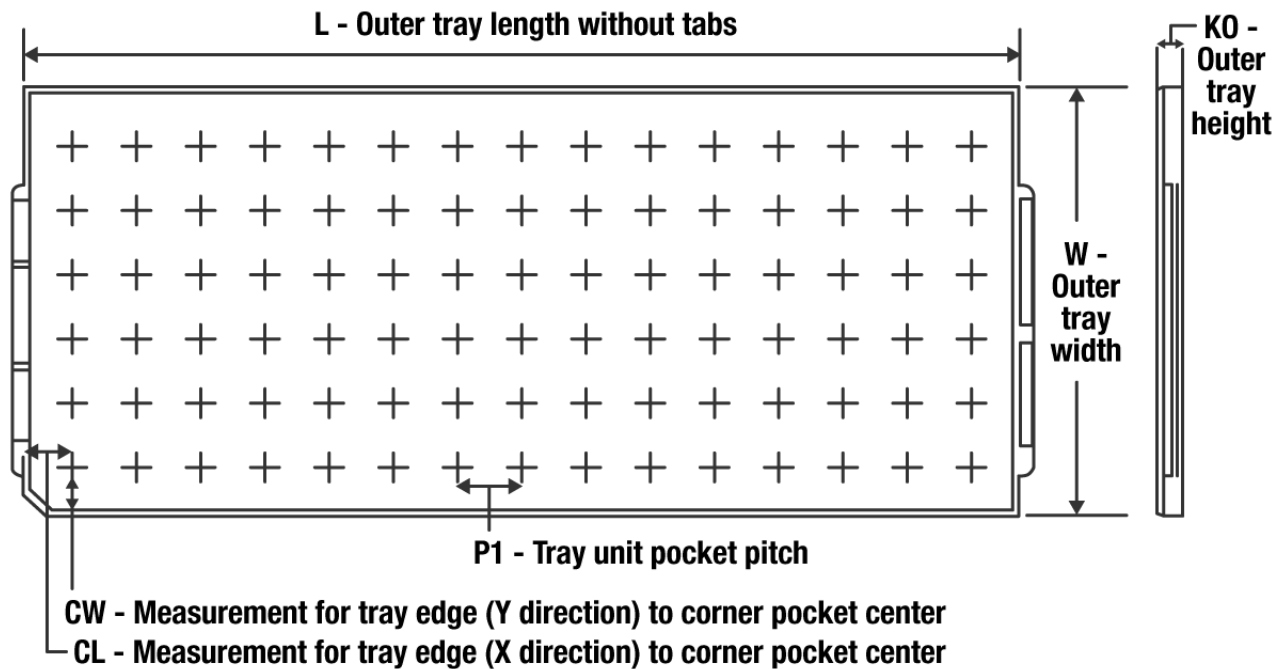
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

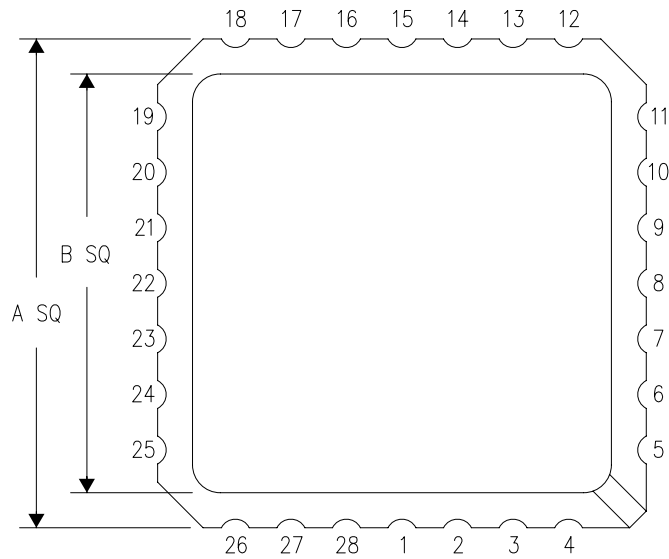
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-9231701M3A	FK	LCCC	28	25	NA	NA	109.22	109.22	7620	12.7	26.01	26.01
DS1776E/883	FK	LCCC	28	25	NA	NA	109.22	109.22	7620	12.7	26.01	26.01

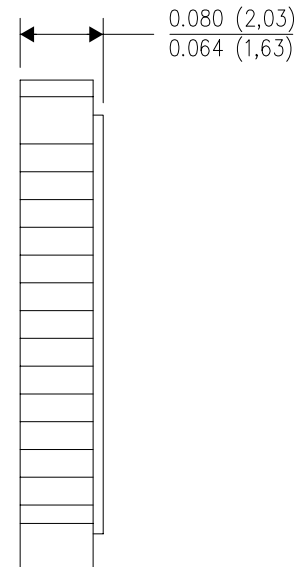
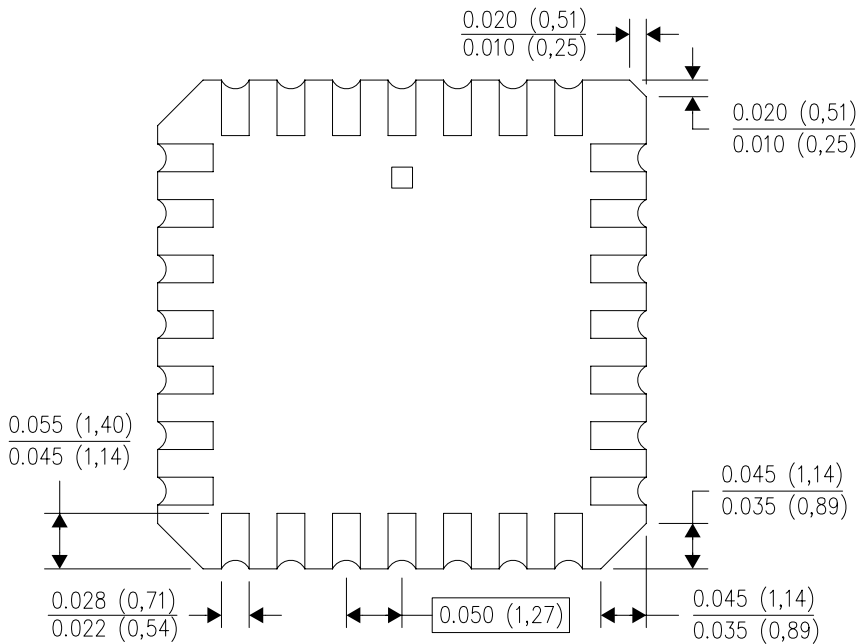
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: Info@DiGi-Electronics.com



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.