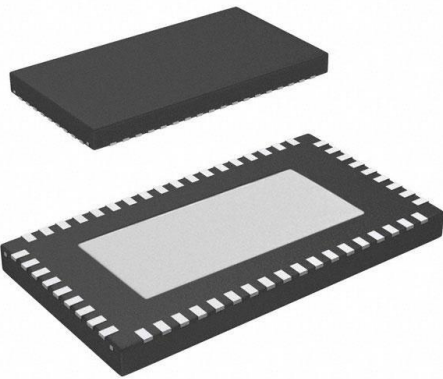


DS80PCI800SQ/NOPB Datasheet

www.digi-electronics.com



DS80PCI800SQ/NOPB

<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--|
| DiGi Electronics Part Number | DS80PCI800SQ/NOPB-DG |
| Manufacturer | Texas Instruments |
| Manufacturer Product Number | DS80PCI800SQ/NOPB |
| Description | IC REDRIVER PCIE 8CH 54WQFN |
| Detailed Description | Buffer, ReDriver 8 Channel 8Gbps 54-WQFN (10x5.5) |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

DS80PCI800SQ/NOPB

Series:

-

Type:

Buffer, ReDriver

Input:

CML

Data Rate (Max):

8Gbps

Delay Time:

200ps

Capacitance - Input:

10 pF

Current - Supply:

-

Mounting Type:

Surface Mount

Supplier Device Package:

54-WQFN (10x5.5)

Manufacturer:

Texas Instruments

Product Status:

Active

Applications:

PCIe

Output:

CML

Number of Channels:

8

Signal Conditioning:

Input Equalization, Output De-Emphasis

Voltage - Supply:

2.375V ~ 3.6V

Operating Temperature:

-40°C ~ 85°C

Package / Case:

54-WFQFN Exposed Pad

Base Product Number:

DS80PCI800

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

2 (1 Year)

ECCN:

EAR99

DS80PCI800 2.5-Gbps / 5.0-Gbps / 8.0-Gbps 8-Channel PCI-Express™ Repeater With Equalization and De-Emphasis

1 Features

- Comprehensive Family, Proven System Interoperability
 - DS80PCI102 : x1 PCIe Gen-1, Gen-2, and Gen-3
 - DS80PCI402 : x4 PCIe Gen-1, Gen-2, and Gen-3
 - DS80PCI800** : x8/x16 PCIe Gen-1, Gen-2, and Gen-3
- Automatic Rate Detect and Adaptation to Gen-1/2/3 Speeds
- Seamless Support for Gen-3 Transmit FIR Handshake
- Receiver EQ (up to 36 dB), Transmit De-Emphasis (up to 12 dB)
- Adjustable Transmit VOD: 0.8 to 1.3 Vp-p (Pin Mode)
- 0.2 UI of Residual Deterministic Jitter at 8 Gbps After 40 Inches of FR4 or 10 m 30-awg PCIe Cable
- Low Power Dissipation With Ability to Turn Off Unused Channels: 65 mW/Channel
- Automatic Receiver Detect (Hot-Plug)
- Multiple Configuration Modes: Pins/SMBus/Direct-EEPROM Load
- Flow-Thru Pinout: 54-Pin WQFN (10-mm x 5.5-mm, 0.5-mm Pitch)
- Single Supply Voltage: 2.5 or 3.3 V (Selectable)
- ±3 kV HBM ESD Rating
- 40°C to 85°C Operating Temperature Range

2 Applications

- PCI Express Gen-1, Gen-2, and Gen-3

3 Description

The DS80PCI800 is a low-power, 8-channel repeater with 4-stage input equalization, and an output de-emphasis driver to enhance the reach of PCI-Express serial links in board-to-board or cable interconnects. This device is ideal for higher density x8 and x16 PCI-Express configurations, and it automatically detects and adapts to Gen-1, Gen-2, and Gen-3 data rates for easy system upgrade.

DS80PCI800 offers programmable transmit de-emphasis (up to 12 dB), transmit VOD (up to 1300 mVp-p) and receive equalization (up to 36 dB) to enable longer distance transmission in lossy copper cables (10 meters or more), or backplanes (40 inches or more) with multiple connectors. The receiver can open an input eye that is completely closed due to inter-symbol interference (ISI) introduced by the interconnect medium.

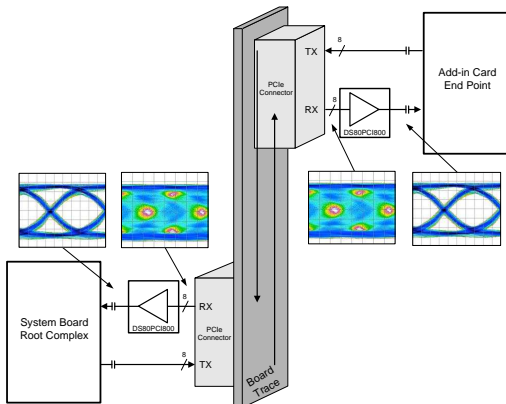
The programmable settings can be applied easily through pins or software (SMBus/I²C), or can be loaded through an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.

Device Information⁽¹⁾

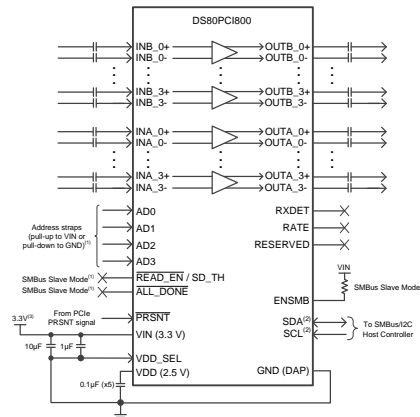
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|--------------------|
| DS80PCI800 | WQFN (54) | 10.00 mm x 5.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Block Diagram



Simplified Schematic Diagram



(1) Schematic shows connection for SMBus Slave Mode (ENSEMB=1kohm to VDD). For SMBus Master Mode or Pin Mode configuration, the connections are different.
 (2) SMBus signals need to be pulled up elsewhere in the system.
 (3) Schematic requires different connections for 2.5 V mode.

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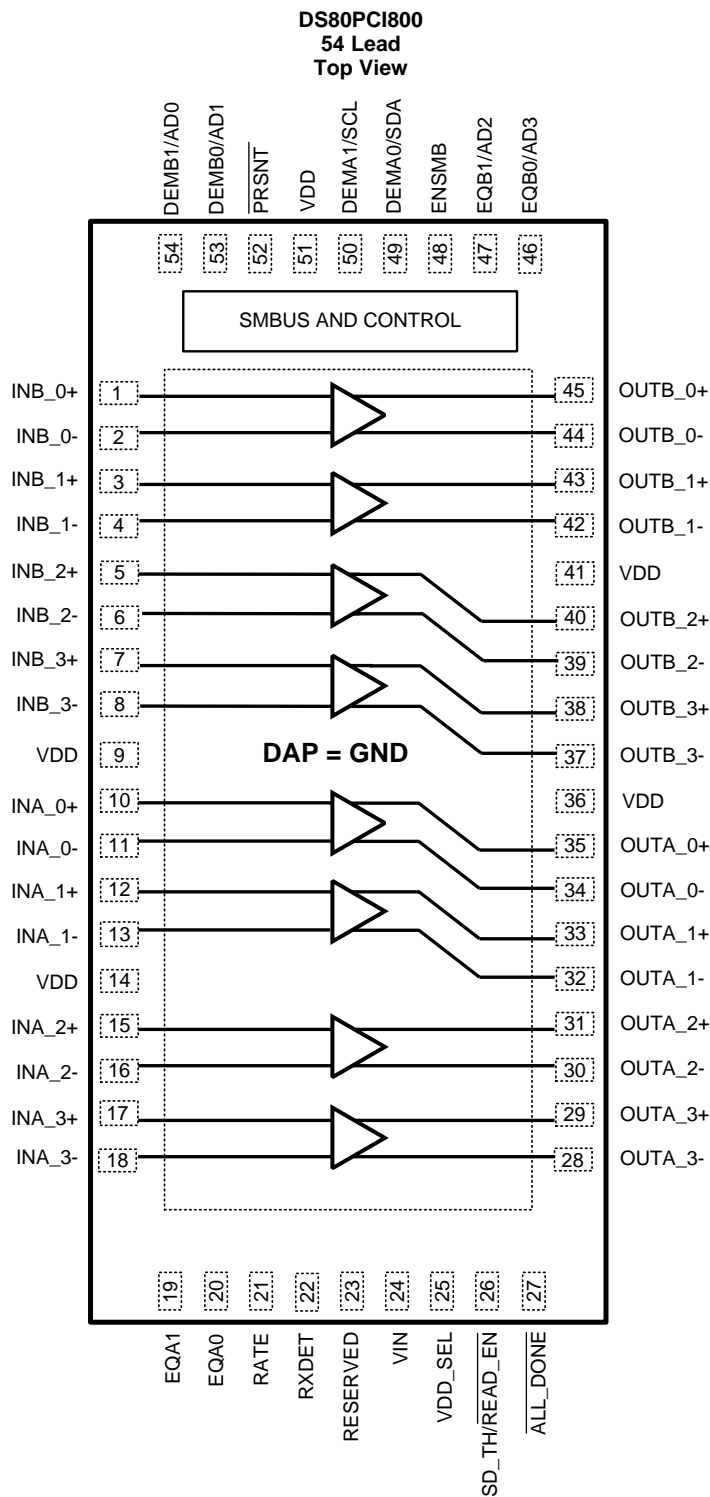
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4 Revision History**Changes from Revision F (April 2013) to Revision G****Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**

5 Pin Configuration and Functions



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Pin Functions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

| PIN | | I/O, TYPE | DESCRIPTION |
|---|--------------------------------------|--|--|
| NAME | NO. | | |
| DIFFERENTIAL HIGH SPEED I/Os | | | |
| INB_0+, INB_0-, INB_1+, INB_1-, INB_2+, INB_2-, INB_3+, INB_3- | 1, 2, 3, 4, 5, 6, 7, 8 | I, CML | Inverting and non-inverting differential inputs to bank B equalizer. A gated on-chip 50-Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD depending on the state of RXDET. See Table 4 AC coupling required on high-speed I/O |
| INA_0+, INA_0-, INA_1+, INA_1-, INA_2+, INA_2-, INA_3+, INA_3- | 10, 11, 12, 13, 15, 16, 17, 18 | I, CML | Inverting and non-inverting differential inputs to bank A equalizer. A gated on-chip 50-Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD depending on the state of RXDET. See Table 4 AC coupling required on high-speed I/O |
| OUTB_0+, OUTB_0-, OUTB_1+, OUTB_1-, OUTB_2+, OUTB_2-, OUTB_3+, OUTB_3- | 45, 44, 43, 42, 40, 39, 38, 37 | O, CML | Inverting and non-inverting 50-Ω driver bank B outputs with de-emphasis. Compatible with AC-coupled CML inputs. |
| OUTA_0+, OUTA_0-, OUTA_1+, OUTA_1-, OUTA_2+, OUTA_2-, OUTA_3+, OUTA_3- | 35, 34, 33, 32, 31, 30, 29, 28 | O, CML | Inverting and non-inverting 50-Ω driver bank A outputs with de-emphasis. Compatible with AC-coupled CML inputs. |
| CONTROL PINS — SHARED (LVCMOS) | | | |
| ENSMB | 48 | I, 4-LEVEL, LVCMOS | System management bus (SMBus) enable pin Tie 1 k to VDD (2.5-V mode) or VIN (3.3 V-mode) = Register access SMBus slave mode FLOAT = Read external EEPROM (master SMBUS mode) Tie 1 kΩ to GND = Pin mode |
| ENSMB = 1 (SMBus SLAVE MODE) | | | |
| SCL | 50 | I, 2-LEVEL, LVCMOS, O, open drain | In SMBus Slave Mode, this pin is the SMBus clock I/O. Clock input or open drain output. External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards. ⁽⁵⁾ |
| SDA | 49 | I, 2-LEVEL, LVCMOS, O, open drain | In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards. ⁽⁵⁾ |
| AD0-AD3 | 54, 53, 47, 46 | I, 4-LEVEL, LVCMOS | SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1-kΩ pullup or pulldown recommended. |
| READ_EN / SD_TH | 26 | I, FLOAT | In SMBus Slave Mode, this pin is not used. Leave it floating. |
| ENSMB = FLOAT (SMBus MASTER MODE) | | | |
| SCL | 50 | I, 2-LEVEL, LVCMOS, O, open drain | Clock output when loading EEPROM configuration, reverting to SMBus clock input when EEPROM load is complete (ALL_DONE = 0). External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards. ⁽⁵⁾ |
| SDA | 49 | I, 2-LEVEL, LVCMOS, O, open drain | In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards. ⁽⁵⁾ |
| AD0-AD3 | 54, 53, 47, 46 | I, 4-LEVEL, LVCMOS | SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1-kΩ pullup or pulldown recommended. |
| READ_EN | 26 | I, 2-LEVEL, LVCMOS | A logic low on this pin starts the load from the external EEPROM ⁽⁶⁾ Once EEPROM load is complete (ALL_DONE = 0), this pin functionality remains as READ_EN. It does not revert to an SD_TH input. |

- (1) LVCMOS inputs without the “FLOAT” conditions must be driven to a logic low or high at all times or operation is not verified.
- (2) Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10% to 90%.
- (3) For 3.3-V mode operation, VIN pin = 3.3 V and the VDD for the 4-level input is 3.3 V.
- (4) For 2.5-V mode operation, VDD pin = 2.5 V and the VDD for the 4-level input is 2.5 V.
- (5) SCL and SDA pins can be tied either to 3.3 V or 2.5 V, regardless of whether the device is operating in 2.5-V mode or 3.3-V mode.
- (6) When READ_EN is asserted low, the device attempts to load EEPROM. If EEPROM cannot be loaded successfully, for example due to an invalid or blank hex file, the DS80PCI800 waits indefinitely in an unknown state where SMBus access is not possible. ALL_DONE pin remains high in this situation.

Pin Functions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (continued)

| PIN | | I/O, TYPE | DESCRIPTION |
|---|-------------------|--------------------|--|
| NAME | NO. | | |
| $\overline{\text{ALL_DONE}}$ | 27 | O, 2-LEVEL, LVCMOS | Valid register load status output HIGH = External EEPROM load failed or incomplete LOW = External EEPROM load passed |
| ENSMB = 0 (PIN MODE) | | | |
| EQA0, EQA1, EQB0, EQB1 | 20, 19, 46, 47 | I, 4-LEVEL, LVCMOS | EQA[1:0] and EQB[1:0] control the level of equalization on the input pins. The pins are active only when ENSMB is deasserted (low). The 8 channels are organized into two banks. Bank A is controlled with the EQA[1:0] pins and bank B is controlled with the EQB[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The EQB[1:0] pins are converted to SMBUS AD2/AD3 inputs. See Table 2 . |
| DEMA0, DEMA1, DEMB0, DEMB1 | 49, 50, 53, 54 | I, 4-LEVEL, LVCMOS | DEMA[1:0] and DEMB[1:0] control the level of de-emphasis of the output driver. The pins are only active when ENSMB is deasserted (low). The 8 channels are organized into two banks. Bank A is controlled with the DEMA[1:0] pins and bank B is controlled with the DEMB[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The DEMA[1:0] pins are converted to SMBUS SCL/SDA and DEMB[1:0] pins are converted to AD0, AD1 inputs. See Table 3 . |
| CONTROL PINS — BOTH PIN AND SMBUS MODES (LVCMOS) | | | |
| RATE | 21 | I, 4-LEVEL, LVCMOS | RATE control pin selects GEN 1,2 and GEN 3 operating modes. Tie 1 k Ω to GND = GEN 1,2 FLOAT = AUTO Rate Select of Gen1/2 and Gen3 with de-emphasis Tie 20 k Ω to GND = GEN 3 without de-emphasis Tied 1 k Ω to VDD = RESERVED |
| RXDET | 22 | I, 4-LEVEL, LVCMOS | The RXDET pin controls the receiver detect function. Depending on the input level, a 50 Ω or > 50 k Ω termination to the power rail is enabled. See Table 4 . |
| RESERVED | 23 | I, FLOAT | Float (leave pin open) = Normal Operation |
| VDD_SEL | 25 | I, LVCMOS | Controls the internal regulator FLOAT = 2.5-V mode Tie GND = 3.3-V mode See Figure 14 |
| SD_TH | 26 | I, 4-LEVEL, LVCMOS | Controls the internal Signal Detect Threshold. See Table 5 . |
| $\overline{\text{PRSNT}}$ | 52 | I, 2-LEVEL, LVCMOS | Cable Present Detect input. High when a cable is not present per PCIe Cabling Spec. 1.0. Puts part into low power mode. When LOW (normal operation) part is enabled. See Table 4 . |
| POWER | | | |
| VIN | 24 | Power | In 3.3-V mode, feed 3.3 V to VIN In 2.5-V mode, leave floating |
| VDD | 9, 14, 36, 41, 51 | Power | Power supply pins 2.5-V mode, connect to 2.5-V supply 3.3-V mode, connect 0.1- μ F capacitor to each VDD pin (output of LDO) |
| GND | DAP | Power | Ground pad (DAP - die attach pad) |

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6 Specifications**6.1 Absolute Maximum Ratings**⁽¹⁾⁽²⁾⁽³⁾

| | MIN | MAX | UNIT |
|---|------|-----------|------|
| Supply voltage (VDD - 2.5-V mode) | -0.5 | 2.75 | V |
| Supply voltage (VIN - 3.3-V mode) | -0.5 | 4.0 | V |
| LVC MOS input/output voltage | -0.5 | 4.0 | V |
| CML input voltage | -0.5 | VDD + 0.5 | V |
| CML input current | -30 | 30 | mA |
| Junction temperature | | 125 | °C |
| Lead temperature soldering (4 s) ⁽⁴⁾ | | 260 | °C |
| Storage temperature, T _{stg} | -40 | 125 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Ratings*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum Numbers are specified for a junction temperature range of -40°C to 125°C. Models are validated to Maximum Operating Voltages only.
- (3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) For soldering specifications: See application note [SNOA549](#).

6.2 ESD Ratings

| | | MAX | UNIT |
|---|--|-------|------|
| V _(ESD) | Electrostatic discharge | | |
| | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±3000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1000 | |
| Machine model (MM), per JEDEC specification JESD22-A115-A | ±200 | | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

| | MIN | NOM | MAX | UNIT |
|--|-------|-----|-------|-------|
| Supply voltage (2.5-V mode) | 2.375 | 2.5 | 2.625 | V |
| Supply voltage (3.3-V mode) | 3.0 | 3.3 | 3.6 | V |
| Ambient temperature | -40 | 25 | 85 | °C |
| SMBus (SDA, SCL) | | | 3.6 | V |
| Supply noise up to 50 MHz ⁽¹⁾ | | | 100 | mVp-p |

- (1) Allowed supply noise (mVp-p sine wave) under typical conditions.

6.4 Electrical Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|------|-----|-----|-------------------|
| POWER | | | | | | |
| PD | Power Dissipation | VDD = 2.5 V supply, EQ Enabled, VOD = 1.0 V _{p-p} , RXDET = 1, PRSNT = 0 | | 500 | 700 | mW |
| | | VIN = 3.3 V supply, EQ Enabled, VOD = 1.0 V _{p-p} , RXDET = 1, PRSNT = 0 | | 660 | 900 | mW |
| LVC MOS / LV TTL DC SPECIFICATIONS | | | | | | |
| V _{IH25} | High-level input voltage (PRSNT, READ_EN pins) | 2.5-V Mode | 2.0 | | VDD | V |
| V _{IH33} | High-level input voltage (PRSNT, READ_EN pins) | 3.3-V Mode | 2.0 | | VIN | V |
| V _{IL} | Low-Level Input Voltage (PRSNT, READ_EN pins) | | 0 | | 0.8 | V |
| V _{OH} | High-level output voltage (ALL_DONE pin) | I _{OH} = -4 mA | 2.0 | | | V |
| V _{OL} | Low-level output voltage (ALL_DONE pin) | I _{OL} = 4 mA | | | 0.4 | V |
| I _{IH} | Input high current (PRSNT pin) | VIN = 3.6 V, LVC MOS = 3.6 V | -15 | | 15 | μA |
| | Input high current with internal resistors (4-level input pin) | | 20 | | 150 | μA |
| I _{IL} | Input low current (PRSNT pin) | VIN = 3.6 V, LVC MOS = 0 V | -15 | | 15 | μA |
| | Input low current with internal resistors (4-level input pin) | | -160 | | -40 | μA |
| CML RECEIVER INPUTS (IN_{n+}, IN_{n-}) | | | | | | |
| RL _{RX-DIFF} | RX differential return loss | 0.05 to 1.25 GHz | | -16 | | dB |
| | | 1.25 to 2.5 GHz | | -16 | | dB |
| | | 2.5 to 4.0 GHz | | -14 | | dB |
| RL _{RX-CM} | RX common mode return loss | 0.05 to 2.5 GHz | | -12 | | dB |
| | | 2.5 to 4.0 GHz | | -8 | | dB |
| Z _{RX-DC} | RX DC single-ended impedance | Tested at VDD = 2.5 V | 40 | 50 | 60 | Ω |
| Z _{RX-DIFF-DC} | RX DC differential mode impedance | Tested at VDD = 2.5 V | 80 | 100 | 120 | Ω |
| Z _{RX-HIGH-IMP-DC-POS} | DC input common mode impedance for V > 0 | VID = 0 to 200 mV, ENSMB = 0, RXDET = 0, VDD = 2.5 V | | 50 | | kΩ |
| V _{RX-DIFF-DC} | Differential RX peak-to-peak voltage (VID) | Tested at pins | | | 1.2 | V |
| V _{RX-SIGNAL-DET-DIFF-PP} | Signal detect assert level for active data signal | SD_TH = float, 0101 pattern at 8 Gbps Measured at pins | | 180 | | mV _{p-p} |
| V _{RX-IDLE-DET-DIFF-PP} | Signal detect deassert level for electrical idle | SD_TH = float, 0101 pattern at 8 Gbps Measured at pins | | 110 | | mV _{p-p} |

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Electrical Characteristics (continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|--|--|-----|------|-----|----------|
| HIGH-SPEED OUTPUTS | | | | | | |
| $V_{TX-DIFF-PP}$ | Output voltage differential swing | Differential measurement with OUT_n+ and OUT_n-, terminated by 50 Ω to GND, AC-Coupled, VID = 1.0 Vp-p, DEM0 = 1, DEM1 = 0 ⁽¹⁾ | 0.8 | 1.0 | 1.2 | Vp-p |
| $V_{TX-DE-RATIO_3.5}$ | TX de-emphasis ratio | VOD = 1.0 Vp-p, DEM0 = 0, DEM1 = R Gen 1 & 2 modes only | | -3.5 | | dB |
| $V_{TX-DE-RATIO_6}$ | TX de-emphasis ratio | VOD = 1.0 Vp-p, DEM0 = R, DEM1 = R Gen 1 & 2 modes only | | -6 | | dB |
| t_{TX-DJ} | Deterministic Jitter | VID = 800 mV, PRBS15 pattern, 8.0 Gbps, VOD = 1.0 V, EQ = 0x00, DE = 0 dB (no input or output trace loss) | | 0.05 | | Upp |
| t_{TX-RJ} | Random Jitter | VID = 800 mV, 0101 pattern, 8.0 Gbps, VOD = 1.0 V, EQ = 0x00, DE = 0 dB, (no input or output trace loss) | | 0.3 | | ps RMS |
| $t_{TX-RISE-FALL}$ | TX rise/fall time | 20% to 80% of differential output voltage ⁽²⁾ | 35 | 45 | | ps |
| $t_{RF-MISMATCH}$ | TX rise/fall mismatch | 20% to 80% of differential output voltage ⁽²⁾ | | 0.01 | 0.1 | UI |
| $RL_{TX-DIFF}$ | TX differential return loss | 0.05 to 1.25 GHz | | -16 | | dB |
| | | 1.25 to 2.5 GHz | | -12 | | dB |
| | | 2.5 to 4 GHz | | -11 | | dB |
| RL_{TX-CM} | TX common mode return loss | 0.05 to 2.5 GHz | | -12 | | dB |
| | | 2.5 to 4 GHz | | -8 | | dB |
| $Z_{TX-DIFF-DC}$ | DC differential TX impedance | | | 100 | | Ω |
| $V_{TX-CM-AC-PP}$ | TX AC peak-peak common mode voltage | VOD = 1.0 Vp-p, DEM0 = 1, DEM1 = 0 ⁽²⁾ | | | 100 | mVp-p |
| $I_{TX-SHORT}$ | TX short circuit current limit | Total current the transmitter can supply when shorted to VDD or GND | | 20 | | mA |
| $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | Absolute delta of DC common mode voltage during L0 and electrical idle | ⁽²⁾ | | | 100 | mV |
| $V_{TX-CM-DC-LINE-DELTA}$ | Absolute delta of DC common mode voltage between TX+ and TX- | ⁽²⁾ | | | 25 | mV |
| $t_{TX-IDLE-DATA}$ | Max time to transition to differential DATA signal after IDLE | VID = 1.0 Vp-p, 8 Gbps | | 3.5 | | ns |
| $t_{TX-DATA-IDLE}$ | Max time to transition to IDLE after differential DATA signal | VID = 1.0 Vp-p, 8 Gbps | | 6.2 | | ns |
| $t_{PLHD/PHLD}$ | High-to-low and low-to-high differential propagation delay | EQ = 0x00 ⁽³⁾ | | 200 | | ps |
| t_{LSK} | Lane-to-lane skew | T = 25°C, VDD = 2.5 V | | 25 | | ps |
| t_{PPSK} | Part-to-part propagation delay skew | T = 25°C, VDD = 2.5 V | | 40 | | ps |

- (1) In GEN3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEMA/B[1:0] in GEN3 mode is dependent on the VID level and the frequency content. The DS80PCI800 repeater in GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support the PCIe GEN3 handshake negotiation link training.
- (2) Parameter is characterized but not tested in production.
- (3) Propagation delay measurements will change slightly based on the level of EQ selected. EQ = 0x00 will result in the largest propagation delays.

Electrical Characteristics (continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|-----|------|-----|------|
| EQUALIZATION | | | | | | |
| DJE1 | Residual deterministic jitter at 8 Gbps | 35" 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 0x1F , DEM = 0 dB | | 0.14 | | Upp |
| DJE2 | Residual deterministic jitter at 5 Gbps | 35" 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 0x1F , DEM = 0 dB | | 0.1 | | Upp |
| DJE3 | Residual deterministic jitter at 2.5 Gbps | 35" 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 0x1F , DEM = 0 dB | | 0.05 | | Upp |
| DJE4 | Residual deterministic jitter at 8 Gbps | 10 meters 30-awg cable, VID = 0.8 Vp-p, PRBS15, EQ = 0x2F , DEM = 0 dB | | 0.16 | | Upp |
| DJE5 | Residual deterministic jitter at 5 Gbps | 10 meters 30-awg cable, VID = 0.8 Vp-p, PRBS15, EQ = 0x2F , DEM = 0 dB | | 0.1 | | Upp |
| DJE6 | Residual deterministic jitter at 2.5 Gbps | 10 meters 30-awg cable, VID = 0.8 Vp-p, PRBS15, EQ = 0x2F , DEM = 0 dB | | 0.05 | | Upp |
| DE-EMPHASIS (GEN 1,2 MODE ONLY) | | | | | | |
| DJD1 | Residual deterministic jitter at 2.5 Gbps and 5.0 Gbps | 10" 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 0x00, VOD = 1.0 Vp-p, DEM = -3.5 dB | | 0.1 | | Upp |
| DJD2 | Residual deterministic jitter at 2.5 Gbps and 5.0 Gbps | 20" 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 0x00, VOD = 1.0 Vp-p, DEM = -9 dB | | 0.1 | | Upp |

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6.5 Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|-------|------|-----|----------|
| SERIAL BUS INTERFACE DC SPECIFICATIONS | | | | | | |
| V_{IL} | Data, clock input low voltage | | | | 0.8 | V |
| V_{IH} | Data, clock input high voltage | | 2.1 | | 3.6 | V |
| I_{PULLUP} | Current through pullup resistor or current source | High Power Specification | 4 | | | mA |
| V_{DD} | Nominal bus voltage | | 2.375 | | 3.6 | V |
| $I_{LEAK-BUS}$ | Input leakage per bus segment | (1) | -200 | | 200 | μ A |
| $I_{LEAK-Pin}$ | Input leakage per device pin | | | -15 | | μ A |
| C_I | Capacitance for SDA and SCL | (1) (2) | | | 10 | pF |
| R_{TERM} | External termination resistance pull to $V_{DD} = 2.5\text{ V} \pm 5\%$ or $3.3\text{ V} \pm 10\%$ | Pullup $V_{DD} = 3.3\text{ V}$ (1) (2) (3) | | 2000 | | Ω |
| | | Pullup $V_{DD} = 2.5\text{ V}$ (1) (2) (3) | | 1000 | | Ω |
| SERIAL BUS INTERFACE TIMING SPECIFICATIONS | | | | | | |
| FSMB | Bus operating frequency | ENSMB = VDD (Slave Mode) | | | 400 | kHz |
| | | ENSMB = FLOAT (Master Mode) | 280 | 400 | 520 | kHz |
| t_{BUF} | Bus free time between stop and start condition | | 1.3 | | | μ s |
| $t_{HD:STA}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. | At I_{PULLUP} , Max | 0.6 | | | μ s |
| $t_{SU:STA}$ | Repeated start condition setup time | | 0.6 | | | μ s |
| $t_{SU:STO}$ | Stop condition setup time | | 0.6 | | | μ s |
| $t_{HD:DAT}$ | Data hold time | | 0 | | | ns |
| $t_{SU:DAT}$ | Data setup time | | 100 | | | ns |
| t_{LOW} | Clock low period | | 1.3 | | | μ s |
| t_{HIGH} | Clock high period | (4) | 0.6 | | 50 | μ s |
| t_F | Clock/data fall time | (4) | | | 300 | ns |
| t_R | Clock/data rise time | (4) | | | 300 | ns |
| t_{POR} | Time in which a device must be operational after power-on reset | (4) (5) | | | 500 | ms |

(1) Recommended value.

(2) Recommended maximum capacitance load per bus segment is 400 pF.

(3) Maximum termination voltage should be identical to the device supply voltage.

(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

(5) Specified by design. Parameter not tested in production.

6.6 Typical Characteristics

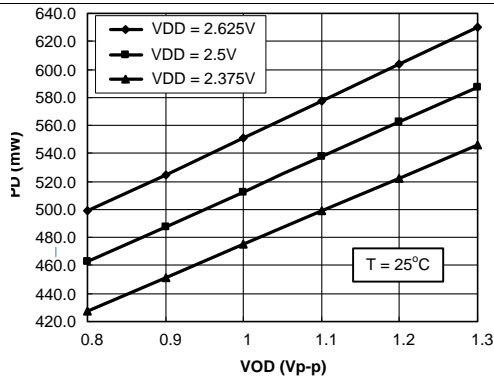


Figure 1. Power Dissipation (PD) vs Output Differential Voltage (VOD)

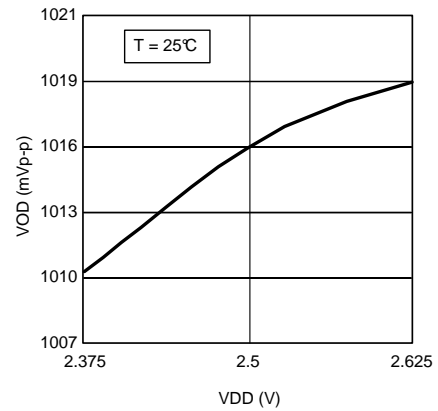


Figure 2. Output Differential Voltage (VOD = 1.0 Vp-p) vs Supply Voltage (VDD)

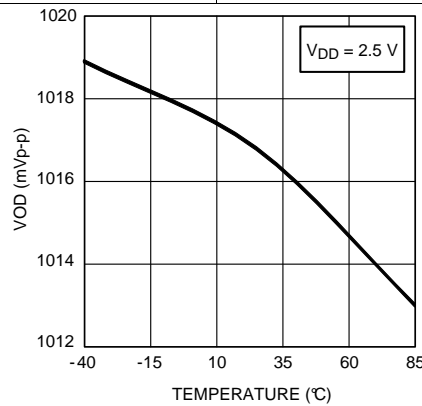
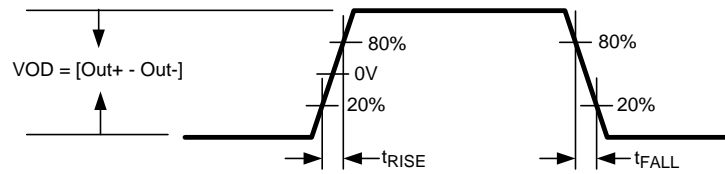
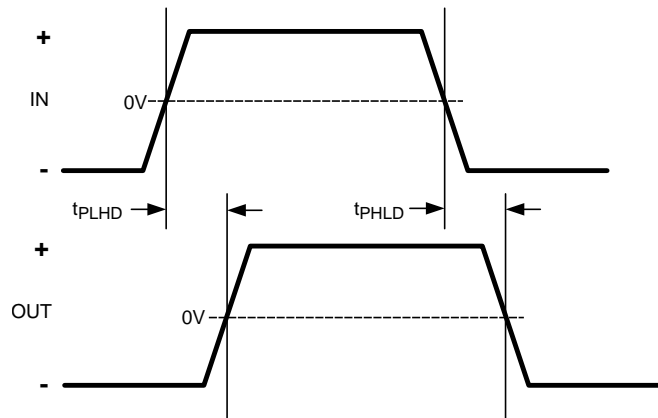
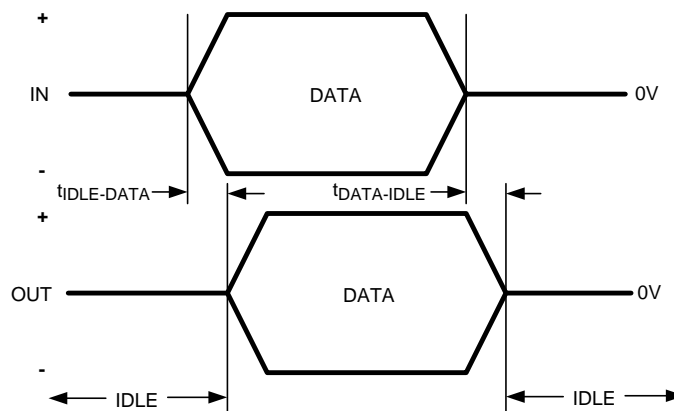
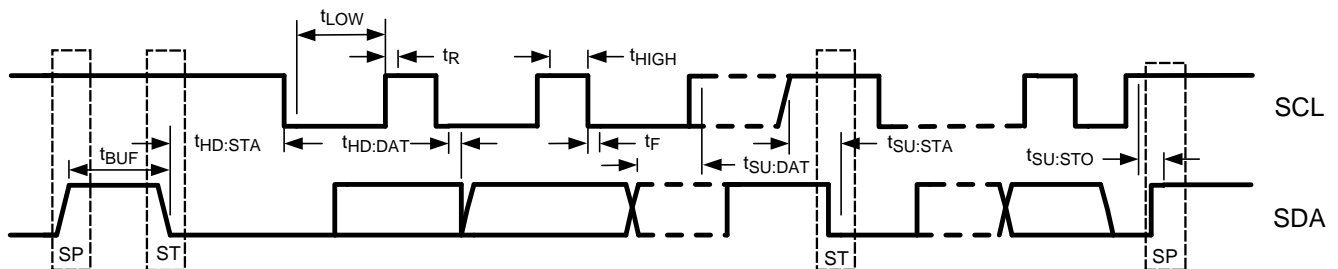


Figure 3. Output Differential Voltage (VOD = 1.0 Vp-p) vs Temperature

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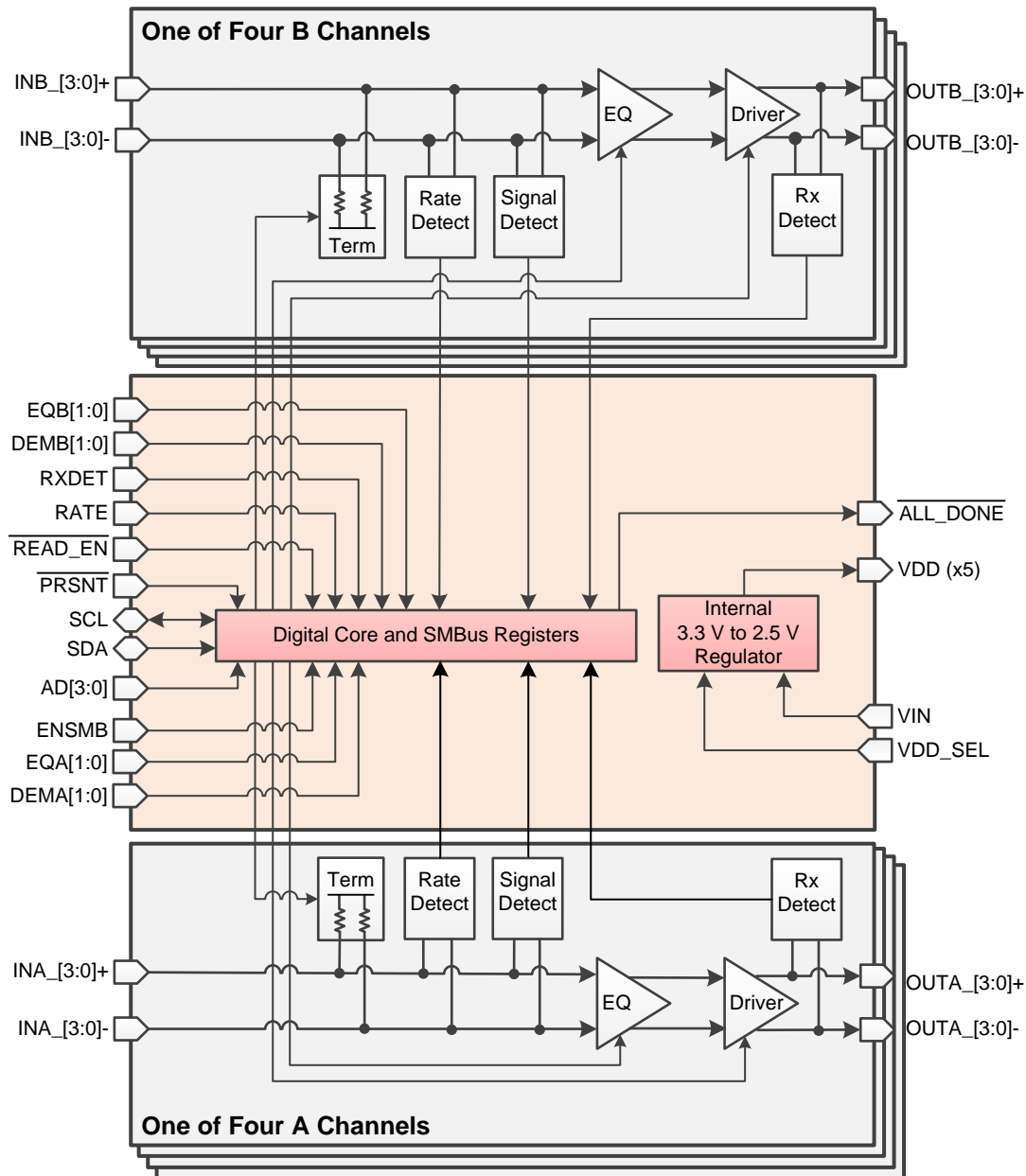
7 Parameter Measurement Information**Figure 4. CML Output and Rise and Fall Transition Time****Figure 5. Propagation Delay Timing Diagram****Figure 6. Transmit IDLE-DATA and DATA-IDLE Response Time****Figure 7. SMBus Timing Parameters**

8 Detailed Description

8.1 Overview

The DS80PCI800 provides input CTLE and output De-emphasis equalization for lossy printed circuit board trace and cables. The DS80PCI800 operates in three modes: Pin Control Mode configuration (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) for register configurations from host controller or SMBus Master Mode (ENSMB = Float) for loading the register configurations from an external EEPROM.

8.2 Functional Block Diagram



Note: This diagram is representative of device signal flow only.

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8.3 Feature Description**8.3.1 4-Level Input Configuration Guidelines**

The 4-level input pins use a resistor divider to help set the four valid levels. There is an internal 30-k Ω pullup and a 60-k Ω pulldown connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1-k Ω pullup, 1-k Ω pulldown, no connect, or 20-k Ω pulldown provide the optimal voltage levels for each of the four input states.

Table 1. 4-Level Input Voltage

| LEVEL | SETTING | 3.3-V MODE | 2.5-V MODE |
|-------|---------------------------------|----------------------|----------------------|
| 0 | 1 k Ω to GND | 0.1 V | 0.08 V |
| R | 20 k Ω to GND | $0.33 \times V_{IN}$ | $0.33 \times V_{DD}$ |
| F | FLOAT | $0.67 \times V_{IN}$ | $0.67 \times V_{DD}$ |
| 1 | 1 k Ω to V_{DD}/V_{IN} | $V_{IN} - 0.05 V$ | $V_{DD} - 0.04 V$ |

Typical 4-level input thresholds:

- Level 1 to 2 = $0.2 V_{IN}$ or V_{DD}
- Level 2 to 3 = $0.5 V_{IN}$ or V_{DD}
- Level 3 to 4 = $0.8 V_{IN}$ or V_{DD}

To minimize the start-up current associated with the integrated 2.5 V regulator, the 1-k Ω pullup and pulldown resistors are recommended. If several 4-level inputs require the same setting, it is possible to combine two or more 1-k Ω resistors into a single lower value resistor. As an example; combining two inputs with a single 500- Ω resistor is a good way to save board space. For the 20 k Ω to GND, this should also scale to 10 k Ω .

Table 2. Equalizer Settings⁽¹⁾

| EQUALIZATION BOOST RELATIVE TO DC | | | | | | | |
|-----------------------------------|--------------|--------------|-------------------|-------------------|------------------|----------------|-------------------------------|
| LEVEL | EQA1 EQB1 | EQA0 EQB0 | EQ – 8 BITS [7:0] | dB at 1.25 GHz | dB at 2.5 GHz | dB at 4 GHz | SUGGESTED USE |
| 1 | 0 | 0 | 0000 0000 = 0x00 | 2.1 | 3.7 | 4.9 | FR4 < 5 inch trace |
| 2 | 0 | R | 0000 0001 = 0x01 | 3.4 | 5.8 | 7.9 | FR4 5 inch 5-mil trace |
| 3 | 0 | Float | 0000 0010 = 0x02 | 4.8 | 7.7 | 9.9 | FR4 5 inch 4-mil trace |
| 4 | 0 | 1 | 0000 0011 = 0x03 | 5.9 | 8.9 | 11.0 | FR4 10 inch 5-mil trace |
| 5 | R | 0 | 0000 0111 = 0x07 | 7.2 | 11.2 | 14.3 | FR4 10 inch 4-mil trace |
| 6 | R | R | 0001 0101 = 0x15 | 6.1 | 11.4 | 14.6 | FR4 15 inch 4-mil trace |
| 7 | R | Float | 0000 1011 = 0x0B | 8.8 | 13.5 | 17.0 | FR4 20 inch 4-mil trace |
| 8 | R | 1 | 0000 1111 = 0x0F | 10.2 | 15.0 | 18.5 | FR4 25 to 30 inch 4-mil trace |
| 9 | Float | 0 | 0101 0101 = 0x55 | 7.5 | 12.8 | 18.0 | FR4 30 inch 4-mil trace |
| 10 | Float | R | 0001 1111 = 0x1F | 11.4 | 17.4 | 22.0 | FR4 35 inch 4-mil trace |
| 11 | Float | Float | 0010 1111 = 0x2F | 13.0 | 19.7 | 24.4 | 10 m, 30-awg cable |
| 12 | Float | 1 | 0011 1111 = 0x3F | 14.2 | 21.1 | 25.8 | 10 m – 12m cable |
| 13 | 1 | 0 | 1010 1010 = 0xAA | 13.8 | 21.7 | 27.4 | |
| 14 | 1 | R | 0111 1111 = 0x7F | 15.6 | 23.5 | 29.0 | |
| 15 | 1 | Float | 1011 1111 = 0xBF | 17.2 | 25.8 | 31.4 | |
| 16 | 1 | 1 | 1111 1111 = 0xFF | 18.4 | 27.3 | 32.7 | |

(1) The suggested equalizer CTLE settings are based on 0 dB of TX preshoot/de-emphasis. In PCIe Gen 3 applications which use TX preshoot/de-emphasis, the CTLE should be set to a lower boost setting to optimize the RX eye opening.

Table 3. Output Voltage and De-Emphasis Settings⁽¹⁾

| LEVEL | DEMA1 DEMB1 | DEMA0 DEMB0 | VOD V _{p-p} | DEM dB ⁽¹⁾ | INNER AMPLITUDE V _{p-p} | SUGGESTED USE |
|-------|----------------|----------------|----------------------|-----------------------|-------------------------------------|--------------------------|
| 1 | 0 | 0 | 0.8 | 0 | 0.8 | FR4 < 5 inch 4-mil trace |
| 2 | 0 | R | 0.9 | 0 | 0.9 | FR4 < 5 inch 4-mil trace |
| 3 | 0 | Float | 0.9 | -3.5 | 0.6 | FR4 10 inch 4-mil trace |
| 4 | 0 | 1 | 1.0 | 0 | 1.0 | FR4 < 5 inch 4-mil trace |
| 5 | R | 0 | 1.0 | -3.5 | 0.7 | FR4 10 inch 4-mil trace |
| 6 | R | R | 1.0 | -6 | 0.5 | FR4 15 inch 4-mil trace |
| 7 | R | Float | 1.1 | 0 | 1.1 | FR4 < 5 inch 4-mil trace |
| 8 | R | 1 | 1.1 | -3.5 | 0.7 | FR4 10 inch 4-mil trace |
| 9 | Float | 0 | 1.1 | -6 | 0.6 | FR4 15 inch 4-mil trace |
| 10 | Float | R | 1.2 | 0 | 1.2 | FR4 < 5 inch 4-mil trace |
| 11 | Float | Float | 1.2 | -3.5 | 0.8 | FR4 10 inch 4-mil trace |
| 12 | Float | 1 | 1.2 | -6 | 0.6 | FR4 15 inch 4-mil trace |
| 13 | 1 | 0 | 1.3 | 0 | 1.3 | FR4 < 5 inch 4-mil trace |
| 14 | 1 | R | 1.3 | -3.5 | 0.9 | FR4 10 inch 4-mil trace |
| 15 | 1 | Float | 1.3 | -6 | 0.7 | FR4 15 inch 4-mil trace |
| 16 | 1 | 1 | 1.3 | -9 | 0.5 | FR4 20 inch 4-mil trace |

- (1) The VOD output amplitude and DEM de-emphasis levels are set with the DEMA/B[1:0] pins. The de-emphasis levels are available in GEN1, GEN2, and GEN 3 modes when RATE = Float.

Table 4. RX-Detect Settings

| PR \overline SNT ⁽¹⁾ (PIN 52) | RXDET (PIN 22) | SMBus REG BIT[3:2] | INPUT TERMINATION | COMMENTS |
|---|-----------------------------|-----------------------|--|--|
| 0 | 0 | 00 | Hi-Z | Manual RX-Detect, input is high-impedance mode |
| 0 | Tie 20 k Ω to GND | 01 | Pre Detect: Hi-Z Post Detect: 50 Ω | Auto RX-Detect, outputs test every 12 ms for 600 ms then stops; termination is hi-Z until detection; once detected input termination is 50 Ω Reset function by pulsing PR \overline SNT high for 5 μ s then low again |
| 0 | Float (Default) | 10 | Pre Detect: Hi-Z Post Detect: 50 Ω | Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω Reset function by pulsing PR \overline SNT high for 5 μ s then low again |
| 0 | 1 | 11 | 50 Ω | Manual RX-Detect, input is 50 Ω |
| 1 | X | | Hi-Z | Power-down mode, input is high impedance, output drivers are disabled Used to reset RX-Detect State Machine when held high for 5 μ s |

- (1) In SMBus Slave Mode, the Rx Detect State Machine can be manually reset in software by overriding the device PR \overline SNT function. This is accomplished by setting the Override RXDET bit (Reg 0x02[7]) and then toggling the RXDET Value bit (Reg 0x02[6]). See Table 9 for more information about resetting the Rx Detect State Machine.

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Table 5. Signal Detect Threshold Level⁽¹⁾

| SD_TH | SMBus REG BIT [3:2] AND [1:0] | ASSERT LEVEL (TYP) | DEASSERT LEVEL (TYP) |
|-------------|-------------------------------|--------------------|----------------------|
| 0 | 10 | 210 mVp-p | 150 mVp-p |
| R | 01 | 160 mVp-p | 100 mVp-p |
| F (default) | 00 | 180 mVp-p | 110 mVp-p |
| 1 | 11 | 190 mVp-p | 130 mVp-p |

(1) VDD = 2.5 V, 25°C, and 0101 pattern at 8 Gbps.

8.4 Device Functional Modes

The DS80PCI800 is a low-power 8-channel repeater optimized for PCI Express Gen 1/2 and 3. The DS80PCI800 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS80PCI800 operates in three modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register information from external EEPROM; refer to [SMBus Master Mode](#) for additional information.

8.4.1 Pin Control Mode

When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the De-Emphasis table below. The RXDET pins provides automatic and manual control for input termination (50 Ω or > 50 kΩ). RATE setting is also pin controllable with pin selections (Gen 1/2, auto detect and Gen 3). The receiver electrical idle detect threshold is also adjustable via the SD_TH pin.

8.4.2 SMBUS Mode

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins (RATE, RXDET and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PRSNT is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most PCIe applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The [4-Level Input Configuration Guidelines](#) show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-emphasis levels are set by registers.

8.5 Programming**8.5.1 System Management Bus (SMBus) and Configuration Registers**

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1 kΩ to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS80PCI800 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pulldown. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is 0xB0. Based on the SMBus 2.0 specification, the DS80PCI800 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

Programming (continued)

Table 6. Device Slave Address Bytes

| AD[3:0] SETTINGS | ADDRESS BYTES (HEX) | 7-BIT SLAVE ADDRESS (HEX) |
|------------------|---------------------|---------------------------|
| 0000 | B0 | 58 |
| 0001 | B2 | 59 |
| 0010 | B4 | 5A |
| 0011 | B6 | 5B |
| 0100 | B8 | 5C |
| 0101 | BA | 5D |
| 0110 | BC | 5E |
| 0111 | BE | 5F |
| 1000 | C0 | 60 |
| 1001 | C2 | 61 |
| 1010 | C4 | 62 |
| 1011 | C6 | 63 |
| 1100 | C8 | 64 |
| 1101 | CA | 65 |
| 1110 | CC | 66 |
| 1111 | CE | 67 |

The SDA/SCL pins are 3.3 V tolerant, but are not 5 V tolerant. An external pullup resistor is required on the SDA and SCL line. The resistor value can be from 2 kΩ to 5 kΩ depending on the voltage, loading, and speed.

8.5.2 Transfer of Data Through the SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A high-to-low transition on SDA while SCL is High indicates a message START condition.

STOP: A low-to-high transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

8.5.3 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit ("0").
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

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8.5.4 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1” indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

8.5.5 SMBus Master Mode

The DS80PCI800 device supports reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS80PCI800 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Set ENSMB = Float — enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0 and capable of 1 MHz operation at 2.5 V and 3.3 V supply. The maximum allowed size is 8 kbits (1024 bytes).
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is 0xB0.

When tying multiple DS80PCI800 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded its configuration from the EEPROM. Example below is for 4 devices.
 - U1: AD[3:0] = 0000 = 0xB0
 - U2: AD[3:0] = 0001 = 0xB2
 - U3: AD[3:0] = 0010 = 0xB4
 - U4: AD[3:0] = 0011 = 0xB6
- Use a pullup resistor on SDA and SCL; value = 2 kΩ
- Daisy-chain $\overline{\text{READ_EN}}$ (pin 26) and $\overline{\text{ALL_DONE}}$ (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
 1. Tie $\overline{\text{READ_EN}}$ of the first device in the chain (U1) to GND
 2. Tie $\overline{\text{ALL_DONE}}$ of U1 to $\overline{\text{READ_EN}}$ of U2
 3. Tie $\overline{\text{ALL_DONE}}$ of U2 to $\overline{\text{READ_EN}}$ of U3
 4. Tie $\overline{\text{ALL_DONE}}$ of U3 to $\overline{\text{READ_EN}}$ of U4
 5. Optional: Tie $\overline{\text{ALL_DONE}}$ output of U4 to a LED to show the devices have been loaded successfully

The following example represents a 2 kbits (256 × 8-bit) EEPROM in hex format for the DS80PCI800 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the SMBus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (0xA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS80PCI800 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS80PCI800 device.

```
:2000000000001000000407002FAD4002FAD4002FAD4002FAD401805F5A8005F5A8005F5AD8
:200020008005F5A8000054540000000000000000000000000000000000000000000000000000F6
:2000600000000000000000000000000000000000000000000000000000000000000000000080
:2000800000000000000000000000000000000000000000000000000000000000000000000060
:2000A00000000000000000000000000000000000000000000000000000000000000000000040
:2000C00000000000000000000000000000000000000000000000000000000000000000000020
:2000E00000000000000000000000000000000000000000000000000000000000000000000000
:20004000000000000000000000000000000000000000000000000000000000000000000000A0
```

For more information in regards to EEPROM programming and the hex format, see [SNLA228](#).

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8.6 Register Maps**Table 7. EEPROM Register Map - Single Device with Default Value**

| EEPROM Address Byte | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|------|--------------------------|--------------------------|--------------------------|--------------------------|---------------------------------|--------------------------|--------------------------|--------------------------|
| Description | 0x00 | CRC EN | Address Map Present | EEPROM > 256 Bytes | RES | DEVICE COUNT[3] | DEVICE COUNT[2] | DEVICE COUNT[1] | DEVICE COUNT[0] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x01 | RES | RES | RES | RES | RES | RES | RES | RES |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x02 | Max EEPROM Burst size[7] | Max EEPROM Burst size[6] | Max EEPROM Burst size[5] | Max EEPROM Burst size[4] | Max EEPROM Burst size[3] | Max EEPROM Burst size[2] | Max EEPROM Burst size[1] | Max EEPROM Burst size[0] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x03 | PWDN_ch7 | PWDN_ch6 | PWDN_ch5 | PWDN_ch4 | PWDN_ch3 | PWDN_ch2 | PWDN_ch1 | PWDN_ch0 |
| SMBus Register | | 0x01[7] | 0x01[6] | 0x01[5] | 0x01[4] | 0x01[3] | 0x01[2] | 0x01[1] | 0x01[0] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x04 | lpbk_1 | lpbk_0 | PWDN_INPUTS | PWDN_OSC | Ovrd_P $\overline{\text{RSNT}}$ | RES | RES | RES |
| SMBus Register | | 0x02[5] | 0x02[4] | 0x02[3] | 0x02[2] | 0x02[0] | 0x04[7] | 0x04[6] | 0x04[5] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x05 | RES | RES | RES | RES | RES | rxdet_btb_en | Ovrd_idle_th | Ovrd_RES |
| SMBus Register | | 0x04[4] | 0x04[3] | 0x04[2] | 0x04[1] | 0x04[0] | 0x06[4] | 0x08[6] | 0x08[5] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Description | 0x06 | Ovrd_IDLE | Ovrd_RX_DET | Ovrd_RATE | RES | RES | rx_delay_sel_2 | rx_delay_sel_1 | rx_delay_sel_0 |
| SMBus Register | | 0x08[4] | 0x08[3] | 0x08[2] | 0x08[1] | 0x08[0] | 0x0B[6] | 0x0B[5] | 0x0B[4] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Description | 0x07 | RD_delay_sel_3 | RD_delay_sel_2 | RD_delay_sel_1 | RD_delay_sel_0 | ch0_Idle_auto | ch0_Idle_sel | ch0_RXDET_1 | ch0_RXDET_0 |
| SMBus Register | | 0x0B[3] | 0x0B[2] | 0x0B[1] | 0x0B[0] | 0x0E[5] | 0x0E[4] | 0x0E[3] | 0x0E[2] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Register Maps (continued)
Table 7. EEPROM Register Map - Single Device with Default Value (continued)

| EEPROM Address Byte | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Description | 0x08 | ch0_BST_7 | ch0_BST_6 | ch0_BST_5 | ch0_BST_4 | ch0_BST_3 | ch0_BST_2 | ch0_BST_1 | ch0_BST_0 |
| SMBus Register | | 0x0F[7] | 0x0F[6] | 0x0F[5] | 0x0F[4] | 0x0F[3] | 0x0F[2] | 0x0F[1] | 0x0F[0] |
| Default Value | | 0x2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| Description | 0x09 | ch0_Sel_scp | ch0_Sel_mode | ch0_RES_2 | ch0_RES_1 | ch0_RES_0 | ch0_VOD_2 | ch0_VOD_1 | ch0_VOD_0 |
| SMBus Register | | 0x10[7] | 0x10[6] | 0x10[5] | 0x10[4] | 0x10[3] | 0x10[2] | 0x10[1] | 0x10[0] |
| Default Value | | 0xAD | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| Description | 0x0A | ch0_DEM_2 | ch0_DEM_1 | ch0_DEM_0 | ch0_Slow | ch0_idle_tha_1 | ch0_idle_tha_0 | ch0_idle_thd_1 | ch0_idle_thd_0 |
| SMBus Register | | 0x11[2] | 0x11[1] | 0x11[0] | 0x12[7] | 0x12[3] | 0x12[2] | 0x12[1] | 0x12[0] |
| Default Value | | 0x40 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x0B | ch1_Idle_auto | ch1_Idle_sel | ch1_RXDET_1 | ch1_RXDET_0 | ch1_BST_7 | ch1_BST_6 | ch1_BST_5 | ch1_BST_4 |
| SMBus Register | | 0x15[5] | 0x15[4] | 0x15[3] | 0x15[2] | 0x16[7] | 0x16[6] | 0x16[5] | 0x16[4] |
| Default Value | | 0x02 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Description | 0x0C | ch1_BST_3 | ch1_BST_2 | ch1_BST_1 | ch1_BST_0 | ch1_Sel_scp | ch1_Sel_mode | ch1_RES_2 | ch1_RES_1 |
| SMBus Register | | 0x16[3] | 0x16[2] | 0x16[1] | 0x16[0] | 0x17[7] | 0x17[6] | 0x17[5] | 0x17[4] |
| Default Value | | 0xFA | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| Description | 0x0D | ch1_RES_0 | ch1_VOD_2 | ch1_VOD_1 | ch1_VOD_0 | ch1_DEM_2 | ch1_DEM_1 | ch1_DEM_0 | ch1_Slow |
| SMBus Register | | 0x17[3] | 0x17[2] | 0x17[1] | 0x17[0] | 0x18[2] | 0x18[1] | 0x18[0] | 0x19[7] |
| Default Value | | 0xD4 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| Description | 0x0E | ch1_idle_tha_1 | ch1_idle_tha_0 | ch1_idle_thd_1 | ch1_idle_thd_0 | ch2_Idle_auto | ch2_Idle_sel | ch2_RXDET_1 | ch2_RXDET_0 |
| SMBus Register | | 0x19[3] | 0x19[2] | 0x19[1] | 0x19[0] | 0x1C[5] | 0x1C[4] | 0x1C[3] | 0x1C[2] |
| Default Value | | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x0F | ch2_BST_7 | ch2_BST_6 | ch2_BST_5 | ch2_BST_4 | ch2_BST_3 | ch2_BST_2 | ch2_BST_1 | ch2_BST_0 |
| SMBus Register | | 0x1D[7] | 0x1D[6] | 0x1D[5] | 0x1D[4] | 0x1D[3] | 0x1D[2] | 0x1D[1] | 0x1D[0] |
| Default Value | | 0x2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

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Register Maps (continued)**Table 7. EEPROM Register Map - Single Device with Default Value (continued)**

| EEPROM Address Byte | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|------|----------------|----------------|----------------|----------------|----------------|-------------------|-------------------|----------------|
| Description | 0x10 | ch2_Sel_scp | ch2_Sel_mode | ch2_RES_2 | ch2_RES_1 | ch2_RES_0 | ch2_VOD_2 | ch2_VOD_1 | ch2_VOD_0 |
| SMBus Register | | 0x1E[7] | 0x1E[6] | 0x1E[5] | 0x1E[4] | 0x1E[3] | 0x1E[2] | 0x1E[1] | 0x1E[0] |
| Default Value | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| Description | 0x11 | ch2_DEM_2 | ch2_DEM_1 | ch2_DEM_0 | ch2_Slow | ch2_idle_tha_1 | ch2_idle_tha_0 | ch2_idle_thd_1 | ch2_idle_thd_0 |
| SMBus Register | | 0x1F[2] | 0x1F[1] | 0x1F[0] | 0x20[7] | 0x20[3] | 0x20[2] | 0x20[1] | 0x20[0] |
| Default Value | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x12 | ch3_Idle_auto | ch3_Idle_sel | ch3_RXDET_1 | ch3_RXDET_0 | ch3_BST_7 | ch3_BST_6 | ch3_BST_5 | ch3_BST_4 |
| SMBus Register | | 0x23[5] | 0x23[4] | 0x23[3] | 0x23[2] | 0x24[7] | 0x24[6] | 0x24[5] | 0x24[4] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Description | 0x13 | ch3_BST_3 | ch3_BST_2 | ch3_BST_1 | ch3_BST_0 | ch3_Sel_scp | ch3_Sel_mode | ch3_RES_2 | ch3_RES_1 |
| SMBus Register | | 0x24[3] | 0x24[2] | 0x24[1] | 0x24[0] | 0x25[7] | 0x25[6] | 0x25[5] | 0x25[4] |
| Default Value | | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Description | 0x14 | ch3_RES_0 | ch3_VOD_2 | ch3_VOD_1 | ch3_VOD_0 | ch3_DEM_2 | ch3_DEM_1 | ch3_DEM_0 | ch3_Slow |
| SMBus Register | | 0x25[3] | 0x25[2] | 0x25[1] | 0x25[0] | 0x26[2] | 0x26[1] | 0x26[0] | 0x27[7] |
| Default Value | | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | 0x15 | ch3_idle_tha_1 | ch3_idle_tha_0 | ch3_idle_thd_1 | ch3_idle_thd_0 | ovrd_fast_idle | en_high_idle_th_n | en_high_idle_th_s | en_fast_idle_n |
| SMBus Register | | 0x27[3] | 0x27[2] | 0x27[1] | 0x27[0] | 0x28[6] | 0x28[5] | 0x28[4] | 0x28[3] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Description | 0x16 | en_fast_idle_s | eqsd_mgain_n | eqsd_mgain_s | ch4_Idle_auto | ch4_Idle_sel | ch4_RXDET_1 | ch4_RXDET_0 | ch4_BST_7 |
| SMBus Register | | 0x28[2] | 0x28[1] | 0x28[0] | 0x2B[5] | 0x2B[4] | 0x2B[3] | 0x2B[2] | 0x2C[7] |
| Default Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x17 | ch4_BST_6 | ch4_BST_5 | ch4_BST_4 | ch4_BST_3 | ch4_BST_2 | ch4_BST_1 | ch4_BST_0 | ch4_Sel_scp |
| SMBus Register | | 0x2C[6] | 0x2C[5] | 0x2C[4] | 0x2C[3] | 0x2C[2] | 0x2C[1] | 0x2C[0] | 0x2D[7] |
| Default Value | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

Register Maps (continued)
Table 7. EEPROM Register Map - Single Device with Default Value (continued)

| EEPROM Address Byte | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Description | 0x18 | ch4_Sel_mode | ch4_RES_2 | ch4_RES_1 | ch4_RES_0 | ch4_VOD_2 | ch4_VOD_1 | ch4_VOD_0 | ch4_DEM_2 |
| SMBus Register | | 0x2D[6] | 0x2D[5] | 0x2D[4] | 0x2D[3] | 0x2D[2] | 0x2D[1] | 0x2D[0] | 0x2E[2] |
| Default Value | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| <hr/> | | | | | | | | | |
| Description | 0x19 | ch4_DEM_1 | ch4_DEM_0 | ch4_Slow | ch4_idle_tha_1 | ch4_idle_tha_0 | ch4_idle_thd_1 | ch4_idle_thd_0 | ch5_idle_auto |
| SMBus Register | | 0x2E[1] | 0x2E[0] | 0x2F[7] | 0x2F[3] | 0x2F[2] | 0x2F[1] | 0x2F[0] | 0x32[5] |
| Default Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <hr/> | | | | | | | | | |
| Description | 0x1A | ch5_Idle_sel | ch5_RXDET_1 | ch5_RXDET_0 | ch5_BST_7 | ch5_BST_6 | ch5_BST_5 | ch5_BST_4 | ch5_BST_3 |
| SMBus Register | | 0x32[4] | 0x32[3] | 0x32[2] | 0x33[7] | 0x33[6] | 0x33[5] | 0x33[4] | 0x33[3] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| <hr/> | | | | | | | | | |
| Description | 0x1B | ch5_BST_2 | ch5_BST_1 | ch5_BST_0 | ch5_Sel_scp | ch5_Sel_mode | ch5_RES_2 | ch5_RES_1 | ch5_RES_0 |
| SMBus Register | | 0x33[2] | 0x33[1] | 0x33[0] | 0x34[7] | 0x34[6] | 0x34[5] | 0x34[4] | 0x34[3] |
| Default Value | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| <hr/> | | | | | | | | | |
| Description | 0x1C | ch5_VOD_2 | ch5_VOD_1 | ch5_VOD_0 | ch5_DEM_2 | ch5_DEM_1 | ch5_DEM_0 | ch5_Slow | ch5_idle_tha_1 |
| SMBus Register | | 0x34[2] | 0x34[1] | 0x34[0] | 0x35[2] | 0x35[1] | 0x35[0] | 0x36[7] | 0x36[3] |
| Default Value | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| <hr/> | | | | | | | | | |
| Description | 0x1D | ch5_idle_tha_0 | ch5_idle_thd_1 | ch5_idle_thd_0 | ch6_Idle_auto | ch6_Idle_sel | ch6_RXDET_1 | ch6_RXDET_0 | ch6_BST_7 |
| SMBus Register | | 0x36[2] | 0x36[1] | 0x36[0] | 0x39[5] | 0x39[4] | 0x39[3] | 0x39[2] | 0x3A[7] |
| Default Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <hr/> | | | | | | | | | |
| Description | 0x1E | ch6_BST_6 | ch6_BST_5 | ch6_BST_4 | ch6_BST_3 | ch6_BST_2 | ch6_BST_1 | ch6_BST_0 | ch6_Sel_scp |
| SMBus Register | | 0x3A[6] | 0x3A[5] | 0x3A[4] | 0x3A[3] | 0x3A[2] | 0x3A[1] | 0x3A[0] | 0x3B[7] |
| Default Value | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| <hr/> | | | | | | | | | |
| Description | 0x1F | ch6_Sel_mode | ch6_RES_2 | ch6_RES_1 | ch6_RES_0 | ch6_VOD_2 | ch6_VOD_1 | ch6_VOD_0 | ch6_DEM_2 |
| SMBus Register | | 0x3B[6] | 0x3B[5] | 0x3B[4] | 0x3B[3] | 0x3B[2] | 0x3B[1] | 0x3B[0] | 0x3C[2] |
| Default Value | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

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Register Maps (continued)**Table 7. EEPROM Register Map - Single Device with Default Value (continued)**

| EEPROM Address Byte | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Description | 0x20 | ch6_DEM_1 | ch6_DEM_0 | ch6_Slow | ch6_idle_tha_1 | ch6_idle_tha_0 | ch6_idle_thd_1 | ch6_idle_thd_0 | ch7_idle_auto |
| SMBus Register | | 0x3C[1] | 0x3C[0] | 0x3D[7] | 0x3D[3] | 0x3D[2] | 0x3D[1] | 0x3D[0] | 0x40[5] |
| Default Value | | 0x80 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x21 | ch7_idle_sel | ch7_RXDET_1 | ch7_RXDET_0 | ch7_BST_7 | ch7_BST_6 | ch7_BST_5 | ch7_BST_4 | ch7_BST_3 |
| SMBus Register | | 0x40[4] | 0x40[3] | 0x40[2] | 0x41[7] | 0x41[6] | 0x41[5] | 0x41[4] | 0x41[3] |
| Default Value | | 0x05 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Description | 0x22 | ch7_BST_2 | ch7_BST_1 | ch7_BST_0 | ch7_Sel_scp | ch7_Sel_mode | ch7_RES_2 | ch7_RES_1 | ch7_RES_0 |
| SMBus Register | | 0x41[2] | 0x41[1] | 0x41[0] | 0x42[7] | 0x42[6] | 0x42[5] | 0x42[4] | 0x42[3] |
| Default Value | | 0xF5 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Description | 0x23 | ch7_VOD_2 | ch7_VOD_1 | ch7_VOD_0 | ch7_DEM_2 | ch7_DEM_1 | ch7_DEM_0 | ch7_Slow | ch7_idle_tha_1 |
| SMBus Register | | 0x42[2] | 0x42[1] | 0x42[0] | 0x43[2] | 0x43[1] | 0x43[0] | 0x44[7] | 0x44[3] |
| Default Value | | 0xA8 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | 0x24 | ch7_idle_tha_0 | ch7_idle_thd_1 | ch7_idle_thd_0 | iph_dac_ns_1 | iph_dac_ns_0 | ipp_dac_ns_1 | ipp_dac_ns_0 | ipp_dac_1 |
| SMBus Register | | 0x44[2] | 0x44[1] | 0x44[0] | 0x47[3] | 0x47[2] | 0x47[1] | 0x47[0] | 0x48[7] |
| Default Value | | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x25 | ipp_dac_0 | RD23_67 | RD01_45 | RD_PD_ovrd | RD_Sel_test | RD_RESET_ovrd | PWDB_input_DC | DEM_VOD_ovrd |
| SMBus Register | | 0x48[6] | 0x4C[7] | 0x4C[6] | 0x4C[5] | 0x4C[4] | 0x4C[3] | 0x4C[0] | 0x59[0] |
| Default Value | | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 0x26 | DEM_ovrd_N2 | DEM_ovrd_N1 | DEM_ovrd_N0 | VOD_ovrd_N2 | VOD_ovrd_N1 | VOD_ovrd_N0 | SPARE0 | SPARE1 |
| SMBus Register | | 0x5A[7] | 0x5A[6] | 0x5A[5] | 0x5A[4] | 0x5A[3] | 0x5A[2] | 0x5A[1] | 0x5A[0] |
| Default Value | | 0x54 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| Description | 0x27 | DEM_ovrd_S2 | DEM_ovrd_S1 | DEM_ovrd_S0 | VOD_ovrd_S2 | VOD_ovrd_S1 | VOD_ovrd_S0 | SPARE0 | SPARE1 |
| SMBus Register | | 0x5B[7] | 0x5B[6] | 0x5B[5] | 0x5B[4] | 0x5B[3] | 0x5B[2] | 0x5B[1] | 0x5B[0] |
| Default Value | | 0x54 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

Table 8. Multi DS80PCI800 EEPROM Data⁽¹⁾

| EEPROM Address | Address (Hex) | EEPROM Data | Comments |
|----------------|---------------|-------------|--|
| 0 | 00 | 0x43 | CRC_EN = 0, Address Map = 1, >256 bytes = 0, Device Count[3:0] = 3 |
| 1 | 01 | 0x00 | |
| 2 | 02 | 0x10 | EEPROM Burst Size |
| 3 | 03 | 0x00 | CRC not used |
| 4 | 04 | 0x0B | Device 0 Address Location |
| 5 | 05 | 0x00 | CRC not used |
| 6 | 06 | 0x0B | Device 1 Address Location |
| 7 | 07 | 0x00 | CRC not used |
| 8 | 08 | 0x30 | Device 2 Address Location |
| 9 | 09 | 0x00 | CRC not used |
| 10 | 0A | 0x30 | Device 3 Address Location |
| 11 | 0B | 0x00 | Begin Device 0, 1 - Address Offset 3 |
| 12 | 0C | 0x00 | |
| 13 | 0D | 0x04 | |
| 14 | 0E | 0x07 | |
| 15 | 0F | 0x00 | |
| 16 | 10 | 0x00 | EQ CHB_0 = 0x00 |
| 17 | 11 | 0xAB | VOD CHB_0 = 1.0 V |
| 18 | 12 | 0x00 | DEM CHB_0 = 0 (0 dB) |
| 19 | 13 | 0x00 | EQ CHB_1 = 0x00 |
| 20 | 14 | 0x0A | VOD CHB_1 = 1.0 V |
| 21 | 15 | 0xB0 | DEM CHB_1 = 0 (0 dB) |
| 22 | 16 | 0x00 | |
| 23 | 17 | 0x00 | EQ CHB_2 = 0x00 |
| 24 | 18 | 0xAB | VOD CHB_2 = 1.0 V |
| 25 | 19 | 0x00 | DEM CHB_2 = 0 (0 dB) |
| 26 | 1A | 0x00 | EQ CHB_3 = 0x00 |
| 27 | 1B | 0x0A | VOD CHB_3 = 1.0 V |
| 28 | 1C | 0xB0 | DEM CHB_3 = 0 (0 dB) |
| 29 | 1D | 0x01 | |
| 30 | 1E | 0x80 | |
| 31 | 1F | 0x01 | EQ CHA_0 = 0x00 |
| 32 | 20 | 0x56 | VOD CHA_0 = 1.0 V |
| 33 | 21 | 0x00 | DEM CHA_0 = 0 (0 dB) |
| 34 | 22 | 0x00 | EQ CHA_1 = 0x00 |
| 35 | 23 | 0x15 | VOD CHA_1 = 1.0 V |
| 36 | 24 | 0x60 | DEM CHA_1 = 0 (0 dB) |
| 37 | 25 | 0x00 | |
| 38 | 26 | 0x01 | EQ CHA_2 = 0x00 |
| 39 | 27 | 0x56 | VOD CHA_2 = 1.0 V |
| 40 | 28 | 0x00 | DEM CHA_2 = 0 (0 dB) |
| 41 | 29 | 0x00 | EQ CHA_3 = 0x00 |
| 42 | 2A | 0x15 | VOD CHA_3 = 1.0 V |
| 43 | 2B | 0x60 | DEM CHA_3 = 0 (0 dB) |
| 44 | 2C | 0x00 | |

(1) CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. This example has all 8 channels set to EQ = 0x00 (min boost), VOD = 1.0 V, DEM = 0 (0 dB) and multiple device can point to the same address map.

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Table 8. Multi DS80PCI800 EEPROM Data⁽¹⁾ (continued)

| EEPROM Address | Address (Hex) | EEPROM Data | Comments |
|----------------|---------------|-------------|--------------------------------------|
| 45 | 2D | 0x00 | |
| 46 | 2E | 0x54 | |
| 47 | 2F | 0x54 | End Device 0, 1 - Address Offset 39 |
| 48 | 30 | 0x00 | Begin Device 2, 3 - Address Offset 3 |
| 49 | 31 | 0x00 | |
| 50 | 32 | 0x04 | |
| 51 | 33 | 0x07 | |
| 52 | 34 | 0x00 | |
| 53 | 35 | 0x00 | EQ CHB_0 = 0x00 |
| 54 | 36 | 0xAB | VOD CHB_0 = 1.0 V |
| 55 | 37 | 0x00 | DEM CHB_0 = 0 (0 dB) |
| 56 | 38 | 0x00 | EQ CHB_1 = 0x00 |
| 57 | 39 | 0x0A | VOD CHB_1 = 1.0 V |
| 58 | 3A | 0xB0 | DEM CHB_1 = 0 (0 dB) |
| 59 | 3B | 0x00 | |
| 60 | 3C | 0x00 | EQ CHB_2 = 0x00 |
| 61 | 3D | 0xAB | VOD CHB_2 = 1.0 V |
| 62 | 3E | 0x00 | DEM CHB_2 = 0 (0 dB) |
| 63 | 3F | 0x00 | EQ CHB_3 = 0x00 |
| 64 | 40 | 0x0A | VOD CHB_3 = 1.0 V |
| 65 | 41 | 0xB0 | DEM CHB_3 = 0 (0 dB) |
| 66 | 42 | 0x01 | |
| 67 | 43 | 0x80 | |
| 68 | 44 | 0x01 | EQ CHA_0 = 0x00 |
| 69 | 45 | 0x56 | VOD CHA_0 = 1.0 V |
| 70 | 46 | 0x00 | DEM CHA_0 = 0 (0 dB) |
| 71 | 47 | 0x00 | EQ CHA_1 = 0x00 |
| 72 | 48 | 0x15 | VOD CHA_1 = 1.0 V |
| 73 | 49 | 0x60 | DEM CHA_1 = 0 (0 dB) |
| 74 | 4A | 0x00 | |
| 75 | 4B | 0x01 | EQ CHA_2 = 0x00 |
| 76 | 4C | 0x56 | VOD CHA_2 = 1.0 V |
| 77 | 4D | 0x00 | DEM CHA_2 = 0 (0 dB) |
| 78 | 4E | 0x00 | EQ CHA_3 = 0x00 |
| 79 | 4F | 0x15 | VOD CHA_3 = 1.0 V |
| 80 | 50 | 0x60 | DEM CHA_3 = 0 (0 dB) |
| 81 | 51 | 0x00 | |
| 82 | 52 | 0x00 | |
| 83 | 53 | 0x54 | |
| 84 | 54 | 0x54 | End Device 2, 3 - Address Offset 39 |

Table 9. SMBus Slave Mode Register Map

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description | |
|---------|----------------------------|-----|---------------------|------|---------|------------|---|--|
| 0x00 | Device Address Observation | 7 | Reserved | R/W | 0x00 | | Set bit to 0 | |
| | | 6:3 | Address Bit AD[3:0] | R | | | Observation of AD[3:0] bit [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0 See Table 6 | |
| | | 2 | EEPROM Read Done | R | | | 1: Device completed the read from external EEPROM | |
| | | 1:0 | Reserved | R/W | | | Reserved | |
| 0x01 | PWDN Channels | 7:0 | PWDN CHx | R/W | 0x00 | Yes | Power Down per Channel [7]: CH7 – CHA_3 [6]: CH6 – CHA_2 [5]: CH5 – CHA_1 [4]: CH4 – CHA_0 [3]: CH3 – CHB_3 [2]: CH2 – CHB_2 [1]: CH1 – CHB_1 [0]: CH0 – CHB_0 0x00 = all channels enabled 0xFF = all channels disabled Note: override PRSNT pin | |
| 0x02 | Override PRSNT Control | 7 | Override RXDET | R/W | 0x00 | | 1 = Override Automatic Rx Detect State Machine Reset | |
| | | 6 | RXDET Value | | | | 1 = Set Rx Detect State Machine Reset 0 = Clear Rx Detect State Machine Reset | |
| | | 5:2 | Reserved | | | | Yes | Set bits to 0 |
| | | 1 | Reserved | | | | | Set bit to 0 |
| | | 0 | Override PRSNT | | | | Yes | 1: Block PRSNT pin control 0: Allow PRSNT pin control |
| 0x03 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 | |
| 0x04 | Reserved | 7:0 | Reserved | R/W | 0x00 | Yes | Set bits to 0 | |
| 0x05 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 | |
| 0x06 | Slave Register Control | 7:5 | Reserved | R/W | 0x10 | | Set bits to 0 | |
| | | 4 | Reserved | | | | Yes | Set bit to 1 |
| | | 3 | Register Enable | | | | | 1 = Enables SMBus Slave Mode Register Control Note: To change VOD, DEM, and EQ of the channels in slave mode, this bit must be set to 1. |
| | | 2:0 | Reserved | | | | | Set bits to 0 |
| 0x07 | Digital Reset Control | 7 | Reserved | R/W | 0x01 | | Set bit to 0 | |
| | | 6 | Reset Registers | | | | | Self clearing bit, set to 1 to reset the register to default values. |
| | | 5:0 | Reserved | | | | | Set bits to 000001'b |

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Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|-------------------------|-----|----------------|------|---------|------------|--|
| 0x08 | Override Pin Control | 7 | Reserved | R/W | 0x00 | | Set bit to 0 |
| | | 6 | Override SD_TH | | | Yes | 1: Block SD_TH pin control 0: Allow SD_TH pin control |
| | | 5 | Reserved | | | Yes | Set bit to 0 |
| | | 4 | Override IDLE | | | Yes | 1: IDLE control by registers 0: IDLE control by signal detect |
| | | 3 | Override RXDET | | | Yes | 1: Block RXDET pin control 0: Allow RXDET pin control |
| | | 2 | Override RATE | | | Yes | 1: Block RATE pin control 0: Allow RATE pin control |
| | | 1:0 | Reserved | | | | Set bit to 0 |
| 0x09 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x0A | Signal Detect Monitor | 7:0 | SD_TH Status | R | 0x00 | | CH7 - CH0 Internal Signal Detector Indicator [7]: CH7 - CHA_3 [6]: CH6 - CHA_2 [5]: CH5 - CHA_1 [4]: CH4 - CHA_0 [3]: CH3 - CHB_3 [2]: CH2 - CHB_2 [1]: CH1 - CHB_1 [0]: CH0 - CHB_0 0 = Signal detected at input (active data) 1 = Signal not detected at input (idle state) NOTE: These bits only function when RATE pin = FLOAT. |
| 0x0B | Reserved | 7 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 6:0 | Reserved | R/W | 0x70 | Yes | Set bits to 111 0000'b |
| 0x0C | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x0D | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x0E | CH0 - CHB_0 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: Override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x0F | CH0 - CHB_0 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_0 EQ Control - total of 256 levels See Table 2 |

Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|----------------------------|-----|--------------------------|------|---------|------------|--|
| 0x10 | CH0 - CHB_0 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | OUTB_0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |
| 0x11 | CH0 - CHB_0 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH0 - CHB_0 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | | Observation bit for RATE_DET CH0 - CHB_0 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | R/W | | Yes | OUTB_0 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |
| 0x12 | CH0 - CHB_0 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x13 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x14 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |

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Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|----------------------------|-----|-----------------------------|------|---------|---|--|
| 0x15 | CH1 - CHB_1 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: Override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0. |
| 0x16 | CH1 - CHB_1 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_1 EQ Control - total of 256 levels. See Table 2 |
| 0x17 | CH1 - CHB_1 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | OUTB_1 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |
| 0x18 | CH1 - CHB_1 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH1 - CHB_1 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | Observation bit for RATE_DET CH1 - CHB_1 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) | |
| | | 4:3 | Reserved | R/W | | Set bits to 0 | |
| | | 2:0 | DEM Control | R/W | | Yes | OUTB_1 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |

Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|-------------------------------|-----|-----------------------------|------|---------|------------|--|
| 0x19 | CH1 - CHB_1 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0. |
| | | 6:4 | Reserved | | | | Set bits to 0. |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x1A | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x1B | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x1C | CH2 - CHB_2 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: Override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x1D | CH2 - CHB_2 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_2 EQ Control - total of 256 levels. See Table 2 |
| 0x1E | CH2 - CHB_2 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | OUTB_2 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |

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Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|----------------------------|-----|-----------------|------|---------|------------|--|
| 0x1F | CH2 - CHB_2 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH2 - CHB_2 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | | Observation bit for RATE_DET CH2 - CHB_2 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) |
| | | 4:3 | Reserved | R/W | | | Set bits to 0. |
| | | 2:0 | DEM Control | R/W | | Yes | OUTB_2 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |
| 0x20 | CH2 - CHB_2 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin. Set bits to 0 |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x21 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x22 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x23 | CH3 - CHB_3 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control. |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: Override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x24 | CH3 - CHB_3 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_3 EQ Control - total of 256 levels. See Table 2 |

Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|------------------------------|-----|---------------------------|------|---------|------------|---|
| 0x25 | CH3 - CHB_3 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | OUTB_3 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |
| 0x26 | CH3 - CHB_3 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH3 - CHB_3 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | | Observation bit for RATE_DET CH3 - CHB_3 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | R/W | | Yes | OUTB_3 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |
| 0x27 | CH3 - CHB_3 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x28 | Signal Detect Status Control | 7 | Reserved | R/W | 0x0C | | Set bit to 0 |
| | | 6 | Reserved | | | Yes | Set bit to 0 |
| | | 5:4 | High SD_TH Status | | | Yes | Enable Higher Range of Signal Detect Status Thresholds [5]: CH0 - CH3 [4]: CH4 - CH7 |
| | | 3:2 | Fast Signal Detect Status | | | Yes | Enable Fast Signal Detect Status [3]: CH0 - CH3 [2]: CH4 - CH7 Note: In Fast Signal Detect, assert/deassert response occurs after approximately 3-4 ns |
| | | 1:0 | Reduced SD Status Gain | | | Yes | Enable Reduced Signal Detect Status Gain [1]: CH0 - CH3 [0]: CH4 - CH7 |

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Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|----------------------------|-----|-----------------------------|------|---------|------------|--|
| 0x29 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x2A | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x2B | CH4 - CHA_0 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: Override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x2C | CH4 - CHA_0 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_0 EQ Control - total of 256 levels See Table 2 |
| 0x2D | CH4 - CHA_0 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | OUTA_0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |
| 0x2E | CH4 - CHA_0 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH4 - CHA_0 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | | Observation bit for RATE_DET CH4 - CHA_0 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | R/W | | Yes | OUTA_0 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |

Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|-------------------------------|-----|-----------------------------|------|---------|------------|--|
| 0x2F | CH4 - CHA_0 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x30 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x31 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x32 | CH5 - CHA_1 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x33 | CH5 - CHA_1 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_1 EQ Control - total of 256 levels See Table 2 |
| 0x34 | CH5 - CHA_1 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | QUTA_1 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |

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Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|----------------------------|-----|-----------------|------|---------|------------|--|
| 0x35 | CH5 - CHA_1 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH5 - CHA_1 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | | Observation bit for RATE_DET CH5 - CHA_1 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | R/W | | Yes | OUTA_1 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |
| 0x36 | CH5 - CHA_1 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x37 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x38 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x39 | CH6 - CHA_2 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: Override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x3A | CH6 - CHA_2 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_2 EQ Control - total of 256 levels See Table 2 |

Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|----------------------------|-----|--------------------------|------|---------|------------|--|
| 0x3B | CH6 - CHA_2 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | OUTA_2 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |
| 0x3C | CH6 - CHA_2 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH6 - CHA_2 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | | Observation bit for RATE_DET CH6 - CHA_2 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | R/W | | Yes | OUTA_2 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |
| 0x3D | CH6 - CHA_2 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x3E | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x3F | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |

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Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|----------------------------|-----|-----------------------------|------|---------|---|--|
| 0x40 | CH7 - CHA_3 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5 | IDLE_AUTO | | | Yes | 1 = Allow IDLE_SEL control in bit 4 0 = Automatic IDLE detect Note: Override IDLE control |
| | | 4 | IDLE_SEL | | | Yes | 1: Output is MUTED (electrical idle) 0: Output is ON Note: Override IDLE control |
| | | 3:2 | RXDET | | | Yes | 00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: Override RXDET pin |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x41 | CH7 - CHA_3 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_3 EQ Control - total of 256 levels See Table 2 |
| 0x42 | CH7 - CHA_3 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1: Enable the short circuit protection 0: Disable the short circuit protection |
| | | 6 | RATE_SEL | | | Yes | 1: Gen 1/2 0: Gen 3 Note: Override the RATE pin |
| | | 5:3 | Reserved | | | Yes | Set bits to default value - 101 |
| | | 2:0 | VOD Control | | | Yes | OUTA_3 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |
| 0x43 | CH7 - CHA_3 DEM | 7 | RXDET STATUS | R | 0x02 | | Observation bit for RXDET CH7 - CHA_3 1: RX = detected 0: RX = not detected |
| | | 6:5 | RATE_DET STATUS | R | | Observation bit for RATE_DET CH7 - CHA_3 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) | |
| | | 4:3 | Reserved | R/W | | Set bits to 0 | |
| | | 2:0 | DEM Control | R/W | | Yes | OUTA_3 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB |

Table 9. SMBus Slave Mode Register Map (continued)

| Address | Register Name | Bit | Field | Type | Default | EEPROM Bit | Description |
|---------|-------------------------------|-----|----------|------|---------|------------|--|
| 0x44 | CH7 - CHA_3 IDLE Threshold | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | IDLE tha | | | Yes | Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: Override the SD_TH pin |
| | | 1:0 | IDLE thd | | | Yes | Deassert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: Override the SD_TH pin |
| 0x45 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x46 | Reserved | 7:0 | Reserved | R/W | 0x38 | | Set bits to 0x38 |
| 0x47 | Reserved | 7:4 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 3:0 | Reserved | R/W | | Yes | Set bits to 0 |
| 0x48 | Reserved | 7:6 | Reserved | R/W | 0x05 | Yes | Set bits to 0 |
| | | 5:0 | Reserved | R/W | | | Set bits to 00 0101'b |
| 0x49 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x4A | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x4B | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x4C | Reserved | 7:3 | Reserved | R/W | 0x00 | Yes | Set bits to 0 |
| | | 2:1 | Reserved | R/W | | | Set bits to 0 |
| | | 0 | Reserved | R/W | | Yes | Set bits to 0 |
| 0x4D | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x4E | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x4F | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x50 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x51 | Device ID | 7:5 | VERSION | R | 0x45 | | 010'b |
| | | 4:0 | ID | | | | 00101'b |
| 0x52 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x53 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x54 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x55 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x56 | Reserved | 7:0 | Reserved | R/W | 0x10 | | Set bits to 0x10 |
| 0x57 | Reserved | 7:0 | Reserved | R/W | 0x64 | | Set bits to 0x64 |
| 0x58 | Reserved | 7:0 | Reserved | R/W | 0x21 | | Set bits to 0x21 |
| 0x59 | Reserved | 7:1 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 0 | Reserved | | | Yes | Set bit to 0 |
| 0x5A | Reserved | 7:0 | Reserved | R/W | 0x54 | Yes | Set bits to 0x54 |
| 0x5B | Reserved | 7:0 | Reserved | R/W | 0x54 | Yes | Set bits to 0x54 |
| 0x5C | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x5D | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x5E | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x5F | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x60 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x61 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |

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9 Application and Implementation**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information**9.1.1 DS80PCI800 versus DS80PCI810**

The DS80PCI800 and DS80PCI810 are pin compatible, and both can be used for PCIe Gen-1, 2, and 3 applications. The DS80PCI800 is ideal for closed PCIe systems where significant insertion losses (> 35 dB at 4 GHz) are expected in the signal path. A closed system is defined as a PCIe environment with a limited number of possible Host-to-Endpoint combinations. The DS80PCI800 can extend the reach of a PCIe system by up to 36 dB beyond the max allowable PCIe channel loss, whereas the DS80PCI810 can extend the system range up to 10 dB while offering a larger dynamic range on output linearity. Due to the larger CTLE gain, the DS80PCI800 is able to compensate insertion loss over longer transmission lines before the repeater. In addition, the DS80PCI800 is able to produce de-emphasis levels up to -12 dB to support significant trace losses after the repeater (-15 dB at 4 GHz).

9.1.2 Signal Integrity in PCIe Applications

In PCIe Gen-3 applications, the specification requires Rx-Tx link training to establish and optimize signal conditioning settings at 8 Gbps. In link training, the Rx partner requests a series of FIR - preshoot and de-emphasis coefficients (10 Presets) from the Tx partner. The Rx partner includes 7-levels (6 dB to 12 dB) of CTLE followed by a single tap DFE. The link training would pre-condition the signal with an equalized link between the root-complex and endpoint. Note that there is no link training in PCIe Gen-1 (2.5 Gbps) or PCIe Gen-2 (5.0 Gbps) applications. The DS80PCI800 is placed in between the Tx and Rx. It would help extend the PCB trace reach distance by boosting the attenuated signals with its equalization, so that the signal can be more easily recovered by the downstream Rx. In Gen 3 mode, DS80PCI800 transmit outputs are designed to pass the Tx Preset signaling onto the Rx for the PCIe Gen 3 link to train and optimize the equalization settings. The suggested setting for the DS80PCI800 are EQ = 0x00, VOD = 1.2 Vp-p and DEM = 0 dB. Additional adjustments to increase the EQ or DEM setting should be performed to optimize the eye opening in the Rx partner. See the tables below for Pin Mode and SMBus Mode configurations.

Table 10. Suggested Device Settings in Pin Mode

| Channel | Pin Mode Settings |
|-----------|---------------------|
| EQx[1:0] | 0, 0 (Level 1) |
| DEMx[1:0] | Float, R (Level 10) |

Table 11. Suggested Device Settings in SMBus Slave Mode

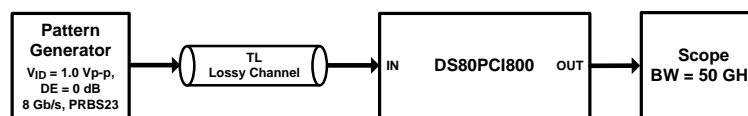
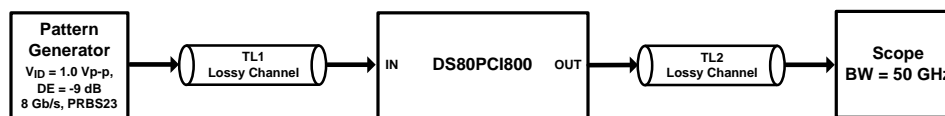
| Register | Write Value | Comments |
|----------|-------------|---|
| 0x06 | 0x18 | Enables SMBus Slave Mode Register Control |
| 0x0F | 0x00 | Set CHB_0 EQ to 0x00. |
| 0x10 | 0xAD | Set CHB_0 VOD to 101'b (1.2 Vp-p). |
| 0x11 | 0x00 | Set CHB_0 DEM to 000'b (0 dB). |
| 0x16 | 0x00 | Set CHB_1 EQ to 0x00. |
| 0x17 | 0xAD | Set CHB_1 VOD to 101'b (1.2 Vp-p). |
| 0x18 | 0x00 | Set CHB_1 DEM to 000'b (0 dB). |
| 0x1D | 0x00 | Set CHB_2 EQ to 0x00. |
| 0x1E | 0xAD | Set CHB_2 VOD to 101'b (1.2 Vp-p). |
| 0x1F | 0x00 | Set CHB_2 DEM to 000'b (0 dB). |
| 0x24 | 0x00 | Set CHB_3 EQ to 0x00. |

Table 11. Suggested Device Settings in SMBus Slave Mode (continued)

| Register | Write Value | Comments |
|----------|-------------|------------------------------------|
| 0x25 | 0xAD | Set CHB_3 VOD to 101'b (1.2 Vp-p). |
| 0x26 | 0x00 | Set CHB_3 DEM to 000'b (0 dB). |
| 0x2C | 0x00 | Set CHA_0 EQ to 0x00. |
| 0x2D | 0xAD | Set CHA_0 VOD to 101'b (1.2 Vp-p). |
| 0x2E | 0x00 | Set CHA_0 DEM to 000'b (0 dB). |
| 0x33 | 0x00 | Set CHA_1 EQ to 0x00. |
| 0x34 | 0xAD | Set CHA_1 VOD to 101'b (1.2 Vp-p). |
| 0x35 | 0x00 | Set CHA_1 DEM to 000'b (0 dB). |
| 0x3A | 0x00 | Set CHA_2 EQ to 0x00. |
| 0x3B | 0xAD | Set CHA_2 VOD to 101'b (1.2 Vp-p). |
| 0x3C | 0x00 | Set CHA_2 DEM to 000'b (0 dB). |
| 0x41 | 0x00 | Set CHA_3 EQ to 0x00. |
| 0x42 | 0xAD | Set CHA_3 VOD to 101'b (1.2 Vp-p). |
| 0x43 | 0x00 | Set CHA_3 DEM to 000'b (0 dB). |

9.2 Typical Application

The DS80PCI800 extends PCB trace and cable reach in PCIe Gen1, 2 and 3 applications by applying equalization to compensate for the insertion loss of the trace or cable. In Gen 3 mode, the device aids specifically in the equalization link training to improve the margin and overall eye inside the Rx. The DS80PCI800 can be used on the motherboard, mid plane (riser card), end-point target cards, and active cable assemblies. The capability of the DS80PCI800 performance is shown in the following two test setup connections.


Figure 8. Test Setup 1 Connections Diagram

Figure 9. Test Setup 2 Connections Diagram

9.2.1 Design Requirements

As with any high speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 100 Ω impedance traces. Length matching on the P and N traces should be done on the single-end segments of the differential pair.
- Use uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- For Gen3, AC-coupling capacitors of 220 nF are recommended, maximum body size is 0402, and add cutout void on GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use Reference plane vias to ensure a low inductance path for the return current.

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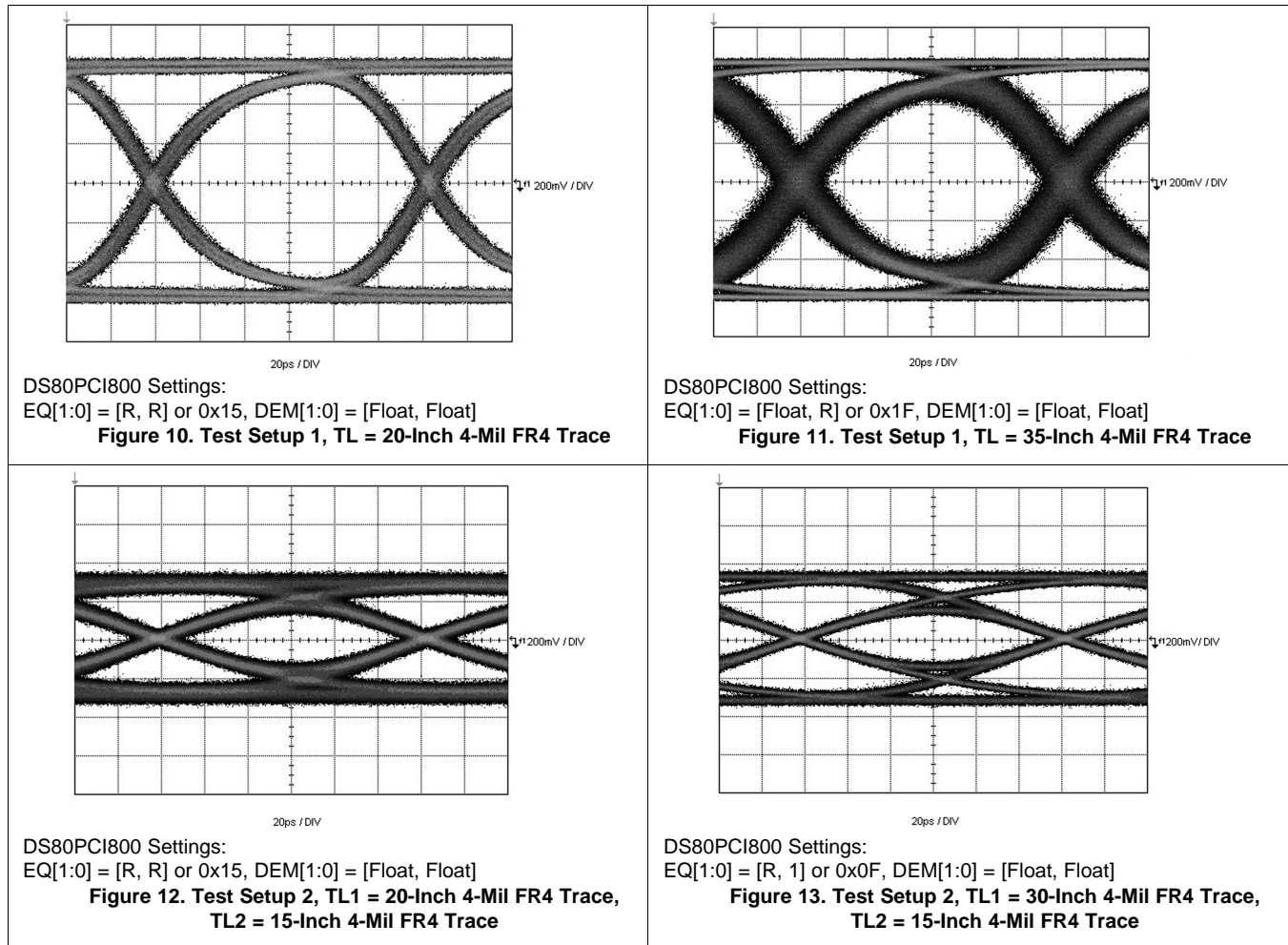
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Typical Application (continued)

9.2.2 Detailed Design Procedure

The DS80PCI800 should be placed at an offset location and close to the Rx with respect to the overall channel attenuation. The suggested settings are recommended as a starting point for most applications. Once these settings are configured, additional adjustments of the DS80PCI800 EQ or DE may be required to optimize the repeater performance. The CTLE and DFE coefficient in the Rx can also be adjusted to further improve the eye opening.

9.2.3 Application Curves



10 Power Supply Recommendations

10.1 3.3-V or 2.5-V Supply Mode Operation

The DS80PCI800 has an optional internal voltage regulator to provide the 2.5 V supply to the device. In 3.3-V mode, the VIN pin = 3.3 V is used to supply power to the device and the VDD pins should be left open. The internal regulator will provide the 2.5 V to the VDD pins of the device and a 0.1 μ F cap is needed at each of the five VDD pins for power supply de-coupling (total capacitance should be \leq 0.5 μ F), and the VDD pins should be left open. The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5-V mode, the VIN pin should be left open and 2.5 V supply must be applied to the VDD pins. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

The DS80PCI800 can be configured for 2.5 V operation or 3.3 V operation. The lists below outline required connections for each supply selection.

3.3-V Mode of Operation

1. Tie VDD_SEL = 0 with 1-k Ω resistor to GND.
2. Feed 3.3-V supply into VIN pin. Local 1.0- μ F decoupling at VIN is recommended.
3. See information on VDD bypass below.
4. SDA and SCL pins should connect pullup resistor to VIN
5. Any 4-Level input which requires a connection to "Logic 1" should use a 1-k Ω resistor to VIN

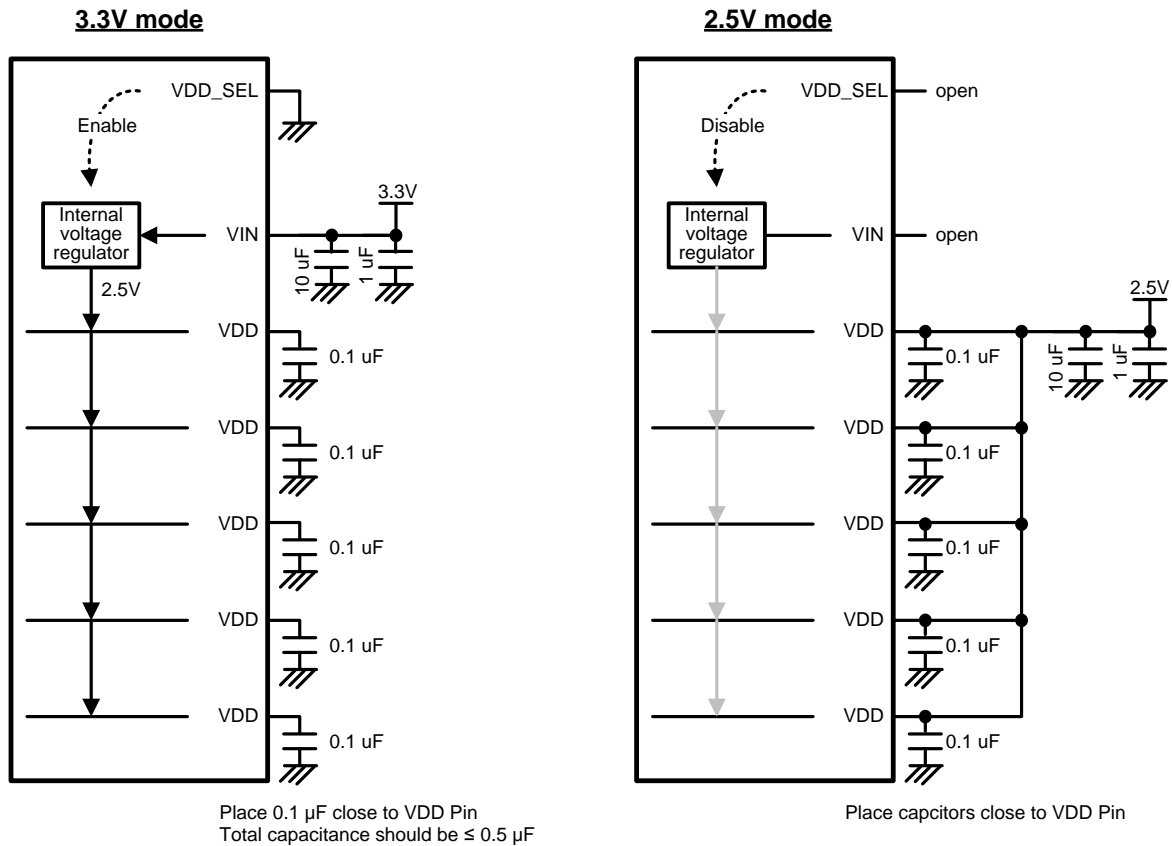
2.5-V Mode of Operation

1. VDD_SEL = Float
2. VIN = Float
3. Feed 2.5-V supply into VDD pins.
4. See information on VDD bypass below.
5. SDA and SCL pins connect pullup resistor to VDD for 2.5-V uC SMBus IO
6. SDA and SCL pins connect pullup resistor to VDD for 3.3-V uC SMBus IO
7. Any 4-Level input which requires a connection to "Logic 1" should use a 1-k Ω resistor to VIN

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3.3-V or 2.5-V Supply Mode Operation (continued)**Figure 14. 3.3 V or 2.5 V Supply Connection Diagram****10.2 Power Supply Bypassing**

Two approaches are recommended to ensure that the DS80PCI800 is provided with an adequate power supply bypass. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1- μF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the device. Small body size capacitors (such as 0402) reduce the parasitic inductance of the capacitor and also help in placement close to the VDD pin. If possible, the layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.

11 Layout

11.1 Layout Guidelines

11.1.1 PCB Layout Considerations for Differential Pairs

The differential inputs and outputs are designed with 100 Ω differential terminations. Therefore, they should be connected to interconnects with controlled differential impedance of approximately 85-110 Ω . It is preferable to route differential lines primarily on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used, the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair spacing and trace width. See AN-1187 *Leadless Leadframe Package (LLP) Application Report (SNOA401)* for additional information on QFN (WQFN) packages.

The DS80PCI800 pinout promotes easy high speed routing and layout. To optimize DS80PCI800 performance refer to the following guidelines:

1. Place local VIN and VDD capacitors as close as possible to the device supply pins. Often the best location is directly under the DS80PCI800 pins to reduce the inductance path to the capacitor. In addition, bypass capacitors may share a via with the DAP GND to minimize ground inductance.
2. Differential pairs going into or out of the DS80PCI800 should have adequate pair-to-pair spacing to minimize crosstalk.
3. Use return current via connections to link reference planes locally. This ensures a low inductance return current path when the differential signal changes layers.
4. Optimize the via structure to minimize trace impedance mismatch.
5. Place GND vias around the DAP perimeter to ensure optimal electrical and thermal performance.
6. Use small body size AC coupling capacitors when possible — 0402 or smaller size is preferred. The AC coupling capacitors should be placed closer to the Rx on the channel.

Figure 15 depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high-frequency effects of stubs on the signal path.

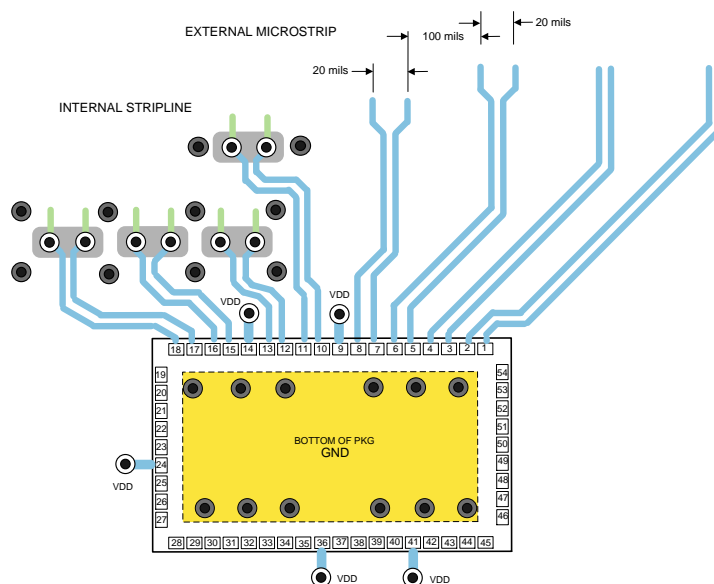


Figure 15. Typical Routing Options

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Trademarks

PCI-Express is a trademark of PCI-SIG.

All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| DS80PCI800SQ/NOPB | Active | Production | WQFN (NJY) 54 | 2000 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 85 | DS80PCI800SQ |
| DS80PCI800SQ/NOPB.A | Active | Production | WQFN (NJY) 54 | 2000 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 85 | DS80PCI800SQ |
| DS80PCI800SQ/NOPB.B | Active | Production | WQFN (NJY) 54 | 2000 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 85 | DS80PCI800SQ |
| DS80PCI800SQE/NOPB | Active | Production | WQFN (NJY) 54 | 250 SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 85 | DS80PCI800SQ |
| DS80PCI800SQE/NOPB.A | Active | Production | WQFN (NJY) 54 | 250 SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 85 | DS80PCI800SQ |
| DS80PCI800SQE/NOPB.B | Active | Production | WQFN (NJY) 54 | 250 SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 85 | DS80PCI800SQ |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

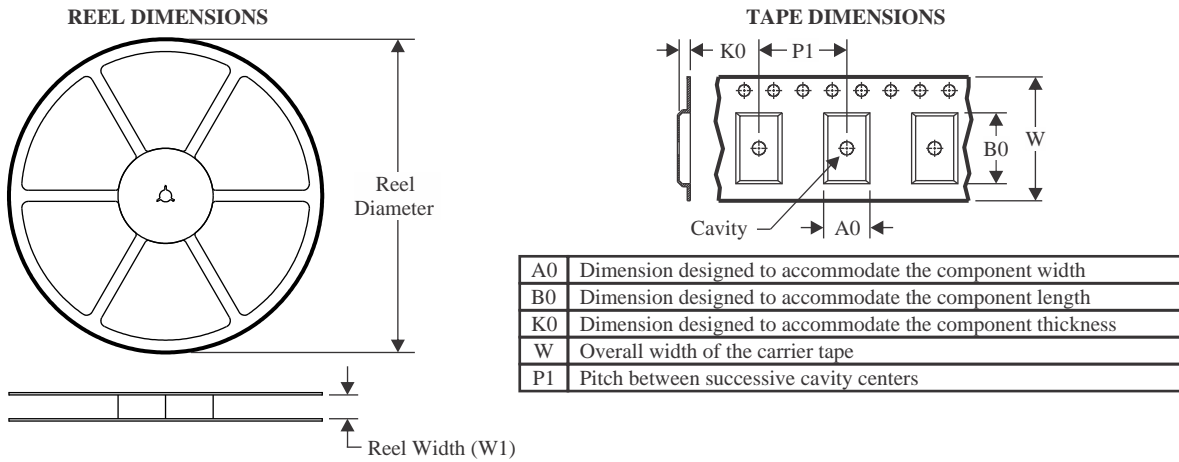
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

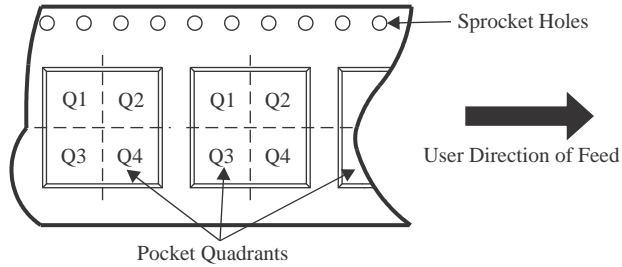
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



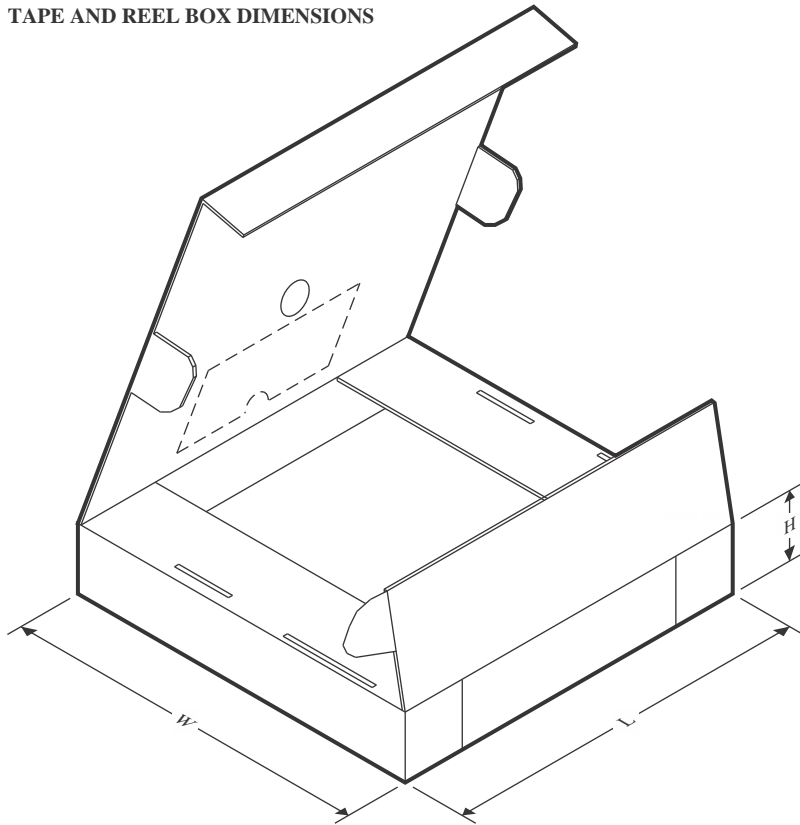
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

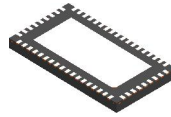
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS80PCI800SQ/NOPB | WQFN | NJY | 54 | 2000 | 330.0 | 16.4 | 5.8 | 10.3 | 1.0 | 12.0 | 16.0 | Q1 |
| DS80PCI800SQE/NOPB | WQFN | NJY | 54 | 250 | 178.0 | 16.4 | 5.8 | 10.3 | 1.0 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

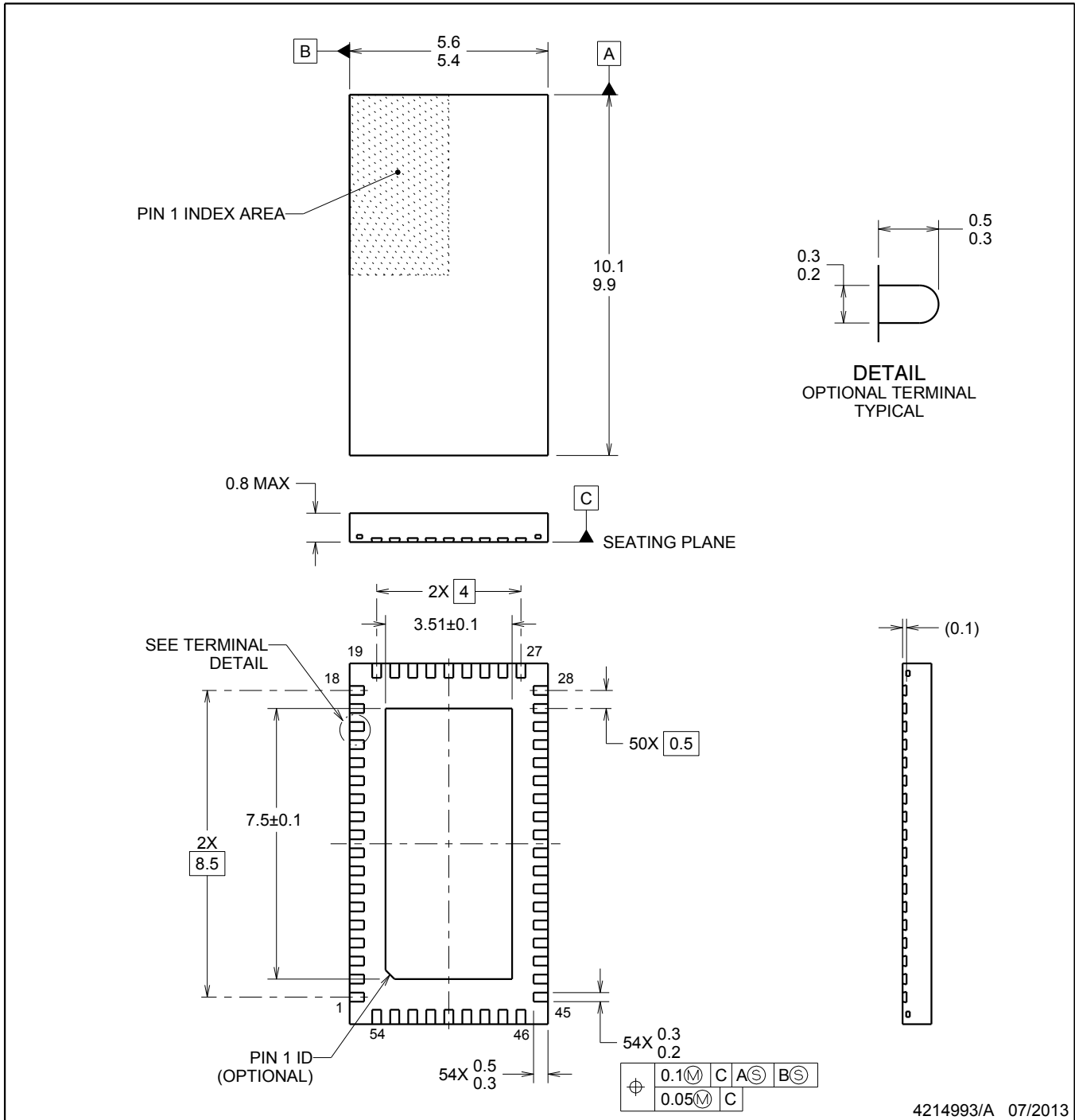
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS80PCI800SQ/NOPB | WQFN | NJY | 54 | 2000 | 356.0 | 356.0 | 36.0 |
| DS80PCI800SQE/NOPB | WQFN | NJY | 54 | 250 | 208.0 | 191.0 | 35.0 |



NJY0054A

WQFN

WQFN



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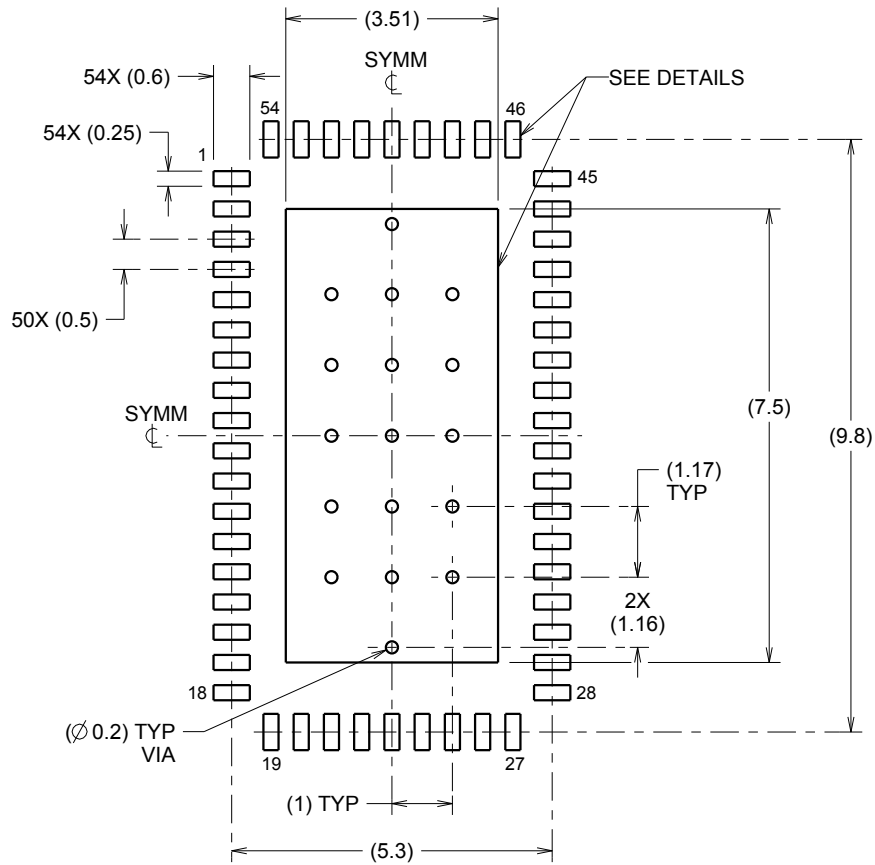
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

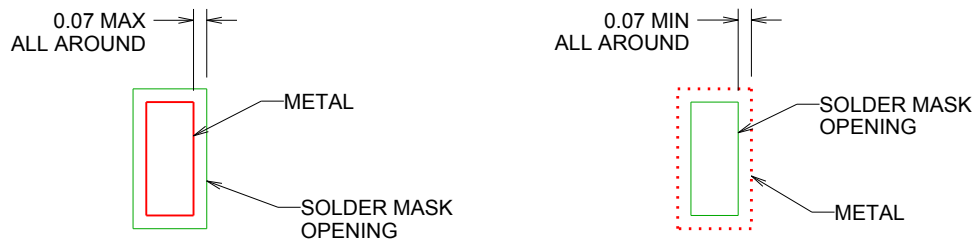
NJY0054A

WQFN

WQFN



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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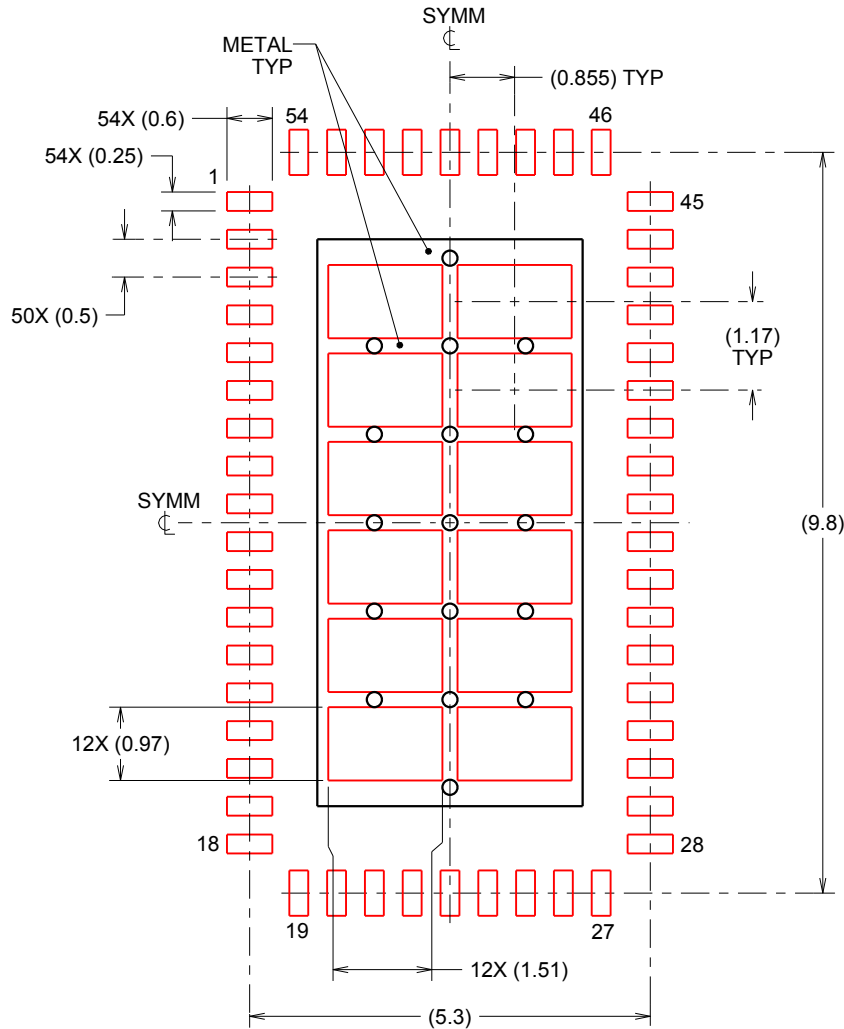
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

NJY0054A

WQFN

WQFN



SOLDERPASTE EXAMPLE
 BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
 67% PRINTED SOLDER COVERAGE BY AREA
 SCALE:10X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025

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