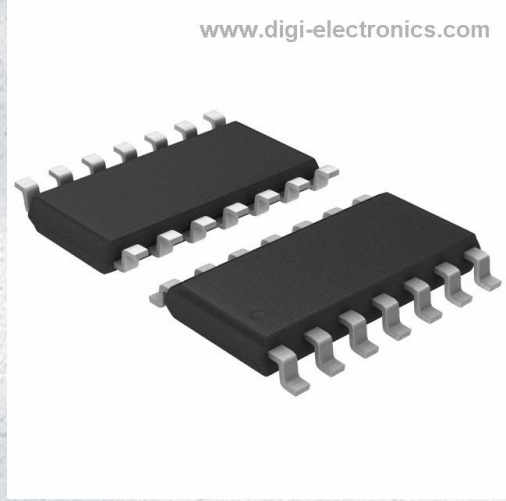
LMH6722MAX Datasheet



DiGi Electronics Part Number	LMH6722MAX-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	LMH6722MAX
Description	IC AMP CURRENT FEEDBACK 14SOIC
Detailed Description	Video Amp 4 Current Feedback 14-SOIC

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
LMH6722MAX	Texas Instruments
Series:	Product Status:
VIP10™	Obsolete
Applications:	Output Type:
Current Feedback	-
Number of Circuits:	-3db Bandwidth:
4	400 MHz
Slew Rate:	Current - Supply:
1800V/µs	5.6 mA
Current - Output / Channel:	Voltage - Supply, Single/Dual (±):
70 mA	8V ~ 12.5V, ±4V ~ 6.25V
Mounting Type:	Package / Case:
Surface Mount	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package:	Base Product Number:
14-SOIC	LMH6722

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Affected	EAR99
HTSUS:	
8542.33.0001	

LMH6714/ LMH6720/ LMH6722/ LMH6722Q Wideband Video Op Amp; Single, Single with Shutdown and Quad

Check for Samples: LMH6714, LMH6720, LMH6722, LMH6722-Q1

FEATURES

- **400MHz (A_V = +2V/V, V_{OUT} = 500mV_{PP}) −3dB BW**
- **250MHz (A_V = +2V/V, V_{OUT} = 2V_{PP}) -3dB BW**
- **0.1dB Gain Flatness to 120MHz**
- **Low Power: 5.6mA**
- **TTL Compatible Shutdown Pin (LMH6720)**
- **Very Low Diff. Gain, Phase: 0.01%, 0.01° (LMH6714)**
- **−58 HD2/ −70 HD3 at 20MHz**
- **Fast Slew Rate: 1800V/µs**
- **Low Shutdown Current: 500uA (LMH6720)**
- **11ns Turn on Time (LMH6720)**
- **7ns Shutdown Time (LMH6720)**
- **Unity Gain Stable**
- **Improved Replacement for CLC400,401,402,404,406 and 446 (LMH6714)**
- **Improved Replacement for CLC405 (LMH6720)**
- **Improved Replacement for CLC415 (LMH6722)**
- **LMH6722QSD is AEC-Q100 Grade 1 Qualified and is Manufactured on an Automotive Grade Flow**

APPLICATIONS

- **HDTV, NTSC & PAL Video Systems**
- **Video Switching and Distribution**
- **Wideband Active Filters**
- **Cable Drivers**
- **High Speed Multiplexer (LMH6720)**
- **Programmable Gain Amplifier (LMH6720)**
- **Automotive (LMH6722Q)**

DESCRIPTION

The LMH6714/LMH6720/LMH6722 series combine Texas Instruments' VIP10 high speed complementary bipolar process with Texas Instruments' current feedback topology to produce a very high speed op amp. These amplifiers provide a 400MHz small signal bandwidth at a gain of +2V/V and a 1800V/µs slew rate while consuming only 5.6mA from ±5V supplies.

The LMH6714/LMH6720/LMH6722 series offer exceptional video performance with its 0.01% and 0.01° differential gain and phase errors for NTSC and PAL video signals while driving a back terminated 75Ω load. They also offer a flat gain response of 0.1dB to 120MHz. Additionally, they can deliver 70mA continuous output current. This level of performance makes them an ideal op amp for broadcast quality video systems.

The LMH6714/LMH6720/LMH6722's small packages (SOIC, SOT-23 and WSON), low power requirement, low noise and distortion allow the LMH6714/LMH6720/LMH6722 to serve portable RF applications. The high impedance state during shutdown makes the LMH6720 suitable for use in multiplexing multiple high speed signals onto a shared transmission line. The LMH6720 is also ideal for portable applications where current draw can be reduced with the shutdown function.

Typical Performance

Non-Inverting Small Signal Frequency Response

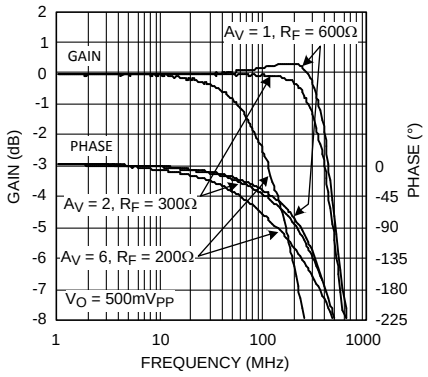


Figure 1.

Differential Gain and Phase vs. Number of Video Loads (LMH6714)

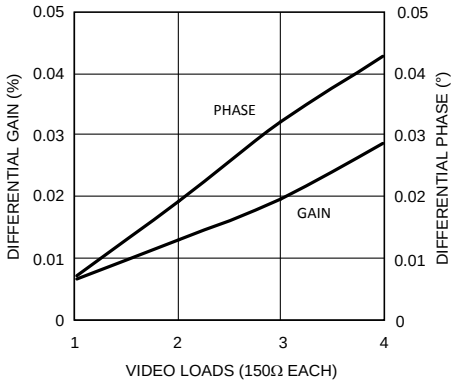


Figure 2.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

ESD Tolerance[3]	Human Body Model	2000V
	Machine Model	200V
V_{CC}		±6.75V
I_{OUT}		See[4]
Common Mode Input Voltage		$\pm V_{CC}$
Differential Input Voltage		2.2V
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering 10 sec)		+300°C
Storage Temperature Range		−65°C to +150°C
Shutdown Pin Voltage[5]		$+V_{CC}$ to V_{CC}/2-1V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specific specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the POWER DISSIPATION section for more details.
(5) The shutdown pin is designed to work between 0 and V_{CC} with split supplies (V_{CC} = -V_{EE}). With single supplies (V_{EE} = ground) the shutdown pin should not be taken below V_{CC}/2.

Operating Ratings[1]

Thermal Resistance Package		(θ_{JA})
5-Pin SOT-23 (DBV)		232°C/W
6-Pin SOT-23 (DBV)		198°C/W
8-Pin SOIC (D)		145°C/W
14-Pin SOIC (D)		130°C/W
14-Pin TSSOP (PW)		160°C/W
14-Pin WSON (NHK)		46°C/W
Operating Temperature	LMH6722Q	−40°C to 125°C
	All others	−40°C to 85°C
Supply Voltage Range		8V (±4V) to 12.5V (±6.25V)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specific specifications, see the Electrical Characteristics tables.

Electrical Characteristics

Unless specified, A_V = +2, R_F = 300Ω: V_{CC} = ±5V, R_L = 100Ω, LMH6714/LMH6720/LMH6722. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
Frequency Domain Response						
SSBW	−3dB Bandwidth	V_{OUT} = 0.5V_{PP}	345	400		MHz
LSBW	−3dB Bandwidth	V_{OUT} = 2.0V_{PP}	200	250		MHz
LSBW	−3dB Bandwidth, LMH6722 TSSOP package only	V_{OUT} = 2.0V_{PP}	170	250		MHz
	Gain Flatness	V_{OUT} = 2V_{PP}				
GFP	Peaking	DC to 120MHz		0.1		dB
GFR	Rolloff	DC to 120MHz		0.1		dB
LPD	Linear Phase Deviation	DC to 120MHz		0.5		deg
DG	Differential Gain	R_L = 150Ω, 4.43MHz (LMH6714)		0.01		%
DG	Differential Gain	R_L = 150Ω, 4.43MHz (LMH6720)		0.02		%
DP	Differential Phase	R_L = 150Ω, 4.43MHz		0.01		deg
Time Domain Response						
TRS	Rise and Fall Time	.5V Step		1.5		ns
TRL		2V Step		2.6		ns
t_s	Settling Time to 0.05%	2V Step		12		ns
SR	Slew Rate	6V Step	1200	1800		V/µs
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP}, 20MHz		−58		dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 20MHz		−70		dBc
IMD	3rd Order Intermodulation Products	10MHz, P_{OUT} = 0dBm		−78		dBc
	Equivalent Input Noise					
VN	Non-Inverting Voltage	>1MHz		3.4		nV/√Hz
NICN	Inverting Current	>1MHz		10		pA/√Hz
ICN	Non-Inverting Current	>1MHz		1.2		pA/√Hz

(1) All limits are specified by testing, design, or statistical analysis.
(2) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Electrical Characteristics (continued)

Unless specified, A_V = +2, R_F = 300Ω: V_{CC} = ±5V, R_L = 100Ω, LMH6714/LMH6720/LMH6722. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions		Min(1)	Typ(2)	Max(1)	Units
Static, DC Performance							
V_{IO}	Input Offset Voltage				±0.2	±6 **±8**	mV
DVIO	Average Drift				8		µV/°C
I_{BN}	Input Bias Current	Non-Inverting			±1	±10 **±15**	µA
DIBN	Average Drift				4		nA/°C
I_{BI}	Input Bias Current	Inverting			−4	±12 **±20**	µA
DIBI	Average Drift				41		nA/°C
PSRR	Power Supply Rejection Ratio	DC		48 **47**	58		dB
CMRR	Common Mode Rejection Ratio	DC		48 **45**	54		dB
I_{CC}	Supply Current	R_L = ∞	LMH6714 LMH6720	4.5 **3**	5.6	7.5 **8**	mA
			LMH6722	18 **15**	22.5	30 **32**	
I_{CCI}	Supply Current During Shutdown	LMH6720			500	670	µA
Miscellaneous Performance							
R_{IN}	Input Resistance	Non-Inverting			2		MΩ
C_{IN}	Input Capacitance	Non-Inverting			1.0		pF
R_{OUT}	Output Resistance	Closed Loop			0.06		Ω
V_{OUT}	Output Voltage Range	R_L = ∞		±3.5 **±3.4**	±3.9		V
		R_L = 100Ω		±3.6 **±3.4**	±3.8		
CMIR	Input Voltage Range	Common Mode			±2.2		V
I_{OUT}	Output Current(3)	V_{IN} = 0V, Max Linear Current		50	70		mA
OFFMAX	Voltage for Shutdown	LMH6720				**0.8**	V
ONMIN	Voltage for Turn On	LMH6720		**2.0**			V
IIH	Current Turn On	LMH6720, $\overline{SD}$ = 2.0V		−20 **−30**	2	20 **30**	µA
IIL	Current Shutdown	LMH6720, $\overline{SD}$ = .8V		**−600**	−400	**−100**	µA
IOZ	R_{OUT} Shutdown	LMH6720, $\overline{SD}$ = .8V		0.2	1.8		MΩ
t_{on}	Turn on Time	LMH6720			11		ns
t_{off}	Turn off Time	LMH6720			7		ns

(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the POWER DISSIPATION section for more details.

CONNECTION DIAGRAMS

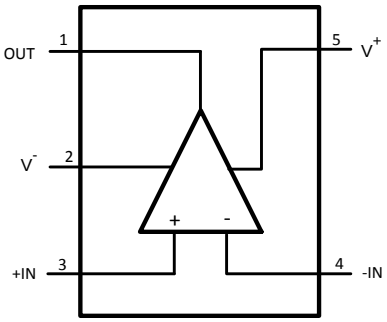


Figure 3. 5-Pin SOT-23 (LMH6714) (Top View) See Package Number DBV

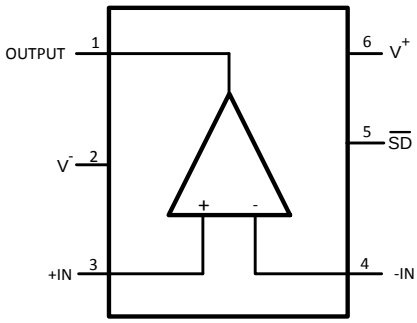


Figure 4. 6-Pin SOT-23 (LMH6720) (Top View) See Package Number DBV

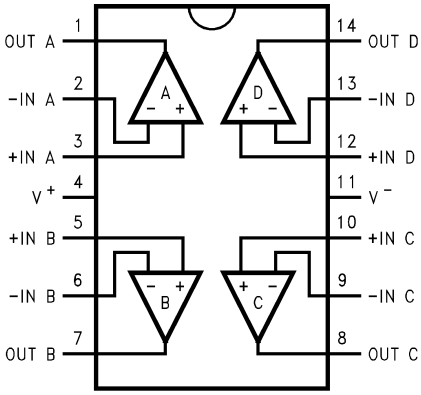


Figure 5. 14-Pin SOIC, TSSOP and WSON (LMH6722) (Top View) See Package Numbers D, PW, and NHK

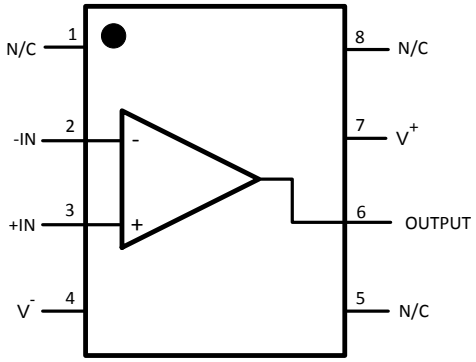


Figure 6. 8-Pin SOIC (LMH6714) (Top View) See Package Number D

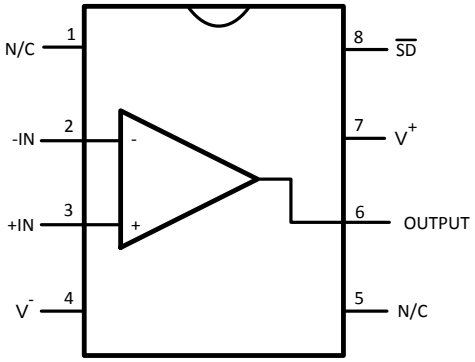


Figure 7. 8-Pin SOIC (LMH6720) (Top View) See Package Number D

Typical Performance Characteristics

(V^+ = +5V, V^- = −5V, A_V = 2, R_F = 300Ω, R_L = 100Ω Unless Specified).

Non-Inverting Small Signal Frequency Response

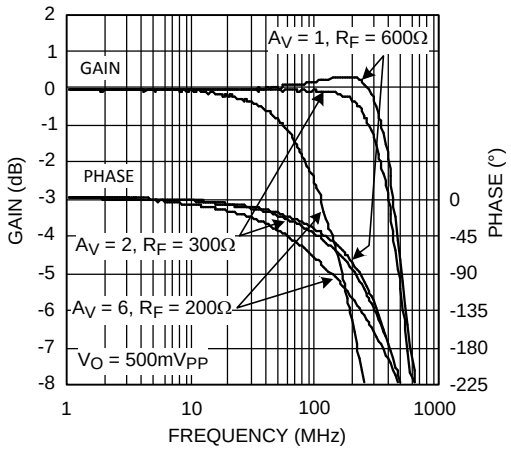


Figure 8.

Non-Inverting Large Signal Frequency Response

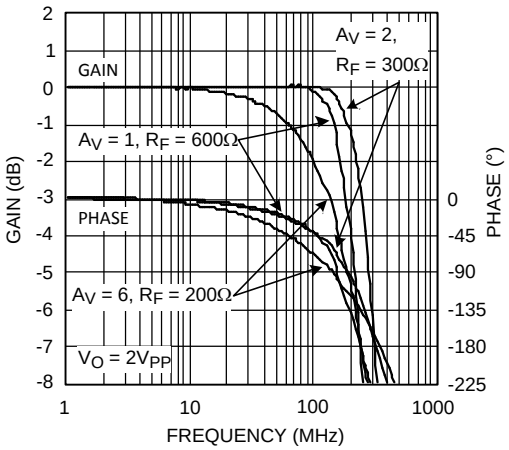


Figure 9.

Inverting Frequency Response

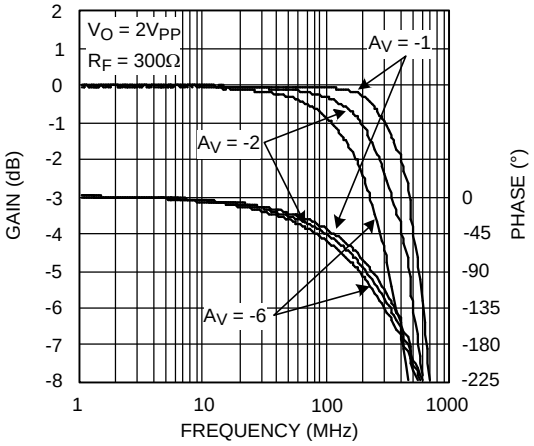


Figure 10.

Non-Inverting Frequency Response vs. V_O

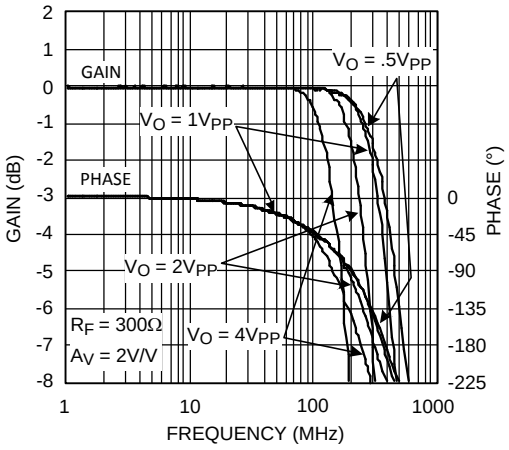


Figure 11.

Inverting Frequency Response vs. V_O

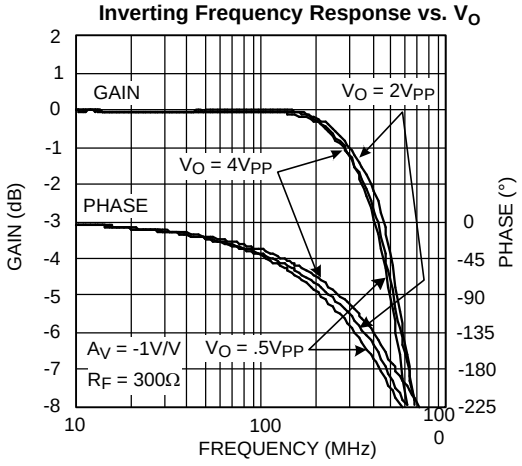


Figure 12.

Harmonic Distortion vs. Frequency

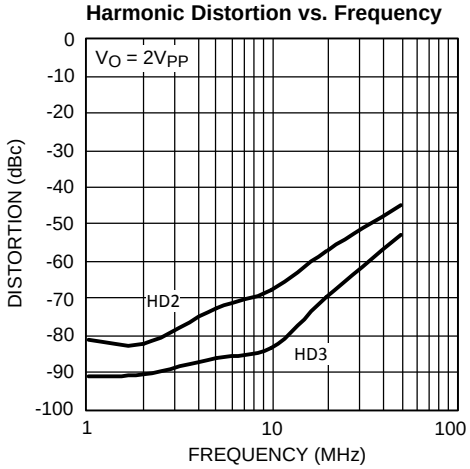


Figure 13.

Typical Performance Characteristics (continued)

(V^+ = +5V, V^- = −5V, A_V = 2, R_F = 300Ω, R_L = 100Ω Unless Specified).

2nd Harmonic Distortion vs. V_{OUT}

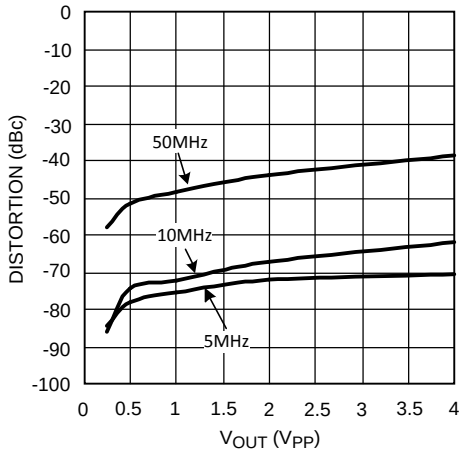


Figure 14.

3rd Harmonic Distortion vs. V_{OUT}

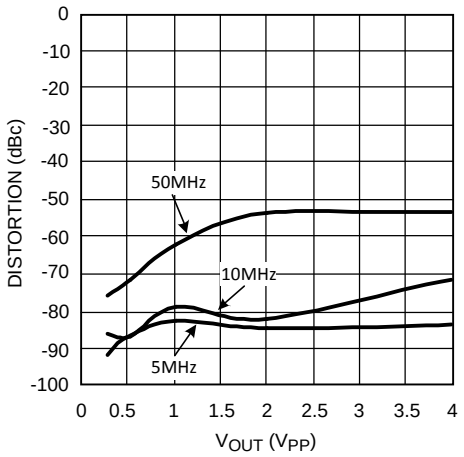


Figure 15.

DG/DP (LMH6714)

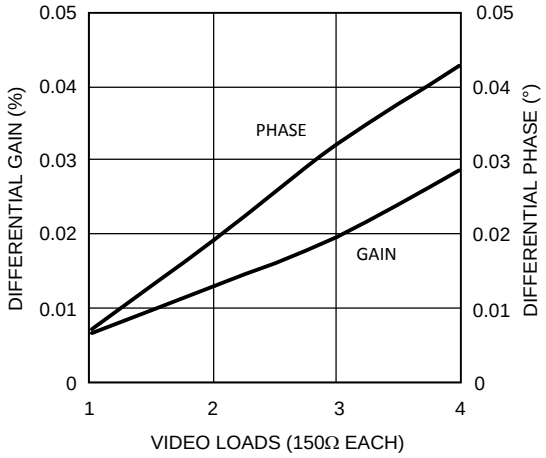


Figure 16.

DG/DP (LMH6720)

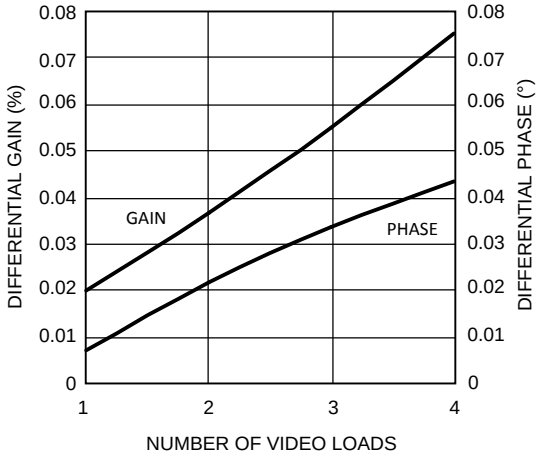


Figure 17.

DG/DP (LMH6722)

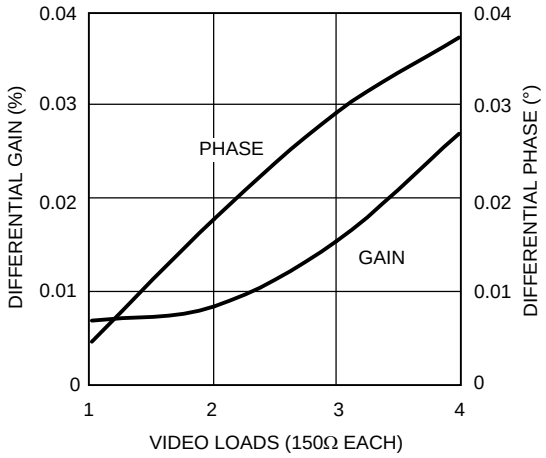


Figure 18.

Large Signal Pulse Response

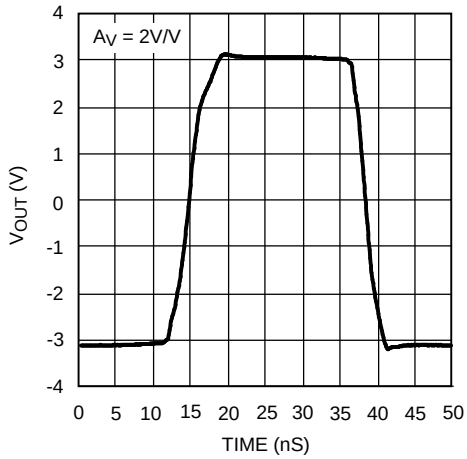


Figure 19.

Typical Performance Characteristics (continued)

(V^+ = +5V, V^- = −5V, A_V = 2, R_F = 300Ω, R_L = 100Ω Unless Specified).

Small Signal Pulse Response

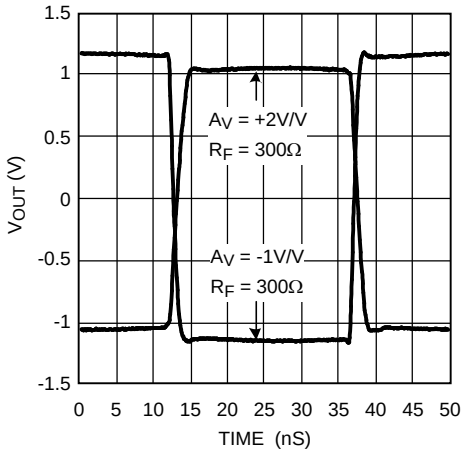


Figure 20.

Closed Loop Output Resistance

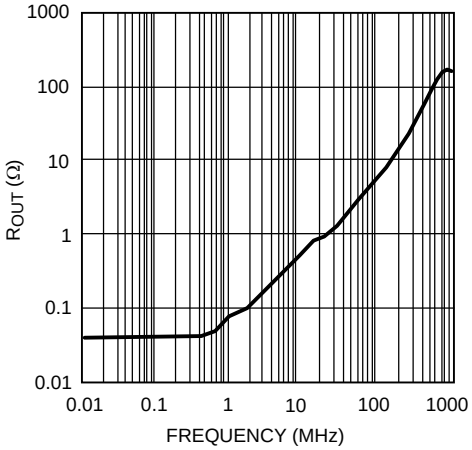


Figure 21.

Open Loop Transimpedance Z(s)

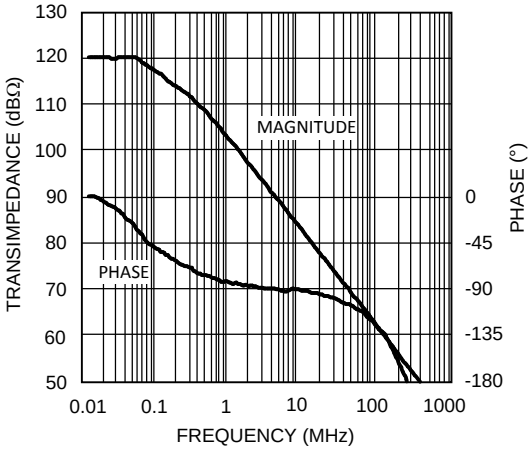


Figure 22.

PSRR vs. Frequency

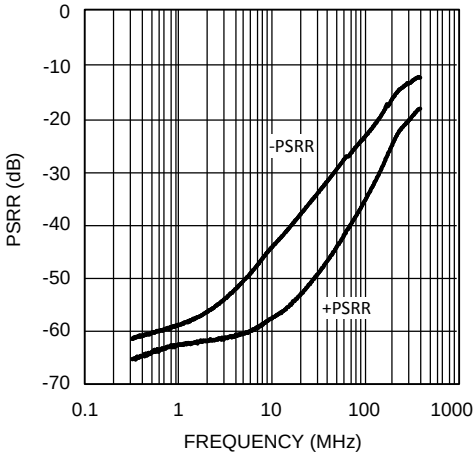


Figure 23.

CMRR vs. Frequency

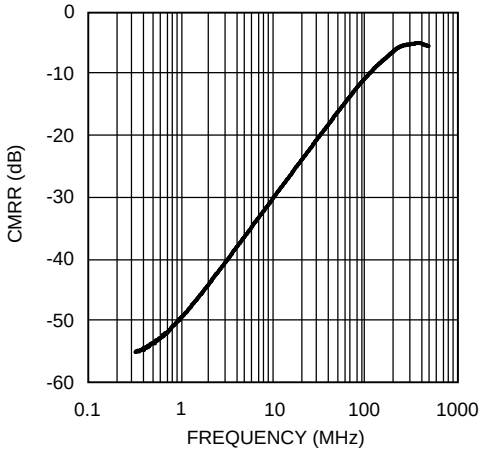


Figure 24.

Frequency Response vs. R_F

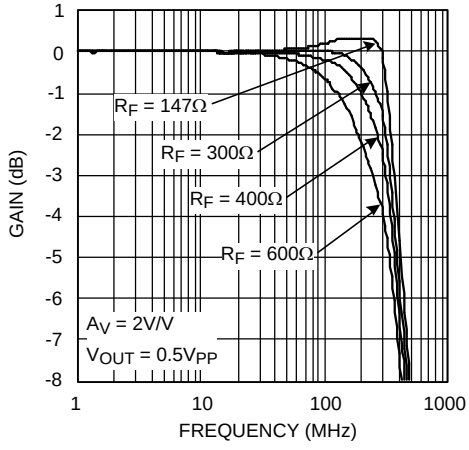


Figure 25.

Typical Performance Characteristics (continued)

(V^+ = +5V, V^- = −5V, A_V = 2, R_F = 300Ω, R_L = 100Ω Unless Specified).

DC Errors vs. Temperature

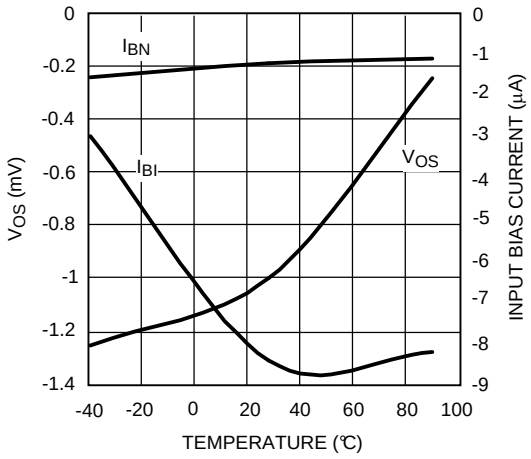


Figure 26.

Maximum V_{OUT} vs. Frequency

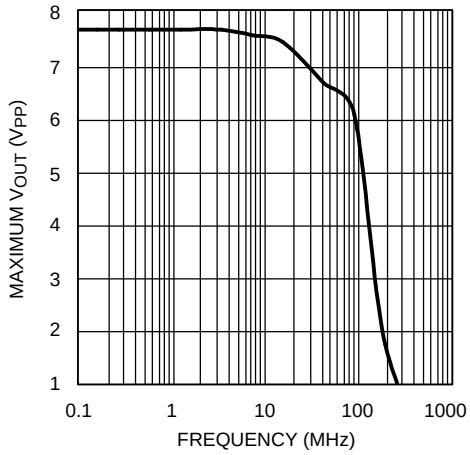


Figure 27.

3rd Order Intermodulation vs. Output Power

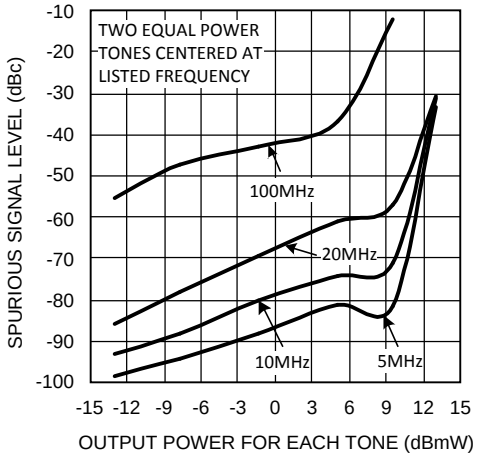


Figure 28.

Crosstalk vs. Frequency (LMH6722) for each channel with all others active

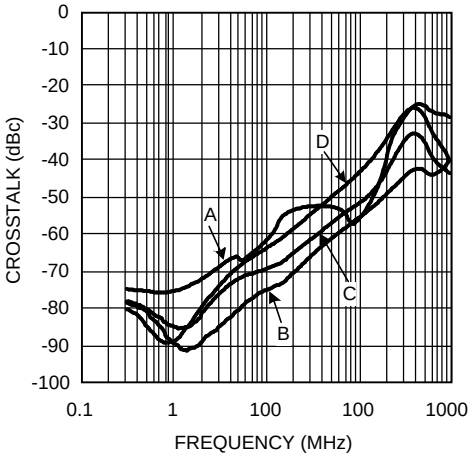


Figure 29.

Noise vs. Frequency

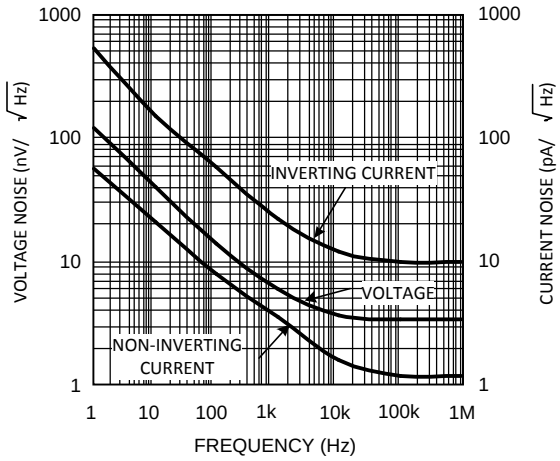


Figure 30.

APPLICATION SECTION

FEEDBACK RESISTOR SELECTION

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Performance plots specify an R_F of 300Ω, a gain of +2V/V and ±5V power supplies (unless otherwise specified). Generally, lowering R_F from it's recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below it's recommended value will cause overshoot, ringing and, eventually, oscillation.

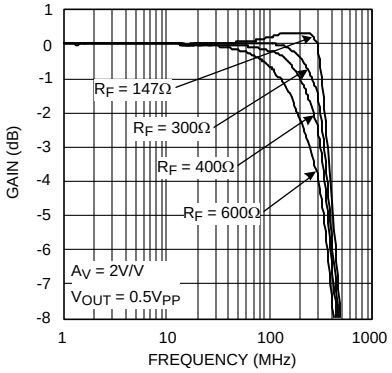


Figure 31. Frequency Response vs. R_F

Figure 31 shows the LMH6714/LMH6720/LMH6722's frequency response as R_F is varied (R_L = 100Ω, A_V = +2). This plot shows that an R_F of 147Ω results in peaking. An R_F of 300Ω gives near maximal bandwidth and gain flatness with good stability. An R_F of 400Ω gives excellent stability with only a small bandwidth penalty. Since all applications are slightly different it is worth some experimentation to find the optimal R_F for a given circuit. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6714/LMH6720/LMH6722 requires a 600Ω feedback resistor for stable operation.

For more information see Application Note OA-13 (SNOA366) which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6714/LMH6720/LMH6722 is approximately 180Ω. The LMH6714/LMH6720/LMH6722 is designed for optimum performance at gains of +1 to +6 V/V and −1 to −5V/V. When using gains of ±7V/V or more the low values of R_G required will make inverting input impedances very low.

When configuring the LMH6714/LMH6720/LMH6722 for gains other than +2V/V, it is usually necessary to adjust the value of the feedback resistor. Figure 32 and Figure 33 provide recommended feedback resistor values for a number of gain selections.

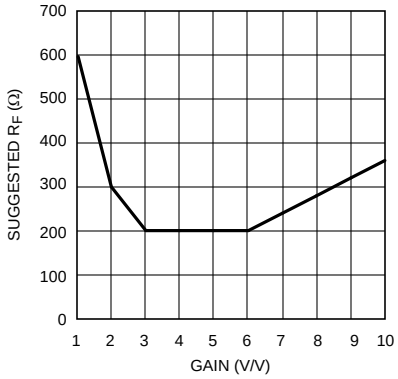


Figure 32. R_F vs. Non-Inverting Gain

In the Figure 32 and Figure 33 charts, the recommended value of R_F is depicted by the solid line, which starts high, decreases to 200Ω and begins increasing again. The reason that a higher R_F is required at higher gains is the need to keep R_G from decreasing too far below the output impedance of the input buffer. For the LMH6714/LMH6720/LMH6722 the output resistance of the input buffer is approximately 180Ω and 50Ω is a practical lower limit for R_G. Due to the limitations on R_G the LMH6714/LMH6720/LMH6722 begins to operate in a gain bandwidth limited fashion for gains of ±5V/V or greater.

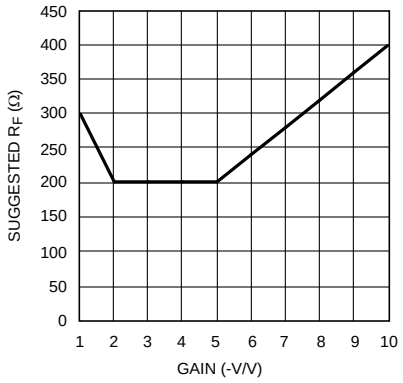


Figure 33. R_F vs. Inverting Gain

ACTIVE FILTERS

When using any current feedback Operational Amplifier as an active filter it is important to be very careful when using reactive components in the feedback loop. Anything that reduces the impedance of the negative feedback, especially at higher frequencies, will almost certainly cause stability problems. Likewise capacitance on the inverting input needs to be avoided. See Application Notes OA-07 (SNOA365) and OA-26 (SNOA387) for more information on Active Filter applications for Current Feedback Op Amps.

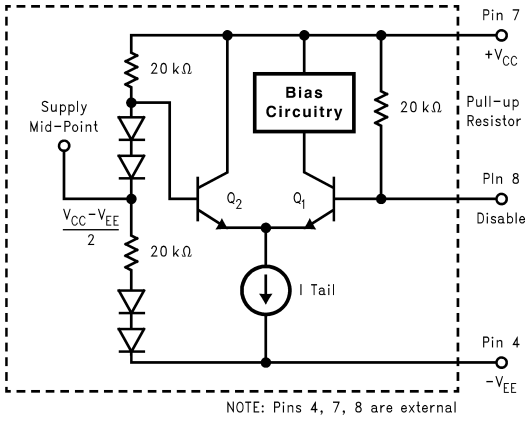


Figure 34. Enable/Disable Operation

ENABLE/DISABLE OPERATION USING ±5V SUPPLIES (LMH6720 ONLY)

The LMH6720 has a TTL logic compatible disable function. Apply a logic low (<.8V) to the DS pin and the LMH6720 is disabled. Apply a logic high (>2.0V), or let the pin float and the LMH6720 is enabled. Voltage, not current, at the Disable pin determines the enable/disable state. Care must be exercised to prevent the disable pin voltage from going more than .8V below the midpoint of the supply voltages (0V with split supplies, $V_{CC}/2$ with single supplies) doing so could cause transistor Q1 to Zener resulting in damage to the disable circuit. The core amplifier is unaffected by this, but disable operation could become slower as a result.

Disabled, the LMH6720 inputs and output become high impedances. While disabled the LMH6720 quiescent current is approximately 500µA. Because of the pull up resistor on the disable circuit the I_{CC} and I_{EE} currents are not balanced in the disabled state. The positive supply current (I_{CC}) is approximately 500µA while the negative supply current (I_{EE}) is only 200µA. The remaining I_{EE} current of 300µA flows through the disable pin.

The disable function can be used to create analog switches or multiplexers. Implement a single analog switch with one LMH6720 positioned between an input and output. Create an analog multiplexer with several LMH6720's. The LMH6720 is at it's best at a gain of 1 for multiplexer applications because there is no R_G to shunt signals to ground.

DISABLE LIMITATIONS (LMH6720 ONLY)

The feedback Resistor (R_F) limits off isolation in inverting gain configurations. During shutdown the impedance of the LMH6720 inputs and output become very high (>1MΩ), however R_F and R_G are the dominant factor for effective output impedance.

Do not apply voltages greater than $+V_{CC}$ or less than 0V (V_{CC}/2 single supply) to the disable pin. The input ESD diodes will also conduct if the signal leakage through the feedback resistors brings the inverting input near either supply rail.

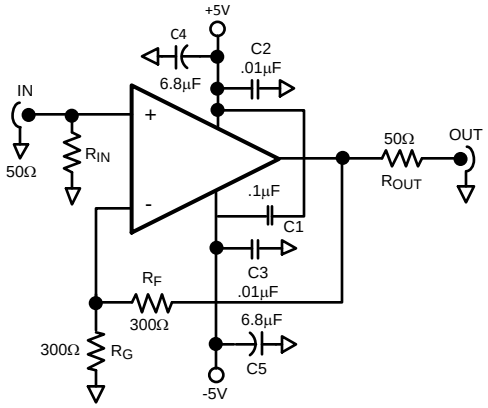


Figure 35. Typical Application with Suggested Supply Bypassing

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The following Evaluation boards are available with sample parts:

LMH6714	SOT-23	LMH730216
	SOIC	LMH730227
LMH6720	SOT-23	LMH730216
	SOIC	LMH730227
LMH6722	SOIC	LMH730231
	TSSOP	LMH730131

To reduce parasitic capacitances, the ground plane should be removed near the input and output pins. To reduce series inductance, trace lengths of components in the feedback loop should be minimized. For long signal paths controlled impedance lines should be used, along with impedance matching at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located anywhere on the board, the smaller ceramic capacitors should be placed as close to the device as possible. In addition Figure 35 shows a capacitor (C1) across the supplies with no connection to ground. This capacitor is optional, however it is required for best 2nd Harmonic suppression. If this capacitor is omitted C2 and C3 should be increased to .1µF each.

VIDEO PERFORMANCE

The LMH6714/LMH6720/LMH6722 has been designed to provide excellent performance with both PAL and NTSC composite video signals. Performance degrades as the loading is increased, therefore best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks capacitance from the amplifier output stage. While all parts offer excellent video performance the LMH6714 and LMH6722 are slightly better than the LMH6720.

WIDE BAND DIGITAL PROGRAMMABLE GAIN AMPLIFIER (LMH6720 ONLY)

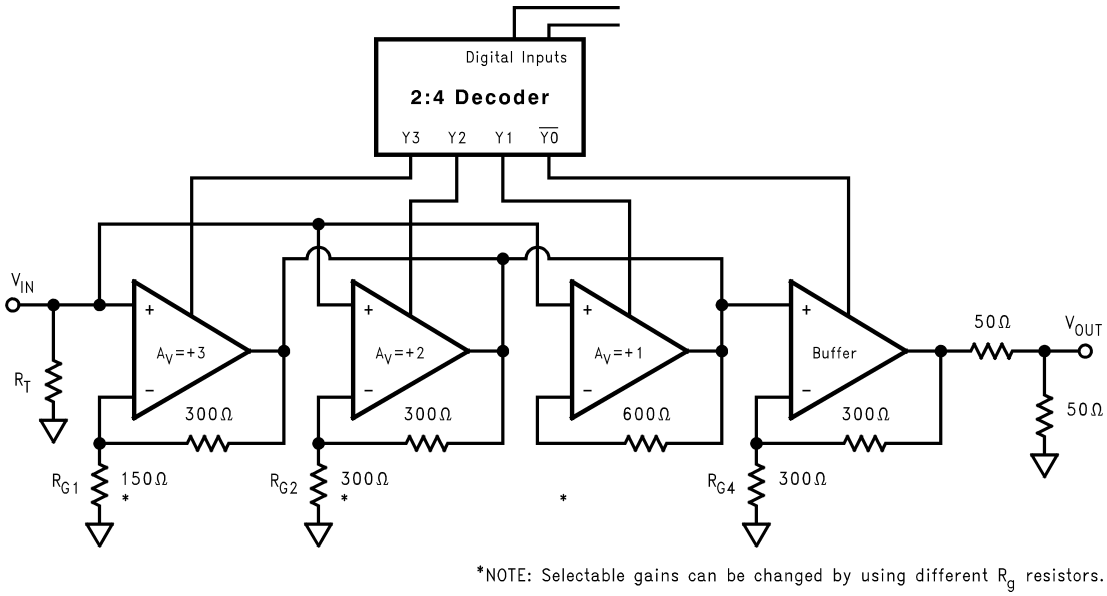


Figure 36. Wideband Digitally Controlled Programmable Gain Amplifier

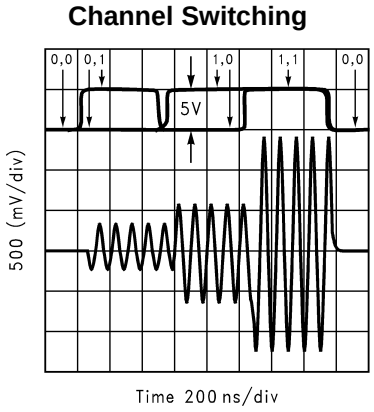


Figure 37. PGA Output

As shown in Figure 36 and Figure 37 the LMH6720 can be used to construct a digitally controlled programmable gain amplifier. Each amplifier is configured to provide a digitally selectable gain. To provide for accurate gain settings, 1% or better tolerance is recommended on the feedback and gain resistors. The gain provided by each digital code is arbitrary through selection of the feedback and gain resistor values.

AMPLITUDE EQUALIZATION

Sending signals over coaxial cable greater than 50 meters in length will attenuate high frequency signal components much more than lower frequency components. An equalizer can be made to pre emphasize the higher frequency components so that the final signal has less distortion. This process can be done at either end of the cable. The circuit in Figure 38 shows a receiver with some additional components in the feedback loop to equalize the incoming signal. The RC networks peak the signal at higher frequencies. This peaking is a piecewise linear approximation of the inverse of the frequency response of the coaxial cable. Figure 39 shows the effect of this equalization on a digital signal that has passed through 150 meters of coaxial cable. Figure 40 shows a Bode plot of the frequency response of the circuit in Figure 38 along with equations needed to design the pole and zero frequencies. Figure 41 shows a network analyzer plot of an LMH6714/LMH6720/LMH6722 with the following component values:

R_G = 309Ω

R1 = 450Ω

C1 = 470pF

R2 = 91Ω

C2 = 68pF

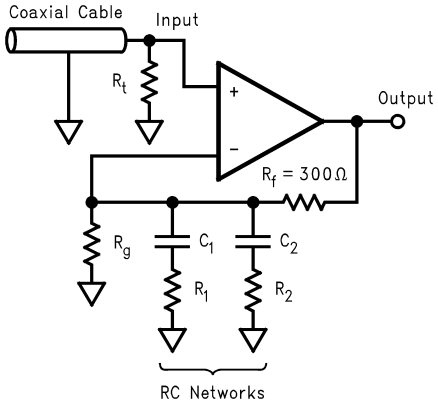


Figure 38. Equalizer Circuit Schematic

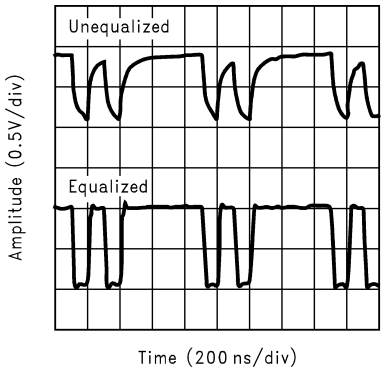


Figure 39. Digital Signal without and with Equalization

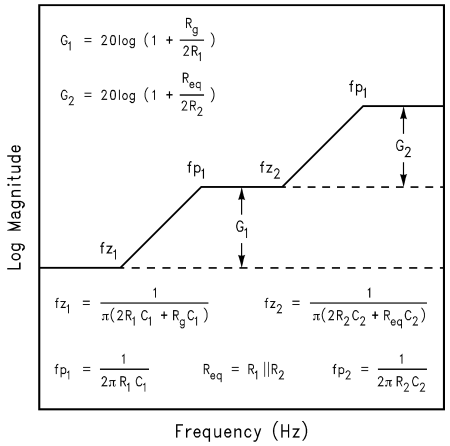


Figure 40. Design Equations

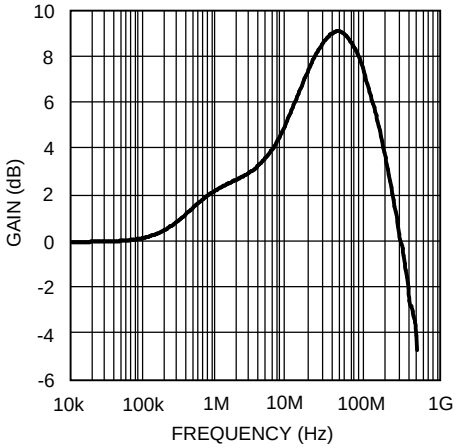


Figure 41. Equalizer Frequency Response

POWER DISSIPATION

Follow these steps to determine the Maximum power dissipation for the LMH6714/LMH6720/LMH6722:

1. Calculate the quiescent (no load) power: $P_{AMP} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage: P_{OUT} (RMS) = ((V_{CC} - V_{OUT} (RMS)) * I_{OUT} (RMS)), where V_{OUT} and I_{OUT} are the voltage and current across the external load.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_{OUT}$

The maximum power that the LMH6714/LMH6720/LMH6722, package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° - T_A)/ \theta_{JA}$, where T_A = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package θ_{JA} is 145°C/W, for the 5-pin SOT-23 it is 232°C/W.

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	15

TEXAS INSTRUMENTS

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6714MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 14MA	Samples
LMH6714MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 14MA	Samples
LMH6714MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A95A	Samples
LMH6714MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A95A	Samples
LMH6720MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 20MA	Samples
LMH6720MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 20MA	Samples
LMH6720MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A96A	Samples
LMH6720MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A96A	Samples
LMH6722MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 22MA	Samples
LMH6722MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 22MA	Samples
LMH6722MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 22MT	Samples
LMH6722MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 22MT	Samples
LMH6722QSD/NOPB	ACTIVE	WSON	NHK	14	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L6722Q	Samples
LMH6722QSDX/NOPB	ACTIVE	WSON	NHK	14	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L6722Q	Samples
LMH6722SD/NOPB	ACTIVE	WSON	NHK	14	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L6722	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMH6722, LMH6722-Q1 :

- Catalog : LMH6722
- Automotive : LMH6722-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

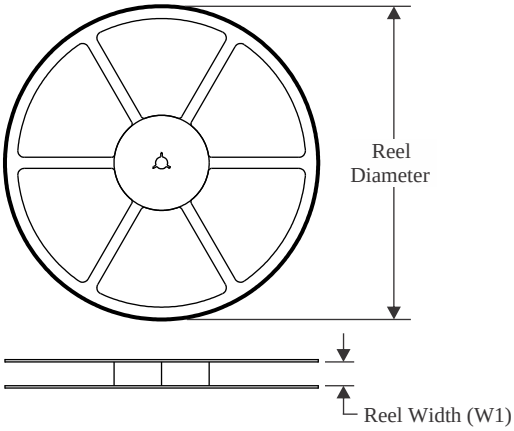
PACKAGE MATERIALS INFORMATION

www.ti.com

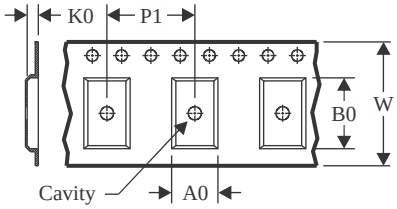
18-Oct-2024

TAPE AND REEL INFORMATION

REEL DIMENSIONS

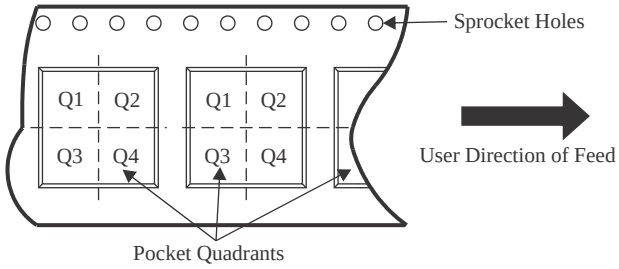


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

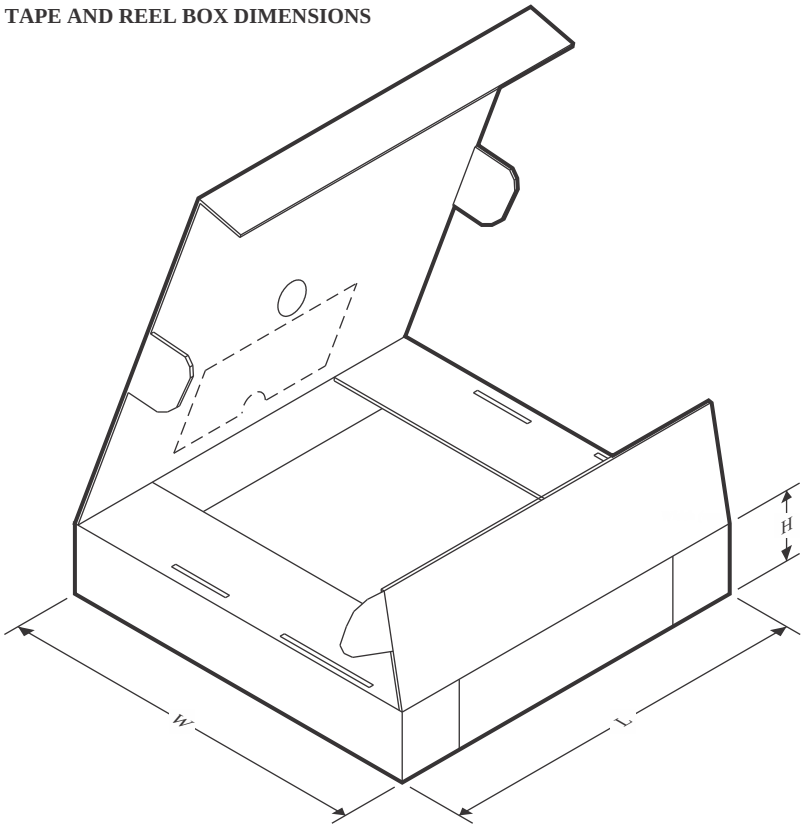


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6714MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6714MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6714MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6720MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6720MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6720MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6722MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMH6722MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMH6722QSD/NOPB	WSON	NHK	14	1000	178.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1
LMH6722QSDX/NOPB	WSON	NHK	14	4500	330.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1
LMH6722SD/NOPB	WSON	NHK	14	1000	178.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

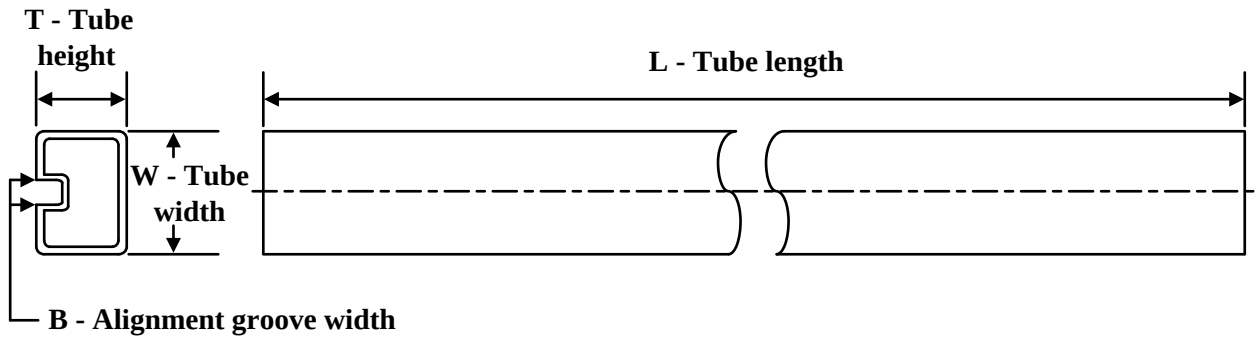


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6714MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6714MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6714MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6720MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6720MF/NOPB	SOT-23	DBV	6	1000	208.0	191.0	35.0
LMH6720MFX/NOPB	SOT-23	DBV	6	3000	208.0	191.0	35.0
LMH6722MAX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMH6722MTX/NOPB	TSSOP	PW	14	2500	356.0	356.0	35.0
LMH6722QSD/NOPB	WSON	NHK	14	1000	208.0	191.0	35.0
LMH6722QSDX/NOPB	WSON	NHK	14	4500	356.0	356.0	35.0
LMH6722SD/NOPB	WSON	NHK	14	1000	208.0	191.0	35.0

PACKAGE MATERIALS INFORMATION

TUBE



*All dimensions are nominal

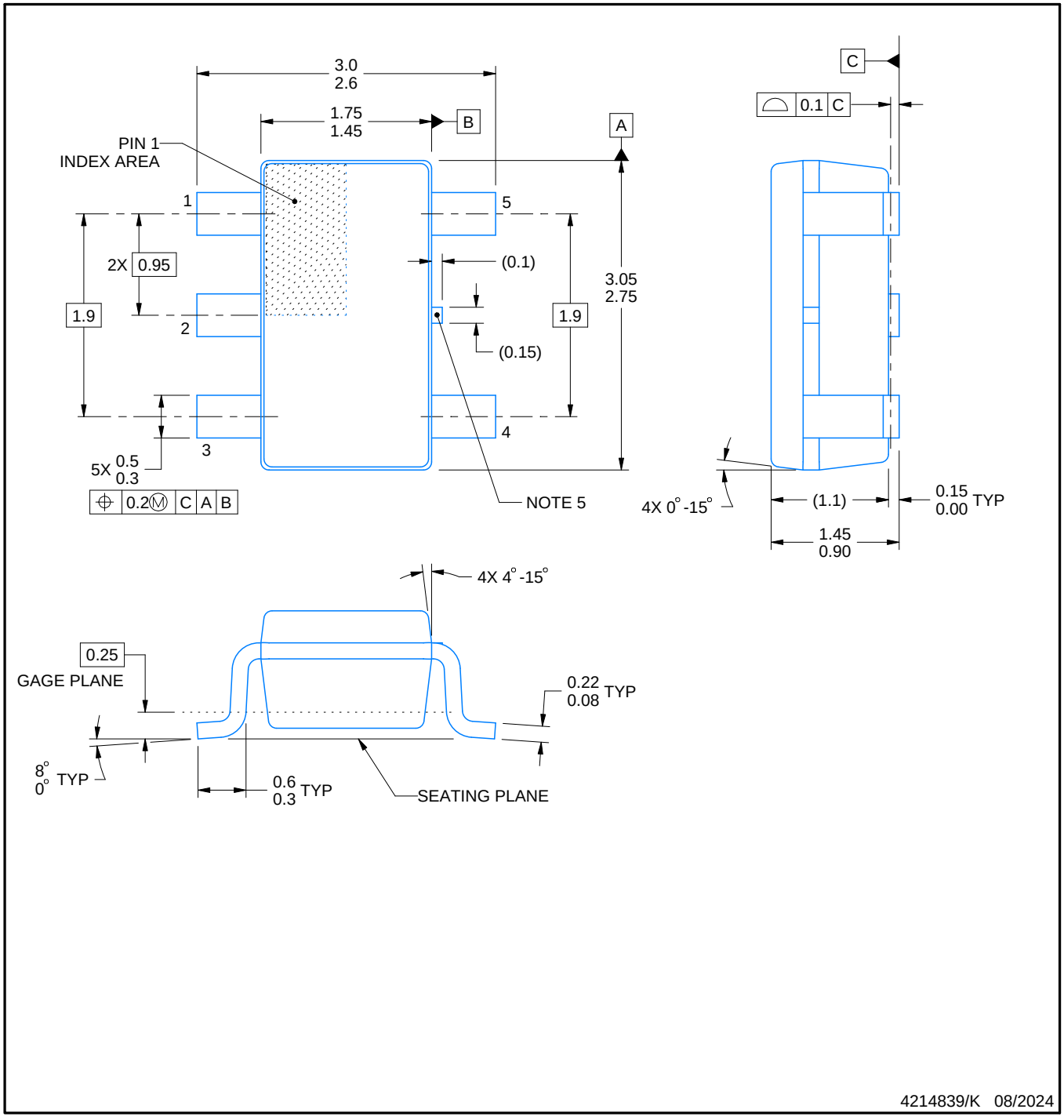
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6714MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6720MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6722MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMH6722MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

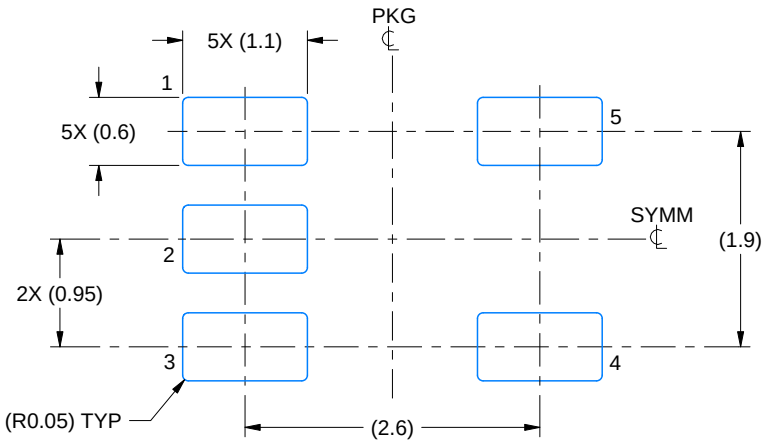
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

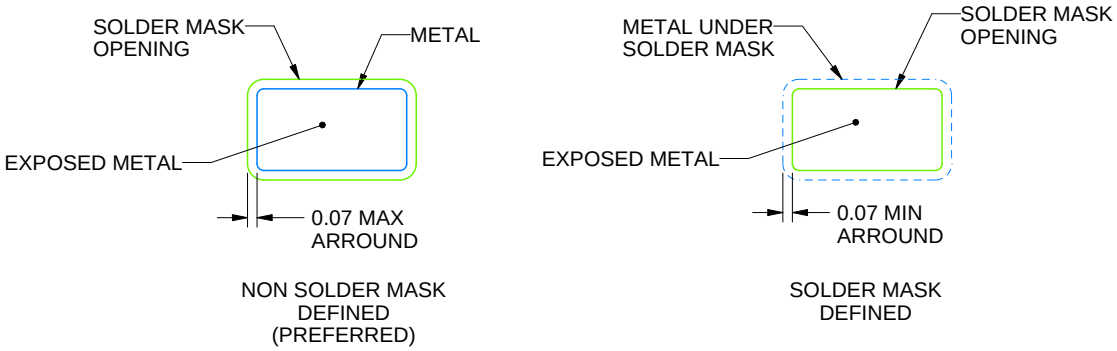
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

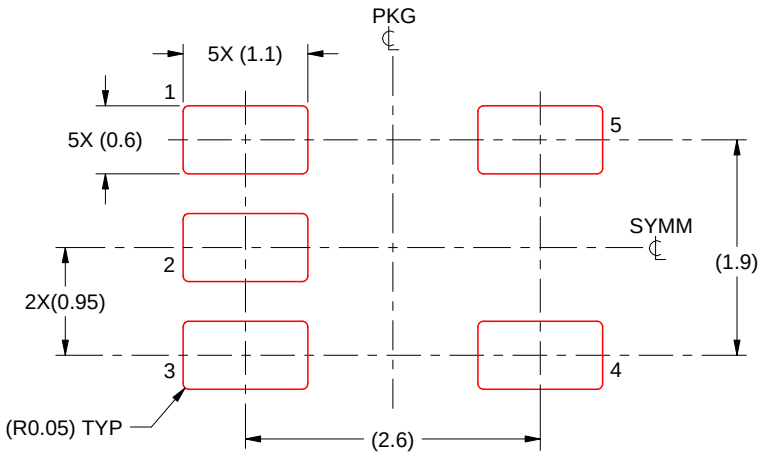
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

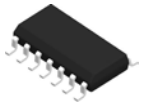


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

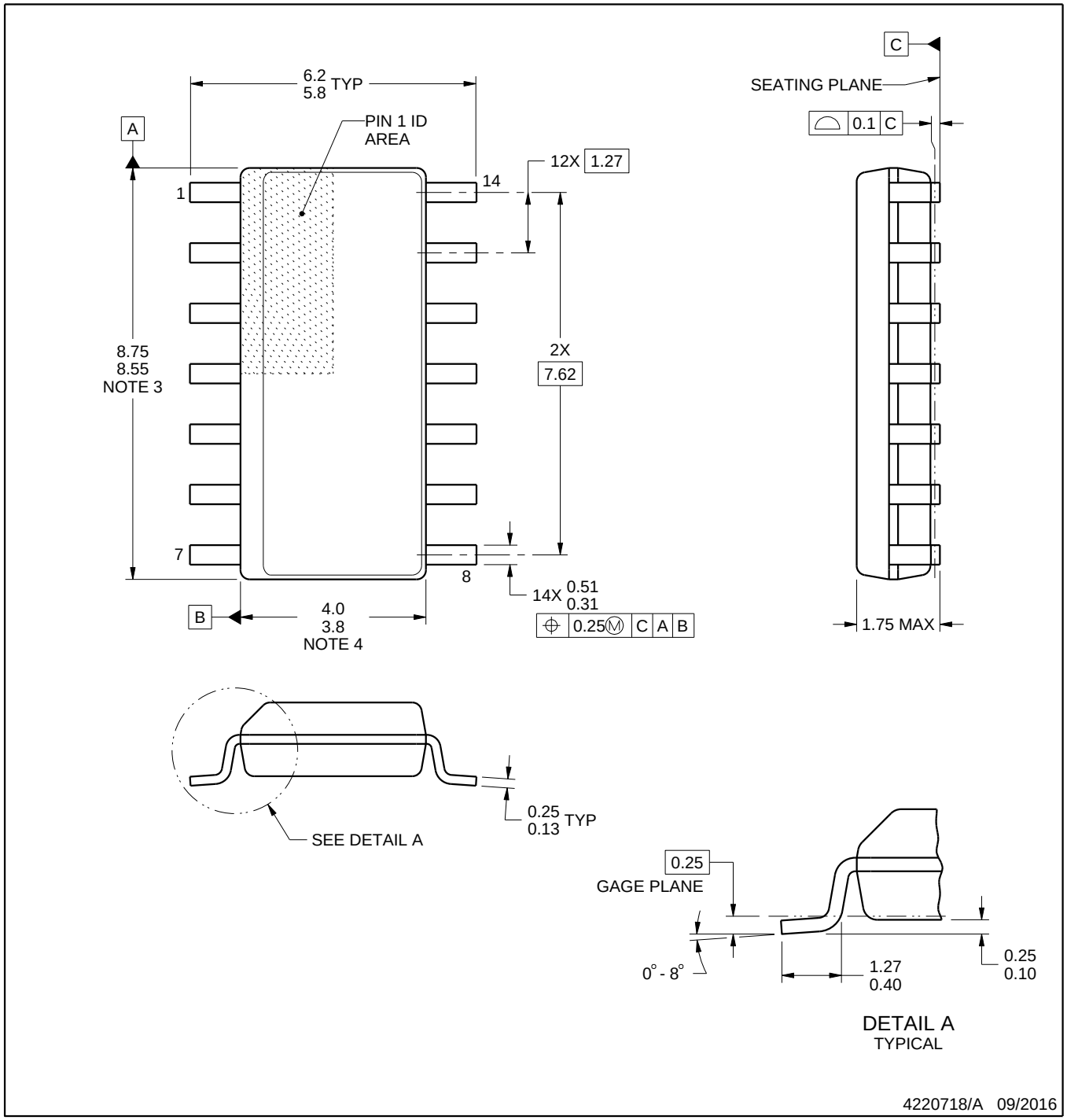


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

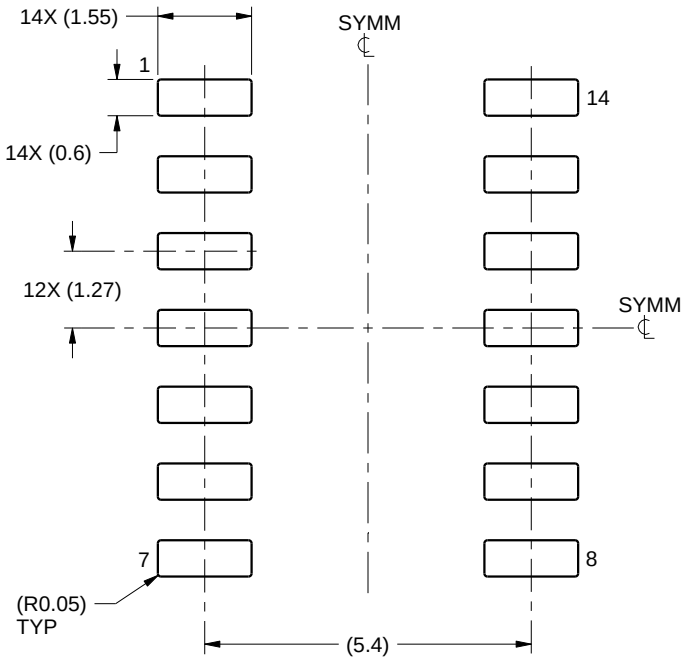
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

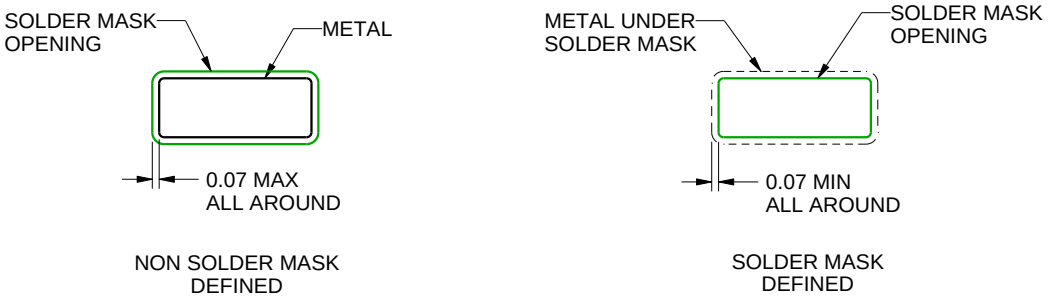
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

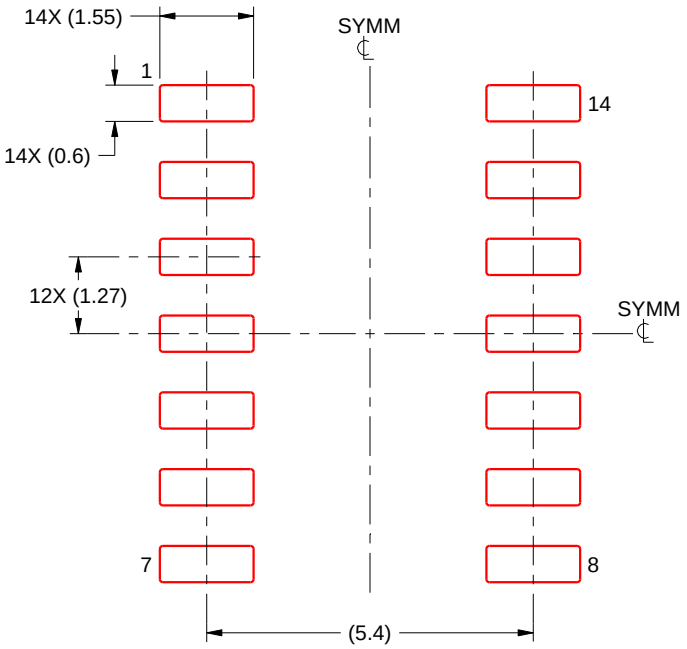
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

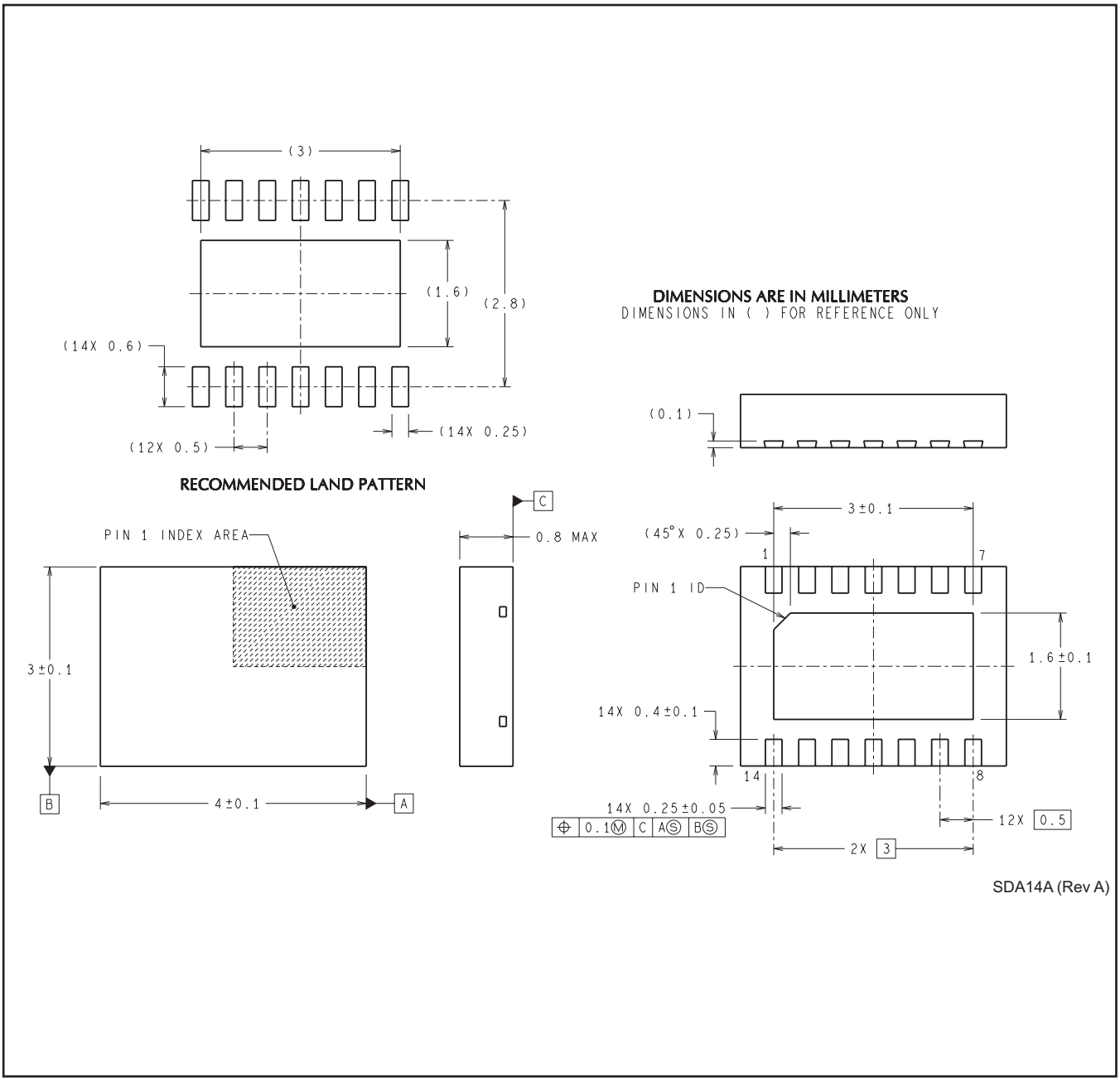
4220718/A 09/2016

NOTES: (continued)

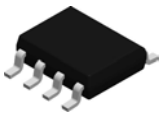
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NHK0014A



SDA14A (Rev A)

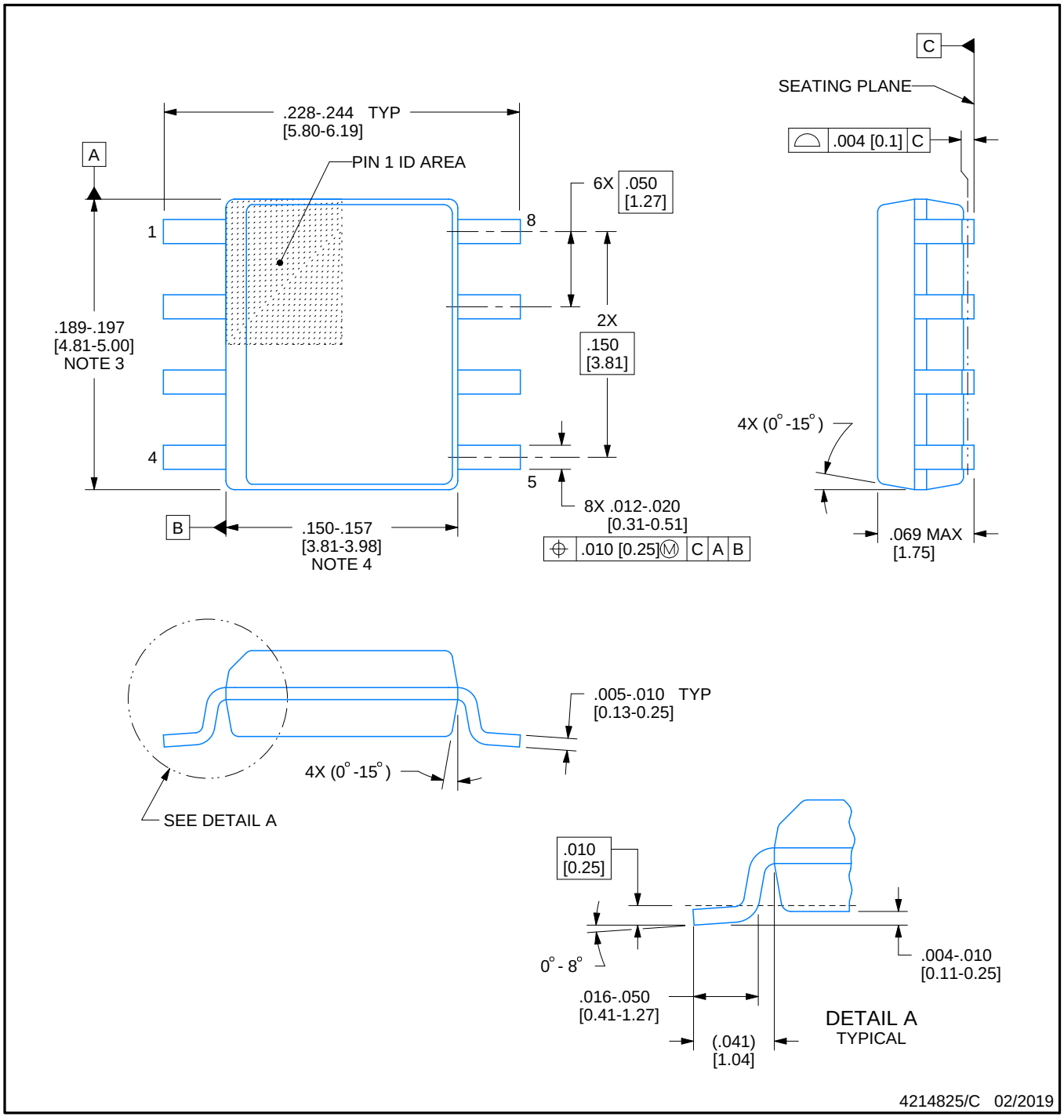


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

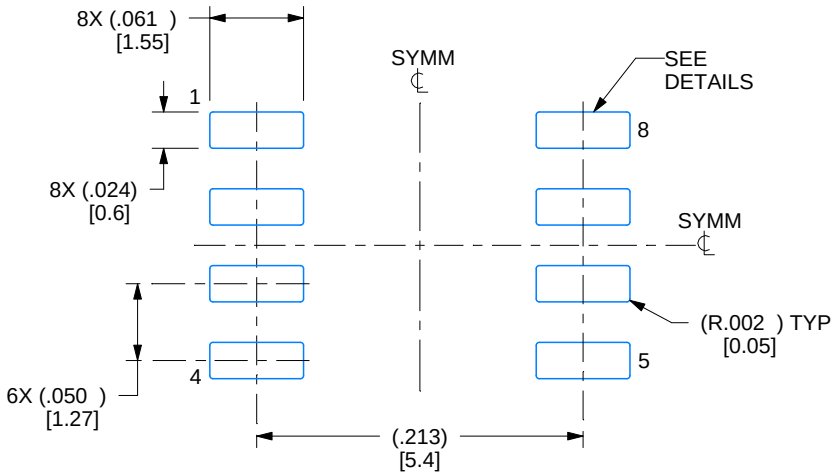
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

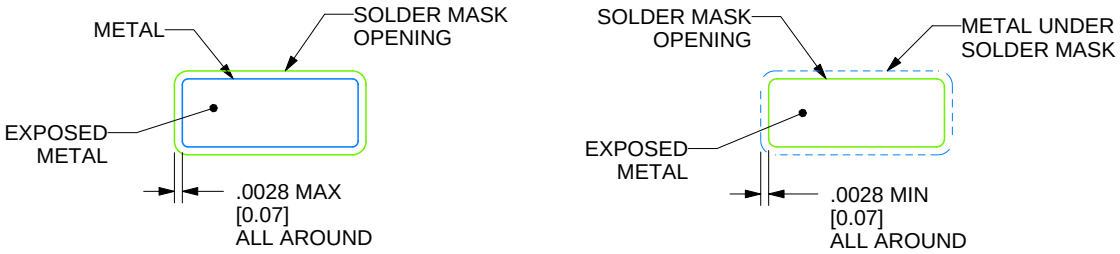
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

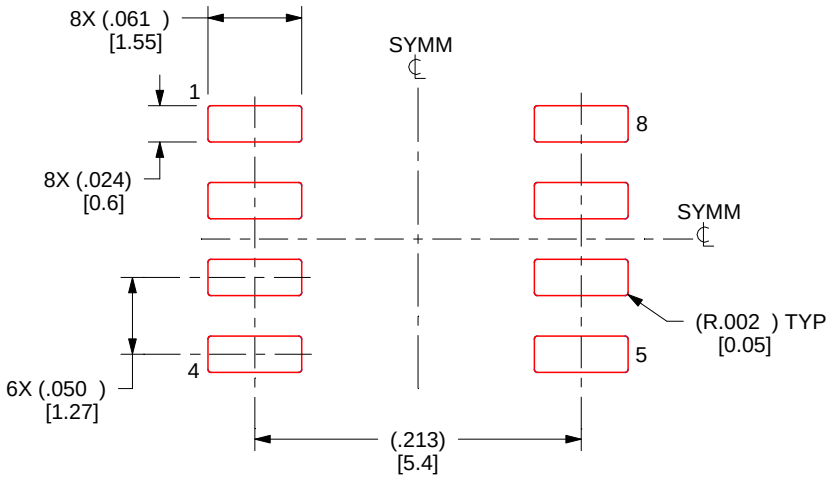
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

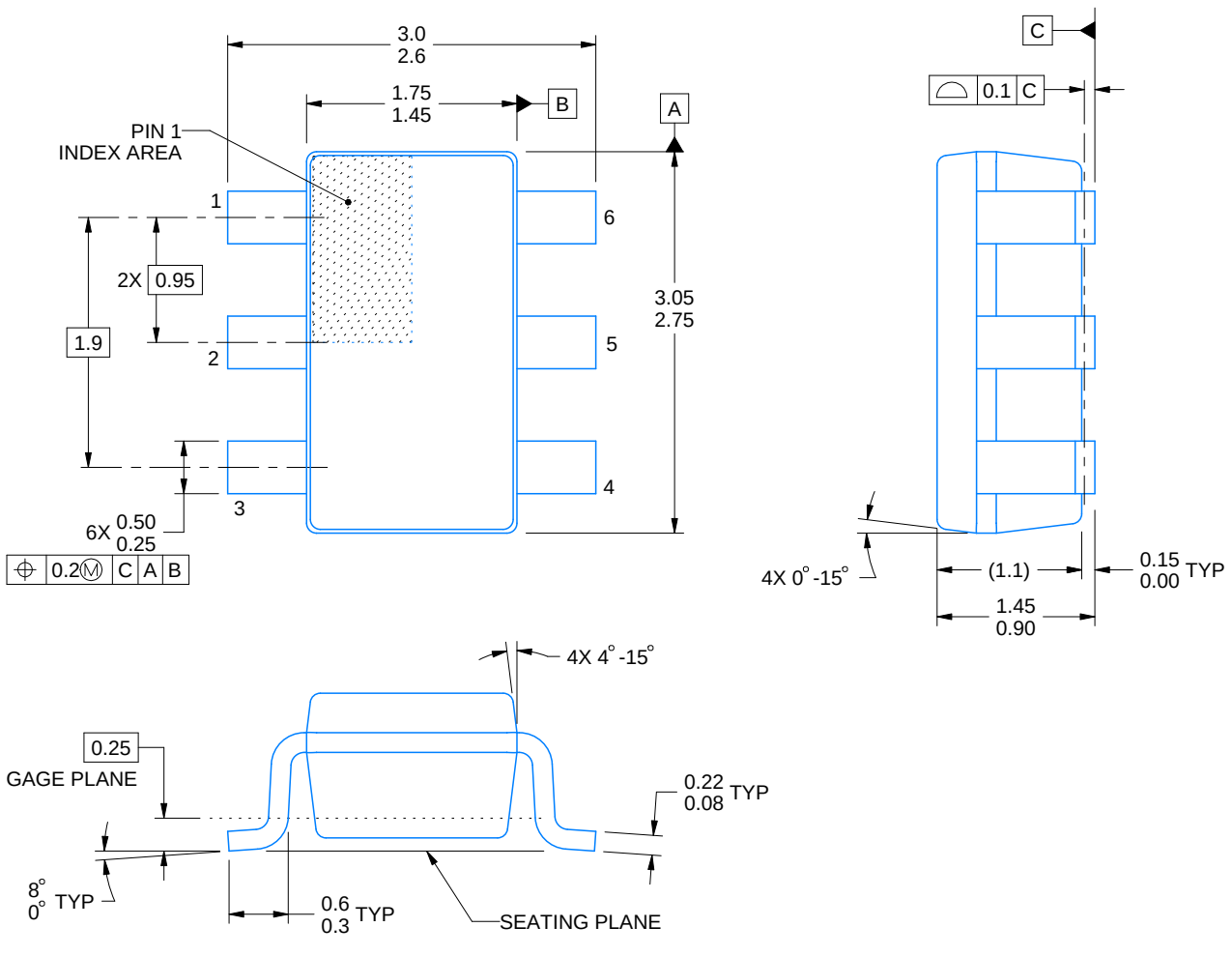
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

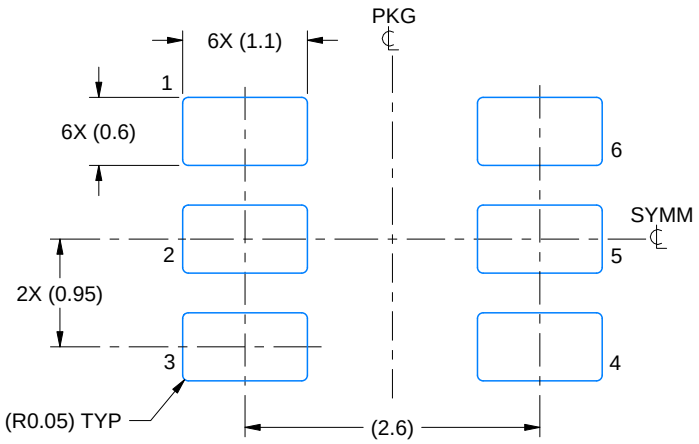
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

EXAMPLE BOARD LAYOUT

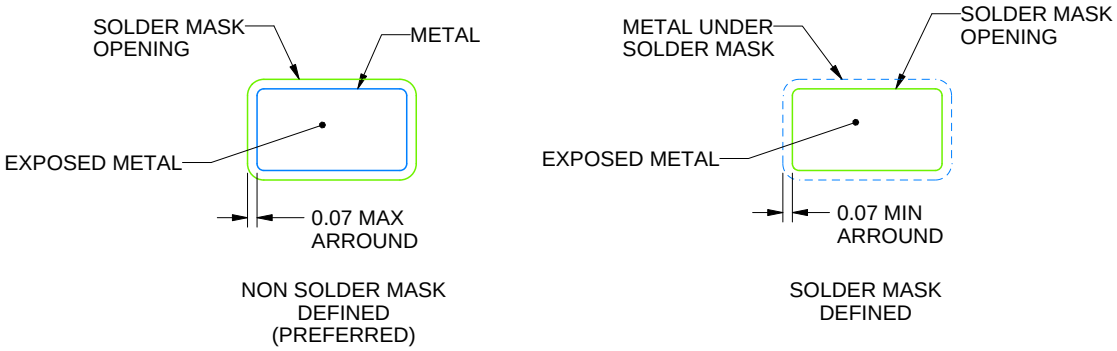
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

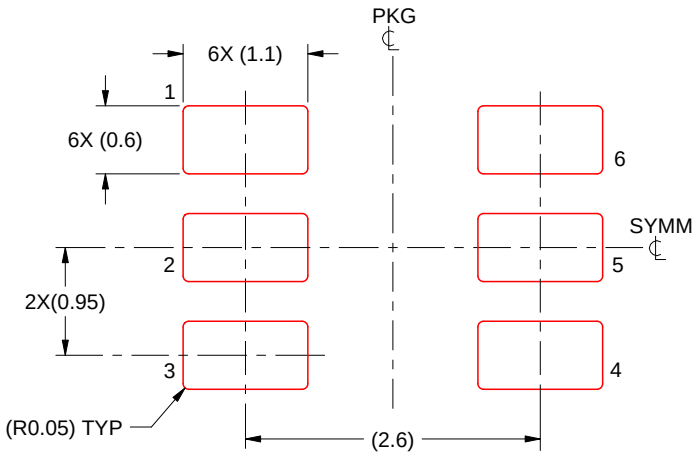
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

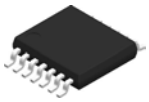


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

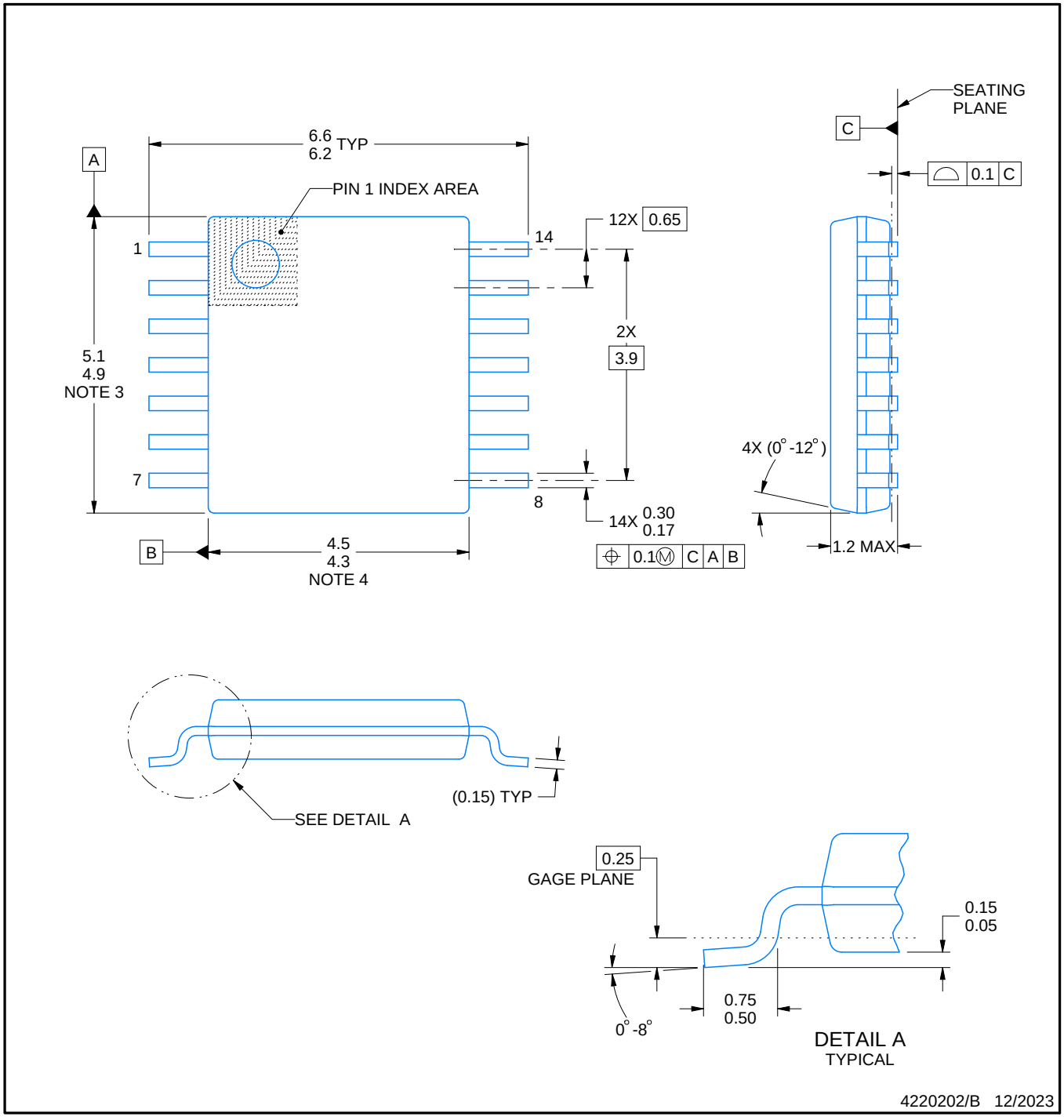


PACKAGE OUTLINE

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

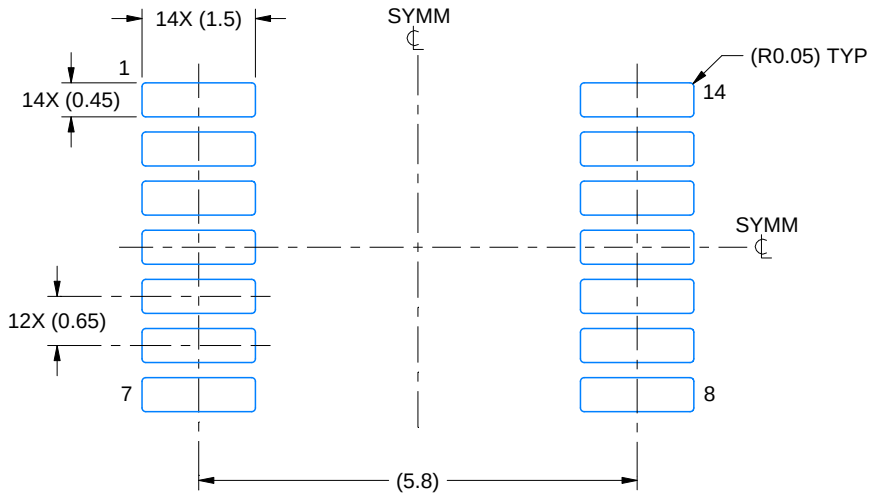
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

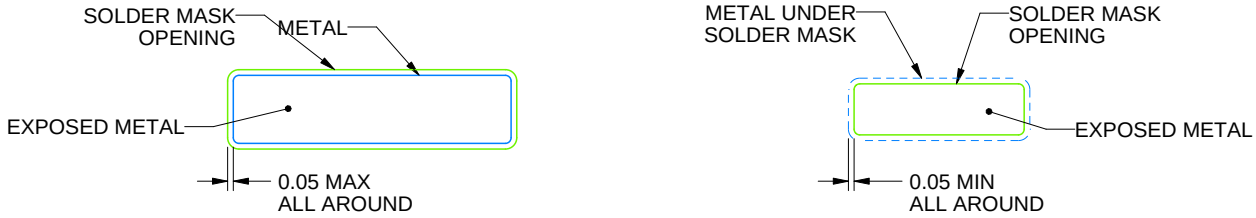
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

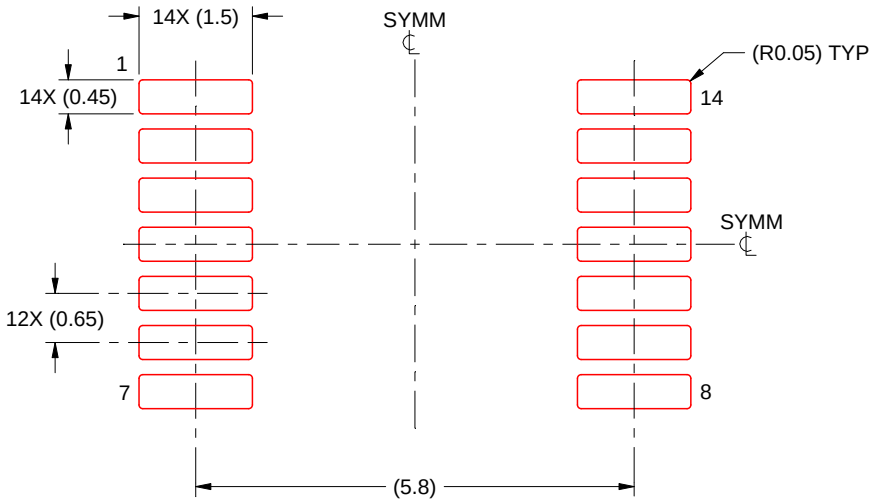
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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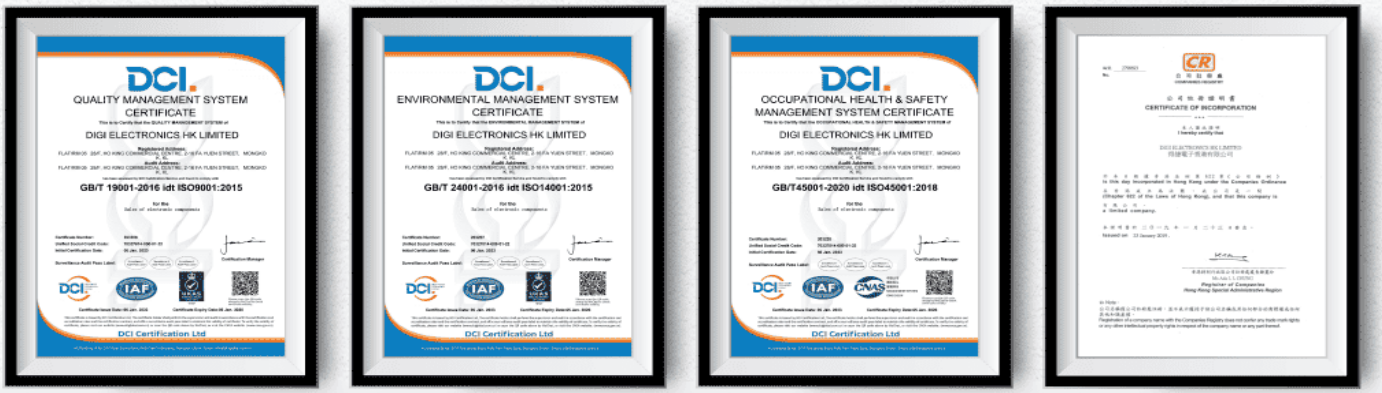

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