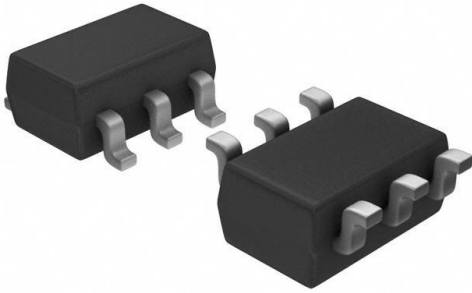


# LMV761MF/NOPB Datasheet

[www.digi-electronics.com](http://www.digi-electronics.com)



LMV761MF/NOPB

<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	LMV761MF/NOPB-DG
Manufacturer	<a href="#">Texas Instruments</a>
Manufacturer Product Number	LMV761MF/NOPB
Description	IC COMPARATOR 1 GEN PUR SOT23-6
Detailed Description	Comparator General Purpose Push-Pull SOT-23-6



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

LMV761MF/NOPB

Series:

-

Type:

General Purpose

Output Type:

Push-Pull

Voltage - Input Offset (Max):

0.2mV @ 5V

Current - Output (Typ):

-

CMRR, PSRR (Typ):

100dB CMRR, 110dB PSRR

Hysteresis:

-

Package / Case:

SOT-23-6

Supplier Device Package:

SOT-23-6

Manufacturer:

Texas Instruments

Product Status:

Active

Number of Elements:

1

Voltage - Supply, Single/Dual ( $\pm$ ):

2.7V ~ 5V

Current - Input Bias (Max):

50pA @ 5V

Current - Quiescent (Max):

700 $\mu$ A

Propagation Delay (Max):

225ns

Operating Temperature:

-40°C ~ 125°C

Mounting Type:

Surface Mount

Base Product Number:

LMV761

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

# LMV76x and LMV762Q-Q1 Low-Voltage, Precision Comparator With Push-Pull Output

## 1 Features

- $V_S = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Typical Values Unless Specified
- Input Offset Voltage 0.2 mV
- Input Offset Voltage (Maximum Over Temp) 1 mV
- Input Bias Current 0.2 pA
- Propagation Delay (OD = 50 mV) 120 ns
- Low Supply Current 300  $\mu\text{A}$
- CMRR 100 dB
- PSRR 110 dB
- Extended Temperature Range  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Push-Pull Output
- Ideal for 2.7-V and 5-V Single-Supply Applications
- Available in Space-Saving Packages:
  - 6-Pin SOT-23 (Single With Shutdown)
  - 8-Pin SOIC (Single With Shutdown)
  - 8-Pin SOIC and VSSOP (Dual Without Shutdown)
- LMV762Q-Q1 is Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level M2

## 2 Applications

- Portable and Battery-Powered Systems
- Scanners
- Set-Top Boxes
- High-Speed Differential Line Receiver
- Window Comparators
- Zero-Crossing Detectors
- High-Speed Sampling Circuits
- Automotive

## 3 Description

The LMV76x devices are precision comparators intended for applications requiring low noise and low input offset voltage. The LMV761 single has a shutdown pin that can be used to disable the device and reduce the supply current. The LMV761 is available in a space-saving 6-pin SOT-23 or 8-Pin SOIC package. The LMV762 dual is available in 8-pin SOIC or VSSOP package. The LMV762Q-Q1 is available VSSOP and SOIC packages.

These devices feature a CMOS input and push-pull output stage. The push-pull output stage eliminates the need for an external pullup resistor.

The LMV76x are designed to meet the demands of small size, low power and high performance required by portable and battery-operated electronics.

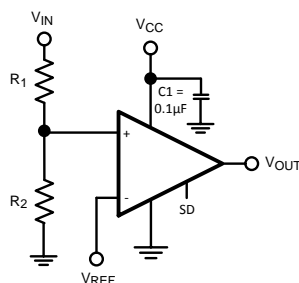
The input offset voltage has a typical value of 200  $\mu\text{V}$  at room temperature and a 1-mV limit over temperature.

### Device Information<sup>(1)</sup>

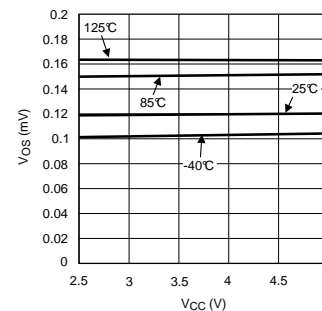
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV761	SOIC (8)	4.90 mm x 3.91 mm
	SOT-23 (6)	2.90 mm x 1.60 mm
LMV762 LMV762Q-Q1	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Threshold Detector



### $V_{OS}$ vs $V_{CC}$



**LMV761, LMV762, LMV762Q-Q1**

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**4 Revision History**

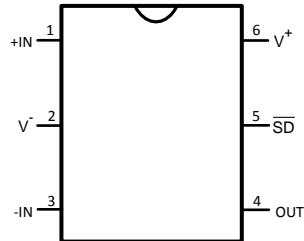
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision H (March 2013) to Revision I</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>

<b>Changes from Revision G (March 2013) to Revision H</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<b>15</b>

## 5 Pin Configuration and Functions

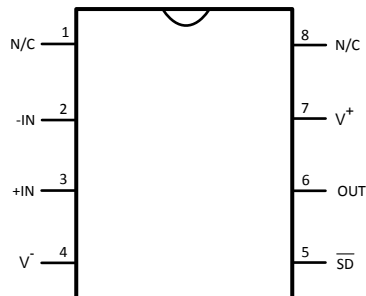
**LMV761 (Single) DBV Package  
6-Pin SOT-23  
Top View**



**Pin Functions for SOT-23**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	+IN	I	Noninverting input
2	V <sup>-</sup>	P	Negative power terminal
3	-IN	I	Inverting input
4	OUT	O	Output
5	SDB	I	Shutdown (active low)
6	V <sup>+</sup>	P	Positive power terminal

**LMV761 (Single) D Package  
8-Pin SOIC  
Top View**



**Pin Functions for SOIC (Single)**

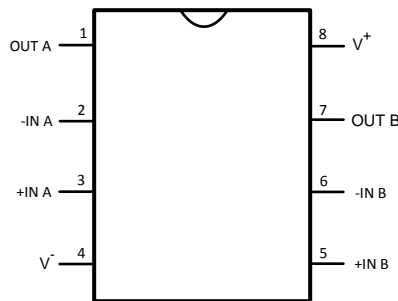
PIN		TYPE	DESCRIPTION
NO.	NAME		
1	N/C	—	No Connect (not internally connected)
2	-IN	I	Inverting Input
3	+IN	I	Noninverting Input
4	V <sup>-</sup>	P	Negative Power Terminal
5	SDB	I	Shutdown (active low)
6	OUT	O	Output
7	V <sup>+</sup>	P	Positive Power Terminal
8	N/C	—	No Connect (not internally connected)

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**LMV762, LMV762Q-Q1 (Dual) DBV or DGK Package  
8-Pin SOIC or VSSOP  
Top View**

**Pin Functions for SOIC and VSSOP (Dual)**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTA	O	Channel A Output
2	-INA	I	Channel A Inverting Input
3	+INA	I	Channel A Noninverting Input
4	V <sup>-</sup>	P	Negative Power Terminal
5	+INB	I	Channel B Noninverting Input
6	-INB	I	Channel B Inverting Input
7	OUTB	O	Channel B Output
8	V <sup>+</sup>	P	Positive Power Terminal

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See <sup>(1)(2)</sup>

		MIN	MAX	UNIT
Supply voltage (V <sup>+</sup> – V <sup>-</sup> )			5.5	V
Differential input voltage		Supply Voltage		
Voltage between any two pins		Supply Voltage		
Output short circuit duration <sup>(3)</sup>	Current at input pin		±5	mA
Soldering information	Infrared or convection (20 sec.)		235	°C
	Wave soldering (10 sec.) (Lead temp)		260	°C
Junction temperature			150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output current in excess of ±25 mA over long term may adversely affect reliability.

## 6.2 ESD Ratings: LMV761, LMV762

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge <sup>(1)</sup>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(2)</sup>	± 2000
		Machine model	± 200

(1) Unless otherwise specified human body model is 1.5 kΩ in series with 100 pF. Machine model 200 pF.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 ESD Ratings: LMV762Q-Q1

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	± 2000
		Machine model	± 200

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.4 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage (V <sup>+</sup> – V <sup>-</sup> )	2.7	5.25	V
Temperature range	-40	125	°C

## 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LMV761	LMV762, LMV762Q-Q1		UNIT
	D (SOIC)	DBV (SOT-23)	DGK (VSSOP)	
	8 PINS	6 PINS	8 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance <sup>(2)</sup>	190	265	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>) R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PCB.

## 6.6 2.7-V Electrical Characteristics

Unless otherwise specified, all limited ensured for T<sub>J</sub> = 25°C, V<sub>CM</sub> = V<sup>+</sup> / 2, V<sup>+</sup> = 2.7 V, V<sup>-</sup> = 0 V<sup>-</sup>.

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
V <sub>OS</sub> Input offset voltage		0.2			mV
	apply at the temperature extremes <sup>(3)</sup>	1			
I <sub>B</sub> Input bias current <sup>(4)</sup>		0.2			pA
I <sub>OS</sub> Input offset current <sup>(4)</sup>		0.001			pA
CMRR Common-mode rejection ratio	0 V < V <sub>CM</sub> < V <sub>CC</sub> – 1.3 V	80	100		dB
PSRR Power supply rejection ratio	V <sup>+</sup> = 2.7 V to 5 V	80	110		dB
CMVR Input common-mode voltage range	CMRR > 50 dB	apply at the temperature extremes <sup>(3)</sup>		1.5	V
V <sub>O</sub> Output swing	Output swing high	V <sup>+</sup> – 0.35 V <sup>+</sup> – 0.1			V
	Output swing low	90			250
I <sub>SC</sub> Output short circuit current <sup>(5)</sup>	Sourcing, V <sub>O</sub> = 1.35 V, V <sub>ID</sub> = 200 mV	6	20		mA
	Sinking, V <sub>O</sub> = 1.35 V, V <sub>ID</sub> = –200 mV	6	15		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Maximum temperature ensured range is –40°C to +125°C.

(4) Specified by design.

(5) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>. See [Recommended Operating Conditions](#) for information on temperature de-rating of this device. Absolute Maximum Rating indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

**LMV761, LMV762, LMV762Q-Q1**

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**2.7-V Electrical Characteristics (continued)**Unless otherwise specified, all limited ensured for  $T_J = 25^\circ\text{C}$ ,  $V_{CM} = V^+ / 2$ ,  $V^+ = 2.7\text{ V}$ ,  $V^- = 0\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$I_S$	Supply current LMV761 (single comparator)			275	700	$\mu\text{A}$
	LMV762, LMV762Q-Q1 (both comparators)			550		$\mu\text{A}$
		apply at the temperature extremes <sup>(3)</sup>			1400	
$I_{OUT\ LEAKAGE}$	Output leakage I at shutdown	$\overline{SD} = \text{GND}$ , $V_O = 2.7\text{ V}$		0.2		$\mu\text{A}$
$I_S\ LEAKAGE$	Supply leakage I at shutdown	$\overline{SD} = \text{GND}$ , $V_{CC} = 2.7\text{ V}$		0.2	2	$\mu\text{A}$

**6.7 5-V Electrical Characteristics**Unless otherwise specified, all limited ensured for  $T_J = 25^\circ\text{C}$ ,  $V_{CM} = V^+ / 2$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OS}$	Input offset voltage			0.2		mV
		apply at the temperature extremes <sup>(3)</sup>			1	
$I_B$	Input bias current <sup>(4)</sup>			0.2	50	pA
$I_{OS}$	Input offset current <sup>(4)</sup>			0.01	5	pA
CMRR	Common-mode rejection ratio	$0\text{ V} < V_{CM} < V_{CC} - 1.3\text{ V}$	80	100		dB
PSRR	Power supply rejection ratio	$V^+ = 2.7\text{ V}$ to $5\text{ V}$	80	110		dB
CMVR	Input common-mode voltage range	CMRR > 50 dB	apply at the temperature extremes <sup>(3)</sup>		3.8	V
$V_O$	Output swing high	$I_L = 4\text{ mA}$ , $V_{ID} = 200\text{ mV}$	$V^+ - 0.35$	$V^+ - 0.1$		V
	Output swing low	$I_L = -4\text{ mA}$ , $V_{ID} = -200\text{ mV}$		120	250	mV
$I_{SC}$	Output short circuit current <sup>(5)</sup>	Sourcing, $V_O = 2.5\text{ V}$ , $V_{ID} = 200\text{ mV}$	6	60		mA
		Sinking, $V_O = 2.5\text{ V}$ , $V_{ID} = -200\text{ mV}$	6	40		
$I_S$	Supply current LMV761 (single comparator)			225	700	$\mu\text{A}$
	LMV762, LMV762Q-Q1 (both comparators)			450		$\mu\text{A}$
		apply at the temperature extremes <sup>(3)</sup>			1400	
$I_{OUT\ LEAKAGE}$	Output leakage I at shutdown	$\overline{SD} = \text{GND}$ , $V_O = 5\text{ V}$		0.2		$\mu\text{A}$
$I_S\ LEAKAGE$	Supply leakage I at shutdown	$\overline{SD} = \text{GND}$ , $V_{CC} = 5\text{ V}$		0.2	2	$\mu\text{A}$

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Maximum temperature ensured range is  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

(4) Specified by design.

(5) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . See [Recommended Operating Conditions](#) for information on temperature de-rating of this device. Absolute Maximum Rating indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

## 6.8 2-V Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}$	Propagation delay $R_L = 5.1 \text{ k}\Omega$ $C_L = 50 \text{ pF}$	Overdrive = 5 mV		270		ns
		Overdrive = 10 mV		205		
		Overdrive = 50 mV		120		
$t_{SKEW}$	Propagation delay skew			5		ns
$t_r$	Output rise time	10% to 90%		1.7		ns
$t_f$	Output fall time	90% to 10%		1.8		ns
$t_{on}$	Turnon time from shutdown			6		$\mu\text{s}$

## 6.9 5-V Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

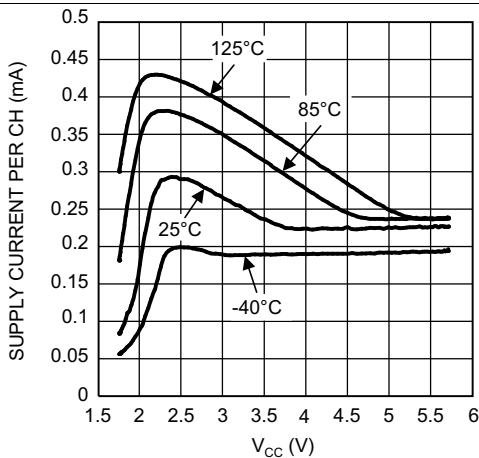
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}$	Propagation delay $R_L = 5.1 \text{ k}\Omega$ $C_L = 50 \text{ pF}$	Overdrive = 5 mV		225		ns
		Overdrive = 10 mV		190		
		Overdrive = 50 mV		120		
$t_{SKEW}$	Propagation delay skew			5		ns
$t_r$	Output rise time	10% to 90%		1.7		ns
$t_f$	Output fall time	90% to 10%		1.5		ns
$t_{on}$	Turnon time from shutdown			4		$\mu\text{s}$

**LMV761, LMV762, LMV762Q-Q1**

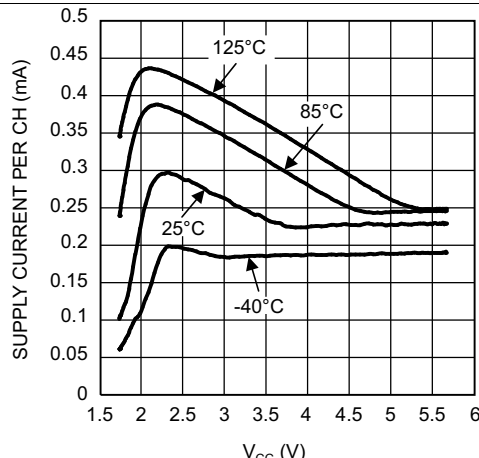
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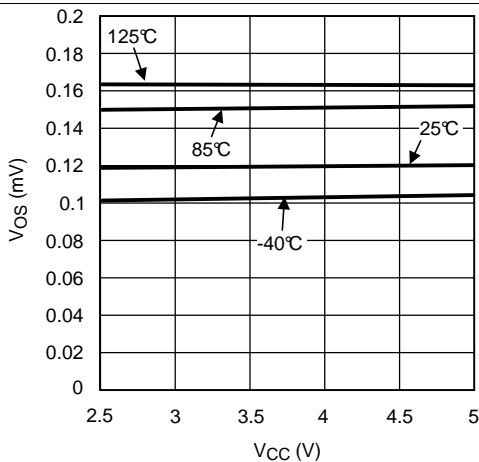
**6.10 Typical Characteristics**



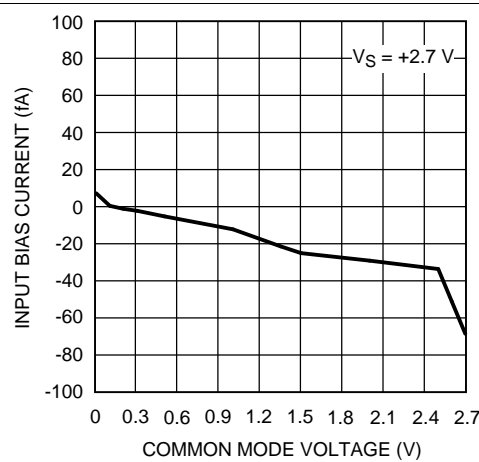
**Figure 1. PSI vs V<sub>CC</sub>**



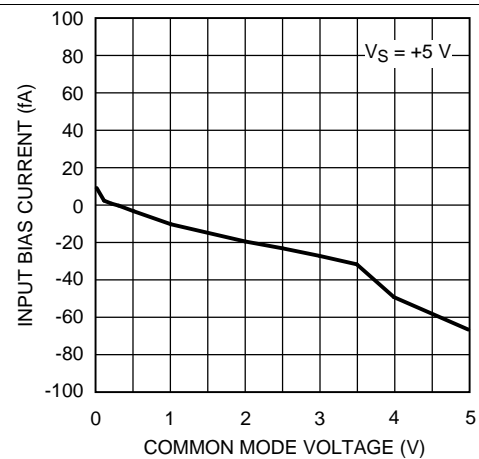
**Figure 2. PSI vs V<sub>CC</sub>**



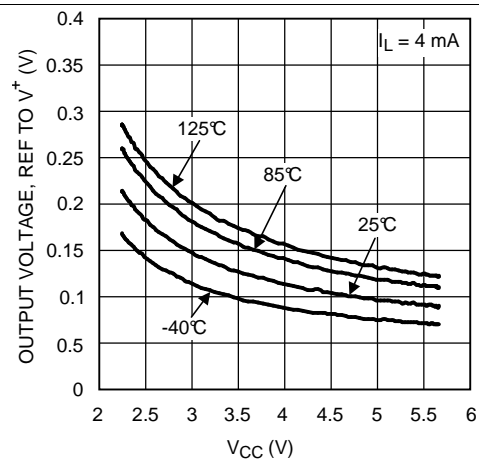
**Figure 3. V<sub>OS</sub> vs V<sub>CC</sub>**



**Figure 4. Input Bias vs Common Mode at 25°C**



**Figure 5. Input Bias vs Common Mode at 25°C**



**Figure 6. Output Voltage vs Supply Voltage**

Typical Characteristics (continued)

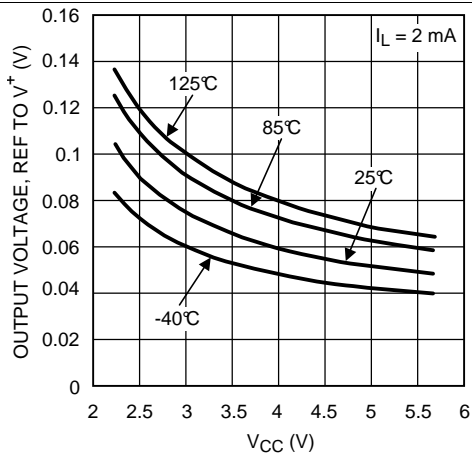


Figure 7. Output Voltage vs Supply Voltage

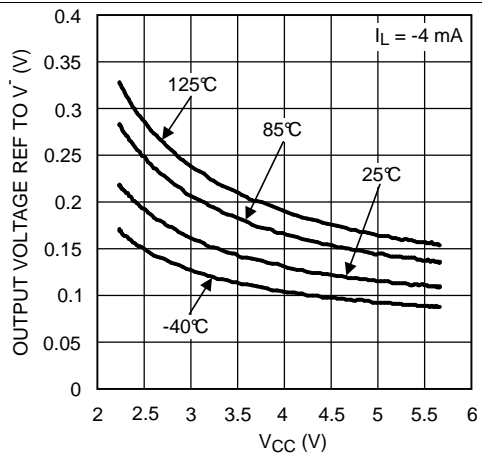


Figure 8. Output Voltage vs Supply Voltage

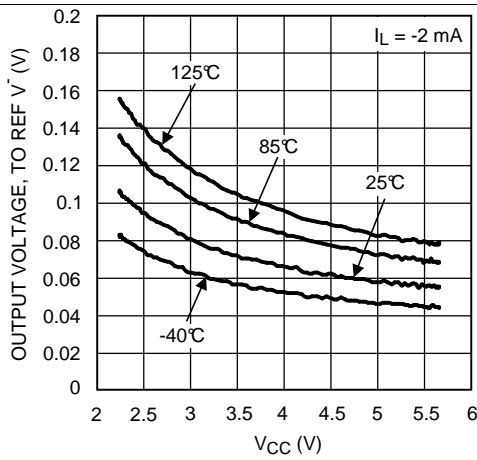


Figure 9. Output Voltage vs Supply Voltage

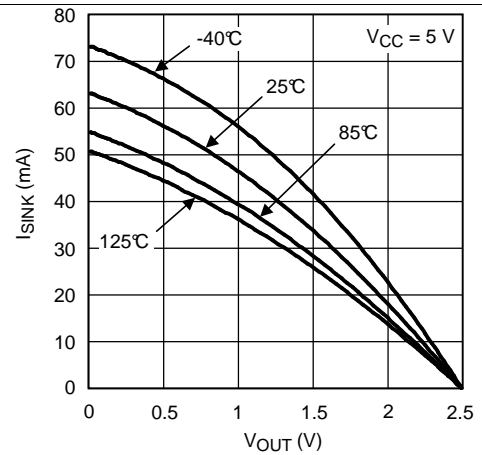


Figure 10. ISOURCE vs VOUT

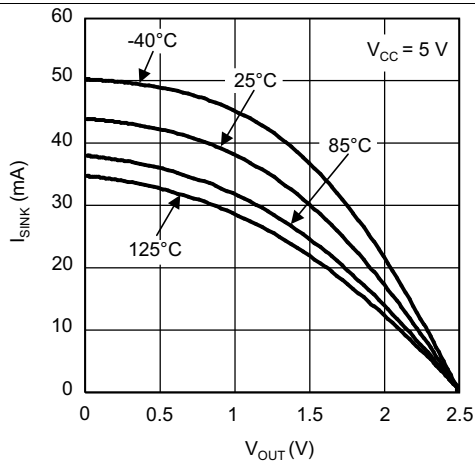


Figure 11. ISINK vs VOUT

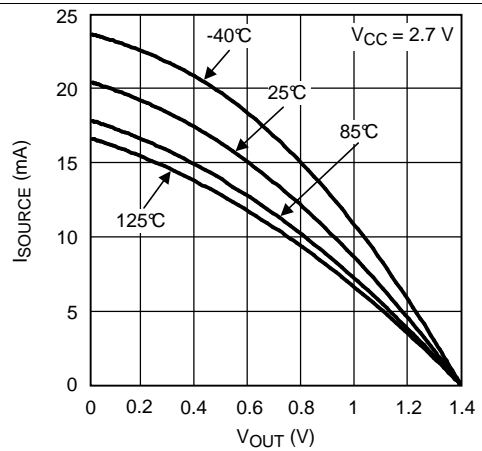


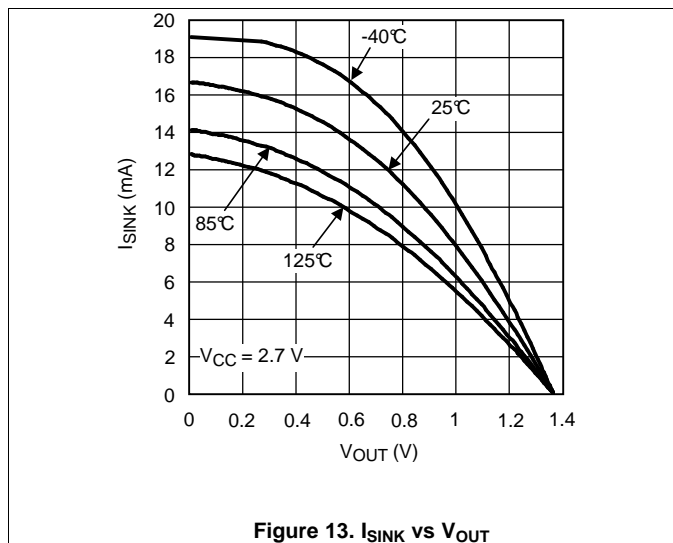
Figure 12. ISOURCE vs VOUT

**LMV761, LMV762, LMV762Q-Q1**

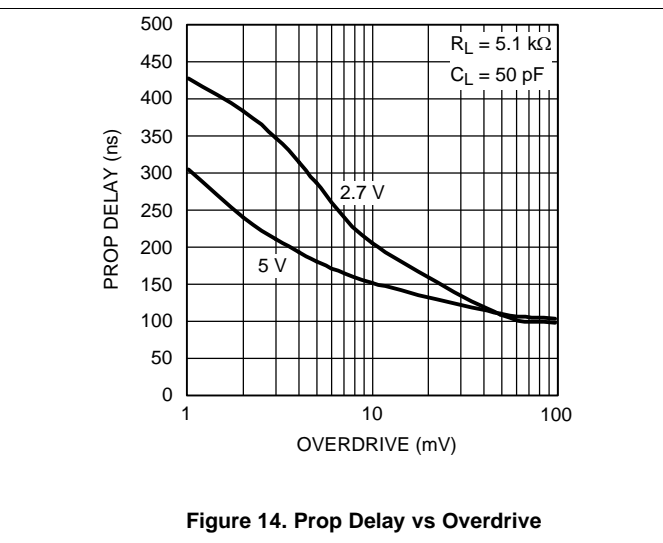
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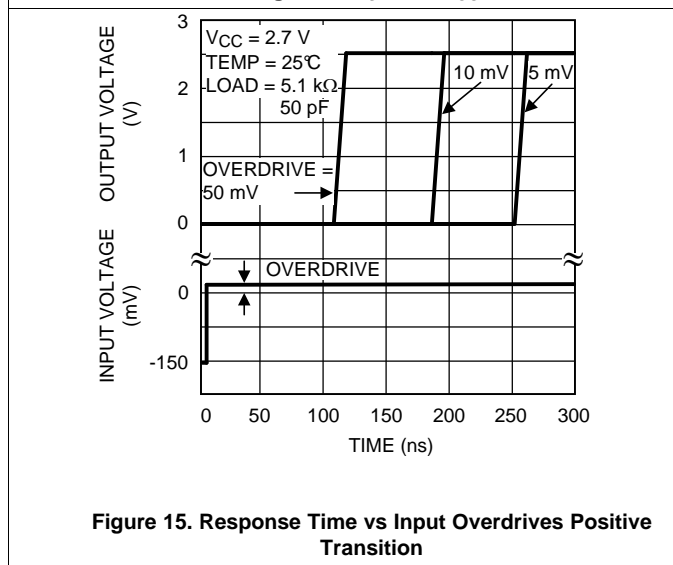
**Typical Characteristics (continued)**



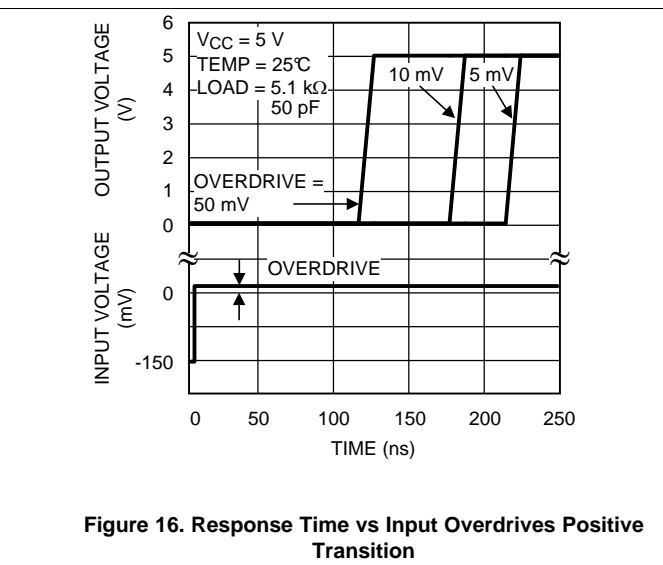
**Figure 13.  $I_{SINK}$  vs  $V_{OUT}$**



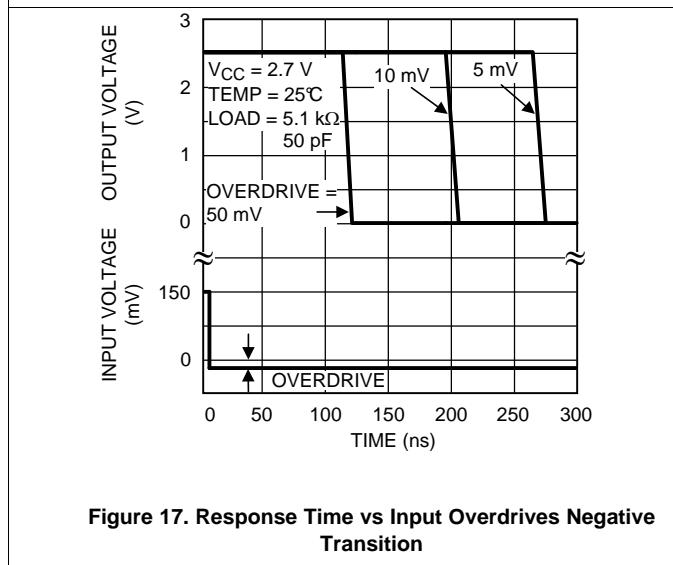
**Figure 14. Prop Delay vs Overdrive**



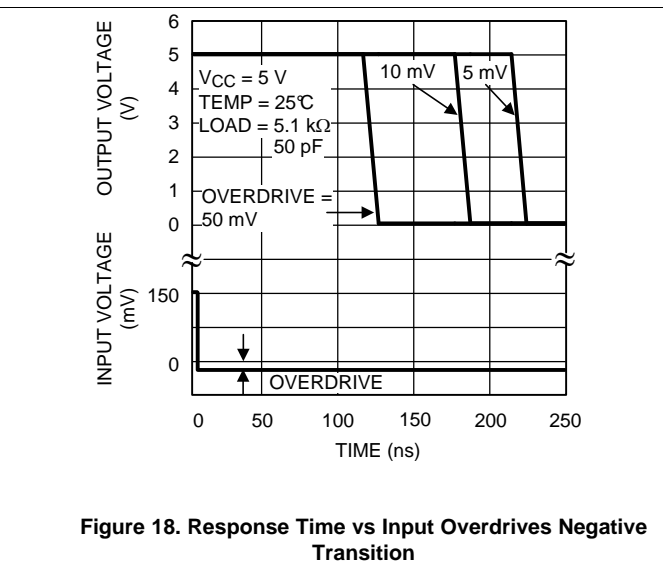
**Figure 15. Response Time vs Input Overdrives Positive Transition**



**Figure 16. Response Time vs Input Overdrives Positive Transition**



**Figure 17. Response Time vs Input Overdrives Negative Transition**



**Figure 18. Response Time vs Input Overdrives Negative Transition**

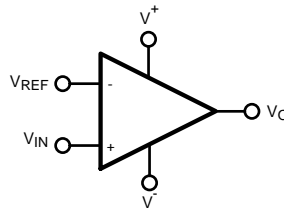
## 7 Detailed Description

### 7.1 Overview

The LMV76x family of precision comparators is available in a variety of packages and is ideal for portable and battery-operated electronics.

To minimize external components, the LMV76x family features a push-pull output stage where the output levels are power-supply determined. In addition, the LMV761 (single) features an active-low shutdown pin that can be used to disable the device and reduce the supply current.

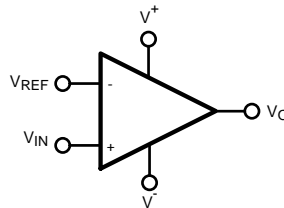
### 7.2 Functional Block Diagram



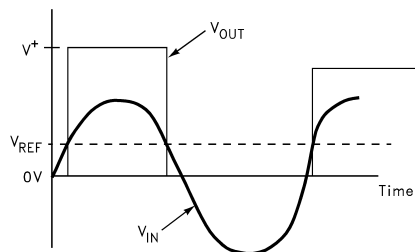
### 7.3 Feature Description

#### 7.3.1 Basic Comparator

A basic comparator circuit is used to convert analog input signals to digital output signals. The comparator compares an input voltage ( $V_{IN}$ ) at the noninverting input to the reference voltage ( $V_{REF}$ ) at the inverting pin. If  $V_{IN}$  is less than  $V_{REF}$  the output ( $V_O$ ) is low ( $V_{OL}$ ). However, if  $V_{IN}$  is greater than  $V_{REF}$ , the output voltage ( $V_O$ ) is high ( $V_{OH}$ ).



**Figure 19. Basic Comparator Without Hysteresis**



**Figure 20. Basic Comparator**

#### 7.3.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near the input offset voltage of the comparator, which tends to occur when the voltage on one input is equal or very close to the other input voltage. Adding hysteresis can prevent this problem. Hysteresis creates two switching thresholds (one for the rising input voltage and the other for the falling input voltage). Hysteresis is the voltage difference between the two switching thresholds. When both inputs are nearly equal, hysteresis causes one input to effectively move quickly past the other. Thus, moving the input out of the region in which oscillation may occur.

**LMV761, LMV762, LMV762Q-Q1**

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**Feature Description (continued)**

Hysteresis can easily be added to a comparator in a noninverting configuration with two resistors and positive feedback [Figure 22](#). The output will switch from low to high when  $V_{IN}$  rises up to  $V_{IN1}$ , where  $V_{IN1}$  is calculated by [Equation 1](#):

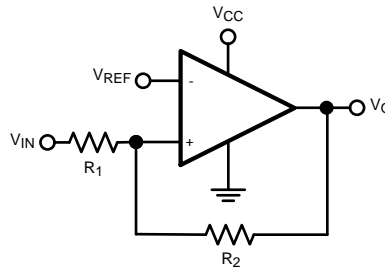
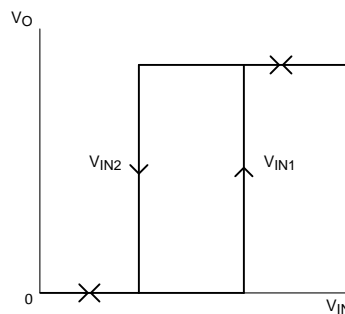
$$V_{IN1} = [V_{REF}(R_1 + R_2)] / R_2 \quad (1)$$

The output will switch from high to low when  $V_{IN}$  falls to  $V_{IN2}$ , where  $V_{IN2}$  is calculated by [Equation 2](#):

$$V_{IN2} = [V_{REF}(R_1 + R_2) - (V_{CC} R_1)] / R_2 \quad (2)$$

The Hysteresis is the difference between  $V_{IN1}$  and  $V_{IN2}$ , as calculated by [Equation 3](#):

$$\Delta V_{IN} = V_{IN1} - V_{IN2} = [V_{REF}(R_1 + R_2) / R_2] - [V_{REF}(R_1 + R_2) - (V_{CC} R_1) / R_2] = V_{CC} R_1 / R_2 \quad (3)$$


**Figure 21. Basic Comparator With Hysteresis**

**Figure 22. Noninverting Comparator Configuration**
**7.3.3 Input**

The LMV76x devices have near-zero input bias current, which allows very high resistance circuits to be used without any concern for matching input resistances. This near-zero input bias also allows the use of very small capacitors in R-C type timing circuits. This reduces the cost of the capacitors and amount of board space used.

**7.4 Device Functional Modes**
**7.4.1 Shutdown Mode**

The LMV761 features a low-power shutdown pin that is activated by driving  $\overline{SD}$  low. In shutdown mode, the output is in a high-impedance state, supply current is reduced to 20 nA and the comparator is disabled. Driving  $\overline{SD}$  high will turn the comparator on. The  $\overline{SD}$  pin must not be left unconnected due to the fact that it is a high-impedance input. When left unconnected, the output will be at an unknown voltage. Do **not** three-state the  $\overline{SD}$  pin.

The maximum input voltage for  $\overline{SD}$  is 5.5 V referred to ground and is not limited by  $V_{CC}$ . This allows the use of 5-V logic to drive  $\overline{SD}$  while  $V_{CC}$  operates at a lower voltage, such as 3 V. The logic threshold limits for  $\overline{SD}$  are proportional to  $V_{CC}$ .

## 8 Application and Implementation

### NOTE

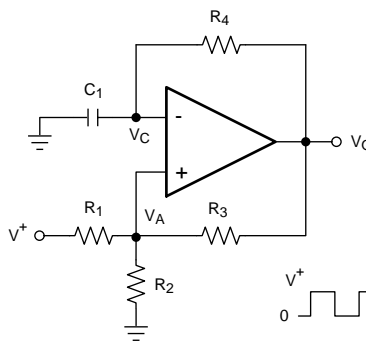
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LMV76x are single-supply comparators with 120 ns of propagation delay and 300  $\mu$ A of supply current.

### 8.2 Typical Application

A typical application for a LMV76x comparator is a programmable square-wave oscillator.



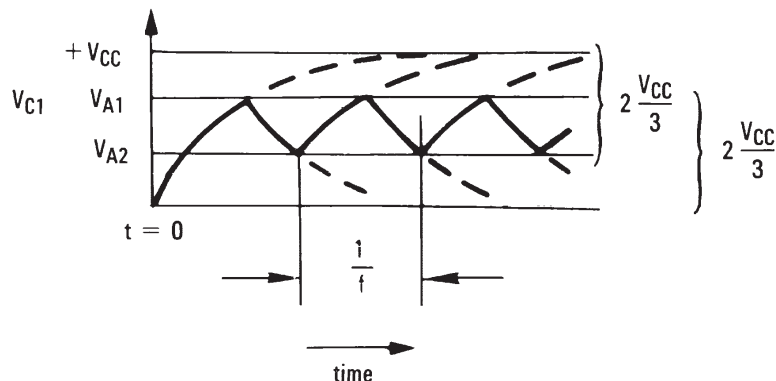
**Figure 23. Square-Wave Oscillator**

#### 8.2.1 Design Requirements

The circuit in [Figure 23](#) generates a square wave whose period is set by the RC time constant of the capacitor  $C_1$  and resistor  $R_4$ .  $V^+ = 5$  V unless otherwise specified.

#### 8.2.2 Detailed Design Procedure

The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.



**Figure 24. Square-Wave Oscillator Timing Thresholds**

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**Typical Application (continued)**

Consider the output of Figure 23 is high to analyze the circuit. That implies that the inverted input ( $V_C$ ) is lower than the noninverting input ( $V_A$ ). This causes the  $C_1$  to be charged through  $R_4$ , and the voltage  $V_C$  increases until it is equal to the noninverting input. The value of  $V_A$  at this point is calculated by Equation 4:

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \parallel R_3} \quad (4)$$

If  $R_1 = R_2 = R_3$ , then  $V_{A1} = 2 V_{CC} / 3$

At this point the comparator switches pulling down the output to the negative rail. The value of  $V_A$  at this point is calculated by Equation 5:

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)} \quad (5)$$

If  $R_1 = R_2 = R_3$ , then  $V_{A2} = V_{CC} / 3$ .

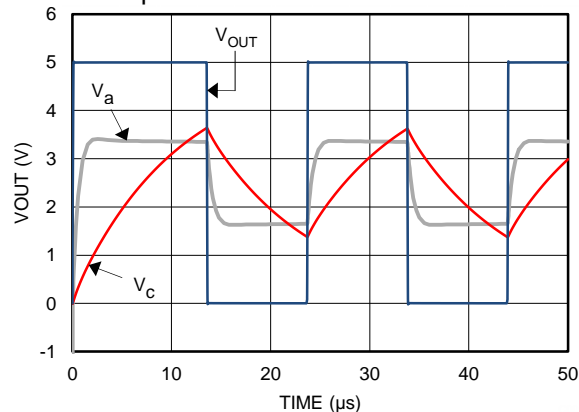
The capacitor  $C_1$  now discharges through  $R_4$ , and the voltage  $V_C$  decreases until it is equal to  $V_{A2}$ , at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge  $C_1$  from  $2 V_{CC} / 3$  to  $V_{CC} / 3$ , which is given by  $R_4 C_1 \times \ln 2$ . Hence, the formula for the frequency is calculated by Equation 6:

$$F = 1 / (2 \times R_4 \times C_1 \times \ln 2) \quad (6)$$

**8.2.3 Application Curve**

Figure Figure 25 shows the simulated results of an oscillator using the following values:

- $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
- $C_1 = 100 \text{ pF}$ ,  $C_L = 20 \text{ pF}$
- $V_+ = 5 \text{ V}$ ,  $V_- = \text{GND}$
- $C_{\text{STRAY}}$  (not shown) from  $V_a$  to GND =  $10 \text{ pF}$



**Figure 25. Square-Wave Oscillator Output Waveform**

## 9 Power Supply Recommendations

To minimize supply noise, power supplies must be decoupled by a 0.1- $\mu\text{F}$  ceramic capacitor in parallel with a 10- $\mu\text{F}$  capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during output transitions. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to *ring* due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV6x as a high-speed device. Keep the ground paths short and place small (low-ESR ceramic) bypass capacitors directly between the  $V^+$  and  $V^-$  pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

## 10 Layout

### 10.1 Layout Guidelines

The LMV76x is designed to be stable and oscillation free, but it is still important to include the proper bypass capacitors and ground pick-ups. Ceramic 0.1- $\mu\text{F}$  capacitors must be placed at both supplies to provide clean switching. Minimize the length of signal traces to reduce stray capacitance.

### 10.2 Layout Example

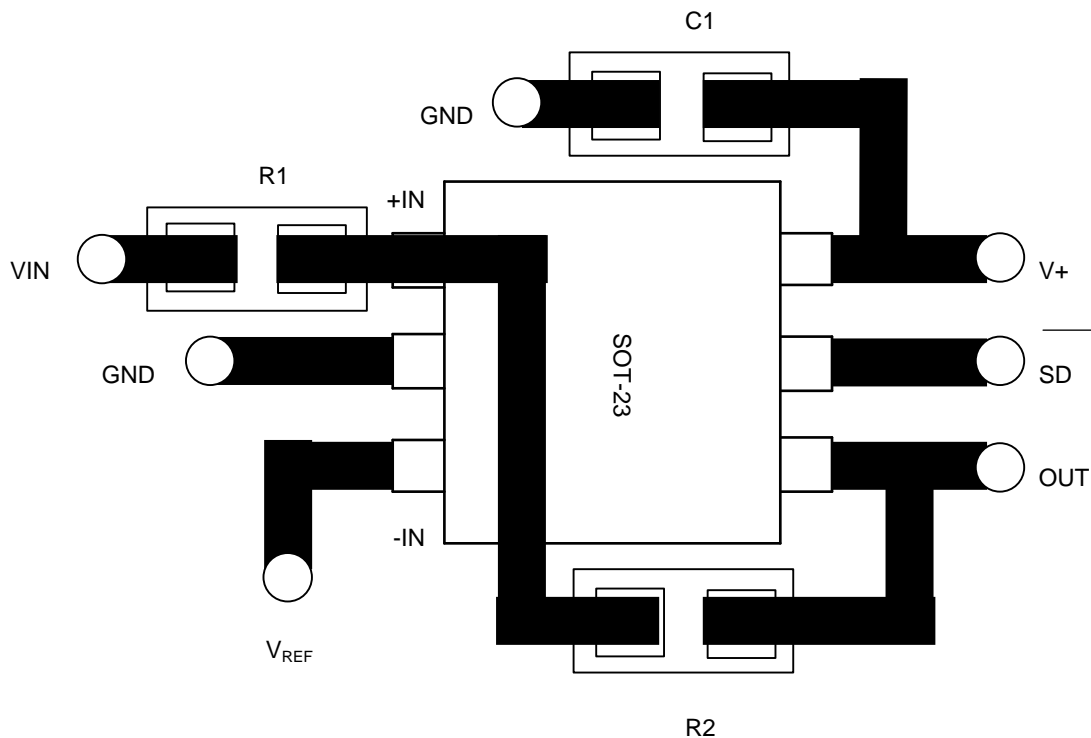


Figure 26. Comparator With Hysteresis

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# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV761	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LMV762	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LMV762Q-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMV761MA</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	LMV76 1MA
<a href="#">LMV761MA/NOPB</a>	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA
LMV761MA/NOPB.A	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA
<a href="#">LMV761MAX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA
LMV761MAX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA
<a href="#">LMV761MF</a>	Obsolete	Production	SOT-23 (DBV)   6	-	-	Call TI	Call TI	-40 to 125	C22A
<a href="#">LMV761MF/NOPB</a>	Active	Production	SOT-23 (DBV)   6	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C22A
LMV761MF/NOPB.A	Active	Production	SOT-23 (DBV)   6	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C22A
<a href="#">LMV761MFX</a>	Obsolete	Production	SOT-23 (DBV)   6	-	-	Call TI	Call TI	-40 to 125	C22A
<a href="#">LMV761MFX/NOPB</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C22A
LMV761MFX/NOPB.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C22A
<a href="#">LMV762MA</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	LMV7 62MA
<a href="#">LMV762MA/NOPB</a>	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA
LMV762MA/NOPB.A	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA
<a href="#">LMV762MAX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA
LMV762MAX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA
<a href="#">LMV762MM/NOPB</a>	Active	Production	VSSOP (DGK)   8	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C23A
LMV762MM/NOPB.A	Active	Production	VSSOP (DGK)   8	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C23A
<a href="#">LMV762MMX</a>	Obsolete	Production	VSSOP (DGK)   8	-	-	Call TI	Call TI	-40 to 125	C23A
<a href="#">LMV762MMX/NOPB</a>	Active	Production	VSSOP (DGK)   8	3500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C23A
LMV762MMX/NOPB.A	Active	Production	VSSOP (DGK)   8	3500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C23A

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMV762QMA/NOPB</a>	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA
LMV762QMA/NOPB.A	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA
<a href="#">LMV762QMAX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA
LMV762QMAX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA
<a href="#">LMV762QMM/NOPB</a>	Active	Production	VSSOP (DGK)   8	1000   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	C32A
LMV762QMM/NOPB.A	Active	Production	VSSOP (DGK)   8	1000   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C32A
<a href="#">LMV762QMMX/NOPB</a>	Active	Production	VSSOP (DGK)   8	3500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	C32A
LMV762QMMX/NOPB.A	Active	Production	VSSOP (DGK)   8	3500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C32A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

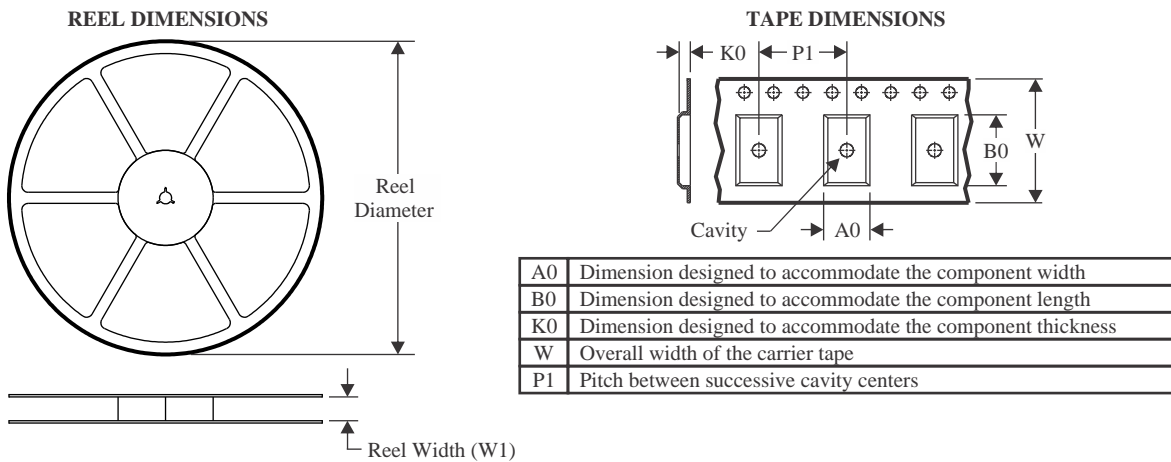
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

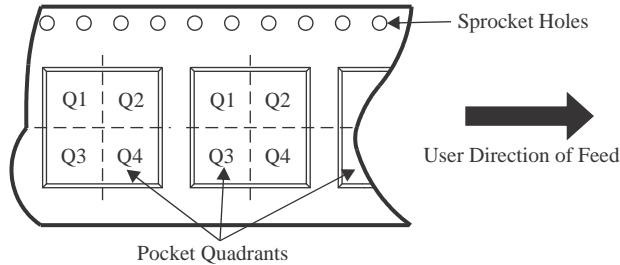
and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



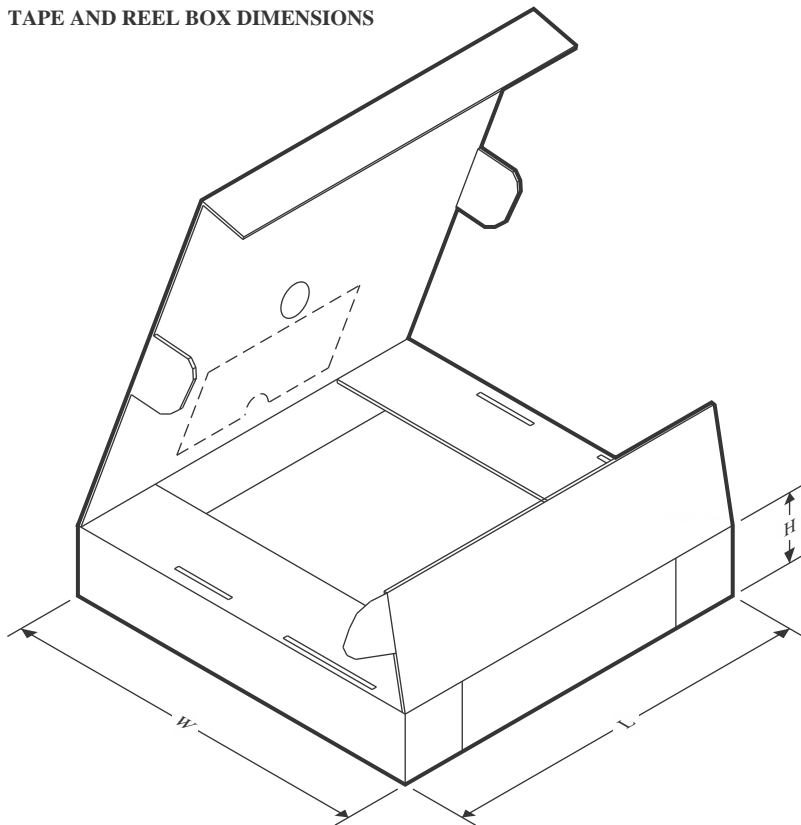
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV761MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV761MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV761MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV762MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762QMM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762QMM/NOPB	VSSOP	DGK	8	1000	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

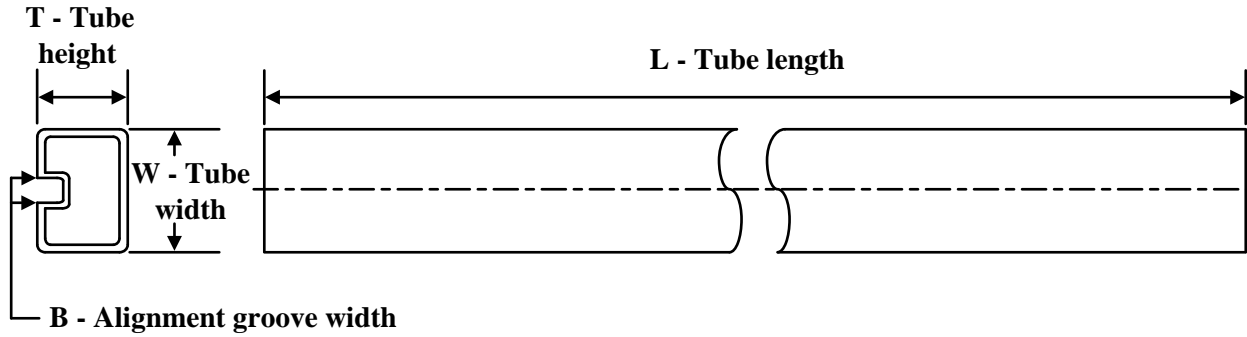
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV761MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV761MF/NOPB	SOT-23	DBV	6	1000	208.0	191.0	35.0
LMV761MFX/NOPB	SOT-23	DBV	6	3000	208.0	191.0	35.0
LMV762MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV762MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV762MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV762QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV762QMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV762QMM/NOPB	VSSOP	DGK	8	1000	213.0	191.0	35.0
LMV762QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMV761MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV761MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMV762MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV762MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMV762QMA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV762QMA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

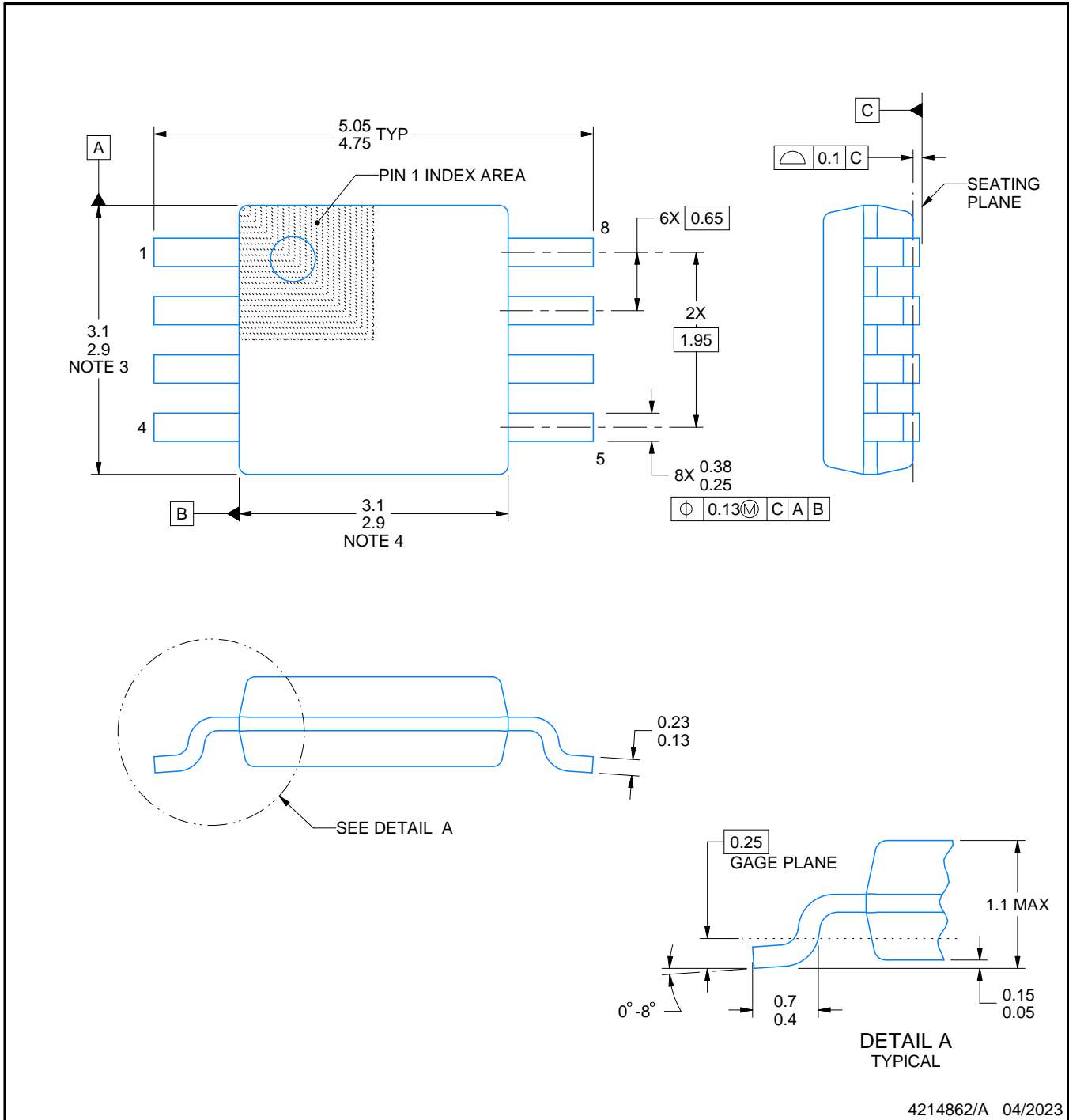


DGK0008A

PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

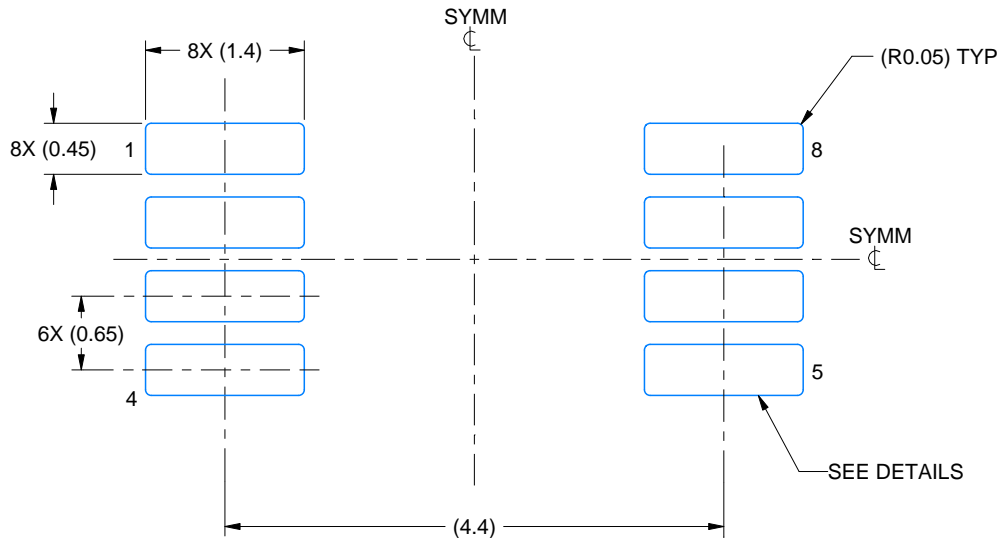
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

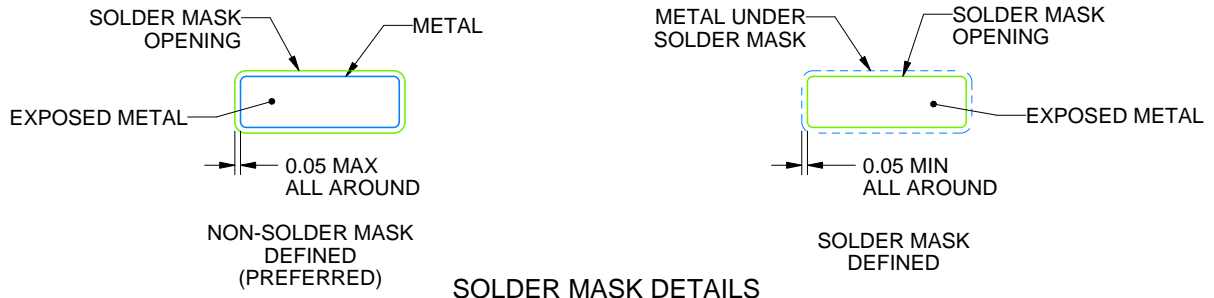
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

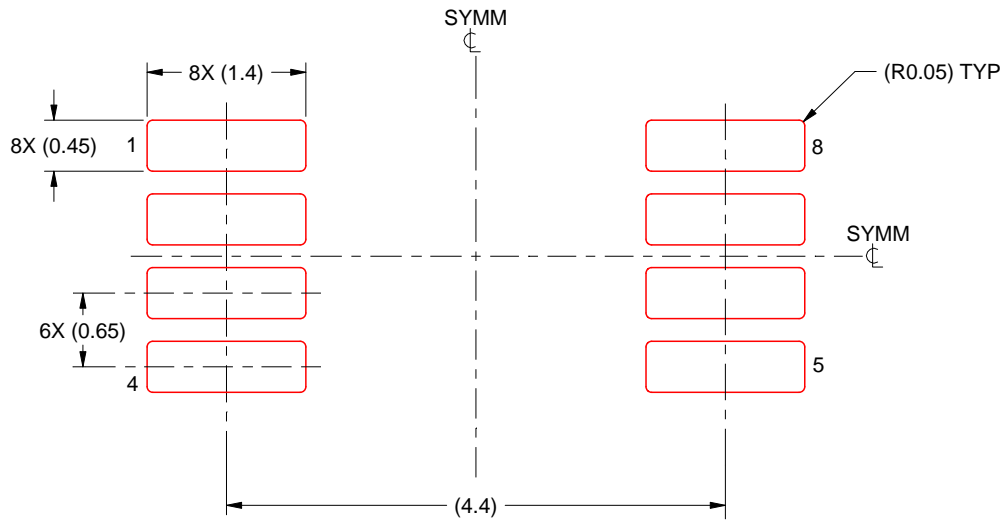
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

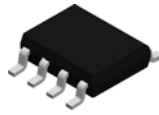


SOLDER PASTE EXAMPLE  
SCALE: 15X

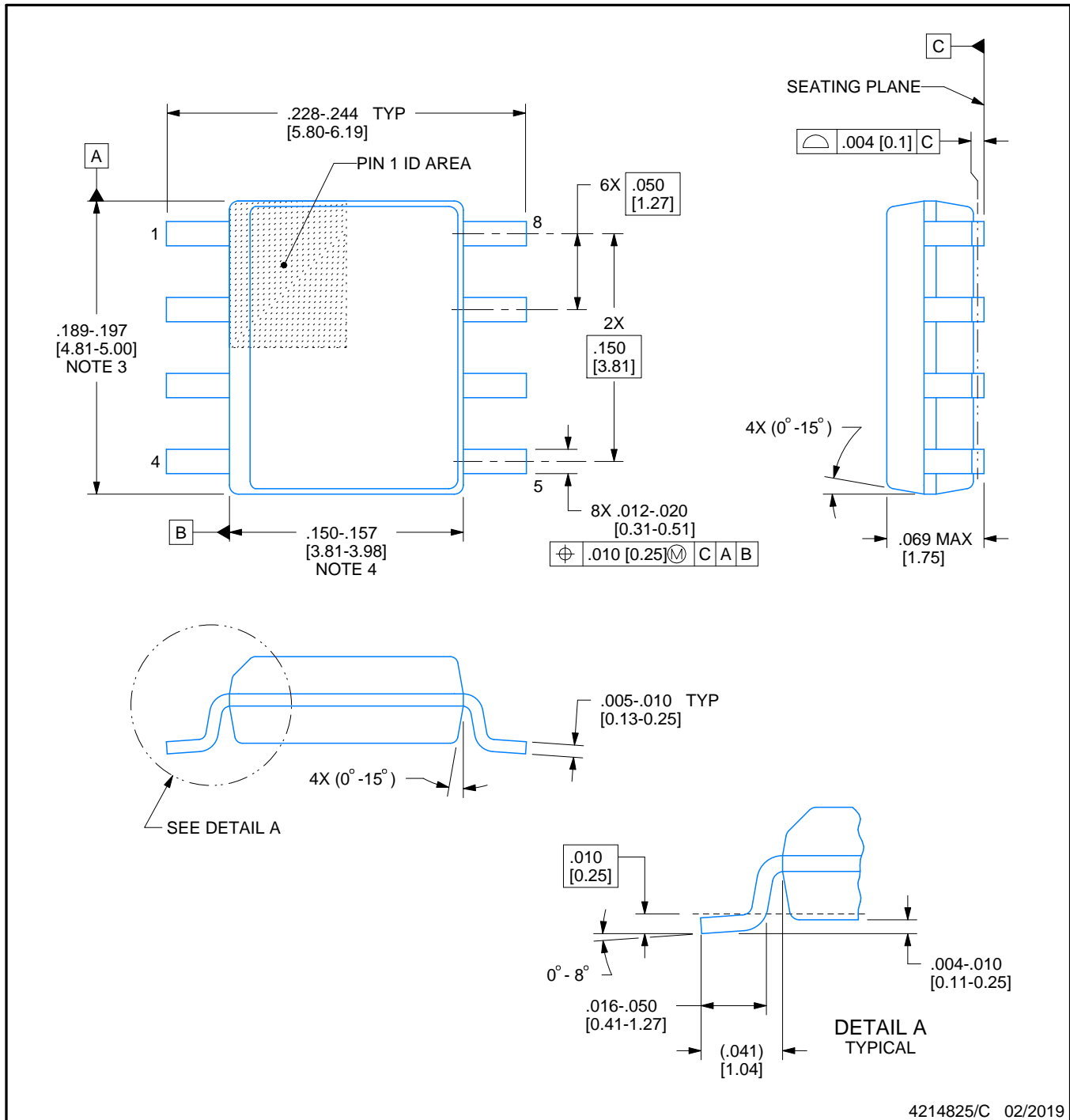
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

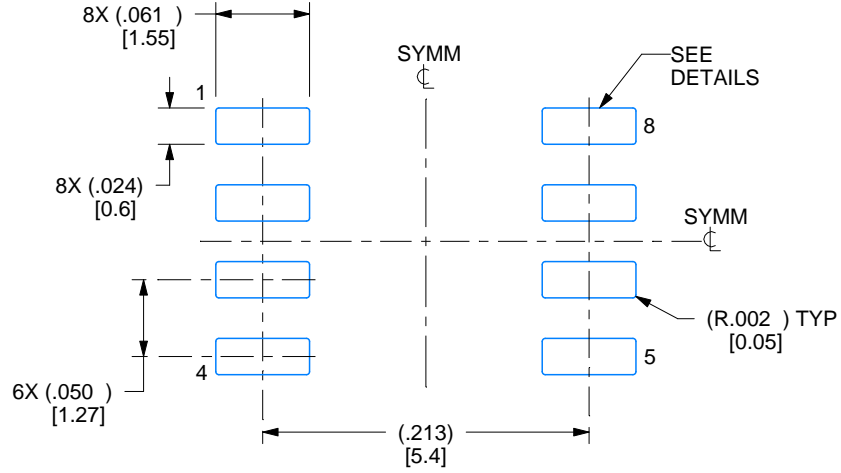
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

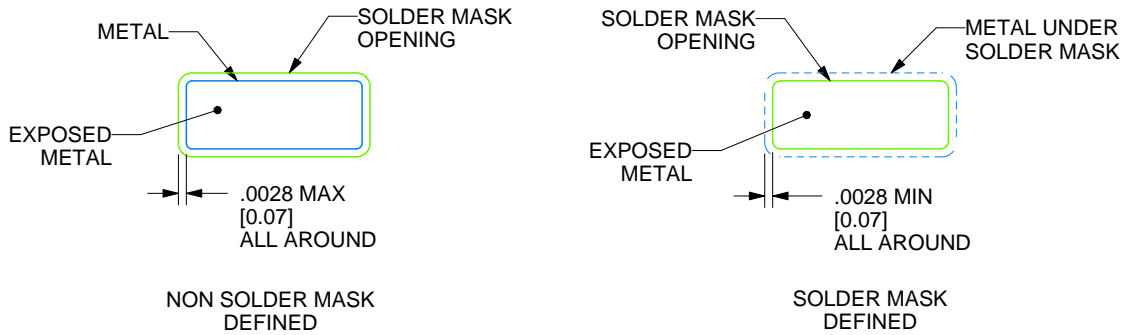
**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:8X



**SOLDER MASK DETAILS**

4214825/C 02/2019

NOTES: (continued)

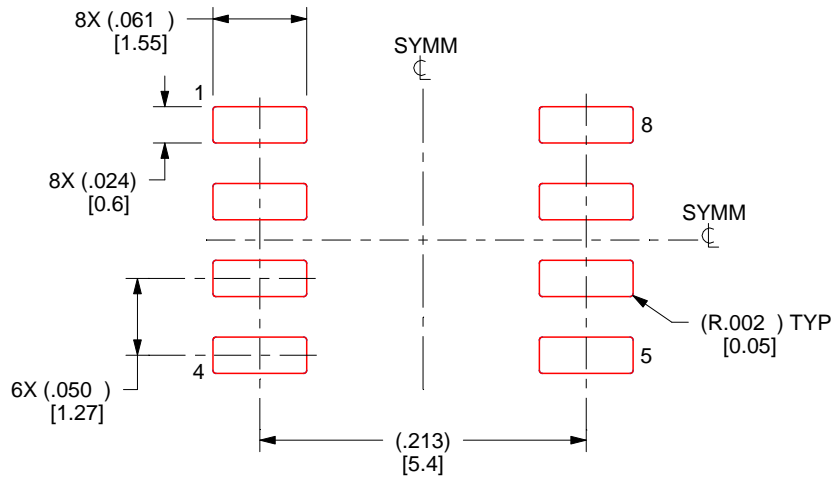
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
 BASED ON .005 INCH [0.125 MM] THICK STENCIL  
 SCALE:8X

4214825/C 02/2019

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

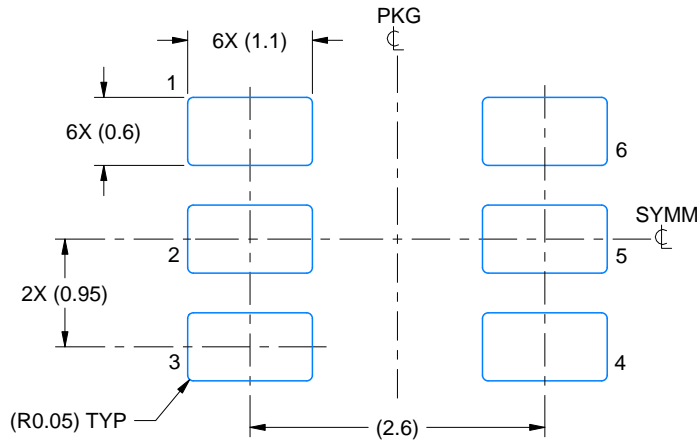


# EXAMPLE BOARD LAYOUT

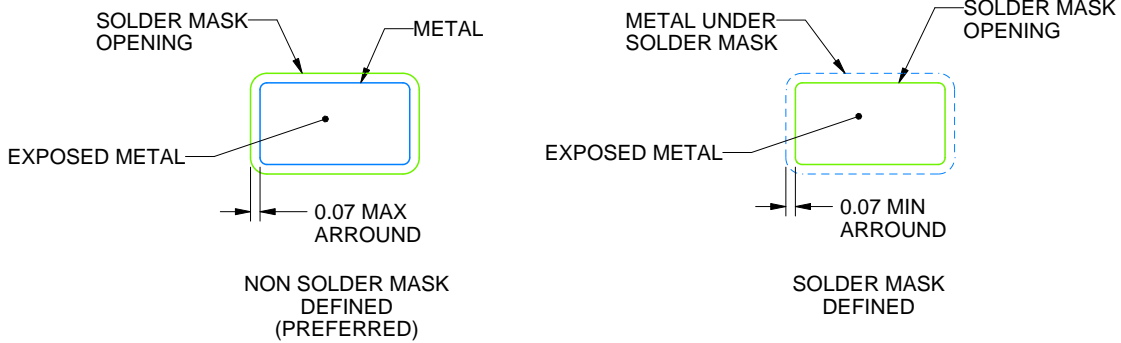
**DBV0006A**

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:15X



**SOLDER MASK DETAILS**

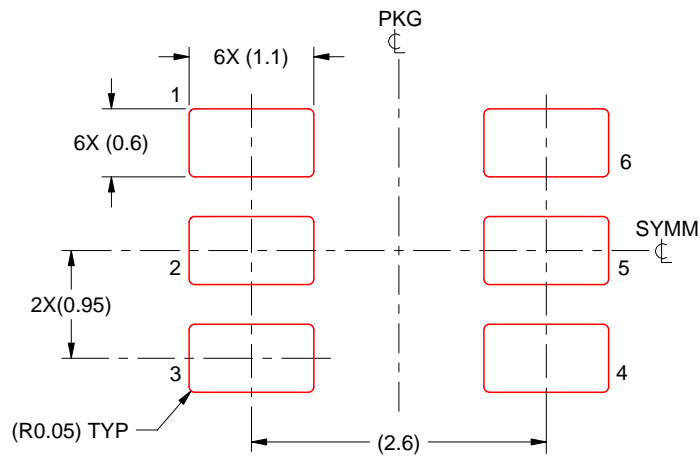
4214840/G 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****DBV0006A****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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