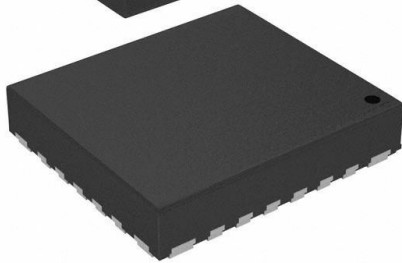
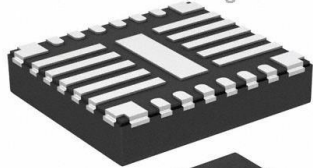


LP87524JRNFRQ1 Datasheet

www.digi-electronics.com



LP87524JRNFRQ1

<https://www.DiGi-Electronics.com>

| | |
|------------------------------|---|
| DiGi Electronics Part Number | LP87524JRNFRQ1-DG |
| Manufacturer | Texas Instruments |
| Manufacturer Product Number | LP87524JRNFRQ1 |
| Description | IC REG BUCK ADJ QUAD 26VQFN |
| Detailed Description | Buck Switching Regulator IC Positive Adjustable 0.6 V 4 Output 4A, 4A, 4A, 4A 26-PowerVFQFN |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

LP87524JRNFRQ1

Series:

-

Function:

Step-Down

Topology:

Buck

Number of Outputs:

4

Voltage - Input (Max):

5.5V

Voltage - Output (Max):

3.36V

Frequency - Switching:

4MHz

Operating Temperature:

-40°C ~ 125°C (TA)

Qualification:

AEC-Q100

Package / Case:

26-PowerVFQFN

Base Product Number:

LP87524

Manufacturer:

Texas Instruments

Product Status:

Active

Output Configuration:

Positive

Output Type:

Adjustable

Voltage - Input (Min):

2.8V

Voltage - Output (Min/Fixed):

0.6V

Current - Output:

4A, 4A, 4A, 4A

Synchronous Rectifier:

Yes

Grade:

Automotive

Mounting Type:

Surface Mount, Wettable Flank

Supplier Device Package:

26-VQFN-HR (4.5x4)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

LP87524B/J/P-Q1 Four 4-MHz Buck Converters for AWR and IWR MMICs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
- Input Voltage: 2.8 V to 5.5 V
- Output Voltage: 0.6 V to 3.36 V
- Four High-Efficiency Step-Down DC-DC Converter Cores:
 - Total Output Current Up To 10 A
 - Output Voltage Slew-Rate 3.8 mV/μs
- 4-MHz Switching Frequency
- Spread-Spectrum Mode and Phase Interleaving
- Configurable General Purpose I/O (GPIOs)
- I²C-Compatible Interface which Supports Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes
- Interrupt Function with Programmable Masking
- Programmable Power Good Signal (PGOOD)
- Output Short-Circuit and Overload Protection
- Overtemperature Warning and Protection
- Overvoltage Protection (OVP) and Undervoltage Lockout (UVLO)

2 Applications

- Automotive Infotainment
- Cluster
- Radar
- Camera Power

3 Description

The LP87524B/J/P-Q1 is designed to meet the power management requirements of the latest processors and platforms in various automotive power applications. The device contains four step-down DC-DC converter cores, which are configured as 4 single phase outputs. The device is controlled by an I²C-compatible serial interface and by enable signals.

The automatic PFM/PWM (AUTO mode) operation maximizes efficiency over a wide output-current range. The LP87524B/J/P-Q1 supports remote voltage sensing to compensate IR drop between the regulator output and the point-of-load (POL) thus improving the accuracy of the output voltage. In addition the switching clock can be forced to PWM mode and also synchronized to an external clock to minimize the disturbances.

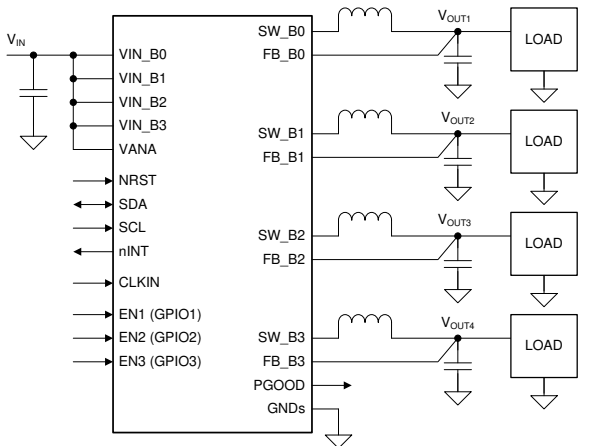
The LP87524B/J/P-Q1 device supports load-current measurement without the addition of external current-sense resistors. In addition, the LP87524B/J/P-Q1 supports programmable start-up and shutdown delays and sequences synchronized to enable signals. The sequences can also include GPIO signals to control external regulators, load switches and processor reset. During start-up and voltage change, the device controls the output slew rate to minimize output voltage overshoot and the in-rush current.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|--------------|-------------------|
| LP87524B-Q1 | VQFN-HR (26) | 4.50 mm × 4.00 mm |
| LP87524J-Q1 | | |
| LP87524P-Q1 | | |

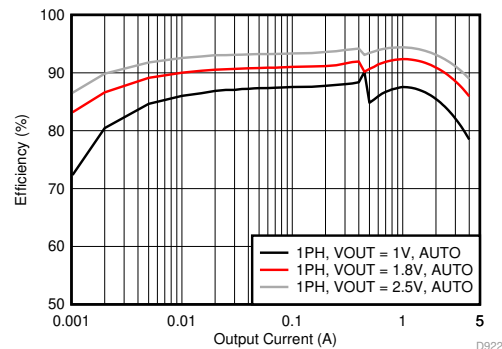
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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Efficiency vs Output Current



D922



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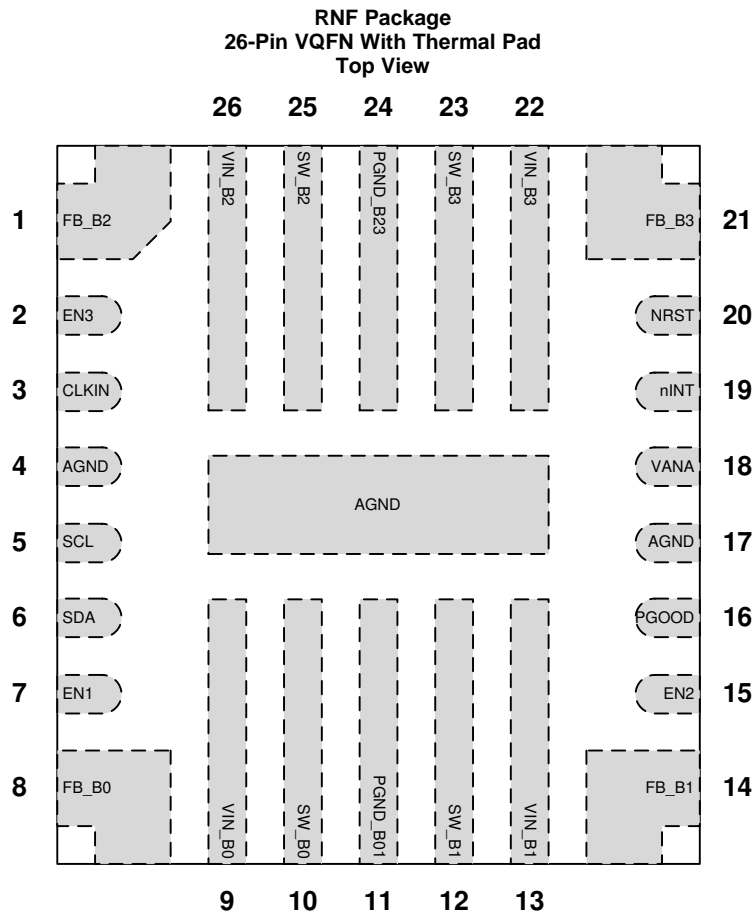
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (December 2017) to Revision B | Page |
|---|------|
| • Added LP87524P-Q1 GPN to SNVSAW2 data sheet | 1 |

| Changes from Original (April 2017) to Revision A | Page |
|---|------|
| • Added LP87524J-Q1 GPN to SNVSAW2 data sheet | 1 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----------------------|----------|-------|--|
| NUMBER | NAME | | |
| 1 | FB_B2 | A | Output voltage feedback (positive) for Buck2. |
| 2 | EN3 | D/I/O | Programmable enable signal for buck regulators (can be also configured to select between two buck output voltage levels). Alternative function is GPIO3. |
| 3 | CLKIN | D/I | External clock input. Connect to ground if external clock is not used. |
| 4, 17, Thermal Pad | AGND | G | Ground |
| 5 | SCL | D/I | Serial interface clock input for I2C access. Connect a pullup resistor. |
| 6 | SDA | D/I/O | Serial interface data input and output for I2C access. Connect a pullup resistor. |
| 7 | EN1 | D/I/O | Programmable Enable signal for buck regulators (can be also configured to select between two buck output voltage levels). Alternative function is GPIO1. |
| 8 | FB_B0 | A | Output voltage feedback (positive) for Buck0 |
| 9 | VIN_B0 | P | Input for Buck0. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed. |
| 10 | SW_B0 | A | Buck0 switch node |
| 11 | PGND_B01 | G | Power ground for Buck0 and Buck1 |
| 12 | SW_B1 | A | Buck1 switch node |
| 13 | VIN_B1 | P | Input for Buck1. The separate power pins VIN_Bx are not connected together internally – VIN_Bx pins must be connected together in the application and be locally bypassed. |
| 14 | FB_B1 | A | Output voltage feedback (positive) for Buck1. |
| 15 | EN2 | D/I/O | Programmable enable signal for Buck regulators (can be also configured to select between two buck output voltage levels). Alternative function is GPIO2. |
| 16 | PGOOD | D/O | Power Good indication signal |
| 18 | VANA | P | Supply voltage for analog and digital blocks. Must be connected to same node as with VIN_Bx. |
| 19 | nINT | D/O | Open-drain interrupt output, active LOW |
| 20 | NRST | D/I | Reset signal for the device. |
| 21 | FB_B3 | A | Output voltage feedback (positive) for Buck3. |
| 22 | VIN_B3 | P | Input for Buck3. The separate power pins VIN_Bx are not connected together internally – VIN_Bx pins must be connected together in the application and be locally bypassed. |
| 23 | SW_B3 | A | Buck3 switch node |
| 24 | PGND_B23 | G | Power Ground for Buck2 and Buck3 |
| 25 | SW_B2 | A | Buck2 switch node |
| 26 | VIN_B2 | P | Input for Buck2. The separate power pins VIN_Bx are not connected together internally – VIN_Bx pins must be connected together in the application and be locally bypassed. |

A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

| | | MIN | MAX | UNIT |
|---|--|------|-----------------------------------|------|
| Voltage on power connections | VIN_Bx, VANA | -0.3 | 6 | V |
| Voltage on buck switch nodes | SW_Bx | -0.3 | (VIN_Bx + 0.3 V) with 6 V maximum | V |
| Voltage on buck voltage sense nodes | FB_Bx | -0.3 | (VANA + 0.3 V) with 6 V maximum | V |
| Voltage on NRST input | NRST | -0.3 | 6 | V |
| Voltage on logic pins (input or output pins) | SDA, SCL, nINT, CLKIN | -0.3 | 6 | V |
| Voltage on logic pins (input or output pins) | EN1 (GPIO1), EN2 (GPIO2), EN3 (GPIO3), PGOOD | -0.3 | (VANA + 0.3 V) with 6 V maximum | V |
| Junction temperature, T _{J-MAX} | | -40 | 150 | °C |
| Storage temperature, T _{stg} | | -65 | 150 | °C |
| Maximum lead temperature (soldering, 10 sec.) | | | 260 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground.

6.2 ESD Ratings

| | | VALUE | UNIT | |
|--|---|-------------------------------|------|------|
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V | |
| | Charged-device model (CDM), per AEC Q100-011 | All pins | | ±500 |
| | | Corner pins (1, 8, 14 and 21) | | ±750 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|--------------|------|-------------------------|------|
| INPUT VOLTAGE | | | | |
| Voltage on power connections | VIN_Bx, VANA | 2.8 | 5.5 | V |
| Voltage on NRST | NRST | 1.65 | VANA with 5.5 V maximum | V |
| Voltage on logic pins | nINT, CLKIN | 1.65 | 5.5 | V |
| Voltage on logic pins (input or output pins) | ENx, PGOOD | 0 | VANA with 5.5 V maximum | V |
| Voltage on I2C interface, standard (100 kHz), fast (400 kHz), fast+ (1 MHz), and high-speed (3.4 MHz) modes | SCL, SDA | 1.65 | 1.95 | V |
| Voltage on I2C interface, standard (100 kHz), fast (400 kHz), and fast+ (1 MHz) modes | | 3.1 | VANA with 3.6 V maximum | V |
| TEMPERATURE | | | | |
| Junction temperature, T _J | | -40 | 140 | °C |
| Ambient temperature, T _A | | -40 | 125 | °C |

LP87524B-Q1
LP87524J-Q1, LP87524P-Q1

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6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LP875xx-Q1 | UNIT |
|-------------------------------|--|------------|------|
| | | RNF (VQFN) | |
| | | 26 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 34.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 16.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 4.7 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.6 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 4.7 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 1.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$, $C_{POL} = 22 \mu\text{F}$ / phase, specified V_{VANA} , V_{VIN_Bx} , V_{NRST} , V_{VOUT_Bx} and I_{OUT} range, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.7 \text{ V}$, and $V_{OUT} = 1 \text{ V}$, unless otherwise noted.^{(1) (2)}

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | | |
|----------------------------|---|---|-----|------|------|--------------------|----|----|
| EXTERNAL COMPONENTS | | | | | | | | |
| C _{IN} | Input filtering capacitance | Connected from VIN_Bx to PGND_Bx | | 1.9 | 10 | μF | | |
| C _{OUT} | Output filtering Capacitance, local | Capacitance per phase | | 10 | 22 | μF | | |
| C _{POL} | Point-of-Load (POL) capacitance | Optional POL capacitance per phase | | | 22 | μF | | |
| C _{OUT-TOTAL} | Output capacitance, total (local and POL) | Total output capacitance, 1-phase output | | | | 100 | μF | |
| ESR _C | Input and output capacitor ESR | [1-10] MHz | | | 2 | 10 | mΩ | |
| L | Inductor | Inductance of the inductor | | | 0.47 | | μH | |
| | | | | -30% | | 30% | | |
| DCR _L | Inductor DCR | | | | 25 | | mΩ | |
| BUCK REGULATOR | | | | | | | | |
| V _{VIN_Bx} | Input voltage range | | | 2.8 | 3.7 | 5.5 | V | |
| V _{VOUT_Bx} | Output voltage | Programmable voltage range, $2.8 \text{ V} \leq V_{VIN_Bx} \leq 4 \text{ V}$ | | 0.6 | | 3.36 | V | |
| | | Programmable voltage range, $2.8 \text{ V} \leq V_{VIN_Bx} \leq 5.5 \text{ V}$ | | 1.0 | | 3.36 | V | |
| | | Step size, $0.6 \text{ V} \leq V_{OUT} < 0.73 \text{ V}$ | | | 10 | | | mV |
| | | Step size, $0.73 \text{ V} \leq V_{OUT} < 1.4 \text{ V}$ | | | 5 | | | mV |
| | | Step size, $1.4 \text{ V} \leq V_{OUT} \leq 3.36 \text{ V}$ | | | 20 | | | mV |
| I _{OUT} | Output current, LP87524B/J | Buck0, Buck1 | | | | 1.5 ⁽³⁾ | A | |
| | | Buck2: $V_{IN} \geq 3 \text{ V}$ | | | | 4 ⁽³⁾ | | |
| | | Buck2: $2.8 \text{ V} \leq V_{IN} < 3 \text{ V}$ | | | | 3 ⁽³⁾ | | |
| | | Buck3 | | | | 2.5 ⁽³⁾ | | |
| I _{OUT} | Output current, LP87524P | Buck0, Buck2 | | | | 3 ⁽³⁾ | A | |
| | | Buck1 | | | | 1.5 ⁽³⁾ | | |
| | | Buck3 | | | | 2.5 ⁽³⁾ | | |

(1) All voltage values are with respect to network ground.

(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm.

(3) The maximum output current can be limited by the forward current limit I_{LIM_FWD} and by the junction temperature. The power dissipation inside the die depends on the length of the current pulse and efficiency and the junction temperature may increase to thermal shutdown level if the board and ambient temperatures are high.

Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$, $C_{POL} = 22 \mu\text{F}$ / phase, specified V_{VANA} , V_{VIN_Bx} , V_{NRST} , V_{VOUT_Bx} and I_{OUT} range, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.7 \text{ V}$, and $V_{OUT} = 1 \text{ V}$, unless otherwise noted.^{(1) (2)}

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|--|---|------|------------|-------------------|------------|
| Input and output voltage difference | Minimum voltage between V_{IN_x} and V_{OUT} to fulfill the electrical characteristics | 0.5 | | | V | |
| V_{VOUT_DC} | DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature | $V_{OUT} < 1 \text{ V}$, PWM mode | | 20 | mV | |
| | | $V_{OUT} \geq 1 \text{ V}$, PWM mode | -2% | 2% | | |
| | | $V_{OUT} < 1 \text{ V}$, PFM mode | -20 | | 40 | mV |
| | | $V_{OUT} \geq 1 \text{ V}$, PFM mode | -2% | 2% + 20 mV | | |
| Ripple voltage | PWM mode, $ESR_C < 2 \text{ m}\Omega$, $L = 0.47 \mu\text{H}$ | | 4 | | mV _{p-p} | |
| | PFM mode, $L = 0.47 \mu\text{H}$ | | 14 | | | |
| DC_{LNR} | DC line regulation | $I_{OUT} = I_{OUT(max)}$ | 0.1 | | %/V | |
| DC_{LDR} | DC load regulation in PWM mode | $V_{OUT} = 1 \text{ V}$, I_{OUT} from 0 to $I_{OUT(max)}$ | 0.8% | | | |
| T_{LDSR} | Transient load step response | $I_{OUT} = 0 \text{ A}$ to 2 A , $T_R = T_F = 10 \mu\text{s}$, PWM mode, $C_{OUT} = 22 \mu\text{F}$, $L = 0.47 \mu\text{H}$, $C_{POL} = 22 \mu\text{F}$ | -3% | | 3% | mV |
| | | $I_{OUT} = 0.1 \text{ A}$ to 2 A , $T_R = T_F = 1 \mu\text{s}$, PWM mode, $C_{OUT} = 22 \mu\text{F}$, $L = 0.47 \mu\text{H}$, $C_{POL} = 22 \mu\text{F}$ | | ± 40 | | |
| T_{LNSR} | Transient line response | V_{VIN_Bx} stepping $3 \text{ V} \leftrightarrow 3.5 \text{ V}$, $T_R = T_F = 10 \mu\text{s}$, $I_{OUT} = I_{OUT(max)}$ | | ± 5 | mV | |
| $I_{LIM FWD}$ | Forward current limit (peak for every switching cycle), LP87524B/J | Buck0, Buck1: $V_{VIN_Bx} \geq 3 \text{ V}$ | 2.3 | 2.7 | 3.0 | A |
| | | Buck0, Buck1: $2.8 \text{ V} \leq V_{VIN_Bx} < 3 \text{ V}$ | 2.0 | 2.7 | 3.0 | |
| | | Buck2: $V_{VIN_Bx} \geq 3 \text{ V}$ | 4.7 | 5.4 | 6.0 | |
| | | Buck2: $2.8 \text{ V} \leq V_{VIN_Bx} < 3 \text{ V}$ | 4.0 | 5.4 | 6.0 | |
| | | Buck3: $V_{VIN_Bx} \geq 3 \text{ V}$ | 4.2 | 4.8 | 5.4 | |
| | | Buck3: $2.8 \text{ V} \leq V_{VIN_Bx} < 3 \text{ V}$ | 3.6 | 4.8 | 5.4 | |
| $I_{LIM FWD}$ | Forward current limit (peak for every switching cycle), LP87524P | Buck0, Buck2: $V_{VIN_Bx} \geq 3 \text{ V}$ | 3.8 | 4.3 | 4.8 | A |
| | | Buck0, Buck2: $2.8 \text{ V} \leq V_{VIN_Bx} < 3 \text{ V}$ | 3.2 | 4.3 | 4.8 | |
| | | Buck1: $V_{VIN_Bx} \geq 3 \text{ V}$ | 2.3 | 2.7 | 3.0 | |
| | | Buck1: $2.8 \text{ V} \leq V_{VIN_Bx} < 3 \text{ V}$ | 2.0 | 2.7 | 3.0 | |
| | | Buck3: $V_{VIN_Bx} \geq 3 \text{ V}$ | 4.2 | 4.8 | 5.4 | |
| | | Buck3: $2.8 \text{ V} \leq V_{VIN_Bx} < 3 \text{ V}$ | 3.6 | 4.8 | 5.4 | |
| $I_{LIM NEG}$ | Negative current limit / phase (peak for every switching cycle) | | 1.6 | 2 | 2.4 | A |
| $R_{DS(ON) HS FET}$ | On-resistance, high-side FET | Each phase, between V_{IN_Bx} and SW_Bx pins ($I = 1 \text{ A}$) | | 29 | 65 | m Ω |
| $R_{DS(ON) LS FET}$ | On-resistance, low-side FET | Each phase, between SW_Bx and $PGND_Bx$ pins ($I = 1 \text{ A}$) | | 17 | 35 | m Ω |
| f_{SW} | Switching frequency, PWM mode | $V_{OUT} > 0.8$ | 3.6 | 4 | 4.4 | MHz |
| | | $0.6 < V_{OUT} \leq 0.8$ | 2.7 | 3 | 3.3 | |
| | | $V_{OUT} = 0.6$ | 1.8 | 2 | 2.2 | |
| Start-up time (soft start) | From ENx to $V_{OUT} = 0.35 \text{ V}$ (slew-rate control begins), $C_{OUT_TOTAL} = 44 \mu\text{F}$ / phase | | 200 | | μs | |
| Output voltage slew-rate ⁽⁴⁾ | | 3.23 | 3.8 | 4.4 | mV/ μs | |

(4) Output capacitance, forward and negative current limits and load current may limit the maximum and minimum slew rates.

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LP87524J-Q1, LP87524P-Q1**

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Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$, $C_{POL} = 22 \mu\text{F}$ / phase, specified V_{VANA} , V_{VIN_Bx} , V_{NRST} , V_{VOUT_Bx} and I_{OUT} range, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.7 \text{ V}$, and $V_{OUT} = 1 \text{ V}$, unless otherwise noted.^{(1) (2)}

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|------|------|------|--------------------|
| $I_{PFM-PWM}$ | PFM-to-PWM - current threshold ⁽⁵⁾ | | | 600 | | mA |
| $I_{PWM-PFM}$ | PWM-to-PFM - current threshold ⁽⁵⁾ | | | 200 | | mA |
| | Output pulldown resistance | Regulator disabled | 160 | 230 | 300 | Ω |
| | Output voltage monitoring for PGOOD pin | Overvoltage monitoring (compared to DC output voltage level, V_{VOUT_DC}) | 39 | 50 | 64 | mV |
| | | Undervoltage monitoring (compared to DC output voltage level, V_{VOUT_DC}) | -53 | -40 | -29 | |
| | | Debounce time during regulator enable PGOOD_SET_DELAY = 0 | 4 | | 10 | μs |
| | | Debounce time during regulator enable PGOOD_SET_DELAY = 1 | 10 | 11 | 13 | ms |
| | | Deglitch time during operation and after voltage change | 4 | | 10 | μs |
| Powergood threshold for interrupt BUCKx_PG_INT, difference from final voltage | | Rising ramp voltage, enable or voltage change | -20 | -14 | -8 | mV |
| | | Falling ramp voltage, voltage change | 8 | 14 | 20 | |
| Powergood threshold for status bit BUCKx_PG_STAT | | During operation, status signal is forced to '0' during voltage change | -20 | -14 | -8 | mV |
| EXTERNAL CLOCK AND PLL | | | | | | |
| External input clock | | Nominal frequency | 1 | | 24 | MHz |
| | | Nominal frequency step size | | 1 | | |
| | | Required accuracy from nominal frequency | -30% | | 10% | |
| External clock detection | | Delay for missing clock detection | | | 1.8 | μs |
| | | Delay and debounce for clock detection | | | 20 | |
| Clock change delay (internal to external) | | Delay from valid clock detection to use of external clock | | 600 | | μs |
| PLL output clock jitter | | Cycle to cycle | | 300 | | ps, p-p |
| PROTECTION FUNCTIONS | | | | | | |
| Thermal warning | | Temperature rising, TDIE_WARN_LEVEL = 0 | 115 | 125 | 135 | $^{\circ}\text{C}$ |
| | | Temperature rising, TDIE_WARN_LEVEL = 1 | 127 | 137 | 147 | |
| | | Hysteresis | | 20 | | |
| Thermal shutdown | | Temperature rising | 140 | 150 | 160 | $^{\circ}\text{C}$ |
| | | Hysteresis | | 20 | | |
| V_{ANA_OVP} VANA overvoltage | | Voltage rising | 5.6 | 5.8 | 6.1 | V |
| | | Voltage falling | 5.45 | 5.73 | 5.96 | |
| | | Hysteresis | 40 | | | mV |
| V_{ANA_UVLO} VANA undervoltage lockout | | Voltage rising | 2.51 | 2.63 | 2.75 | V |
| | | Voltage falling | 2.5 | 2.6 | 2.7 | |
| LOAD CURRENT MEASUREMENT | | | | | | |

(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependent on the output voltage, input voltage, and the inductor current level.

Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$, $C_{POL} = 22 \mu\text{F}$ / phase, specified V_{VANA} , V_{VIN_Bx} , V_{NRST} , V_{VOUT_Bx} and I_{OUT} range, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.7 \text{ V}$, and $V_{OUT} = 1 \text{ V}$, unless otherwise noted.^{(1) (2)}

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------------------------------|------------------|------------|---------------|
| Current measurement range | Output current for maximum code | | | 20.47 | A |
| Resolution | LSB | | 20 | | mA |
| Measurement accuracy | $I_{OUT} > 1 \text{ A}$ | | <10% | | |
| Measurement time | PFM mode (automatically changing to PWM mode for the measurement) | | 45 | | μs |
| | PWM mode | | 4 | | |
| CURRENT CONSUMPTION | | | | | |
| Shutdown current consumption | From VANA and VIN_Bx pins: NRST = 0 V, VANA = VIN_Bx = 3.7 V | | 1.4 | | μA |
| Standby current consumption, regulators disabled | From VANA and VIN_Bx pins: NRST = 1.8 V, VANA = VIN_Bx = 3.7 V | | 6.7 | | |
| Active current consumption in PFM mode, one regulator enabled, internal RC oscillator, PGOOD monitoring enabled | From VANA and VIN_Bx pins: NRST = 1.8 V, VANA = VIN_Bx = 3.7 V, $I_{OUT} = 0 \text{ mA}$, not switching | | 57 | | μA |
| Active current consumption during PWM operation, per phase | | | 19 | | mA |
| PLL and clock detector current consumption | Additional current consumption when internal RC oscillator, clock detector and PLL are enabled | | 2 | | mA |
| DIGITAL INPUT SIGNALS NRST, EN1, EN2, EN3, EN4, SCL, SDA, GPIO1, GPIO2, GPIO3, CLKIN | | | | | |
| V_{IL} | Input low level | | | 0.4 | V |
| V_{IH} | Input high level | 1.2 | | | |
| V_{HYS} | Hysteresis of Schmitt Trigger inputs | 10 | 77 | 200 | mV |
| | ENx pulldown resistance | ENx_PD = 1 | 500 | | k Ω |
| | NRST pulldown resistance | Always present | 650 | 1700 | |
| DIGITAL OUTPUT SIGNALS nINT | | | | | |
| V_{OL} | Output low level | $I_{SOURCE} = 2 \text{ mA}$ | | 0.4 | V |
| R_P | External pullup resistor | To VIO supply | 10 | | k Ω |
| DIGITAL OUTPUT SIGNALS SDA | | | | | |
| V_{OL} | Output low level | $I_{SOURCE} = 10 \text{ mA}$ | | 0.4 | V |
| DIGITAL OUTPUT SIGNALS PGOOD, GPIO1, GPIO2, GPIO3 | | | | | |
| V_{OL} | Output low level | $I_{SOURCE} = 2 \text{ mA}$ | | 0.4 | V |
| V_{OH} | Output high level, configured to push-pull | $I_{SINK} = 2 \text{ mA}$ | $V_{VANA} - 0.4$ | V_{VANA} | V |
| V_{PU} | Supply voltage for external pull-up resistor, configured to open-drain | | | V_{VANA} | V |
| R_{PU} | External pullup resistor, configured to open-drain | | 10 | | k Ω |
| ALL DIGITAL INPUTS | | | | | |

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LP87524J-Q1, LP87524P-Q1

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Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$, $C_{POL} = 22 \mu\text{F}$ / phase, specified V_{VANA} , V_{VIN_Bx} , V_{NRST} , V_{VOUT_Bx} and I_{OUT} range, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.7 \text{ V}$, and $V_{OUT} = 1 \text{ V}$, unless otherwise noted.^{(1) (2)}

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|---------------|---|-----|-----|-----|---------------|
| I_{LEAK} | Input current | All logic inputs over pin voltage range (except NRST) | -1 | | 1 | μA |

6.6 I2C Serial Bus Timing Requirements

These specifications are ensured by design. Unless otherwise noted, $V_{IN_Bx} = 3.7\text{ V}$.

| | | MIN | MAX | UNIT | |
|--------------|--|--|------|---------------|----|
| f_{SCL} | Serial clock frequency | Standard mode | 100 | kHz | |
| | | Fast mode | 400 | | |
| | | Fast mode+ | 1 | MHz | |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 3.4 | | |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 1.7 | | |
| t_{LOW} | SCL low time | Standard mode | 4.7 | μs | |
| | | Fast mode | 1.3 | | |
| | | Fast mode+ | 0.5 | ns | |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 160 | | |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 320 | | |
| t_{HIGH} | SCL high time | Standard mode | 4 | μs | |
| | | Fast mode | 0.6 | | |
| | | Fast mode+ | 0.26 | ns | |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 60 | | |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 120 | | |
| $t_{SU;DAT}$ | Data setup time | Standard mode | 250 | ns | |
| | | Fast mode | 100 | | |
| | | Fast mode+ | 50 | | |
| | | High-speed mode | 10 | | |
| $t_{HD;DAT}$ | Data hold time | Standard mode | 10 | 3450 | ns |
| | | Fast mode | 10 | 900 | |
| | | Fast mode+ | 10 | | ns |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 10 | 70 | |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 10 | 150 | |
| $t_{SU;STA}$ | Setup time for a start or a repeated start condition | Standard mode | 4.7 | μs | |
| | | Fast mode | 0.6 | | |
| | | Fast mode+ | 0.26 | ns | |
| | | High-speed mode | 160 | | |
| $t_{HD;STA}$ | Hold time for a start or a repeated start condition | Standard mode | 4.0 | μs | |
| | | Fast mode | 0.6 | | |
| | | Fast mode+ | 0.26 | ns | |
| | | High-speed mode | 160 | | |
| t_{BUF} | Bus free time between a stop and start condition | Standard mode | 4.7 | μs | |
| | | Fast mode | 1.3 | | |
| | | Fast mode+ | 0.5 | | |
| $t_{SU;STO}$ | Setup time for a stop condition | Standard mode | 4 | μs | |
| | | Fast mode | 0.6 | | |
| | | Fast mode+ | 0.26 | ns | |
| | | High-speed mode | 160 | | |
| t_{rDA} | Rise time of SDA signal | Standard mode | | 1000 | ns |
| | | Fast mode | 20 | 300 | |
| | | Fast mode+ | | 120 | |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 10 | 80 | |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 20 | 160 | |

I²C Serial Bus Timing Requirements (continued)

These specifications are ensured by design. Unless otherwise noted, $V_{IN_BX} = 3.7\text{ V}$.

| | | MIN | MAX | UNIT | |
|------------|--|---|-------------------------------------|------|-----|
| t_{fDA} | Fall time of SDA signal | Standard mode | 300 | ns | |
| | | Fast mode | $20 \times (V_{DD} / 5.5\text{ V})$ | | 300 |
| | | Fast mode+ | $20 \times (V_{DD} / 5.5\text{ V})$ | | 120 |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 10 | | 80 |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 30 | | 160 |
| t_{rCL} | Rise time of SCL signal | Standard mode | 1000 | ns | |
| | | Fast mode | 20 | | 300 |
| | | Fast mode+ | | | 120 |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 10 | | 40 |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 20 | | 80 |
| t_{rCL1} | Rise time of SCL signal after a repeated start condition and after an acknowledge bit | High-speed mode, $C_b = 100\text{ pF}$ | 10 | ns | |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 20 | | 160 |
| t_{fCL} | Fall time of a SCL signal | Standard mode | 300 | ns | |
| | | Fast mode | $20 \times (V_{DD} / 5.5\text{ V})$ | | 300 |
| | | Fast mode+ | $20 \times (V_{DD} / 5.5\text{ V})$ | | 120 |
| | | High-speed mode, $C_b = 100\text{ pF}$ | 10 | | 40 |
| | | High-speed mode, $C_b = 400\text{ pF}$ | 20 | | 80 |
| C_b | Capacitive load for each bus line (SCL and SDA) | | 400 | pF | |
| t_{SP} | Pulse width of spike suppressed (SCL and SDA spikes that are less than the indicated width are suppressed) | Standard mode, fast mode and fast mode+ | 50 | ns | |
| | | High-speed mode | 10 | | |

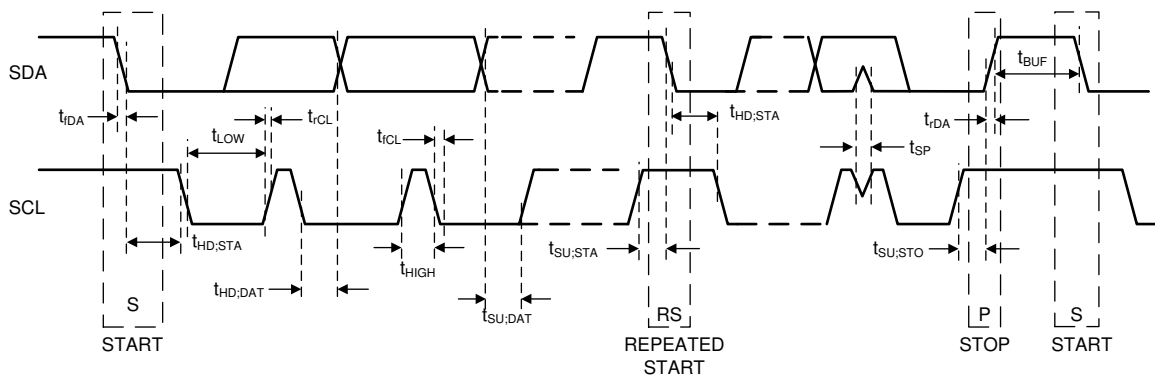
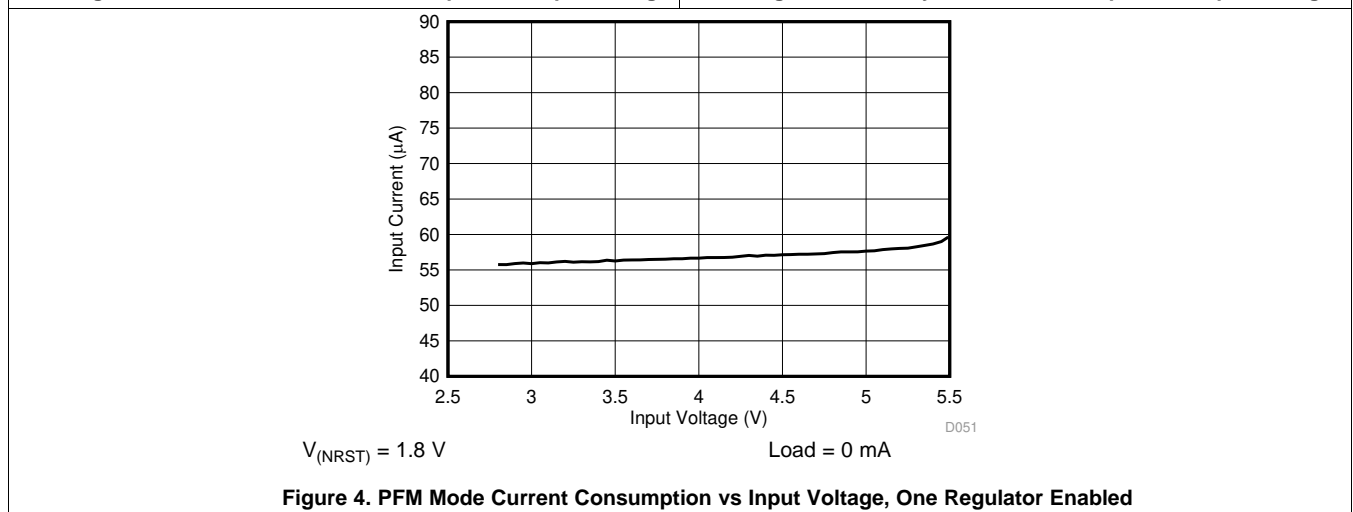
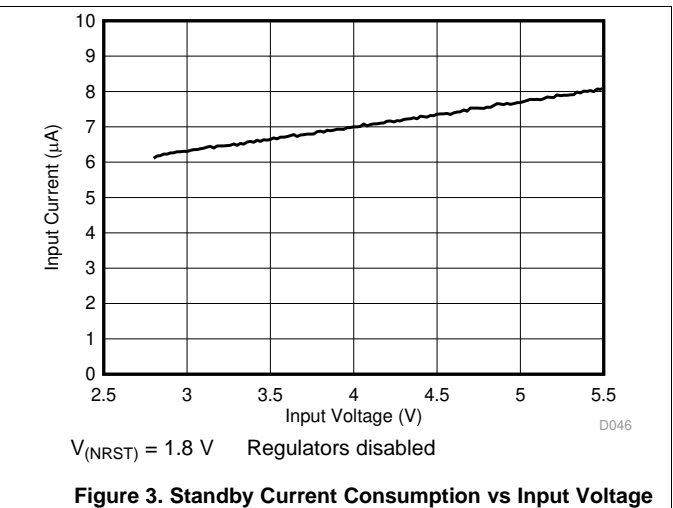
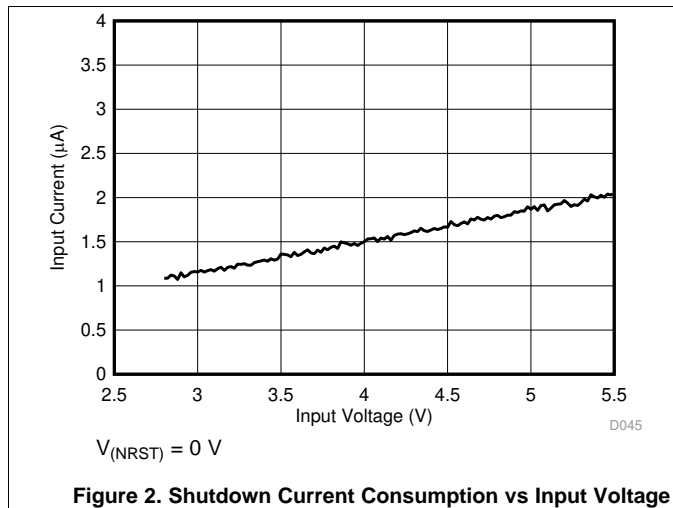


Figure 1. I²C Timing

6.7 Typical Characteristics

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 1\text{ V}$, $V_{(NRST)} = 1.8\text{ V}$, $f_{SW} = 4\text{ MHz}$, $L = 0.47\text{ }\mu\text{H}$ (TOKO DFE252012PD-R47M), $C_{OUT} = 22\text{ }\mu\text{F / phase}$, $C_{POL} = 22\text{ }\mu\text{F / phase}$.



7 Detailed Description

7.1 Overview

The LP87524B/J/P-Q1 is a high-efficiency, high-performance power supply device with four step-down DC-DC converter cores for automotive applications. [Table 1](#) lists the output characteristics of the regulators.

Table 1. Supply Specification

| SUPPLY | OUTPUT | | |
|--------------------------------------|--|---|---|
| | V _{OUT} RANGE (V) | RESOLUTION (mV) | I _{MAX} MAXIMUM OUTPUT CURRENT (A) |
| Buck0 | 0.6 to 3.36 (V _{IN} = 2.8 V - 4 V) 1.0 to 3.36 (V _{IN} = 2.8 V - 5.5 V) | 10 (0.6 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V) | 10 A total |
| Buck1 | 0.6 to 3.36 (V _{IN} = 2.8 V - 4 V) 1.0 to 3.36 (V _{IN} = 2.8 V - 5.5 V) | 10 (0.6 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V) | |
| Buck2 | 0.6 to 3.36 (V _{IN} = 2.8 V - 4 V) 1.0 to 3.36 (V _{IN} = 2.8 V - 5.5 V) | 10 (0.6 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V) | |
| Buck3 | 0.6 to 3.36 (V _{IN} = 2.8 V - 4 V) 1.0 to 3.36 (V _{IN} = 2.8 V - 5.5 V) | 10 (0.6 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V) | |
| LP87524B-Q1 default settings: | V_{OUT} (V) | I_{MAX} MAXIMUM OUTPUT CURRENT (A) | AWR / IWR Rail |
| Buck0 | 3.3 V | 1.5 A | IO |
| Buck1 | 1.2 V | 1.5 A | Digital |
| Buck2 | 1.8 V | 4 A | RF, with external LDO |
| Buck3 | 2.3 V | 2.5 A | RF, with external LDO |
| LP87524J-Q1 default settings: | V_{OUT} (V) | I_{MAX} MAXIMUM OUTPUT CURRENT (A) | AWR / IWR Rail |
| Buck0 | 3.3 V | 1.5 A | IO |
| Buck1 | 1.2 V | 1.5 A | Digital |
| Buck2 | 1 V | 4 A | RF, with ferrite filter |
| Buck3 | 1.8 V | 2.5 A | RF, with ferrite filter |
| LP87524P-Q1 default settings: | V_{OUT} (V) | I_{MAX} MAXIMUM OUTPUT CURRENT (A) | AWR / IWR Rail |
| Buck0 | 1 V | 3 A | RF, with ferrite filter |
| Buck1 | 1.2 V | 1.5 A | Digital |
| Buck2 | 1 V | 3 A | RF, with ferrite filter |
| Buck3 | 1.8 V | 2.5 A | RF, with ferrite filter |

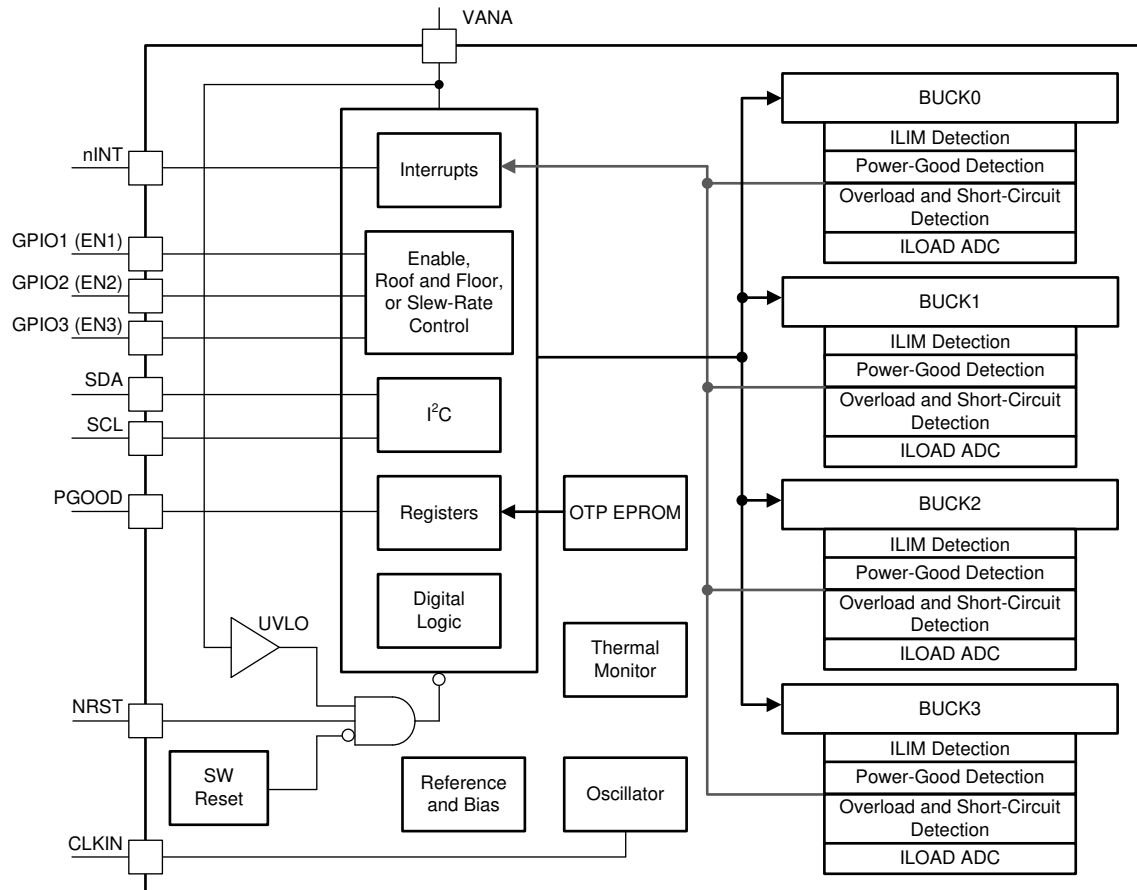
The LP87524B/J/P-Q1 also supports switching clock synchronization to an external clock. The nominal frequency of the external clock can be from 1 MHz to 24 MHz with 1-MHz steps.

Additional features include:

- Soft start
- Input voltage protection:
 - Undervoltage lockout
 - Overvoltage protection
- Output voltage monitoring and protection:
 - Overvoltage monitoring
 - Undervoltage monitoring
 - Overload protection
- Thermal warning
- Thermal shutdown

Three enable signals can be multiplexed to general purpose I/O (GPIO) signals. The direction and output type (open-drain or push-pull) are programmable for the GPIOs.

7.2 Functional Block Diagram



7.3 Feature Descriptions

7.3.1 DC-DC Converters

7.3.1.1 Overview

The LP87524B/J/P-Q1 includes four step-down DC-DC converter cores configured for four single-phase outputs. The cores are designed for flexibility; most of the functions are programmable, thus giving a possibility to optimize the regulator operation for each application.

The LP87524B/J/P-Q1 has the following features:

- DVS support
- Automatic mode control based on the loading (PFM or PWM mode)
- Forced-PWM mode operation
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Phase control for optimized EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Power Good flag with maskable interrupt
- Power Good signal (PGOOD) with selectable sources
- Average output current sensing (for PFM entry and load current measurement)

Feature Descriptions (continued)

The following parameters can be programmed via registers:

- Output voltage
- Forced-PWM operation
- Enable and disable delays for regulators and GPIOs controlled by ENx pins

There are two modes of operation for the converter, depending on the output current required: pulse-width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 600 mA or higher. Lighter output current loads cause the converter to automatically switch into PFM mode for reduced current consumption when forced-PWM mode is disabled.

A multi-phase synchronous buck converter offers several advantages over a single power stage converter. For application processor power delivery, lower ripple on the input and output currents and faster transient response to load steps are the most significant advantages. Also, because the load current is evenly shared among multiple channels in multi-phase output configuration, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. The physical size of the output inductor shrinks significantly due to this heat reduction. A block diagram of a single core is shown in [Figure 5](#).

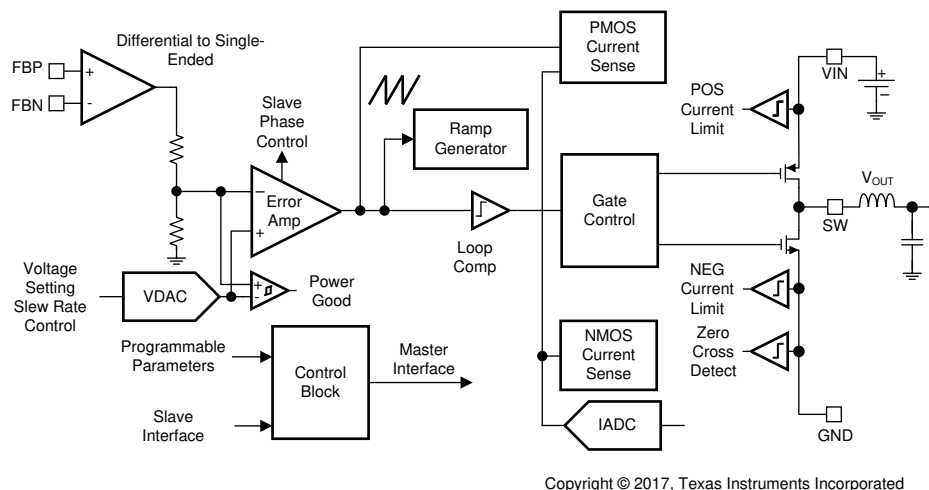


Figure 5. Detailed Block Diagram Showing One Core

7.3.1.2 Transition Between PWM and PFM Modes

The LP87524B/J/P-Q1 converter operates in PWM mode at load current of about 600 mA or higher. At lighter load-current levels the device automatically switches into PFM mode for reduced current consumption when forced-PWM mode is disabled (AUTO-mode operation). By combining the PFM and the PWM modes a high efficiency is achieved over a wide output-load-current range.

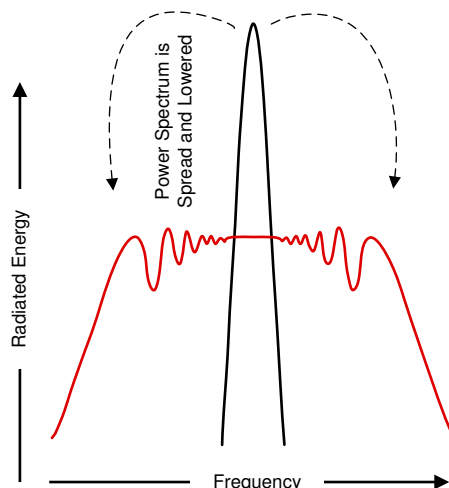
7.3.1.3 Buck Converter Load-Current Measurement

Buck load current can be monitored via I²C registers. The monitored buck converter is selected with the LOAD_CURRENT_BUCK_SELECT[1:0] bits in SEL_I_LOAD register. A write to this selection register starts a current measurement sequence. The regulator is forced to PWM mode during the measurement. The measurement sequence is 50 μ s long, maximum. LP87524B/J/P-Q1 can be configured to give out an interrupt (I_LOAD_READY bit in INT_TOP1 register) after the load current measurement sequence is finished. Load current measurement interrupt can be masked with I_LOAD_READY_MASK bit (TOP_MASK1 register). The measurement result can be read from registers I_LOAD_1 and I_LOAD_2. Register I_LOAD_1 bits BUCK_LOAD_CURRENT[7:0] give out the LSB bits and register I_LOAD_2 bits BUCK_LOAD_CURRENT[9:8] the MSB bits. The measurement result BUCK_LOAD_CURRENT[9:0] LSB is 20 mA, and maximum value of the measurement corresponds to 20.46 A.

Feature Descriptions (continued)

7.3.1.4 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI filters and shields to the boards. The LP87524B/J/P-Q1 device has register selectable spread-spectrum mode which minimizes the need for output filters, ferrite beads, or chokes. In spread-spectrum mode, the switching frequency varies around the center frequency, reducing the EMI emissions radiated by the converter and associated passive components and PCB traces (see Figure 6). This feature is available only when internal RC oscillator is used (PLL_MODE[1:0] = 00 in PLL_CTRL register), and it is enabled with the EN_SPREAD_SPEC bit (PIN_FUNCTION register), and it affects all the buck cores.



Where a fixed-frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread-spectrum architecture of the LP87524B/J/P-Q1 spreads that energy over a large bandwidth.

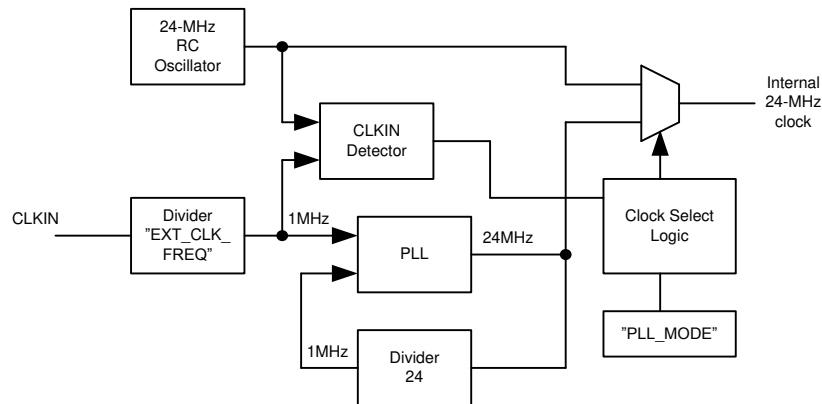
Figure 6. Spread-Spectrum Modulation

7.3.2 Sync Clock Functionality

The LP87524B/J/P-Q1 device contains a CLKIN input to synchronize switching clock of the buck regulator with the external clock. The block diagram of the clocking and PLL module is shown in Figure 7. Depending on the PLL_MODE[1:0] bits (in PLL_CTRL register) and the external clock availability, the external clock is selected and interrupt is generated as shown in Table 2. The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits (in PLL_CTRL register) and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/+10%) for valid clock detection.

The NO_SYNC_CLK interrupt (in INT_TOP1 register) is also generated in cases the external clock is expected but it is not available. These cases are start-up (read OTP-to-STANDBY transition) when PLL_MODE[1:0] = 01 and regulator enable (STANDBY-to-ACTIVE transition) when PLL_MODE[1:0] = 10.

Feature Descriptions (continued)



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Figure 7. Clock and PLL Module
Table 2. PLL Operation

| DEVICE OPERATION MODE | PLL_MODE[1:0] | PLL AND CLOCK DETECTOR STATE | INTERRUPT FOR EXTERNAL CLOCK | CLOCK |
|-----------------------|---------------|------------------------------|---|---|
| STANDBY | 00 | Disabled | No | Internal RC |
| ACTIVE | 00 | Disabled | No | Internal RC |
| STANDBY | 01 | Enabled | When external clock appears or disappears | Automatic change to external clock when available |
| ACTIVE | 01 | Enabled | When external clock appears or disappears | Automatic change to external clock when available |
| STANDBY | 10 | Disabled | No | Internal RC |
| ACTIVE | 10 | Enabled | When external clock appears or disappears | Automatic change to external clock when available |
| STANDBY | 11 | | Reserved | |
| ACTIVE | 11 | | Reserved | |

7.3.3 Power-Up

The power-up sequence for the LP87524B/J/P-Q1 is as follows:

- VANA (and VIN_Bx) reach minimum recommended level ($V_{VANA} > V_{ANA_{UVLO}}$).
- NRST is set to high level (or shorted to VANA). This initiates power-on-reset (POR), OTP reading and enables the system I/O interface. The I²C host must allow at least 1.2 ms before writing or reading data to the LP87524B/J/P-Q1.
- Device enters STANDBY-mode.
- The host can change the default register setting by I²C if needed.
- The regulator(s) can be enabled/disabled by ENx pin(s) and by I²C interface.

7.3.4 Regulator Control

7.3.4.1 Enabling and Disabling Regulators

The regulator(s) can be enabled when the device is in STANDBY or ACTIVE state. There are two ways for enable and disable the regulators:

- Using EN_BUCKx bit in BUCKx_CTRL1 register (EN_PIN_CTRLx register bit is 0)
- Using EN1/2/3 control pins (EN_BUCKx bit is 1 **AND** EN_PIN_CTRLx register bit is 1 in BUCKx_CTRL1 register)

If the EN1/2/3 control pins are used for enable and disable then the control pin is selected with BUCKx_EN_PIN_SELECT[1:0] bits (in BUCKx_CTRL1 register). The delay from the control signal rising edge to enabling of the regulator is set by BUCKx_STARTUP_DELAY[3:0] bits and the delay from control signal falling edge to disabling of the regulator is set by BUCKx_SHUTDOWN_DELAY[3:0] bits in BUCKx_DELAY register. The delays are valid only for EN1/2/3 signal control. The control with EN_BUCKx bit is immediate without the delays.

The control of the regulator (with 0-ms delays) is shown in [Table 3](#).

NOTE

The control of the regulator cannot be changed from one ENx pin to a different ENx pin because the control is ENx signal edge sensitive. The control from ENx pin to register bit and back to the original ENx pin can be done during operation.

Table 3. Regulator Control

| CONTROL METHOD | EN_BUCKx | EN_PIN_CTRLx | BUCKx_EN_PIN_SELECT[1:0] | EN_ROOF_FLOOR_x | EN1 PIN | EN2 PIN | EN3 PIN | BUCKx OUTPUT VOLTAGE |
|--|----------|--------------|--------------------------|-----------------|------------|------------|------------|-----------------------|
| Enable/disable control with EN_BUCKx bit | 0 | Don't Care | Don't Care | Don't Care | Don't Care | Don't Care | Don't Care | Disabled |
| | 1 | 0 | Don't Care | Don't Care | Don't Care | Don't Care | Don't Care | BUCKx_VSET[7:0] |
| Enable/disable control with EN1 pin | 1 | 1 | 00 | 0 | Low | Don't Care | Don't Care | Disabled |
| | 1 | 1 | 00 | 0 | High | Don't Care | Don't Care | BUCKx_VSET[7:0] |
| Enable/disable control with EN2 pin | 1 | 1 | 01 | 0 | Don't Care | Low | Don't Care | Disabled |
| | 1 | 1 | 01 | 0 | Don't Care | High | Don't Care | BUCKx_VSET[7:0] |
| Enable/disable control with EN3 pin | 1 | 1 | 10 | 0 | Don't Care | Don't Care | Low | Disabled |
| | 1 | 1 | 10 | 0 | Don't Care | Don't Care | High | BUCKx_VSET[7:0] |
| Roof/floor control with EN1 pin | 1 | 1 | 00 | 1 | Low | Don't Care | Don't Care | BUCKx_FLOOR_VSET[7:0] |
| | 1 | 1 | 00 | 1 | High | Don't Care | Don't Care | BUCKx_VSET[7:0] |
| Roof/floor control with EN2 pin | 1 | 1 | 01 | 1 | Don't Care | Low | Don't Care | BUCKx_FLOOR_VSET[7:0] |
| | 1 | 1 | 01 | 1 | Don't Care | High | Don't Care | BUCKx_VSET[7:0] |
| Roof/floor control with EN3 pin | 1 | 1 | 10 | 1 | Don't Care | Don't Care | Low | BUCKx_FLOOR_VSET[7:0] |
| | 1 | 1 | 10 | 1 | Don't Care | Don't Care | High | BUCKx_VSET[7:0] |

The regulator is enabled by the ENx pin or by I²C writing as shown in [Figure 8](#). The soft-start circuit limits the in-rush current during start-up. When the output voltage rises to 0.35-V level, the output voltage becomes slew-rate controlled. If there is a short circuit at the output and the output voltage does not increase above 0.35-V level in 1 ms, the regulator is disabled, and interrupt is set. When the output voltage reaches the Power-Good threshold level the BUCKx_PG_INT interrupt flag (in INT_BUCK_x register) is set. The Power-Good interrupt flag can be masked using BUCKx_PG_MASK bit (in BUCKx_MASK register).

The ENx input pins have integrated pulldown resistors. The pulldown resistors are enabled by default, and the host can disable those with ENx_PD bits (in CONFIG register).

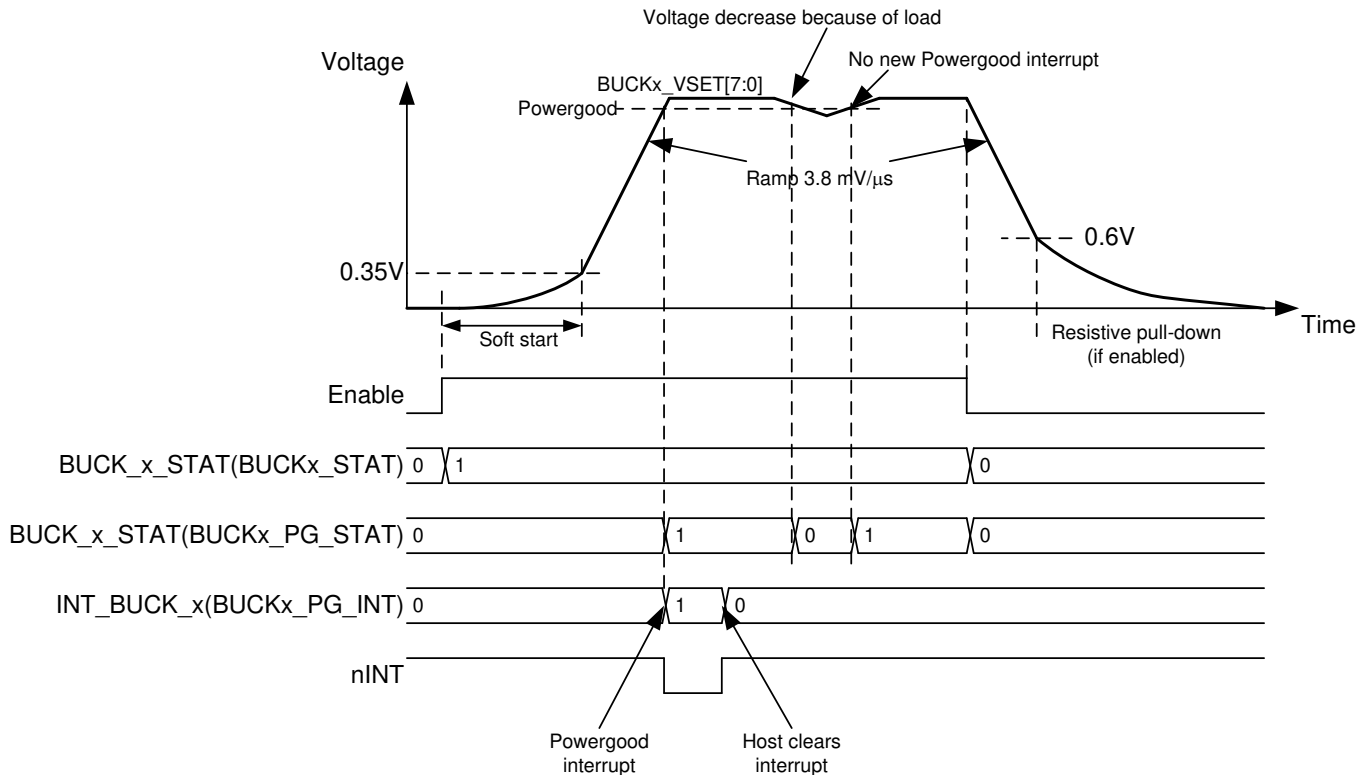


Figure 8. Regulator Enable and Disable

7.3.4.2 Changing Output Voltage

The output voltage of the regulator can be changed by the ENx pin (voltage levels defined by the BUCKx_VOUT and BUCKx_FLOOR_VOUT registers) or by writing to the BUCKx_VOUT and BUCKx_FLOOR_VOUT registers. The voltage change is always slew-rate controlled, 3.8 mV/μs. During voltage change the forced-PWM mode is used automatically. When the programmed output voltage is achieved, the mode becomes the one defined by the load current and the BUCKx_FPWM bit in BUCKx_CTRL1 register.

The Power-Good interrupt is generated when the output voltage reaches the programmed voltage level, as shown in [Figure 9](#).

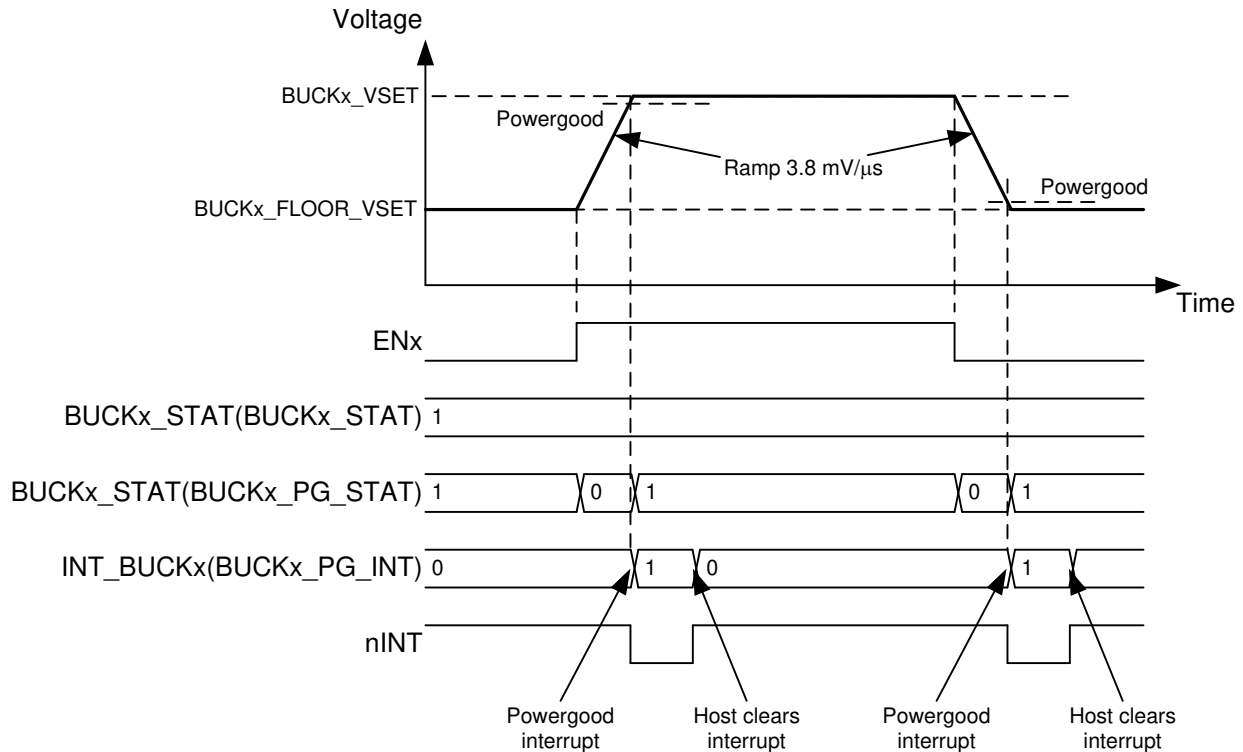


Figure 9. Regulator Output Voltage Change With ENx pin

7.3.5 Enable and Disable Sequences

The LP87524B/J/P-Q1 device supports start-up and shutdown sequencing with programmable delays for different regulator outputs using single EN1/2/3 control signal. The regulator is selected for delayed control with:

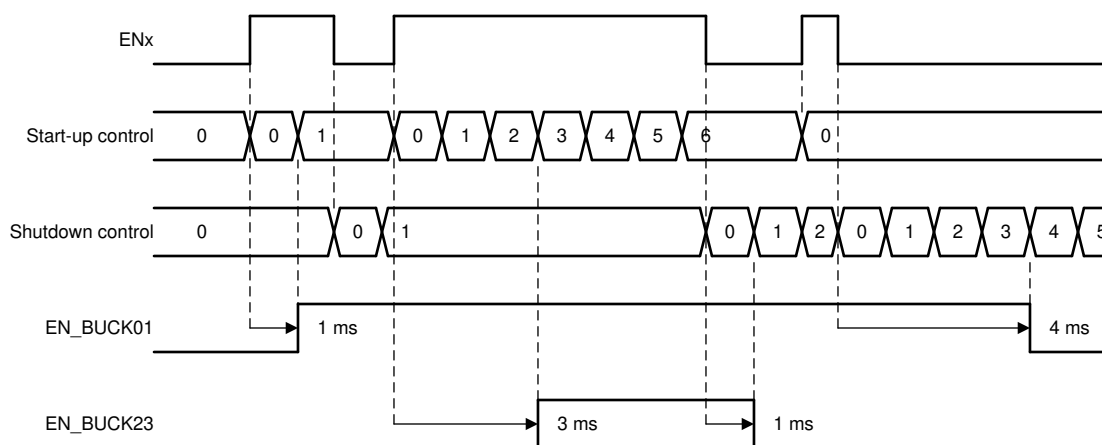
- EN_BUCKx = 1 (in BUCKx_CTRL1 register)
- EN_PIN_CTRLx = 1 (in BUCKx_CTRL1 register)
- EN_ROOF_FLOORx = 0 (in BUCKx_CTRL1 register)
- BUCKx_VSET[7:0] = Required voltage when ENx is high (in BUCKx_VOUT register)
- The ENABLE pin for control is selected with BUCKx_EN_PIN_SELECT[1:0] (in BUCKx_CTRL1 register)
- The delay from rising edge of ENx signal to the regulator enable is set by BUCKx_STARTUP_DELAY[3:0] bits (in BUCKx_DELAY register) and
- The delay from falling edge of ENx signal to the regulator disable is set by BUCKx_SHUTDOWN_DELAY[3:0] bits (in BUCKx_DELAY register)

There are four time steps available for start-up and shutdown sequences. The delay times are selected with DOUBLE_DELAY bit in CONFIG register and HALF_DELAY bit in PGOOD_CTRL2 register as shown in Table 4.

Table 4. Start-up and Shutdown Delays

| X_STARTUP_DELAY / X_SHUTDOWN_DELAY | DOUBLE_DELAY = 0 HALF_DELAY = 1 | DOUBLE_DELAY = 1 HALF_DELAY = 1 | DOUBLE_DELAY = 0 HALF_DELAY = 0 | DOUBLE_DELAY = 1 HALF_DELAY = 0 |
|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| 0000 | 0 ms | 0 ms | 0 ms | 0 ms |
| 0001 | 0.32 ms | 0.64 ms | 1 ms | 2 ms |
| 0010 | 0.64 ms | 1.28 ms | 2 ms | 4 ms |
| 0011 | 0.96 ms | 1.92 ms | 3 ms | 6 ms |
| 0100 | 1.28 ms | 2.56 ms | 4 ms | 8 ms |
| 0101 | 1.6 ms | 3.2 ms | 5 ms | 10 ms |
| 0110 | 1.92 ms | 3.84 ms | 6 ms | 12 ms |
| 0111 | 2.24 ms | 4.48 ms | 7 ms | 14 ms |
| 1000 | 2.56 ms | 5.12 ms | 8 ms | 16 ms |
| 1001 | 2.88 ms | 5.76 ms | 9 ms | 18 ms |
| 1010 | 3.2 ms | 6.4 ms | 10 ms | 20 ms |
| 1011 | 3.52 ms | 7.04 ms | 11 ms | 22 ms |
| 1100 | 3.84 ms | 7.68 ms | 12 ms | 24 ms |
| 1101 | 4.16 ms | 8.32 ms | 13 ms | 26 ms |
| 1110 | 4.48 ms | 8.96 ms | 14 ms | 28 ms |
| 1111 | 4.8 ms | 9.6 ms | 15 ms | 30 ms |

An example of start-up and shutdown sequences is shown in [Figure 10](#) and [Figure 11](#). The start-up and shutdown delays for the Buck0/1 regulators are 1 ms and 4 ms and for the Buck2/3 regulators 3 ms and 1 ms. The delay settings are used only for enable/disable control with EN1/2/3 signals, not for Roof/Floor control.

**Figure 10. Typical Start-Up and Shutdown Sequencing****Figure 11. Start-Up and Shutdown Sequencing With Short ENx Low and High Periods**

7.3.6 Device Reset Scenarios

There are three reset methods implemented on the LP87524B/J/P-Q1:

- Software reset with SW_RESET register bit (in RESET register)
- POR from rising edge of NRST signal
- Undervoltage lockout (UVLO) reset from VANA supply

A SW-reset occurs when SW_RESET bit is written 1. The bit is automatically cleared after writing. This event disables all the regulators immediately, resets all the register bits to the default values and OTP bits are loaded (see [Figure 15](#)). I²C interface is not reset during software reset. The host must wait at least 1.2 ms after writing SW reset until making a new I²C read or write to the device.

If VANA supply voltage falls below UVLO threshold level or NRST signal is set low then all the regulators are disabled immediately, and all the register bits are reset to the default values. When the VANA supply voltage rises above UVLO threshold level **AND** NRST signal rises above threshold level an internal power-on reset (POR) occurs. OTP bits are loaded to the registers and a start-up is initiated according to the register settings. The host must wait at least 1.2 ms after POR until reading or writing to I²C interface.

7.3.7 Diagnostics and Protection Features

The LP87524B/J/P-Q1 is capable of providing four levels of protection features:

- Information of valid regulator output voltage which sets interrupt or PGOOD signal;
- Warnings for diagnostics which sets interrupt;
- Protection events which are disabling the regulators affected; and
- Faults which are causing the device to shutdown.

The LP87524B/J/P-Q1 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. nINT is released again after a clear of flags is complete. The nINT signal stays low until all the pending interrupts are cleared.

When a fault is detected, it is indicated by a RESET_REG interrupt flag (in INT2_TOP register) after next start-up.

Table 5. Summary of Interrupt Signals

| EVENT | RESULT | INTERRUPT REGISTER AND BIT | INTERRUPT MASK | STATUS BIT | RECOVERY/INTERRUPT CLEAR |
|---|---|-------------------------------------|-------------------|------------------|--|
| Current limit triggered (20- μ s debounce) | Interrupt | INT_BUCKx = 1 BUCKx_ILIM_INT = 1 | BUCKx_ILIM_MASK | BUCKx_ILIM_STAT | Write 1 to BUCKx_ILIM_INT bit Interrupt is not cleared if current limit is active |
| Short circuit ($V_{OUT} < 0.35$ V at 1 ms after enable) or overload (V_{OUT} decreasing below 0.35 V during operation, 1 ms debounce) | Regulator disable and interrupt | INT_BUCKx = 1 BUCKx_SC_INT = 1 | N/A | N/A | Write 1 to BUCKx_SC_INT bit |
| Thermal warning | Interrupt | TDIE_WARN = 1 | TDIE_WARN_MASK | TDIE_WARN_STAT | Write 1 to TDIE_WARN bit Interrupt is not cleared if temperature is above thermal warning level |
| Thermal shutdown | All regulators disabled and Output GPIOx set to low and interrupt | TDIE_SD = 1 | N/A | TDIE_SD_STAT | Write 1 to TDIE_SD bit Interrupt is not cleared if temperature is above thermal shutdown level |
| VANA overvoltage ($VANA_{OVP}$) | All regulators disabled and Output GPIOx set to low and interrupt | INT_OVP | N/A | OVP_STAT | Write 1 to INT_OVP bit Interrupt is not cleared if VANA voltage is above VANA OVP level |
| Power Good, output voltage reaches the programmed value | Interrupt | INT_BUCKx = 1 BUCKx_PG_INT = 1 | BUCKx_PG_MASK | BUCKx_PG_STAT | Write 1 to BUCKx_PG_INT bit |
| GPIO | Interrupt | INT_GPIO | GPIO_MASK | GPIO_IN register | Write 1 to INT_GPIO bit |
| External clock appears or disappears | Interrupt | NO_SYNC_CLK ⁽¹⁾ | SYNC_CLK_MASK | SYNC_CLK_STAT | Write 1 to NO_SYNC_CLK bit |
| Load current measurement ready | Interrupt | I_LOAD_READY = 1 | I_LOAD_READY_MASK | N/A | Write 1 to I_LOAD_READY bit |

(1) Interrupt is generated during clock detector operation and in case clock is not available when clock detector is enabled.

Table 5. Summary of Interrupt Signals (continued)

| EVENT | RESULT | INTERRUPT REGISTER AND BIT | INTERRUPT MASK | STATUS BIT | RECOVERY/INTERRUPT CLEAR |
|---|--|----------------------------|----------------|------------|--------------------------|
| Start-up (NRST rising edge) | Device ready for operation, registers reset to default values and interrupt | RESET_REG = 1 | RESET_REG_MASK | N/A | Write 1 to RESET_REG bit |
| Glitch on supply voltage and UVLO triggered (VANA falling and rising) | Immediate shutdown followed by power up, registers reset to default values and interrupt | RESET_REG = 1 | RESET_REG_MASK | N/A | Write 1 to RESET_REG bit |
| Software requested reset | Immediate shutdown followed by power up, registers reset to default values and interrupt | RESET_REG = 1 | RESET_REG_MASK | N/A | Write 1 to RESET_REG bit |

7.3.7.1 Power-Good Information (PGOOD pin)

In addition to the interrupt based indication of current limit and Power-Good level the LP87524B/J/P-Q1 device supports the indication with PGOOD signal. Either voltage and current monitoring or a voltage monitoring only can be selected for PGOOD indication. This selection is individual for all buck regulators and is set by PGx_SEL[1:0] bits (in PGOOD_CTRL1 register). When both voltage and current are monitored, PGOOD signal active indicates that regulator output is inside the Power-Good voltage window and that load current is below I_{LIM_FWD} . If only voltage is monitored, then the current monitoring is ignored for the PGOOD signal. When a regulator is disabled, the monitoring is automatically masked to prevent it forcing PGOOD inactive. This allows connecting PGOOD signals from various devices together when open-drain outputs are used. When regulator voltage is transitioning from one target voltage to another, the voltage monitoring PGOOD signal is set inactive. The monitoring from all the output rails are combined, and PGOOD is active only if all the sources shows active status. The status from all the voltage rails are summarized in [Table 6](#).

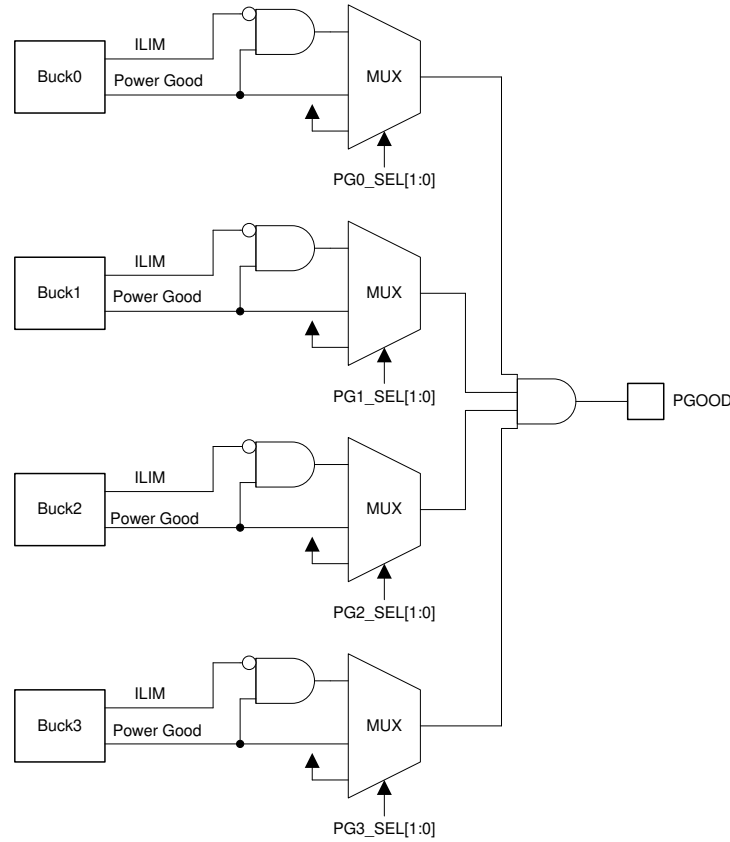
If the PGOOD signal is inactive or it changes the state to inactive, the source for the state can be read from PGOOD_FLT register. During reading all the PGx_FLT bit are cleared that are not driving the PGOOD inactive. When PGOOD signal goes active, the host must read the PGOOD_FLT register to clear all the bits. The PGOOD signal follows the status of all the monitored outputs.

The PGOOD signal can be also configured so that it maintains inactive state even when the monitored outputs are valid but there are PGx_FLT bits pending clearance in PGOOD_FLT register. This mode of operation is selected by setting EN_PGFLT_STAT bit to 1 (in PGOOD_CTRL2 register).

The type of output voltage monitoring for PGOOD signal is selected by PGOOD_WINDOW bit (in PGOOD_CTRL2 register). If the bit is 0, only undervoltage is monitored; if the bit is 1, both undervoltage and overvoltage are monitored.

The polarity and the output type (push-pull or open-drain) are selected by PGOOD_POL and PGOOD_OD bits in PGOOD_CTRL2 register.

The filtering time for invalid output voltage is always typically 7 μ s and for valid output voltage the filtering time is selected with PGOOD_SET_DELAY bit (in PGOOD_CTRL2 register). The Power-Good waveforms are shown in [Figure 13](#).



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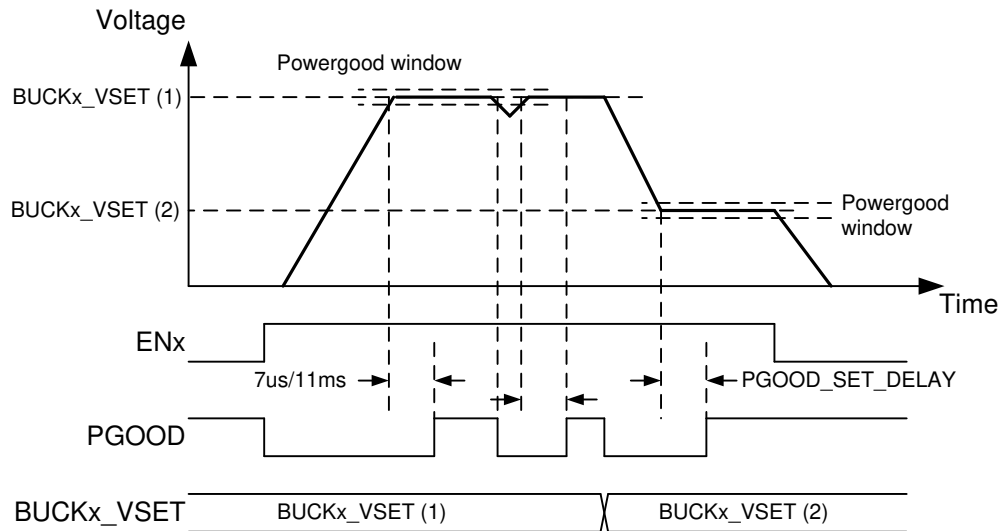
Figure 12. PGOOD Block Diagram

Table 6. PGOOD Operation

| STATUS / USE CASE | CONDITION | INPUT TO PGOOD SIGNAL |
|---|--|--|
| Buck not selected for PGOOD monitoring | PGx_SEL = 00 (in PGOOD_CTRL1 register) | Active |
| Buck disabled | | Active |
| BUCK SELECTED FOR PGOOD MONITORING | | |
| Buck start-up delay | | Inactive |
| Buck soft start | $V_{OUT} < 0.35 V$ | Inactive |
| Buck voltage ramp-up | $0.35 V < V_{OUT} < V_{SET}$ | Inactive |
| Output voltage within window limits after start-up | Must be inside limits longer than debounce time | Active |
| Output voltage inside voltage window and current limit active | Current limit active longer than debounce time | Active (if only voltage monitoring selected) Inactive (if also current monitoring selected) |
| Output voltage spikes (overvoltage or undervoltage) | If spikes are outside voltage window longer than debounce time | Inactive |
| Voltage setting change, output voltage ramp | | Inactive |
| Output voltage within window limits after voltage change | Must be inside limits longer than debounce time | Active |
| Buck shutdown delay | | Active |
| Buck output voltage ramp down | | Active |

Table 6. PGOOD Operation (continued)

| STATUS / USE CASE | CONDITION | INPUT TO PGOOD SIGNAL |
|--|-----------|-----------------------|
| Buck disabled by thermal shutdown and interrupt pending | | Inactive |
| Buck disabled by overvoltage and interrupt pending | | Inactive |
| Buck disabled by short-circuit detection and interrupt pending | | Inactive |

**Figure 13. PGOOD Waveforms (PGOOD_POL=0)**

7.3.7.2 Warnings for Diagnostics (Interrupt)

7.3.7.2.1 Output Power Limit

The regulators have output peak current limits. The peak current limits are described in [Specifications](#). If the load current is increased so that the current limit is triggered, the regulator continues to regulate to the limit current level (current peak regulation, peak on every switching cycle). The voltage may decrease if the load current is higher than the average output current. If the current regulation continues for 20 μ s, the LP87524B/J/P-Q1 device sets the BUCKx_ILIM_INT bit (in INT_BUCKx register) and pulls the nINT pin low. The host processor can read BUCKx_ILIM_STAT bits (in BUCKx_STAT register) to see if the regulator is still in peak current regulation mode.

If the load is so high that the output voltage decreases below a 350-mV level, the LP87524B/J/P-Q1 device disables the regulator and sets the BUCKx_SC_INT bit (in INT_BUCKx register). In addition the BUCKx_STAT bit (in BUCKx_STAT register) is set to 0. The interrupt is cleared when the host processor writes 1 to BUCKx_SC_INT bit. The overload situation is shown in [Figure 14](#).

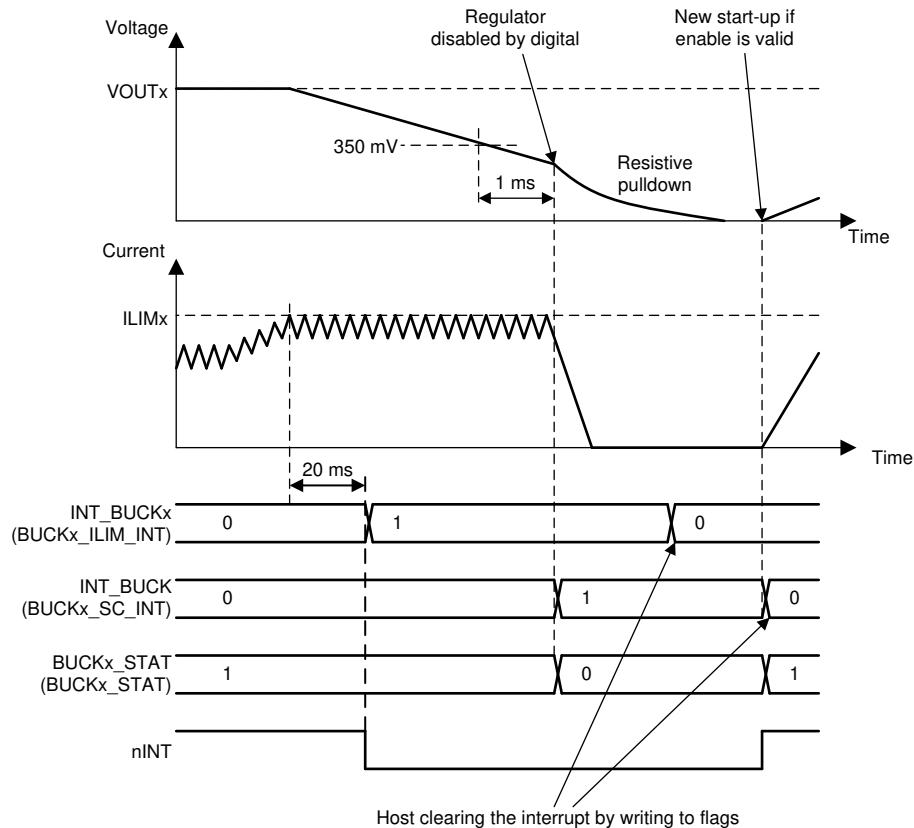


Figure 14. Overload Situation

7.3.7.2.2 Thermal Warning

The LP87524B/J/P-Q1 device includes a monitoring feature against overtemperature by setting an interrupt for host processor. The threshold level of the thermal warning is selected with TDIE_WARN_LEVEL bit (in CONFIG register).

If the LP87524B/J/P-Q1 device temperature increases above thermal warning level the device sets TDIE_WARN bit (in INT_TOP1 register) and pulls nINT pin low. The status of the thermal warning can be read from TDIE_WARN_STAT bit (in TOP_STAT register), and the interrupt is cleared by writing 1 to TDIE_WARN bit.

7.3.7.3 Protection (Regulator Disable)

If the regulator is disabled because of protection or fault (short-circuit protection, overload protection, thermal shutdown, overvoltage protection, or UVLO), the output power FETs are set to high-impedance mode, and the output pulldown resistor is enabled (if enabled with EN_RDISx bits in BUCKx_CTRL1 register). The turnoff time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pulldown resistor. The pulldown resistors are active as long as VANA voltage is above approximately a 1.2-V level.

7.3.7.3.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP87524B/J/P-Q1 to protect itself and external components against short circuit at the output or against overload during start-up. The fault threshold is 350 mV, the protection is triggered, and the regulator is disabled if the output voltage is below the threshold level 1 ms after the regulator is enabled.

In a similar way the overload situation is protected during normal operation. If the voltage on the feedback pin of the regulator falls below 0.35 V and remains below the threshold level for 1 ms, the regulator is disabled.

In the short-circuit and overload situations the BUCKx_SC_INT (in INT_BUCKx register) and the INT_BUCKx bits (in INT_TOP1 register) are set to 1, the BUCKx_STAT bit (in BUCKx_STAT register) is set to 0, and the nINT signal is pulled low. The host processor clears the interrupt by writing 1 to the BUCKx_SC_INT bit. Upon clearing the interrupt the regulator makes a new start-up attempt if the regulator is in enabled state.

7.3.7.3.2 Overvoltage Protection

The LP87524B/J/P-Q1 device monitors the input voltage from the VANA pin in standby and active operation modes. If the input voltage rises above $VANA_{OVP}$ voltage level, all the regulators are disabled, pulldown resistors discharge the output voltages (if EN_RDISx = 1 in BUCKx_CTRL1 register), GPIOs that are configured to outputs are set to logic low level, nINT signal is pulled low, INT_OVP bit (in INT_TOP1 register) is set to 1, and BUCKx_STAT bits (in BUCK_x_STAT register) are set to 0. The host processor can clear the interrupt by writing 1 to the INT_OVP bit. If the input voltage is above the overvoltage detection level the interrupt is not cleared. The host can read the status of the overvoltage from the OVP_STAT bit (in TOP_STAT register). Regulators cannot be enabled as long as the input voltage is above overvoltage detection level or the overvoltage interrupt is pending.

7.3.7.3.3 Thermal Shutdown

The LP87524B/J/P-Q1 has an overtemperature protection function that operates to protect the device from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the regulators are disabled, the TDIE_SD bit (in INT_TOP1 register) is set to 1, the nINT signal is pulled low, and the device enters STANDBY. The host processor can clear the interrupt by writing 1 to the TDIE_SD bit. If the temperature is above thermal shutdown level the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE_SD_STAT bit (in TOP_STAT register). Regulators cannot be enabled as long as the junction temperature is above thermal shutdown level or the thermal shutdown interrupt is pending.

7.3.7.4 Fault (Power Down)

7.3.7.4.1 Undervoltage Lockout

When the input voltage falls below $VANA_{UVLO}$ at the VANA pin, the buck converters are disabled immediately, and the output capacitors are discharged using the pulldown resistor, and the LP87524B/J/P-Q1 device enters SHUTDOWN. When VANA voltage is above UVLO threshold level and NRST signal is high, the device powers up to STANDBY state.

If the reset interrupt is unmasked by default (RESET_REG_MASK = 0 in TOP_MASK2 register) the RESET_REG interrupt (in INT_TOP2 register) indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the RESET_REG bit. If the host processor reads the RESET_REG flag after detecting an nINT low signal, it knows that the input supply voltage has been below UVLO level (or the host has requested reset), and the registers are reset to default values.

7.3.8 GPIO Signal Operation

The LP87524B/J/P-Q1 device supports up to 3 GPIO signals. The GPIO signals are multiplexed with enable signals. The selection between enable and GPIO function is set with GPIOx_SEL bits in PIN_FUNCTION register. The GPIOs are mapped to EN signals so that:

- EN1 is multiplexed with GPIO1
- EN2 is multiplexed with GPIO2
- EN3 is multiplexed with GPIO3

When the pin is selected for GPIO function, additional bits defines how the GPIO operates:

- GPIOx_DIR defines the direction of the GPIO, input or output (GPIO_CONFIG register)
- GPIOx_OD defines the type of the output when the GPIO is set to output, either push-pull with VANA level or open-drain (GPIO_CONFIG register)

When the GPIOx is defined as output, the logic level of the pin is set by GPIOx_OUT bit (in GPIO_OUT register).

When the GPIOx is defined as input, the logic level of the pin can be read from GPIOx_IN bit (in GPIO_IN register).

The control of the GPIOs configured to outputs can be included to start-up and shutdown sequences. The GPIO control for a sequence with ENx signal is selected by EN_PIN_CTRL_GPIOx and EN_PIN_SELECT_GPIOx bits (in PIN_FUNCTION register). The delays during start-up and shutdown are set by GPIOx_STARTUP_DELAY[3:0] and GPIOx_SHUTDOWN_DELAY[3:0] bits (in GPIOx_DELAY register) in the same way as control of the regulators.

The GPIOx signals have a selectable pulldown resistor. The pulldown resistors are selected by ENx_PD bits (in CONFIG register).

NOTE

The control of the GPIOx pin cannot be changed from one ENx pin to a different ENx pin because the control is ENx signal edge sensitive. The control from ENx pin to register bit and back to the original ENx pin can be done during operation.

7.3.9 Digital Signal Filtering

The digital signals have a debounce filtering. The signal/supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

Table 7. Digital Signal Filtering

| EVENT | SIGNAL/SUPPLY | RISING EDGE DEBOUNCE TIME | FALLING EDGE DEBOUNCE TIME |
|---|---------------------------------------|--|-----------------------------------|
| Enable/disable/voltage select for Buckx | EN1 | 3 μ s ⁽¹⁾ | 3 μ s ⁽¹⁾ |
| Enable/disable/voltage select for Buckx | EN2 | 3 μ s ⁽¹⁾ | 3 μ s ⁽¹⁾ |
| Enable/disable/voltage select for Buckx | EN3 | 3 μ s ⁽¹⁾ | 3 μ s ⁽¹⁾ |
| VANA UVLO | VANA | 20 μ s (VANA voltage rising) | Immediate (VANA voltage falling) |
| VANA overvoltage | VANA | 20 μ s (VANA voltage rising) | 20 μ s (VANA voltage falling) |
| Thermal warning | TDIE_WARN | 20 μ s | 20 μ s |
| Thermal shutdown | TDIE_SD | 20 μ s | 20 μ s |
| Current limit | VOUTx_ILIM | 20 μ s | 20 μ s |
| Overload | FB_B0, FB_B1, FB_B2, FB_F3 | 1 ms | 20 μ s |
| Power-Good interrupt | FB_B0, FB_B1, FB_B2, FB_F3 | 20 μ s | 20 μ s |
| PGOOD pin (voltage monitoring) | PGOOD / FB_B0, FB_B1, FB_B2, FB_F3 | 4-8 μ s (start-up debounce time during start-up) | 4 to 8 μ s |
| PGOOD pin (current monitoring) | PGOOD | 20 μ s | 20 μ s |

(1) No glitch filtering, only synchronization.

7.4 Device Functional Modes

7.4.1 Modes of Operation

SHUTDOWN: The NRST voltage is below threshold level. All switch, reference, control, and bias circuits of the LP87524B/J/P-Q1 device are turned off.

READ OTP: The main supply voltage VANA is above $VANA_{UVLO}$ level and NRST voltage is above threshold level. The regulators are disabled and the reference and bias circuits of the LP87524B/J/P-Q1 are enabled. The OTP bits are loaded to registers.

STANDBY: The main supply voltage VANA is above $VANA_{UVLO}$ level and NRST voltage is above threshold level. The regulators are disabled and the reference, control and bias circuits of the LP87524B/J/P-Q1 are enabled. All registers can be read or written by the host processor via the system serial interface. The regulators can be enabled if needed.

ACTIVE: The main supply voltage VANA is above $VANA_{UVLO}$ level and NRST voltage is above threshold level. At least one DC-DC converter is enabled. All registers can be read or written by the host processor via the system serial interface.

The operating modes and transitions between the modes are shown in [Figure 15](#).

Device Functional Modes (continued)

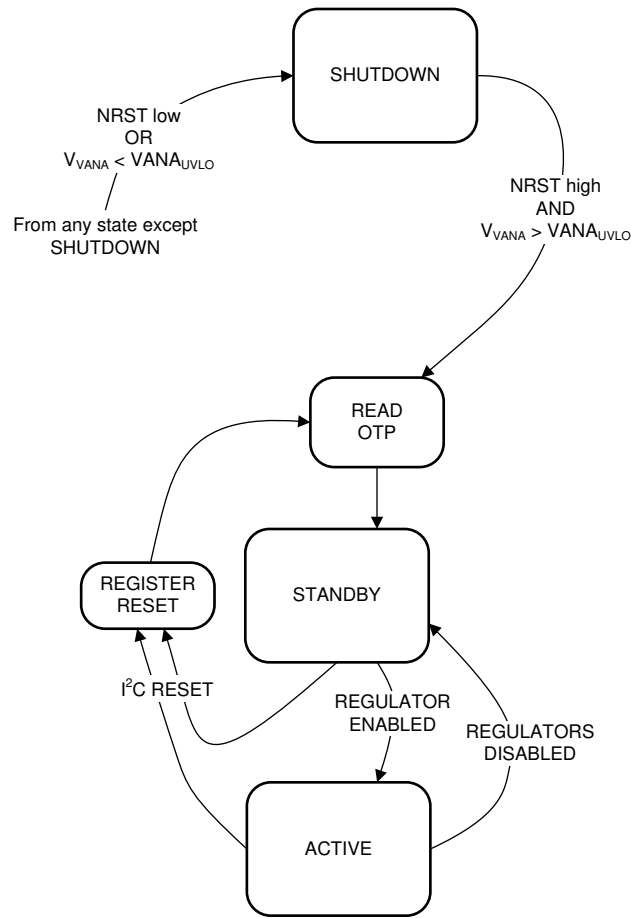


Figure 15. Device Operation Modes

7.5 Programming

7.5.1 I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. Note: CLK pin is not used for serial bus data transfer. The LP87524B/J/P-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode+ (1 MHz), and high-speed mode (3.4 MHz).

7.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

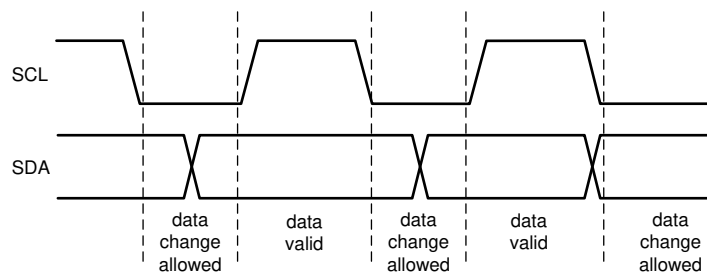


Figure 16. Data Validity Diagram

7.5.1.2 Start and Stop Conditions

The LP87524B/J/P-Q1 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

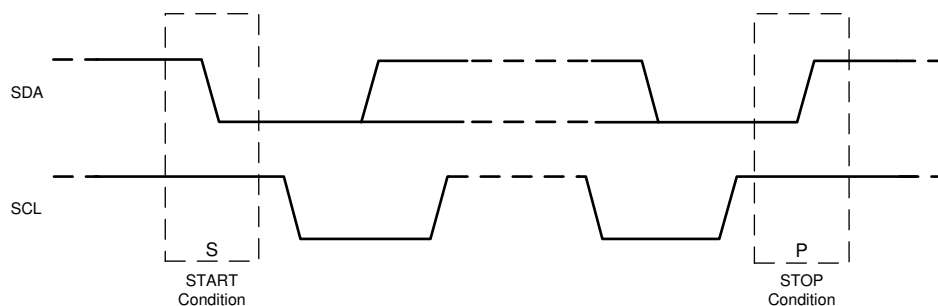


Figure 17. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. [Figure 18](#) shows the SDA and SCL signal timing for the I²C-compatible bus. See the [Figure 1](#) for timing values.

Programming (continued)

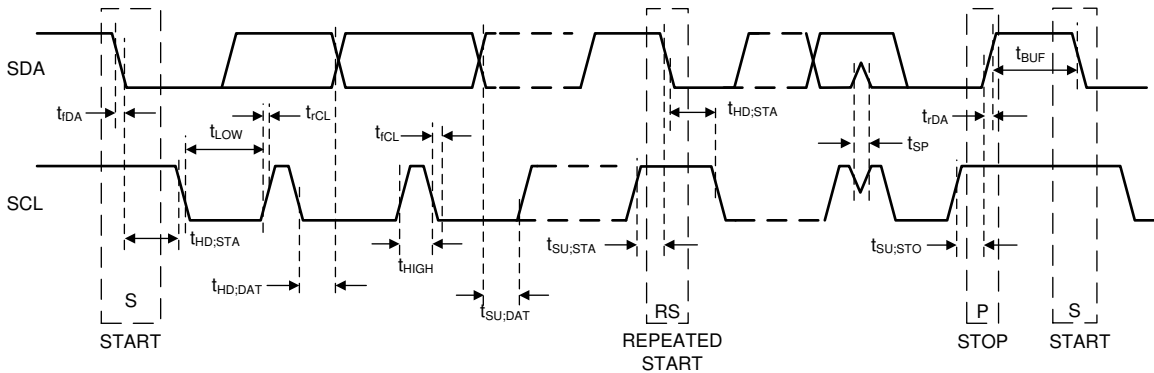


Figure 18. I²C-Compatible Timing

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP87524B/J/P-Q1 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP87524B/J/P-Q1 generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

NOTE

If the NRST signal is low during I²C communication the LP87524B/J/P-Q1 device does not drive SDA line. The ACK signal and data transfer to the master is disabled at that time.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

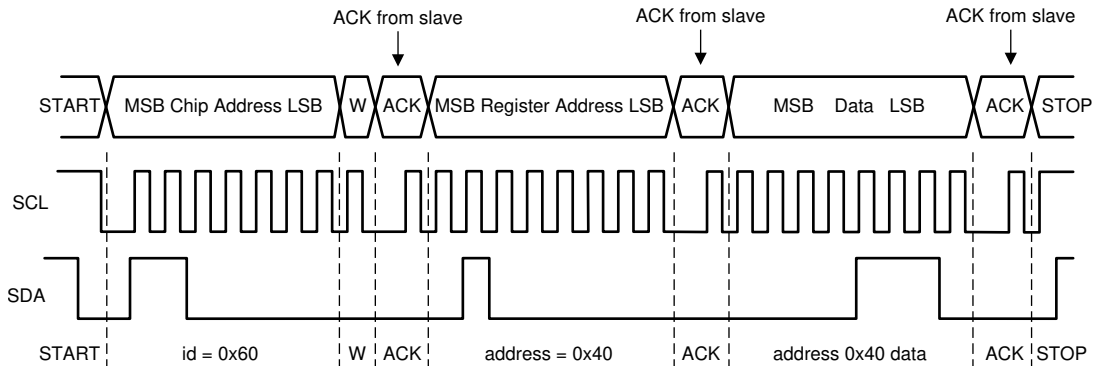
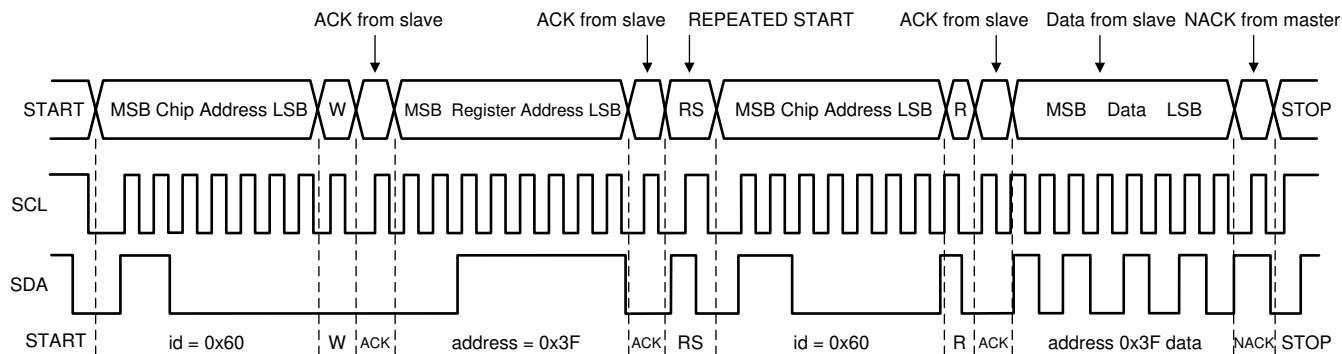


Figure 19. Write Cycle (w = write; SDA = 0), id = Device Address = 0x60 for LP87524B/J/P-Q1

Programming (continued)



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

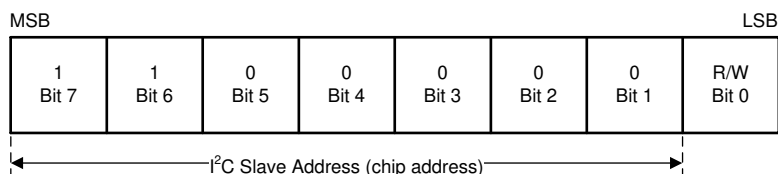
Figure 20. Read Cycle (r = read; SDA = 1), id = Device Address = 0x60 for LP87524B/J/P-Q1

7.5.1.4 I²C-Compatible Chip Address

NOTE

The device address for the LP87524B/J/P-Q1 is 0x60

After the START condition, the I²C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



A. Here device address is 1100000Bin = 60Hex.

Figure 21. Example Device Address

7.5.1.5 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the device, the internal address index counter is incremented by one and the next register is written. Table 8 below shows writing sequence to two consecutive registers. Note that auto increment feature does not work for read.

Table 8. Auto-Increment Example

| MASTER ACTION | START | DEVICE ADDRESS = 0x60 | WRITE | | REGISTER ADDRESS | | DATA | | DATA | | STOP |
|-----------------|-------|-----------------------|-------|-----|------------------|-----|------|-----|------|-----|------|
| LP87524B/J/P-Q1 | | | | ACK | | ACK | | ACK | | ACK | |

7.6 Register Maps

7.6.1 Register Descriptions

The LP87524B/J/P-Q1 is controlled by a set of registers through the I²C-compatible interface. The device registers, their addresses, and their abbreviations are listed in [Table 9](#). A more detailed description is given in the [OTP_REV](#) to [GPIO_OUT](#) sections.

The asterisk (*) marking indicates register bits which are updated from OTP memory during READ OTP state.

NOTE

This register map describes the default values read from OTP memory for a device with orderable code of LP87524BRNFRQ1, LP87524JRNFRQ1 and LP87524PRNFRQ1. For other LP8752x versions the default values read from OTP memory can be different.

Table 9. Summary of LP87524B/J/P-Q1 Control Registers

| Addr | Register | Read / Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|------|------------------|--------------|---------------------------|--------------|--------------------------|----------------|--------------------------|------------|----------|----|----------|
| 0x01 | OTP_REV | R | OTP_ID[7:0] | | | | | | | | |
| 0x02 | BUCK0_CTRL1 | R/W | EN_BUCK0 | EN_PIN_CTRL0 | BUCK0_EN_PIN_SELECT[1:0] | EN_ROOF_FLOOR0 | EN_RDIS0 | BUCK0_FPWM | Reserved | | |
| 0x04 | BUCK1_CTRL1 | R/W | EN_BUCK1 | EN_PIN_CTRL1 | BUCK1_EN_PIN_SELECT[1:0] | EN_ROOF_FLOOR1 | EN_RDIS1 | BUCK1_FPWM | Reserved | | |
| 0x06 | BUCK2_CTRL1 | R/W | EN_BUCK2 | EN_PIN_CTRL2 | BUCK2_EN_PIN_SELECT[1:0] | EN_ROOF_FLOOR2 | EN_RDIS2 | BUCK2_FPWM | Reserved | | |
| 0x08 | BUCK3_CTRL1 | R/W | EN_BUCK3 | EN_PIN_CTRL3 | BUCK3_EN_PIN_SELECT[1:0] | EN_ROOF_FLOOR3 | EN_RDIS3 | BUCK3_FPWM | Reserved | | |
| 0x0A | BUCK0_VOUT | R/W | BUCK0_VSET[7:0] | | | | | | | | |
| 0x0B | BUCK0_FLOOR_VOUT | R/W | BUCK0_FLOOR_VSET[7:0] | | | | | | | | |
| 0x0C | BUCK1_VOUT | R/W | BUCK1_VSET[7:0] | | | | | | | | |
| 0x0D | BUCK1_FLOOR_VOUT | R/W | BUCK1_FLOOR_VSET[7:0] | | | | | | | | |
| 0x0E | BUCK2_VOUT | R/W | BUCK2_VSET[7:0] | | | | | | | | |
| 0x0F | BUCK2_FLOOR_VOUT | R/W | BUCK2_FLOOR_VSET[7:0] | | | | | | | | |
| 0x10 | BUCK3_VOUT | R/W | BUCK3_VSET[7:0] | | | | | | | | |
| 0x11 | BUCK3_FLOOR_VOUT | R/W | BUCK3_FLOOR_VSET[7:0] | | | | | | | | |
| 0x12 | BUCK0_DELAY | R/W | BUCK0_SHUTDOWN_DELAY[3:0] | | | | BUCK0_STARTUP_DELAY[3:0] | | | | |
| 0x13 | BUCK1_DELAY | R/W | BUCK1_SHUTDOWN_DELAY[3:0] | | | | BUCK1_STARTUP_DELAY[3:0] | | | | |
| 0x14 | BUCK2_DELAY | R/W | BUCK2_SHUTDOWN_DELAY[3:0] | | | | BUCK2_STARTUP_DELAY[3:0] | | | | |
| 0x15 | BUCK3_DELAY | R/W | BUCK3_SHUTDOWN_DELAY[3:0] | | | | BUCK3_STARTUP_DELAY[3:0] | | | | |
| 0x16 | GPIO2_DELAY | R/W | GPIO2_SHUTDOWN_DELAY[3:0] | | | | GPIO2_STARTUP_DELAY[3:0] | | | | |
| 0x17 | GPIO3_DELAY | R/W | GPIO3_SHUTDOWN_DELAY[3:0] | | | | GPIO3_STARTUP_DELAY[3:0] | | | | |
| 0x18 | RESET | R/W | Reserved | | | | | | | | SW_RESET |

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Register Maps (continued)
Table 9. Summary of LP87524B/J/P-Q1 Control Registers (continued)

| Addr | Register | Read / Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|------|---------------|--------------|------------------------|------------------|---------------------|-------------------|---------------------|----------------|--------------|-------------------------------|--|
| 0x19 | CONFIG | R/W | DOUBLE_DELAY | CLKIN_PD | Reserved | EN3_PD | TDIE_WARN_LEVEL | EN2_PD | EN1_PD | Reserved | |
| 0x1A | INT_TOP1 | R/W | Reserved | INT_BUCK23 | INT_BUCK01 | NO_SYNC_CLK | TDIE_SD | TDIE_WARN | INT_OVP | I_LOAD_READY | |
| 0x1B | INT_TOP2 | R/W | Reserved | | | | | | | RESET_REG | |
| 0x1C | INT_BUCK_0_1 | R/W | Reserved | BUCK1_PG_INT | BUCK1_SC_INT | BUCK1_ILIM_INT | Reserved | BUCK0_PG_INT | BUCK0_SC_INT | BUCK0_ILIM_INT | |
| 0x1D | INT_BUCK_2_3 | R/W | Reserved | BUCK3_PG_INT | BUCK3_SC_INT | BUCK3_ILIM_INT | Reserved | BUCK2_PG_INT | BUCK2_SC_INT | BUCK2_ILIM_INT | |
| 0x1E | TOP_STAT | R | Reserved | | | SYNC_CLK_STAT | TDIE_SD_STAT | TDIE_WARN_STAT | OVP_STAT | Reserved | |
| 0x1F | BUCK_0_1_STAT | R | BUCK1_STAT | BUCK1_PG_STAT | Reserved | BUCK1_ILIM_STAT | BUCK0_STAT | BUCK0_PG_STAT | Reserved | BUCK0_ILIM_STAT | |
| 0x20 | BUCK_2_3_STAT | R | BUCK3_STAT | BUCK3_PG_STAT | Reserved | BUCK3_ILIM_STAT | BUCK2_STAT | BUCK2_PG_STAT | Reserved | BUCK2_ILIM_STAT | |
| 0x21 | TOP_MASK1 | R/W | Reserved | Reserved | | SYNC_CLK_MASK | Reserved | TDIE_WARN_MASK | Reserved | I_LOAD_READY_MASK | |
| 0x22 | TOP_MASK2 | R/W | Reserved | | | | | | | RESET_REG_MASK | |
| 0x23 | BUCK_0_1_MASK | R/W | Reserved | BUCK1_PG_MASK | Reserved | BUCK1_ILIM_MASK | Reserved | BUCK0_PG_MASK | Reserved | BUCK0_ILIM_MASK | |
| 0x24 | BUCK_2_3_MASK | R/W | Reserved | BUCK3_PG_MASK | Reserved | BUCK3_ILIM_MASK | Reserved | BUCK2_PG_MASK | Reserved | BUCK2_ILIM_MASK | |
| 0x25 | SEL_I_LOAD | R/W | Reserved | | | | | | | LOAD_CURRENT_BUCK_SELECT[1:0] | |
| 0x26 | I_LOAD_2 | R | Reserved | | | | | | | BUCK_LOAD_CURRENT[9:8] | |
| 0x27 | I_LOAD_1 | R | BUCK_LOAD_CURRENT[7:0] | | | | | | | | |
| 0x28 | PGOOD_CTRL1 | R/W | PG3_SEL[1:0] | | PG2_SEL[1:0] | | PG1_SEL[1:0] | | PG0_SEL[1:0] | | |
| 0x29 | PGOOD_CTRL2 | R/W | HALF_DELAY | EN_PG0_NINT | PGOOD_SE_T_DELAY | EN_PGFLT_STAT | Reserved | PGOOD_WINDOW | PGOOD_OD | PGOOD_POL | |
| 0x2A | PGOOD_FLT | R | Reserved | | | | PG3_FLT | PG2_FLT | PG1_FLT | PG0_FLT | |
| 0x2B | PLL_CTRL | R/W | PLL_MODE[1:0] | | Reserved | EXT_CLK_FREQ[4:0] | | | | | |
| 0x2C | PIN_FUNCTION | R/W | EN_SPREAD_SPEC | EN_PIN_CTL_GPIO3 | EN_PIN_SELECT_GPIO3 | EN_PIN_CTL_GPIO2 | EN_PIN_SELECT_GPIO2 | GPIO3_SEL | GPIO2_SEL | GPIO1_SEL | |
| 0x2D | GPIO_CONFIG | R/W | Reserved | GPIO3_OD | GPIO2_OD | GPIO1_OD | Reserved | GPIO3_DIR | GPIO2_DIR | GPIO1_DIR | |
| 0x2E | GPIO_IN | R | Reserved | | | | | GPIO3_IN | GPIO2_IN | GPIO1_IN | |
| 0x2F | GPIO_OUT | R/W | Reserved | | | | | GPIO3_OUT | GPIO2_OUT | GPIO1_OUT | |

7.6.1.1 OTP_REV

Address: 0x01

Figure 22. OTP_REV Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|----|----|----|----|----|
| OTP_ID[7:0] | | | | | | | |

Table 10. OTP_REV Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-------------|------|---|--|
| 7:0 | OTP_ID[7:0] | R | 0x71 for LP87524B, 0x72 for LP87524J, 0x3B for LP87524P * | Identification code of the OTP EPROM version |

7.6.1.2 BUCK0_CTRL1

Address: 0x02

Figure 23. BUCK0_CTRL1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|------------------|--------------------------|--------------------|----------|------------|----------|----|
| EN_BUCK0 | EN_PIN_CTRL 0 | BUCK0_EN_PIN_SELECT[1:0] | EN_ROOF_ FLOOR0 | EN_RDIS0 | BUCK0_FPWM | Reserved | |

Table 11. BUCK0_CTRL1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------------------|------|--|---|
| 7 | EN_BUCK0 | R/W | 1 * | Enable Buck0 regulator: 0 - Buck0 regulator is disabled 1 - Buck0 regulator is enabled |
| 6 | EN_PIN_CTRL0 | R/W | 1 * | Enable EN1/2/3 pin control for Buck0: 0 - Only the EN_BUCK0 bit controls Buck0 1 - EN_BUCK0 bit AND ENx pin control Buck0 |
| 5:4 | BUCK0_EN_PIN_SELECT[1:0] | R/W | 0x0* | Enable EN1/2/3 pin control for Buck0: 0x0 - EN_BUCK0 bit AND EN1 pin control Buck0 0x1 - EN_BUCK0 bit AND EN2 pin control Buck0 0x2 - EN_BUCK0 bit AND EN3 pin control Buck0 0x3 - Reserved |
| 3 | EN_ROOF_ FLOOR0 | R/W | 0 | Enable Roof/Floor control of EN1/2/3 pin if EN_PIN_CTRL0 = 1: 0 - Enable/disable (1/0) control 1 - Roof/floor (1/0) control |
| 2 | EN_RDIS0 | R/W | 1 | Enable output discharge resistor when Buck0 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled |
| 1 | BUCK0_FPWM | R/W | 0 for LP87524B, LP87524J, 1 for LP87524P * | Forces the Buck0 regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation |
| 0 | Reserved | R/W | 0 * | |

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7.6.1.3 BUCK1_CTRL1

Address: 0x04

Figure 24. BUCK1_CTRL1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|------------------|--------------------------|--------------------|----------|------------|----------|----|
| EN_BUCK1 | EN_PIN_CTRL 1 | BUCK1_EN_PIN_SELECT[1:0] | EN_ROOF_ FLOOR1 | EN_RDIS1 | BUCK1_FPWM | Reserved | |

Table 12. BUCK1_CTRL1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------------------|------|---|---|
| 7 | EN_BUCK1 | R/W | 1 * | Enable Buck1 regulator: 0 - Buck1 regulator is disabled 1 - Buck1 regulator is enabled |
| 6 | EN_PIN_CTRL1 | R/W | 1 * | Enable EN1/2/3 pin control for Buck1: 0 - Only EN_BUCK1 bit controls Buck1 1 - EN_BUCK1 bit AND ENx pin control Buck1 |
| 5:4 | BUCK1_EN_PIN_SELECT[1:0] | R/W | 0x0* | Enable EN1/2/3 pin control for Buck1: 0x0 - EN_BUCK1 bit AND EN1 pin control Buck1 0x1 - EN_BUCK1 bit AND EN2 pin control Buck1 0x2 - EN_BUCK1 bit AND EN3 pin control Buck1 0x3 - Reserved |
| 3 | EN_ROOF_ FLOOR1 | R/W | 0 | Enable Roof/Floor control of EN1/2/3 pin if EN_PIN_CTRL1 = 1: 0 - Enable/Disable (1/0) control 1 - Roof/Floor (1/0) control |
| 2 | EN_RDIS1 | R/W | 1 | Enable output discharge resistor when Buck1 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled |
| 1 | BUCK1_FPWM | R/W | 0 for LP87524B, LP87524J, 1 for LP87524P * | Forces the Buck1 regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation |
| 0 | Reserved | R/W | 0 | |

7.6.1.4 BUCK2_CTRL1

Address: 0x06

Figure 25. BUCK2_CTRL1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|------------------|--------------------------|--------------------|----------|------------|----------|----|
| EN_BUCK2 | EN_PIN_CTRL 2 | BUCK2_EN_PIN_SELECT[1:0] | EN_ROOF_ FLOOR2 | EN_RDIS2 | BUCK2_FPWM | Reserved | |

Table 13. BUCK2_CTRL1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------------------|------|---------|---|
| 7 | EN_BUCK2 | R/W | 1 * | Enable Buck2 regulator: 0 - Buck2 regulator is disabled 1 - Buck2 regulator is enabled |
| 6 | EN_PIN_CTRL2 | R/W | 1 * | Enable EN1/2/3 pin control for Buck2: 0 - Only EN_BUCK2 bit controls Buck2 1 - EN_BUCK2 bit AND ENx pin control Buck2 |
| 5:4 | BUCK2_EN_PIN_SELECT[1:0] | R/W | 0x0* | Enable EN1/2/3 pin control for Buck2: 0x0 - EN_BUCK2 bit AND EN1 pin control Buck2 0x1 - EN_BUCK2 bit AND EN2 pin control Buck2 0x2 - EN_BUCK2 bit AND EN3 pin control Buck2 0x3 - Reserved |
| 3 | EN_ROOF_ FLOOR2 | R/W | 0 | Enable Roof/Floor control of EN1/2/3 pin if EN_PIN_CTRL2 = 1: 0 - Enable/Disable (1/0) control 1 - Roof/Floor (1/0) control |
| 2 | EN_RDIS2 | R/W | 1 | Enable output discharge resistor when Buck2 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled |
| 1 | BUCK2_FPWM | R/W | 1 * | Forces the Buck2 regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode) 1 - Forced to PWM operation |
| 0 | Reserved | R/W | 0 * | |

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7.6.1.5 BUCK3_CTRL1

Address: 0x08

Figure 26. BUCK3_CTRL1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|------------------|--------------------------|--------------------|----------|------------|----------|----|
| EN_BUCK3 | EN_PIN_CTRL 3 | BUCK3_EN_PIN_SELECT[1:0] | EN_ROOF_ FLOOR3 | EN_RDIS3 | BUCK3_FPWM | Reserved | |

Table 14. BUCK3_CTRL1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------------------|------|---------|---|
| 7 | EN_BUCK3 | R/W | 1 * | Enable Buck3 regulator: 0 - Buck3 regulator is disabled 1 - Buck3 regulator is enabled |
| 6 | EN_PIN_CTRL3 | R/W | 1 * | Enable EN1/2/3 pin control for Buck3: 0 - Only EN_BUCK3 bit controls Buck3 1 - EN_BUCK3 bit AND ENx pin control Buck3 |
| 5:4 | BUCK3_EN_PIN_SELECT[1:0] | R/W | 0x0* | Enable EN1/2/3 pin control for Buck3: 0x0 - EN_BUCK3 bit AND EN1 pin control Buck3 0x1 - EN_BUCK3 bit AND EN2 pin control Buck3 0x2 - EN_BUCK3 bit AND EN3 pin control Buck3 0x3 - Reserved |
| 3 | EN_ROOF_ FLOOR3 | R/W | 0 | Enable Roof/Floor control of EN1/2/3 pin if EN_PIN_CTRL3 = 1: 0 - Enable/Disable (1/0) control 1 - Roof/Floor (1/0) control |
| 2 | EN_RDIS3 | R/W | 1 | Enable output discharge resistor when Buck3 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled |
| 1 | BUCK3_FPWM | R/W | 1 * | Forces the Buck3 regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode) 1 - Forced to PWM operation |
| 0 | Reserved | R/W | 0 | |

7.6.1.6 BUCK0_VOUT

Address: 0x0A

Figure 27. BUCK0_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|----|----|----|----|----|----|----|
| BUCK0_VSET[7:0] | | | | | | | |

Table 15. BUCK0_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|--|--|
| 7:0 | BUCK0_VSET[7:0] | R/W | 0xFC for LP87524B, LP87524J, 0x4D for LP87524P * | Sets the output voltage of Buck0 regulator Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6 V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.7 BUCK0_FLOOR_VOUT

Address: 0x0B

Figure 28. BUCK0_FLOOR_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|----|----|----|----|----|----|----|
| BUCK0_FLOOR_VSET[7:0] | | | | | | | |

Table 16. BUCK0_FLOOR_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------------|------|---------|--|
| 7:0 | BUCK0_FLOOR_VSET[7:0] | R/W | 0x00 | Sets the output voltage of Buck0 regulator when floor state is used: Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6 V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.8 BUCK1_VOUT

Address: 0x0C

Figure 29. BUCK1_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|----|----|----|----|----|----|----|
| BUCK1_VSET[7:0] | | | | | | | |

Table 17. BUCK1_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|---------|---|
| 7:0 | BUCK1_VSET[7:0] | R/W | 0x75* | Sets the output voltage of Buck1 regulator: Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6 V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.9 BUCK1_FLOOR_VOUT

Address: 0x0D

Figure 30. BUCK1_FLOOR_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|----|----|----|----|----|----|----|
| BUCK1_FLOOR_VSET[7:0] | | | | | | | |

Table 18. BUCK1_FLOOR_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------------|------|---------|--|
| 7:0 | BUCK1_FLOOR_VSET[7:0] | R/W | 0x00 | Sets the output voltage of Buck1 regulator when floor state is used: Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6 V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.10 BUCK2_VOUT

Address: 0x0E

Figure 31. BUCK2_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|----|----|----|----|----|----|----|
| BUCK2_VSET[7:0] | | | | | | | |

Table 19. BUCK2_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|--|--|
| 7:0 | BUCK2_VSET[7:0] | R/W | 0xB1 for LP87524B, 0x4D for LP87524J, LP87524P * | Sets the output voltage of Buck2 regulator: Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.11 BUCK2_FLOOR_VOUT

Address: 0x0F

Figure 32. BUCK2_FLOOR_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|----|----|----|----|----|----|----|
| BUCK2_FLOOR_VSET[7:0] | | | | | | | |

Table 20. BUCK2_FLOOR_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------------|------|---------|--|
| 7:0 | BUCK2_FLOOR_VSET[7:0] | R/W | 0x00 | Sets the output voltage of Buck2 regulator when floor state is used: Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6 V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.12 BUCK3_VOUT

Address: 0x10

Figure 33. BUCK3_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|----|----|----|----|----|----|----|
| BUCK3_VSET[7:0] | | | | | | | |

Table 21. BUCK3_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|---|---|
| 7:0 | BUCK3_VSET[7:0] | R/W | 0xCA for LP87524B, LP87524J, 0xB1 for LP87524P* | Sets the output voltage of Buck3 regulator: Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6 V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.13 BUCK3_FLOOR_VOUT

Address: 0x11

Figure 34. BUCK3_FLOOR_VOUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|----|----|----|----|----|----|----|
| BUCK3_FLOOR_VSET[7:0] | | | | | | | |

Table 22. BUCK3_FLOOR_VOUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------------|------|---------|--|
| 7:0 | BUCK3_FLOOR_VSET[7:0] | R/W | 0x00 | Sets the output voltage of Buck3 regulator when Floor state is used: Reserved, DO NOT USE 0x00...0x09 0.6 V - 0.73 V, 10 mV steps 0x0A - 0.6 V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V If the input voltage is above 4 V, do not use output voltages below 1.0 V. |

7.6.1.14 BUCK0_DELAY

Address: 0x12

Figure 35. BUCK0_DELAY Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| BUCK0_SHUTDOWN_DELAY[3:0] | | | | BUCK0_STARTUP_DELAY[3:0] | | | |

Table 23. BUCK0_DELAY Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------------------|------|---|--|
| 7:4 | BUCK0_SHUTDOWN_DELAY[3:0] | R/W | 0x0 for LP87524B, LP87524J, 0x1 for LP87524P * | Shutdown delay of Buck0 from falling edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |
| 3:0 | BUCK0_STARTUP_DELAY[3:0] | R/W | 0x5 for LP87524B, LP87524J, 0x3 for LP87524P * | Start-up delay of Buck0 from rising edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |

7.6.1.15 BUCK1_DELAY

Address: 0x13

Figure 36. BUCK1_DELAY Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| BUCK1_SHUTDOWN_DELAY[3:0] | | | | BUCK1_STARTUP_DELAY[3:0] | | | |

Table 24. BUCK1_DELAY Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------------------|------|---|--|
| 7:4 | BUCK1_SHUTDOWN_DELAY[3:0] | R/W | 0x0 for LP87524B, LP87524J, 0x1 for LP87524P * | Shutdown delay of Buck1 from falling edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |
| 3:0 | BUCK1_STARTUP_DELAY[3:0] | R/W | 0x5 for LP87524B, LP87524J, 0x7 for LP87524P * | start-up delay of Buck1 from rising edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |

7.6.1.16 BUCK2_DELAY

Address: 0x14

Figure 37. BUCK2_DELAY Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| BUCK2_SHUTDOWN_DELAY[3:0] | | | | BUCK2_STARTUP_DELAY[3:0] | | | |

Table 25. BUCK2_DELAY Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------------------|------|---|--|
| 7:4 | BUCK2_SHUTDOWN_DELAY[3:0] | R/W | 0x0 for LP87524B, LP87524J, 0x1 for LP87524P * | Shutdown delay of Buck2 from falling edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |

Table 25. BUCK2_DELAY Register Field Descriptions (continued)

| Bits | Field | Type | Default | Description |
|------|--------------------------|------|--|--|
| 3:0 | BUCK2_STARTUP_DELAY[3:0] | R/W | 0x2 for LP87524B, LP87524J, 0x5 for LP87524P * | start-up delay of Buck2 from rising edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |

7.6.1.17 BUCK3_DELAY

Address: 0x15

Figure 38. BUCK3_DELAY Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| BUCK3_SHUTDOWN_DELAY[3:0] | | | | BUCK3_STARTUP_DELAY[3:0] | | | |

Table 26. BUCK3_DELAY Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------------------|------|---------|--|
| 7:4 | BUCK3_SHUTDOWN_DELAY[3:0] | R/W | 0x1* | Shutdown delay of Buck3 from falling edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |
| 3:0 | BUCK3_STARTUP_DELAY[3:0] | R/W | 0x0* | Startup delay of Buck3 from rising edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |

7.6.1.18 GPIO2_DELAY

Address: 0x16

Figure 39. GPIO2_DELAY Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| GPIO2_SHUTDOWN_DELAY[3:0] | | | | GPIO2_STARTUP_DELAY[3:0] | | | |

Table 27. GPIO2_DELAY Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------------------|------|---|---|
| 7:4 | GPIO2_SHUTDOWN_DELAY[3:0] | R/W | 0x0 for LP87524B, LP87524J, 0x1 for LP87524P* | Delay for GPIO2 falling edge from falling edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |
| 3:0 | GPIO2_STARTUP_DELAY[3:0] | R/W | 0x5 for LP87524B, LP87524J, 0x9 for LP87524P* | Delay for GPIO2 rising edge from rising edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |

7.6.1.19 GPIO3_DELAY

Address: 0x17

Figure 40. GPIO3_DELAY Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| GPIO3_SHUTDOWN_DELAY[3:0] | | | | GPIO3_STARTUP_DELAY[3:0] | | | |

Table 28. GPIO3_DELAY Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------------------|------|--|---|
| 7:4 | GPIO3_SHUTDOWN_DELAY[3:0] | R/W | 0x0 * | Delay for GPIO3 falling edge from falling edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |
| 3:0 | GPIO3_STARTUP_DELAY[3:0] | R/W | 0x3 for LP87524B, LP87524J, 0xD for LP87524P * | Delay for GPIO3 rising edge from rising edge of ENx signal (DOUBLE_DELAY = 0 in CONTROL register and HALF_DELAY = 0 in PGOOD_CTRL2 register. See other delay options in Table 4): 0x0 - 0 ms 0x1 - 1 ms ... 0xF - 15 ms |

7.6.1.20 RESET

Address: 0x18

Figure 41. RESET Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|----|----|----|----------|
| Reserved | | | | | | | SW_RESET |

Table 29. RESET Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|----------|------|---------|--|
| 7:1 | Reserved | R/W | 0x00 | |
| 0 | SW_RESET | R/W | 0 | Software commanded reset. When written to 1, the registers are reset to default values, OTP memory is read, and the I ² C interface is reset. The bit is automatically cleared. |

7.6.1.21 CONFIG

Address: 0x19

Figure 42. CONFIG Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|----------|--------|--------|-----------------|--------|--------|----------|
| DOUBLE_DELAY | CLKIN_PD | EN4_PD | EN3_PD | TDIE_WARN_LEVEL | EN2_PD | EN1_PD | Reserved |

Table 30. CONFIG Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|--|--|
| 7 | DOUBLE_DELAY | R/W | 0 * | Start-up and shutdown delays from ENx signals: 0 - 0 ms - 15 ms with 1-ms steps 1 - 0 ms - 30 ms with 2-ms steps |
| 6 | CLKIN_PD | R/W | 1 * | Selects the pulldown resistor on the CLKIN input pin: 0 - Pulldown resistor is disabled. 1 - Pulldown resistor is enabled. |
| 5 | Reserved | R/W | 0 * | |
| 4 | EN3_PD | R/W | 0 * | Selects the pulldown resistor on the EN3 (GPIO3) input pin: 0 - Pulldown resistor is disabled. 1 - Pulldown resistor is enabled. |
| 3 | TDIE_WARN_LEVEL | R/W | 1 for LP87524B, LP87524J, 0 for LP87524P * | Thermal warning threshold level: 0 - 125°C 1 - 137°C. |

Table 30. CONFIG Register Field Descriptions (continued)

| Bits | Field | Type | Default | Description |
|------|----------|------|---------|--|
| 2 | EN2_PD | R/W | 0 * | Selects the pull down resistor on the EN2 (GPIO2) input pin: 0 - Pulldown resistor is disabled. 1 - Pull-down resistor is enabled. |
| 1 | EN1_PD | R/W | 1 * | Selects the pull down resistor on the EN1 (GPIO1) input pin: 0 - Pulldown resistor is disabled. 1 - Pulldown resistor is enabled. |
| 0 | Reserved | R/W | 0 | |

7.6.1.22 INT_TOP1

Address: 0x1A

Figure 43. INT_TOP1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|------------|------------|-------------|---------|-----------|---------|--------------|
| Reserved | INT_BUCK23 | INT_BUCK01 | NO_SYNC_CLK | TDIE_SD | TDIE_WARN | INT_OVP | I_LOAD_READY |

Table 31. INT_TOP1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------|------|---------|--|
| 7 | Reserved | R/W | 0 | |
| 6 | INT_BUCK23 | R | 0 | Interrupt indicating that output Buck3 and/or Buck2 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK_2_3 register. This bit is cleared automatically when INT_BUCK_2_3 register is cleared to 0x00. |
| 5 | INT_BUCK01 | R | 0 | Interrupt indicating that output Buck1 and/or Buck0 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK_0_1 register. This bit is cleared automatically when INT_BUCK_0_1 register is cleared to 0x00. |
| 4 | NO_SYNC_CLK | R/W | 0 | Latched status bit indicating that the external clock is not valid. Write 1 to clear interrupt. |
| 3 | TDIE_SD | R/W | 0 | Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The regulators have been disabled if they were enabled. The regulators cannot be enabled if this bit is active. The actual status of the thermal warning is indicated by TDIE_SD_STAT bit in TOP_STAT register. Write 1 to clear interrupt. |
| 2 | TDIE_WARN | R/W | 0 | Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TDIE_WARN_STAT bit in TOP_STAT register. Write 1 to clear interrupt. |
| 1 | INT_OVP | R/W | 0 | Latched status bit indicating that the input voltage has exceeded the overvoltage detection level. The actual status of the overvoltage is indicated by OVP_STAT bit in TOP_STAT register. Write 1 to clear interrupt. |
| 0 | I_LOAD_READY | R/W | 0 | Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt. |

7.6.1.23 INT_TOP2

Address: 0x1B

Figure 44. INT_TOP2 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|----|----|----|-----------|
| Reserved | | | | | | | RESET_REG |

Table 32. INT_TOP2 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------|------|---------|---|
| 7:1 | Reserved | R/W | 0x00 | |
| 0 | RESET_REG | R/W | 0 | Latched status bit indicating that either start-up (NRST rising edge) is done, VANA supply voltage has been below undervoltage threshold level, or the host has requested a reset (SW_RESET bit in RESET register). The regulators have been disabled, and registers are reset to default values and the normal start-up procedure is done. Write 1 to clear interrupt. |

7.6.1.24 INT_BUCK_0_1

Address: 0x1C

Figure 45. INT_BUCK_0_1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|--------------|--------------|----------------|----------|--------------|--------------|----------------|
| Reserved | BUCK1_PG_INT | BUCK1_SC_INT | BUCK1_ILIM_INT | Reserved | BUCK0_PG_INT | BUCK0_SC_INT | BUCK0_ILIM_INT |

Table 33. INT_BUCK_0_1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|----------------|------|---------|--|
| 7 | Reserved | R/W | 0 | |
| 6 | BUCK1_PG_INT | R/W | 0 | Latched status bit indicating that Buck1 output voltage has reached Power-Good-threshold level. Write 1 to clear. |
| 5 | BUCK1_SC_INT | R/W | 0 | Latched status bit indicating that the Buck1 output voltage has fallen below 0.35-V level during operation or Buck1 output did not reach 0.35-V level in 1 ms from enable. Write 1 to clear. |
| 4 | BUCK1_ILIM_INT | R/W | 0 | Latched status bit indicating that output current limit has been active. Write 1 to clear. |
| 3 | Reserved | R/W | 0 | |
| 2 | BUCK0_PG_INT | R/W | 0 | Latched status bit indicating that Buck0 output voltage has reached Power-Good-threshold level. Write 1 to clear. |
| 1 | BUCK0_SC_INT | R/W | 0 | Latched status bit indicating that the Buck0 output voltage has fallen below 0.35-V level during operation or Buck0 output did not reach 0.35-V level in 1 ms from enable. Write 1 to clear. |
| 0 | BUCK0_ILIM_INT | R/W | 0 | Latched status bit indicating that output current limit has been active. Write 1 to clear. |

7.6.1.25 INT_BUCK_2_3

Address: 0x1D

Figure 46. INT_BUCK_2_3 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|--------------|--------------|----------------|----------|--------------|--------------|----------------|
| Reserved | BUCK3_PG_INT | BUCK3_SC_INT | BUCK3_ILIM_INT | Reserved | BUCK2_PG_INT | BUCK2_SC_INT | BUCK2_ILIM_INT |

Table 34. INT_BUCK_2_3 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------|------|---------|--|
| 7 | Reserved | R/W | 0 | |
| 6 | BUCK3_PG_INT | R/W | 0 | Latched status bit indicating that Buck3 output voltage has reached Power-Good-threshold level. Write 1 to clear. |
| 5 | BUCK3_SC_INT | R/W | 0 | Latched status bit indicating that the Buck3 output voltage has fallen below 0.35-V level during operation or Buck3 output did not reach 0.35-V level in 1 ms from enable. Write 1 to clear. |

Table 34. INT_BUCK_2_3 Register Field Descriptions (continued)

| Bits | Field | Type | Default | Description |
|------|----------------|------|---------|--|
| 4 | BUCK3_ILIM_INT | R/W | 0 | Latched status bit indicating that output current limit has been active. Write 1 to clear. |
| 3 | Reserved | R/W | 0 | |
| 2 | BUCK2_PG_INT | R/W | 0 | Latched status bit indicating that Buck2 output voltage has reached Power-Good-threshold level. Write 1 to clear. |
| 1 | BUCK2_SC_INT | R/W | 0 | Latched status bit indicating that the Buck2 output voltage has fallen below 0.35-V level during operation or Buck2 output did not reach 0.35-V level in 1 ms from enable. Write 1 to clear. |
| 0 | BUCK2_ILIM_INT | R/W | 0 | Latched status bit indicating that output current limit has been active. Write 1 to clear. |

7.6.1.26 TOP_STAT

Address: 0x1E

Figure 47. TOP_STAT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|---------------|--------------|----------------|----------|----------|
| Reserved | | | SYNC_CLK_STAT | TDIE_SD_STAT | TDIE_WARN_STAT | OVP_STAT | Reserved |

Table 35. TOP_STAT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|----------------|------|---------|---|
| 7:5 | Reserved | R | 0x0 | |
| 4 | SYNC_CLK_STAT | R | 0 | Status bit indicating the status of external clock (CLKIN): 0 - External clock frequency is valid 1 - External clock frequency is not valid |
| 3 | TDIE_SD_STAT | R | 0 | Status bit indicating the status of thermal shutdown: 0 - Die temperature below thermal shutdown level 1 - Die temperature above thermal shutdown level |
| 2 | TDIE_WARN_STAT | R | 0 | Status bit indicating the status of thermal warning: 0 - Die temperature below thermal warning level 1 - Die temperature above thermal warning level |
| 1 | OVP_STAT | R | 0 | Status bit indicating the status of input overvoltage monitoring: 0 - Input voltage below overvoltage threshold level 1 - Input voltage above overvoltage threshold level |
| 0 | Reserved | R | 0 | |

7.6.1.27 BUCK_0_1_STAT

Address: 0x1F

Figure 48. BUCK_0_1_STAT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|---------------|----------|-----------------|------------|---------------|----------|-----------------|
| BUCK1_STAT | BUCK1_PG_STAT | Reserved | BUCK1_ILIM_STAT | BUCK0_STAT | BUCK0_PG_STAT | Reserved | BUCK0_ILIM_STAT |

Table 36. BUCK_0_1_STAT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------|------|---------|--|
| 7 | BUCK1_STAT | R | 0 | Status bit indicating the enable/disable status of Buck1: 0 - Buck1 regulator is disabled 1 - Buck1 regulator is enabled |
| 6 | BUCK1_PG_STAT | R | 0 | Status bit indicating Buck1 output voltage validity (raw status) 0 - Buck1 output is below Power-Good-threshold level 1 - Buck1 output is above Power-Good-threshold level |

Table 36. BUCK_0_1_STAT Register Field Descriptions (continued)

| Bits | Field | Type | Default | Description |
|------|-----------------|------|---------|---|
| 5 | Reserved | R | 0 | |
| 4 | BUCK1_ILIM_STAT | R | 0 | Status bit indicating Buck1 current limit status (raw status) 0 - Buck1 output current is below current limit level 1 - Buck1 output current limit is active |
| 3 | BUCK0_STAT | R | 0 | Status bit indicating the enable/disable status of Buck0: 0 - Buck0 regulator is disabled 1 - Buck0 regulator is enabled |
| 2 | BUCK0_PG_STAT | R | 0 | Status bit indicating Buck0 output voltage validity (raw status): 0 - Buck0 output is below Power-Good-threshold level 1 - Buck0 output is above Power-Good-threshold level |
| 1 | Reserved | R | 0 | |
| 0 | BUCK0_ILIM_STAT | R | 0 | Status bit indicating Buck0 current limit status (raw status): 0 - Buck0 output current is below current limit level 1 - Buck0 output current limit is active |

7.6.1.28 BUCK_2_3_STAT

Address: 0x20

Figure 49. BUCK_2_3_STAT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|---------------|----------|-----------------|------------|---------------|----------|-----------------|
| BUCK3_STAT | BUCK3_PG_STAT | Reserved | BUCK3_ILIM_STAT | BUCK2_STAT | BUCK2_PG_STAT | Reserved | BUCK2_ILIM_STAT |

Table 37. BUCK_2_3_STAT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|---------|---|
| 7 | BUCK3_STAT | R | 0 | Status bit indicating the enable/disable status of Buck3: 0 - Buck3 regulator is disabled 1 - Buck3 regulator is enabled |
| 6 | BUCK3_PG_STAT | R | 0 | Status bit indicating Buck3 output voltage validity (raw status): 0 - Buck3 output is below Power-Good-threshold level 1 - Buck3 output is above Power-Good-threshold level |
| 5 | Reserved | R | 0 | |
| 4 | BUCK3_ILIM_STAT | R | 0 | Status bit indicating Buck3 current limit status (raw status): 0 - Buck3 output current is below current limit level 1 - Buck3 output current limit is active |
| 3 | BUCK2_STAT | R | 0 | Status bit indicating the enable/disable status of Buck2: 0 - Buck2 regulator is disabled 1 - Buck2 regulator is enabled |
| 2 | BUCK2_PG_STAT | R | 0 | Status bit indicating Buck2 output voltage validity (raw status): 0 - Buck2 output is below Power-Good-threshold level 1 - Buck2 output is above Power-Good-threshold level |
| 1 | Reserved | R | 0 | |
| 0 | BUCK2_ILIM_STAT | R | 0 | Status bit indicating Buck2 current limit status (raw status): 0 - Buck2 output current is below current limit level 1 - Buck2 output current limit is active |

7.6.1.29 TOP_MASK1

Address: 0x21

Figure 50. TOP_MASK1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----------|----|---------------|----------|----------------|----------|-------------------|
| Reserved | Reserved | | SYNC_CLK_MASK | Reserved | TDIE_WARN_MASK | Reserved | I_LOAD_READY_MASK |

Table 38. TOP_MASK1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-------------------|------|---------|---|
| 7 | Reserved | R/W | 1 * | |
| 6:5 | Reserved | R/W | 0x0 | |
| 4 | SYNC_CLK_MASK | R/W | 0 * | Masking for external clock detection interrupt (NO_SYNC_CLK in INT_TOP1 register): 0 - Interrupt generated 1 - Interrupt not generated |
| 3 | Reserved | R/W | 0 | |
| 2 | TDIE_WARN_MASK | R/W | 0 * | Masking for thermal warning interrupt (TDIE_WARN in INT_TOP1 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect TDIE_WARN_STAT status bit in TOP_STAT register. |
| 1 | Reserved | R/W | 0 | |
| 0 | I_LOAD_READY_MASK | R/W | 1 * | Masking for load current measurement ready interrupt (I_LOAD_READY in INT_TOP register). 0 - Interrupt generated 1 - Interrupt not generated |

7.6.1.30 TOP_MASK2

Address: 0x22

Figure 51. TOP_MASK2 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|----|----|----|----------------|
| Reserved | | | | | | | RESET_REG_MASK |

Table 39. TOP_MASK2 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|----------------|------|---------|--|
| 7:1 | Reserved | R/W | 0x00 | |
| 0 | RESET_REG_MASK | R/W | 1 * | Masking for register reset interrupt (RESET_REG in INT_TOP2 register): 0 - Interrupt generated 1 - Interrupt not generated |

7.6.1.31 BUCK_0_1_MASK

Address: 0x23

Figure 52. BUCK_0_1_MASK Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|---------------|----------|-----------------|----------|---------------|----------|-----------------|
| Reserved | BUCK1_PG_MASK | Reserved | BUCK1_ILIM_MASK | Reserved | BUCK0_PG_MASK | Reserved | BUCK0_ILIM_MASK |

Table 40. BUCK_0_1_MASK Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|---------|--|
| 7 | Reserved | R/W | 0 | |
| 6 | BUCK1_PG_MASK | R/W | 1 * | Masking for Buck1 Power-Good interrupt (BUCK1_PG_INT in INT_BUCK_0_1 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK1_PG_STAT status bit in BUCK_0_1_STAT register. |
| 5 | Reserved | R | 0 | |
| 4 | BUCK1_ILIM_MASK | R/W | 1 * | Masking for Buck1 current-limit-detection interrupt (BUCK1_ILIM_INT in INT_BUCK_0_1 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK1_ILIM_STAT status bit in BUCK_0_1_STAT register. |

Table 40. BUCK_0_1_MASK Register Field Descriptions (continued)

| Bits | Field | Type | Default | Description |
|------|-----------------|------|---------|--|
| 3 | Reserved | R/W | 0 | |
| 2 | BUCK0_PG_MASK | R/W | 1 * | Masking for Buck0 Power-Good interrupt (BUCK0_PG_INT in INT_BUCK_0_1 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK0_PG_STAT status bit in BUCK_0_1_STAT register. |
| 1 | Reserved | R | 0 | |
| 0 | BUCK0_ILIM_MASK | R/W | 1 * | Masking for Buck0 current-limit-detection interrupt (BUCK0_ILIM_INT in INT_BUCK_0_1 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK0_ILIM_STAT status bit in BUCK_0_1_STAT register. |

7.6.1.32 BUCK_2_3_MASK

Address: 0x24

Figure 53. BUCK_2_3_MASK Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|---------------|----------|-----------------|----------|---------------|----------|-----------------|
| Reserved | BUCK3_PG_MASK | Reserved | BUCK3_ILIM_MASK | Reserved | BUCK2_PG_MASK | Reserved | BUCK2_ILIM_MASK |

Table 41. BUCK_2_3_MASK Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|---------|--|
| 7 | Reserved | R/W | 0 | |
| 6 | BUCK3_PG_MASK | R/W | 1 * | Masking for Buck3 Power-Good interrupt (BUCK3_PG_INT in INT_BUCK_2_3 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK3_PG_STAT status bit in BUCK_2_3_STAT register. |
| 5 | Reserved | R | 0 | |
| 4 | BUCK3_ILIM_MASK | R/W | 1 * | Masking for Buck3 current-limit-detection interrupt (BUCK3_ILIM_INT in INT_BUCK_2_3 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK3_ILIM_STAT status bit in BUCK_2_3_STAT register. |
| 3 | Reserved | R/W | 0 | |
| 2 | BUCK2_PG_MASK | R/W | 1 * | Masking for Buck2 Power-Good interrupt (BUCK2_PG_INT in INT_BUCK_2_3 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK2_PG_STAT status bit in BUCK_2_3_STAT register. |
| 1 | Reserved | R | 0 | |
| 0 | BUCK2_ILIM_MASK | R/W | 1 * | Masking for Buck2 current limit-detection interrupt (BUCK2_ILIM_INT in INT_BUCK_2_3 register): 0 - Interrupt generated 1 - Interrupt not generated This bit does not affect BUCK2_ILIM_STAT status bit in BUCK_2_3_STAT register. |

7.6.1.33 SEL_I_LOAD

Address: 0x25

Figure 54. SEL_I_LOAD Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|----|----|-------------------------------|----|
| Reserved | | | | | | LOAD_CURRENT_BUCK_SELECT[1:0] | |

Table 42. SEL_I_LOAD Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------------------------|------|---------|---|
| 7:2 | Reserved | R/W | 0x00 | |
| 1:0 | LOAD_CURRENT_BUCK_SELECT [1:0] | R/W | 0x0 | Start the current measurement on the selected regulator: 0x0 - Buck0 0x1 - Buck1 0x2 - Buck2 0x3 - Buck3 A single measurement is started when register is written. |

7.6.1.34 I_LOAD_2

Address: 0x26

Figure 55. I_LOAD_2 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|----|----|------------------------|----|
| Reserved | | | | | | BUCK_LOAD_CURRENT[9:8] | |

Table 43. I_LOAD_2 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|------------------------|------|---------|--|
| 7:2 | Reserved | R | 0x00 | |
| 1:0 | BUCK_LOAD_CURRENT[9:8] | R | 0x0 | This register describes 3 MSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and max code corresponding to 20.47-A current. |

7.6.1.35 I_LOAD_1

Address: 0x27

Figure 56. I_LOAD_1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|----|----|----|----|----|----|----|
| BUCK_LOAD_CURRENT[7:0] | | | | | | | |

Table 44. I_LOAD_1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|------------------------|------|---------|--|
| 7:0 | BUCK_LOAD_CURRENT[7:0] | R | 0x00 | This register describes 8 LSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and max code corresponding to a 20.47-A current. |

7.6.1.36 PGOOD_CTRL1

Address: 0x28

Figure 57. PGOOD_CTRL1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|----|--------------|----|--------------|----|--------------|----|
| PG3_SEL[1:0] | | PG2_SEL[1:0] | | PG1_SEL[1:0] | | PG0_SEL[1:0] | |

Table 45. PGOOD_CTRL1 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|--------------|------|---------|--|
| 7:6 | PG3_SEL[1:0] | R/W | 0x1* | PGOOD signal source control from Buck3 0x0 - Masked 0x1 - Power-Good-threshold voltage 0x2 - Reserved, do not use 0x3 - Power-Good-threshold voltage AND current limit |
| 5:4 | PG2_SEL[1:0] | R/W | 0x1* | PGOOD signal source control from Buck2 0x0 - Masked 0x1 - Power-Good-threshold voltage 0x2 - Reserved, do not use 0x3 - Power-Good threshold voltage AND current limit |
| 3:2 | PG1_SEL[1:0] | R/W | 0x1* | PGOOD signal source control from Buck1 0x0 - Masked 0x1 - Power-Good-threshold voltage 0x2 - Reserved, do not use 0x3 - Power-Good-threshold voltage AND current limit |
| 1:0 | PG0_SEL[1:0] | R/W | 0x1* | PGOOD signal source control from Buck0 0x0 - Masked 0x1 - Power-Good-threshold voltage 0x2 - Reserved, do not use 0x3 - Power-Good-threshold voltage AND current limit |

7.6.1.37 PGOOD_CTRL2

Address: 0x29

Figure 58. PGOOD_CTRL2 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-------------|-----------------|---------------|----------|--------------|----------|-----------|
| HALF_DELAY | EN_PGO_NINT | PGOOD_SET_DELAY | EN_PGFLT_STAT | Reserved | PGOOD_WINDOW | PGOOD_OD | PGOOD_POL |

Table 46. PGOOD_CTRL2 Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------------|------|--|--|
| 7 | HALF_DELAY | R/W | 0 for LP87524B, LP87524J, 1 for LP87524P * | Select the time step for start-up and shutdown delays: 0 - Start-up and shutdown delays have 0.5-ms or 1-ms time steps, based on DOUBLE_DELAY bit in CONFIG register. 1 - Start-up and shutdown delays have 0.32-ms or 0.64-ms time steps, based on DOUBLE_DELAY bit in CONFIG register. |
| 6 | EN_PGO_NINT | R/W | 0 * | Combine Buck0 PGOOD signal to nINT signal: 0 - Buck0 PGOOD signal not included to nINT signal 1 - Buck0 PGOOD signal included to nINT signal. If nINT OR Buck0 PGOOD is low then nINT signal is low. |
| 5 | PGOOD_SET_DELAY | R/W | 1 * | Debounce time of output voltage monitoring for PGOOD signal (only when PGOOD signal goes valid): 0 - 4-10 μ s 1 - 11 ms |
| 4 | EN_PGFLT_STAT | R/W | 0 * | Operation mode for PGOOD signal: 0 - Indicates live status of monitored voltage outputs. 1 - Indicates status of PGOOD_FLT register, inactive if at least one of PGx_FLT bit is inactive. |
| 3 | Reserved | R/W | 0 | |
| 2 | PGOOD_WINDOW | R/W | 1 * | Voltage monitoring method for PGOOD signal: 0 - Only undervoltage monitoring 1 - Overvoltage and undervoltage monitoring |
| 1 | PGOOD_OD | R/W | 1 * | PGOOD signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output |
| 0 | PGOOD_POL | R/W | 0 * | PGOOD signal polarity: 0 - PGOOD signal high when monitored outputs are valid 1 - PGOOD signal low when monitored outputs are valid |

7.6.1.38 PGOOD_FLT

Address: 0x2A

Figure 59. PGOOD_FLT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|---------|---------|---------|---------|
| Reserved | | | | PG3_FLT | PG2_FLT | PG1_FLT | PG0_FLT |

Table 47. PGOOD_FLT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|----------|------|---------|--|
| 7:4 | Reserved | R/W | 0x0 | |
| 3 | PG3_FLT | R | 0 | Source for PGOOD inactive signal: 0 - Buck3 has not set PGOOD signal inactive. 1 - Buck3 has set PGOOD signal inactive. This bit can be cleared by reading this register when Buck3 output is valid. |
| 2 | PG2_FLT | R | 0 | Source for PGOOD inactive signal: 0 - Buck2 has not set PGOOD signal inactive. 1 - Buck2 has set PGOOD signal inactive. This bit can be cleared by reading this register when Buck2 output is valid. |

Table 47. PGOOD_FLT Register Field Descriptions (continued)

| Bits | Field | Type | Default | Description |
|------|---------|------|---------|--|
| 1 | PG1_FLT | R | 0 | Source for PGOOD inactive signal: 0 - Buck1 has not set PGOOD signal inactive. 1 - Buck1 has set PGOOD signal inactive. This bit can be cleared by reading this register when Buck1 output is valid. |
| 0 | PG0_FLT | R | 0 | Source for PGOOD inactive signal: 0 - Buck0 has not set PGOOD signal inactive. 1 - Buck0 has set PGOOD signal inactive. This bit can be cleared by reading this register when Buck0 output is valid. |

7.6.1.39 PLL_CTRL

Address: 0x2B

Figure 60. PLL_CTRL Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|----|----------|-------------------|----|----|----|----|
| PLL_MODE[1:0] | | Reserved | EXT_CLK_FREQ[4:0] | | | | |

Table 48. PLL_CTRL Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-------------------|------|---------|--|
| 7:6 | PLL_MODE[1:0] | R/W | 0x2* | Selection of external clock and PLL operation: 0x0 - Forced to internal RC oscillator — PLL disabled. 0x1 - PLL is enabled in STANDBY and ACTIVE modes. Automatic external clock use when available, interrupt generated if external clock appears or disappears. 0x2 - PLL is enabled only in ACTIVE mode. Automatic external clock use when available, interrupt generated if external clock appears or disappears. 0x3 - Reserved |
| 5 | Reserved | R/W | 0 | |
| 4:0 | EXT_CLK_FREQ[4:0] | R/W | 0x01* | Frequency of the external clock (CLKIN): 0x00 - 1 MHz 0x01 - 2 MHz 0x02 - 3 MHz ... 0x16 - 23 MHz 0x17 - 24 MHz 0x18...0x1F - Reserved See Specifications for input clock frequency tolerance. |

7.6.1.40 PIN_FUNCTION

Address: 0x2C

Figure 61. PIN_FUNCTION Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------|-------------------|---------------------|-------------------|---------------------|-----------|-----------|-----------|
| EN_SPREAD_SPEC | EN_PIN_CTRL_GPIO3 | EN_PIN_SELECT_GPIO3 | EN_PIN_CTRL_GPIO2 | EN_PIN_SELECT_GPIO2 | GPIO3_SEL | GPIO2_SEL | GPIO1_SEL |

Table 49. PIN_FUNCTION Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|---------------------|------|---------|--|
| 7 | EN_SPREAD_SPEC | R/W | 0 * | Enable spread-spectrum feature: 0 - Disabled 1 - Enabled |
| 6 | EN_PIN_CTRL_GPIO3 | R/W | 1 * | Enable EN1/2 pin control for GPIO3 (GPIO3_SEL=1 AND GPIO3_DIR=1): 0 - Only GPIO3_OUT bit controls GPIO3. 1 - GPIO3_OUT bit AND ENx pin control GPIO3 |
| 5 | EN_PIN_SELECT_GPIO3 | R/W | 0 * | Enable EN1/2 pin control for GPIO3: 0 - GPIO3_SEL bit AND EN1 pin control GPIO3 1 - GPIO3_SEL bit AND EN2 pin control GPIO3 |

Table 49. PIN_FUNCTION Register Field Descriptions (continued)

| Bits | Field | Type | Default | Description |
|------|---------------------|------|---------|--|
| 4 | EN_PIN_CTRL_GPIO2 | R/W | 1 * | Enable EN1/3 pin control for GPIO2 (GPIO2_SEL=1 AND GPIO2_DIR=1): 0 - Only GPIO2_OUT bit controls GPIO2. 1 - GPIO2_OUT bit AND ENx pin control GPIO2 |
| 3 | EN_PIN_SELECT_GPIO2 | R/W | 0 * | Enable EN1/3 pin control for GPIO2: 0 - GPIO2_SEL bit AND EN1 pin control GPIO2 1 - GPIO2_SEL bit AND EN3 pin control GPIO2 |
| 2 | GPIO3_SEL | R/W | 1 * | EN3 pin function: 0 - EN3 1 - GPIO3 |
| 1 | GPIO2_SEL | R/W | 1 * | EN2 pin function: 0 - EN2 1 - GPIO2 |
| 0 | GPIO1_SEL | R/W | 0 * | EN1 pin function: 0 - EN1 1 - GPIO1 |

7.6.1.41 GPIO_CONFIG

Address: 0x2D

Figure 62. GPIO_CONFIG Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----------|----------|----------|----------|-----------|-----------|-----------|
| Reserved | GPIO3_OD | GPIO2_OD | GPIO1_OD | Reserved | GPIO3_DIR | GPIO2_DIR | GPIO1_DIR |

Table 50. GPIO_CONFIG Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------|------|---------|--|
| 7 | Reserved | R | 0 | |
| 6 | GPIO3_OD | R/W | 1 * | GPIO3 signal type when configured to output: 0 - Push-pull output (VANA level) 1 - Open-drain output |
| 5 | GPIO2_OD | R/W | 1 * | GPIO2 signal type when configured to output: 0 - Push-pull output (VANA level) 1 - Open-drain output |
| 4 | GPIO1_OD | R/W | 0 * | GPIO1 signal type when configured to output: 0 - Push-pull output (VANA level) 1 - Open-drain output |
| 3 | Reserved | R | 0 | |
| 2 | GPIO3_DIR | R/W | 1 * | GPIO3 signal direction: 0 - Input 1 - Output |
| 1 | GPIO2_DIR | R/W | 1 * | GPIO2 signal direction: 0 - Input 1 - Output |
| 0 | GPIO1_DIR | R/W | 0 * | GPIO1 signal direction: 0 - Input 1 - Output |

7.6.1.42 GPIO_IN

Address: 0x2E

Figure 63. GPIO_IN Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|----|----------|----------|----------|
| Reserved | | | | | GPIO3_IN | GPIO2_IN | GPIO1_IN |

Table 51. GPIO_IN Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|----------|------|---------|---|
| 7:3 | Reserved | R | 0x00 | |
| 2 | GPIO3_IN | R | 0 | State of GPIO3 signal: 0 - Logic low level 1 - Logic high level |
| 1 | GPIO2_IN | R | 0 | State of GPIO2 signal: 0 - Logic low level 1 - Logic high level |
| 0 | GPIO1_IN | R | 0 | State of GPIO1 signal: 0 - Logic low level 1 - Logic high level |

7.6.1.43 GPIO_OUT

Address: 0x2F

Figure 64. GPIO_OUT Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|----|----|----|----|-----------|-----------|-----------|
| Reserved | | | | | GPIO3_OUT | GPIO2_OUT | GPIO1_OUT |

Table 52. GPIO_OUT Register Field Descriptions

| Bits | Field | Type | Default | Description |
|------|-----------|------|---------|---|
| 7:3 | Reserved | R/W | 0x00 | |
| 2 | GPIO3_OUT | R/W | 1 * | Control for GPIO3 signal when configured to GPIO Output: 0 - Logic low level 1 - Logic high level |
| 1 | GPIO2_OUT | R/W | 1 * | Control for GPIO2 signal when configured to GPIO Output: 0 - Logic low level 1 - Logic high level |
| 0 | GPIO1_OUT | R/W | 0 | Control for GPIO1 signal when configured to GPIO Output: 0 - Logic low level 1 - Logic high level |

8 Application and Implementation

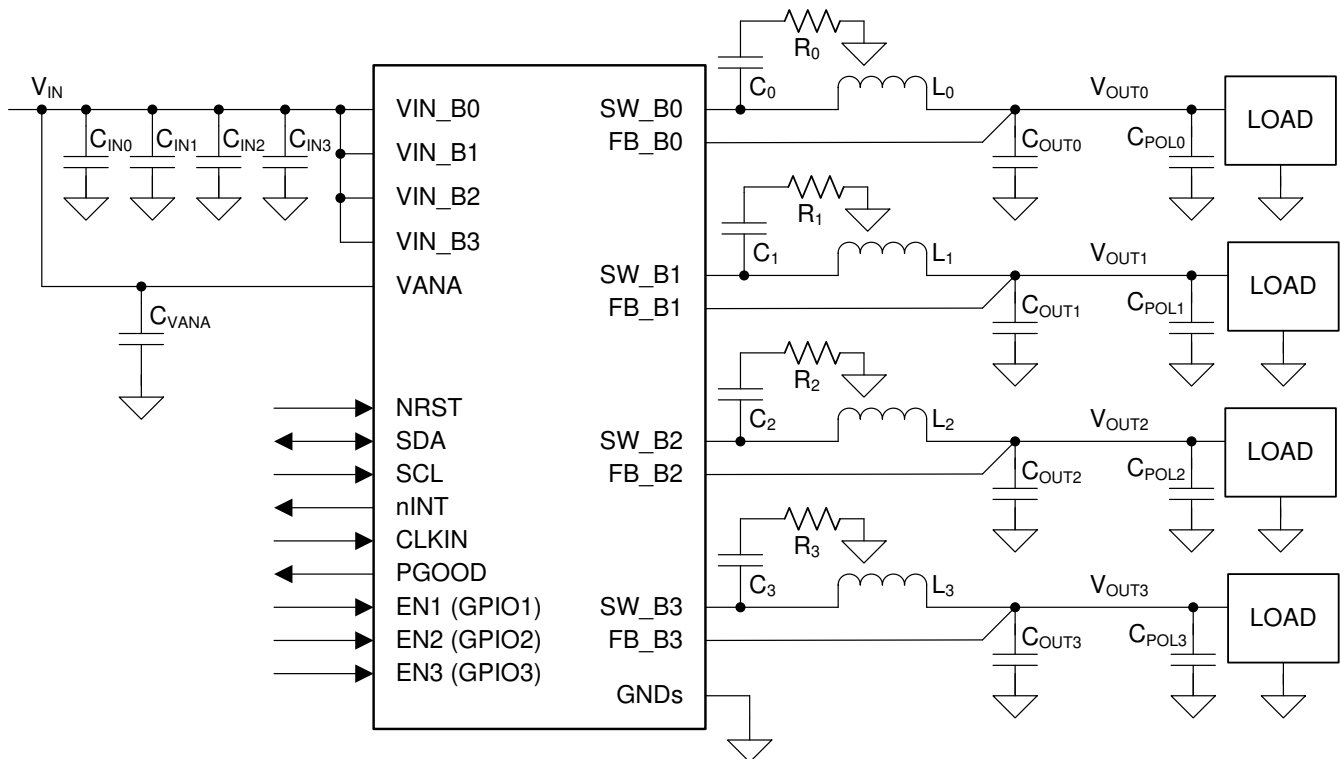
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP87524B/J/P-Q1 is a multi-phase step-down converter with four switcher cores, which are configured to four one-phase regulators configuration.

8.2 Typical Application



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Figure 65. Four 1-Phase Configuration

8.2.1 Design Requirements

8.2.1.1 Inductor Selection

The inductors L_0 , L_1 , L_2 , and L_3 are shown in the [Typical Application](#). The inductance and DCR of the inductor affects the control loop of the buck regulator. TI recommends using inductors similar to those listed in [Table 53](#). Pay attention to the saturation current and temperature rise current of the inductor. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. Minimum effective inductance to ensure good performance is $0.22 \mu\text{H}$ at maximum peak output current over the operating temperature range. DC resistance of the inductor must be less than 0.05Ω for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred as they radiate less noise.

Typical Application (continued)

Table 53. Recommended Inductors

| MANUFACTURER | PART NUMBER | VALUE | DIMENSIONS L × W × H (mm) | RATED DC CURRENT, I _{SAT} maximum (typical) / I _{TEMP} maximum (typical) (A) | DCR typical / maximum (mΩ) |
|--------------|------------------|---------------|------------------------------|--|----------------------------------|
| TOKO | DFE252012PD-R47M | 0.47 μH (20%) | 2.5 × 2 × 1.2 | 5.2 (-) / 4 (-) ⁽¹⁾ | - / 27 |
| Vishay | IHLP1616AB-1A | 0.47 μH (20%) | 4.1 × 4.5 × 1.2 | - (6) / - (6) ⁽¹⁾ | 19 / 21 |

(1) Operating temperature range is up to 125°C including self temperature rise.

8.2.1.2 Input Capacitor Selection

The input capacitors C_{INO}, C_{IN1}, C_{IN2}, and C_{IN3} are shown in the [Typical Application](#). A ceramic input bypass capacitor of 10 μF is required for each phase of the regulator. Place the input capacitor as close as possible to the VIN_Bx pin and PGND_Bx pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. DC bias characteristics capacitors must be considered, minimum effective input capacitance to ensure good performance is 1.9 μF per buck input at maximum input voltage including tolerances and ambient temperature range, assuming that there are at least 22 μF of additional capacitance common for all the power input pins on the system power rail. See [Table 54](#).

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition ferrite can be used in front of the input capacitor to reduce the EMI.

Table 54. Recommended Input Capacitors (X7R Dielectric)

| MANUFACTURER | PART NUMBER | VALUE | CASE SIZE | DIMENSIONS L × W × H (mm) | VOLTAGE RATING (V) |
|--------------|-------------------|-------------|-----------|------------------------------|-----------------------|
| Murata | GCM21BR71A106KE22 | 10 μF (10%) | 0805 | 2 × 1.25 × 1.25 | 10 V |

8.2.1.3 Output Capacitor Selection

The output capacitors C_{OUT0}, C_{OUT1}, C_{OUT2}, and C_{OUT3} are shown in [Typical Application](#). A ceramic local output capacitor of 22 μF is required per phase. Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance to ensure good performance is 10 μF per phase including the DC voltage roll-off, tolerances, aging and temperature effects.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR}. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part. See [Table 55](#).

POL capacitors (C_{POL0}, C_{POL1}, C_{POL2}, C_{POL3}) can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreases the PFM switching frequency. However, output capacitance higher than 100 μF per phase is not necessarily of any benefit. Note that the output capacitor may be the limiting factor in the output voltage ramp and the maximum total output capacitance listed in electrical characteristics must not be exceeded. At shutdown the output voltage is discharged to 0.6 V level using forced-PWM operation. This can increase the input voltage if the load current is small and the output capacitor is large. Below 0.6 V level the output capacitor is discharged by the internal discharge resistor and with large capacitor more time is required to settle V_{OUT} down as a consequence of the increased time constant.

Table 55. Recommended Output Capacitors (X7R or X7T Dielectric)

| MANUFACTURER | PART NUMBER | VALUE | CASE SIZE | DIMENSIONS L x W x H (mm) | VOLTAGE RATING (V) |
|--------------|-------------------|------------------|-----------|---------------------------|--------------------|
| Murata | GCM31CR71A226KE02 | 22 μ F (10%) | 1206 | 3.2 x 1.6 x 1.6 | 10 |

8.2.1.4 Snubber Components

If the input voltage for the regulators is above 4 V, snubber components are needed at the switching nodes to decrease voltage spiking in the switching node and to improve EMI. The snubber capacitors C_0 , C_1 , C_2 , and C_3 and the snubber resistors R_0 , R_1 , R_2 , and R_3 are shown in [Figure 65](#). The recommended components are shown in [Table 56](#) and these component values give good performance on LP87524B/J/P-Q1 EVM. The optimal resistance and capacitance values finally depend on the PCB layout.

Table 56. Recommended Snubber Components

| MANUFACTURER | PART NUMBER | VALUE | CASE SIZE | DIMENSIONS L x W x H (mm) | VOLTAGE / POWER RATING |
|--------------|-------------------|-------------------|-----------|---------------------------|------------------------|
| Vishay-Dale | CRCW04023R90JNED | 3.9 Ω (5%) | 0402 | 1 x 0.5 x 0.4 | 62 mW |
| Murata | GCM1555C1H391JA16 | 390 pF (5%) | 0402 | 1 x 0.5 x 0.5 | 50 V |

8.2.1.5 Supply Filtering Components

The VANA input is used to supply analog and digital circuits in the device. See [Table 57](#) for recommended components for VANA input supply filtering.

Table 57. Recommended Supply Filtering Components

| MANUFACTURER | PART NUMBER | VALUE | CASE SIZE | DIMENSIONS L x W x H (mm) | VOLTAGE RATING (V) |
|--------------|-------------------|--------------|-----------|---------------------------|--------------------|
| Murata | GCM155R71C104KA55 | 100 nF (10%) | 0402 | 1.0 x 0.5 x 0.5 | 16 |
| Murata | GCM188R71C104KA37 | 100 nF (10%) | 0603 | 1.6 x 0.8 x 0.8 | 16 |

8.2.2 Current Limit vs. Maximum Output Current

The worst case inductor current ripple can be calculated using [Equation 1](#) and [Equation 2](#):

$$D = \frac{V_{OUT}}{V_{IN(max)} \times \eta} \quad (1)$$

$$\Delta I_L = \frac{(V_{IN(max)} - V_{OUT}) \times D}{f_{SW} \times L} \quad (2)$$

Example using [Equation 1](#) and [Equation 2](#):

$$V_{IN(max)} = 5.5 \text{ V}$$

$$V_{OUT(max)} = 1 \text{ V}$$

$$\eta_{(min)} = 0.75$$

$$f_{SW(min)} = 1.8 \text{ MHz}$$

$$L_{(min)} = 0.38 \text{ } \mu\text{H}$$

$$\text{then } D_{(max)} = 0.242 \text{ and } \Delta I_{L(max)} = 1.59 \text{ A}$$

Peak current is half of the current ripple. If $I_{LIM_FWD_SET_OTP}$ is 4 A, the minimum forward current limit would be 3.8 A when $V_{IN} \geq 3 \text{ V}$ and when taking the tolerance into account. In the worst case situation difference between set peak current and maximum load current = $0.795 \text{ A} + 0.2 \text{ A} = 0.995 \text{ A}$.

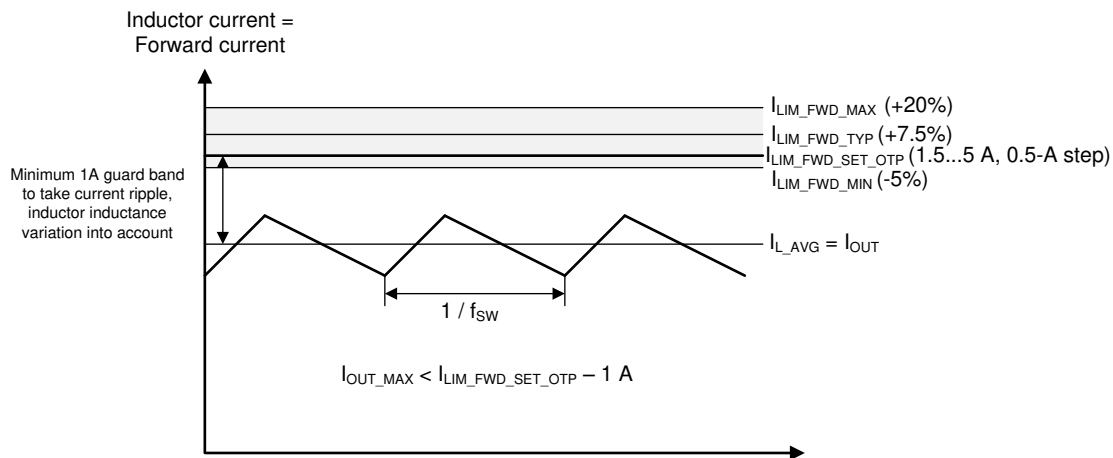


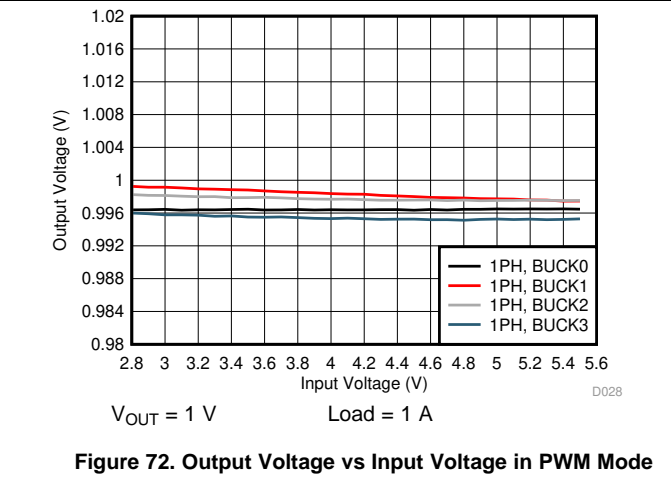
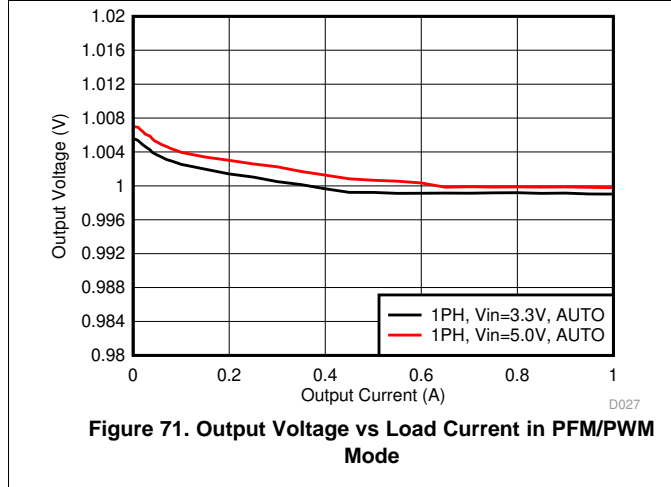
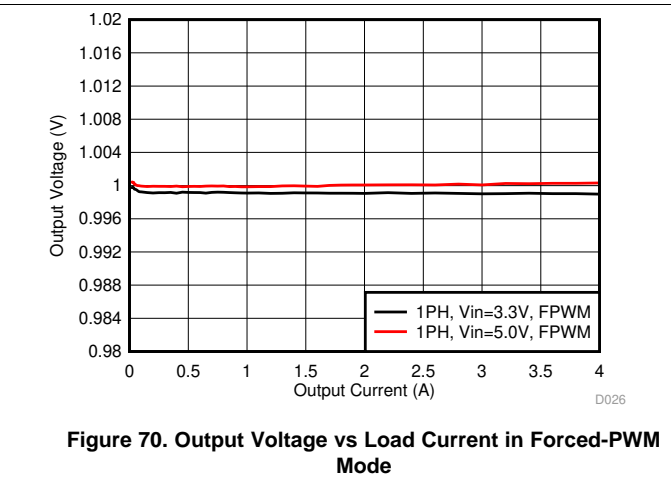
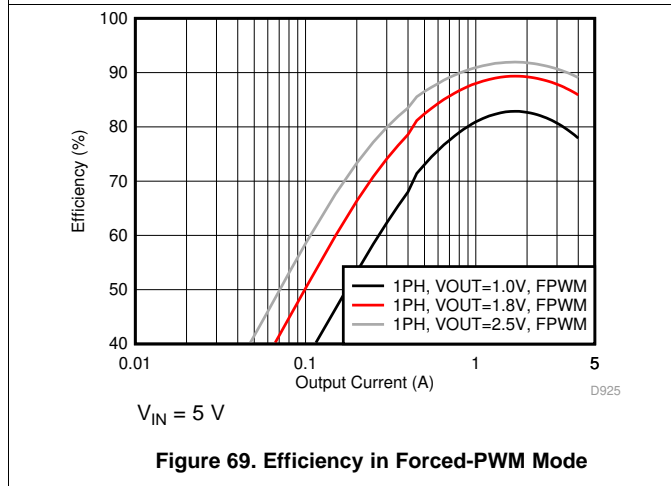
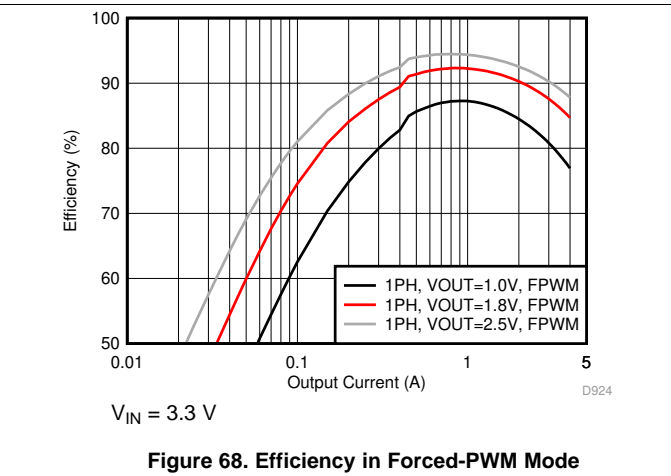
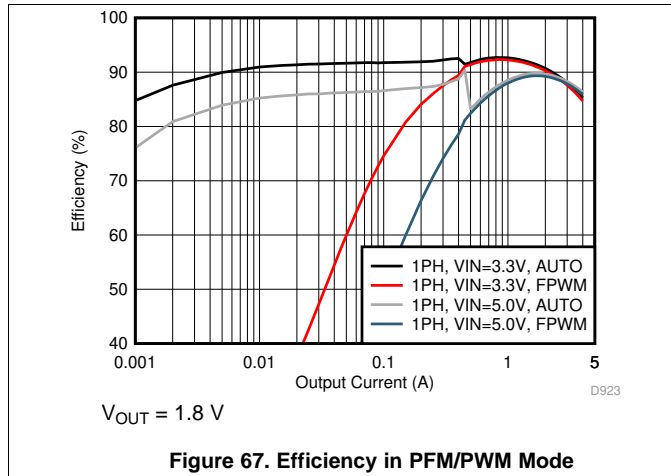
Figure 66. Current Limit vs Maximum Output Current

8.2.3 Detailed Design Procedure

The performance of the LP87524B/J/P-Q1 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention must be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from system power rail during turnon of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate power pins V_{IN_Bx} are not connected together internally. Connect the V_{IN_Bx} power connections together outside the package using power plane construction.

8.2.4 Application Curves

Measurements are done using typical application set up with connections shown in [Figure 65](#) (snubber components included when $V_{IN} > 4$ V). Graphs may not reflect the OTP default settings. Unless otherwise specified: $V_{IN} = 3.7$ V, $V_{OUT} = 1$ V, $V_{(NRST)} = 1.8$ V, $T_A = 25^\circ\text{C}$, $f_{SW} = 4$ MHz, $L = 0.47$ μH (TOKO DFE252012PD-R47M), $C_{OUT} = 22$ μF / phase, and $C_{POL} = 22$ μF / phase. Measurements are done using connections in the [Typical Application](#).



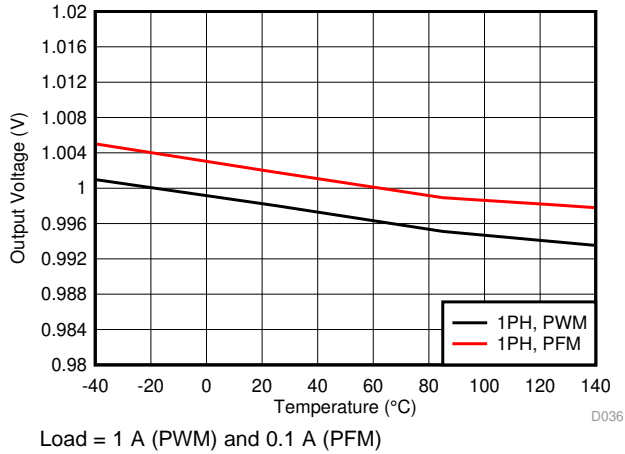


Figure 73. Output Voltage vs Temperature

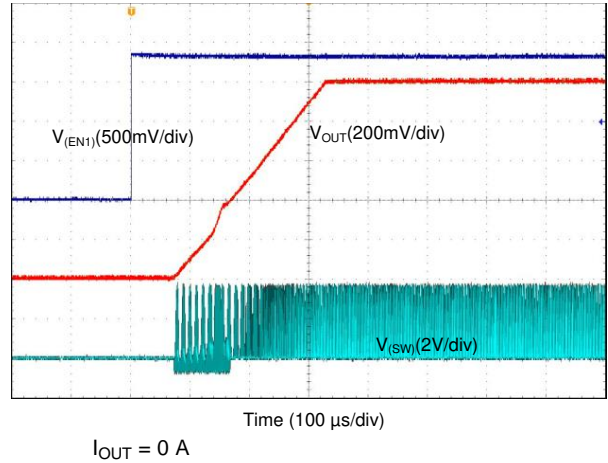


Figure 74. Start-Up With EN1, Forced PWM

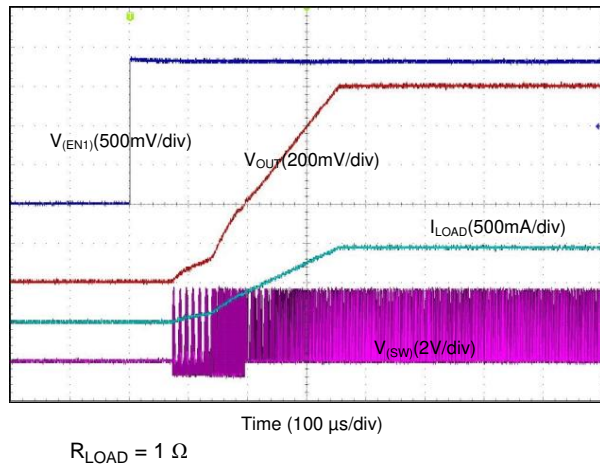


Figure 75. Start-Up With EN1, Forced PWM (1-Phase Output)

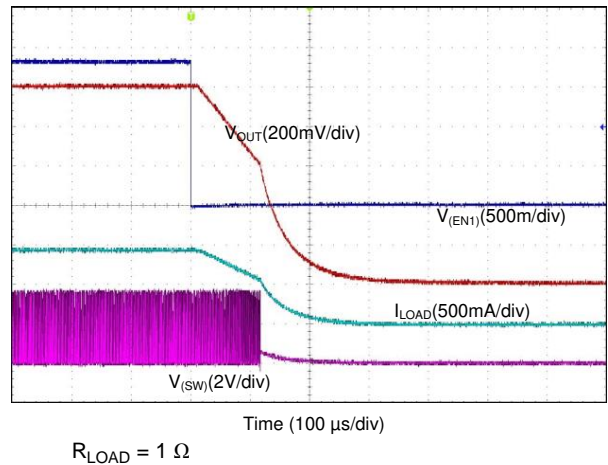


Figure 76. Shutdown With EN1, Forced PWM (1-Phase Output)

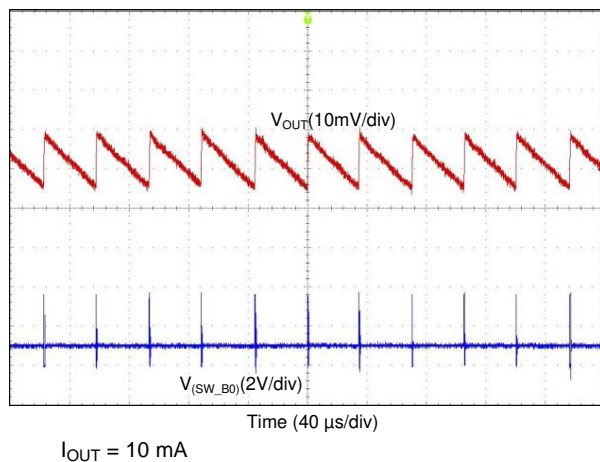


Figure 77. Output Voltage Ripple, PFM Mode (1-Phase Output)

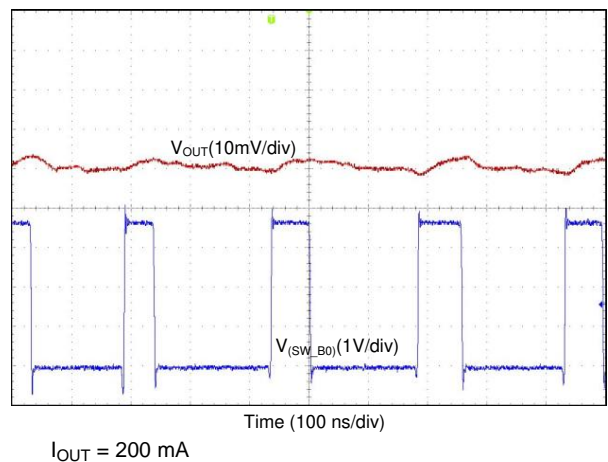


Figure 78. Output Voltage Ripple, Forced-PWM Mode (1-Phase Output)

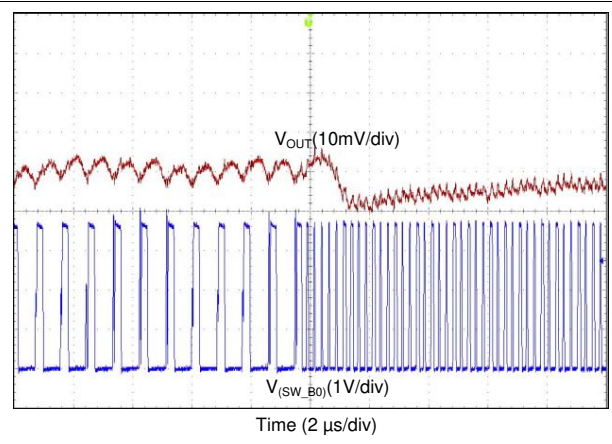
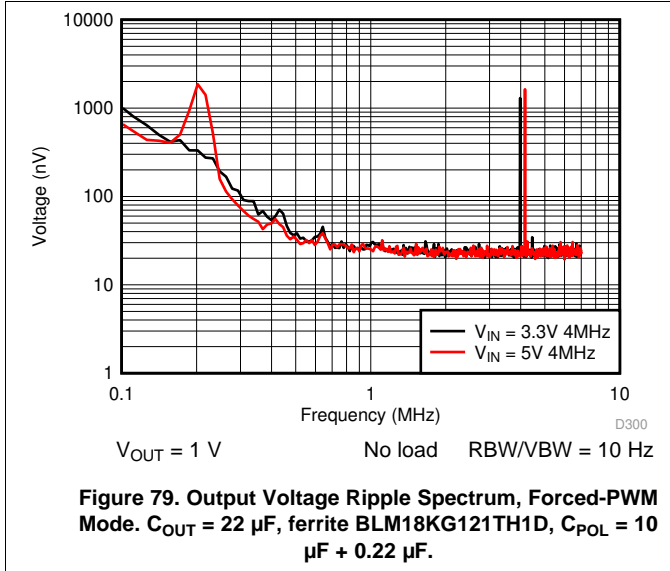


Figure 80. Transient from PFM-to-PWM Mode (1-Phase Output)

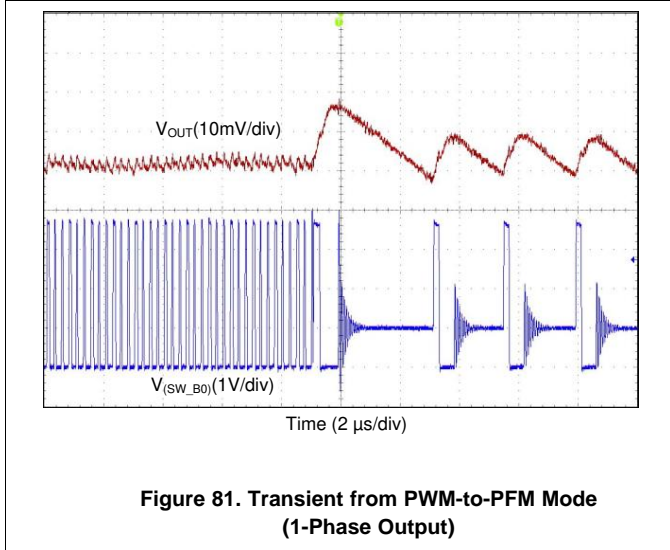
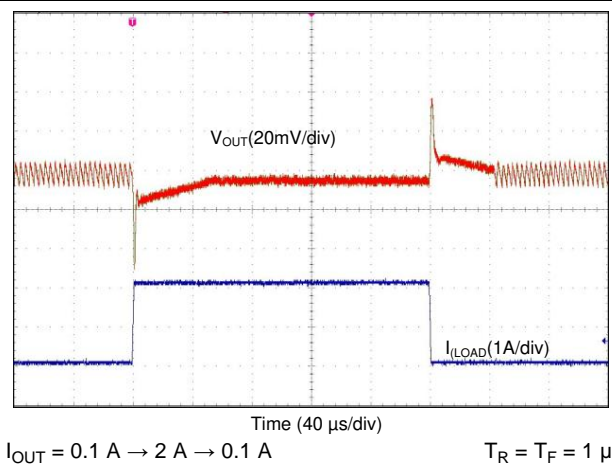
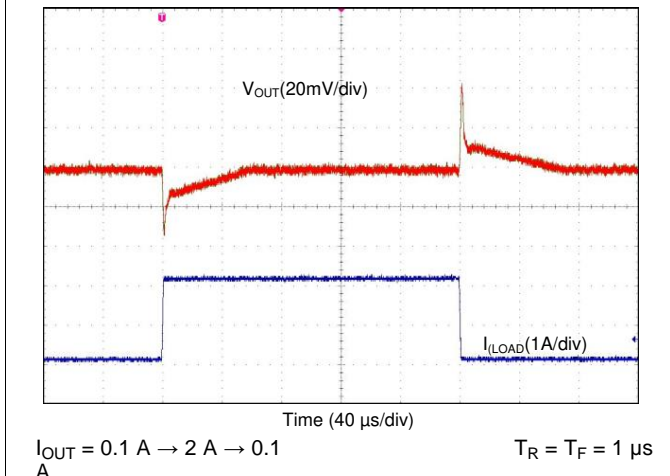


Figure 81. Transient from PWM-to-PFM Mode (1-Phase Output)



$I_{OUT} = 0.1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 0.1 \text{ A}$ $T_R = T_F = 1 \mu\text{s}$

Figure 82. Transient Load Step Response, AUTO Mode (1-Phase Output)



$I_{OUT} = 0.1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 0.1 \text{ A}$ $T_R = T_F = 1 \mu\text{s}$

Figure 83. Transient Load Step Response, Forced-PWM Mode (1-Phase Output)

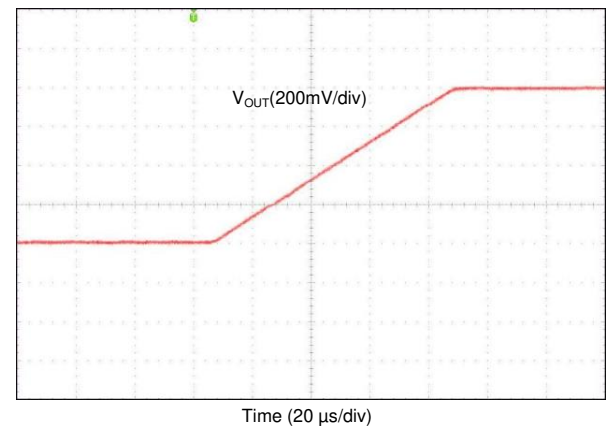


Figure 84. V_{OUT} Transition from 0.6 V to 1.4 V

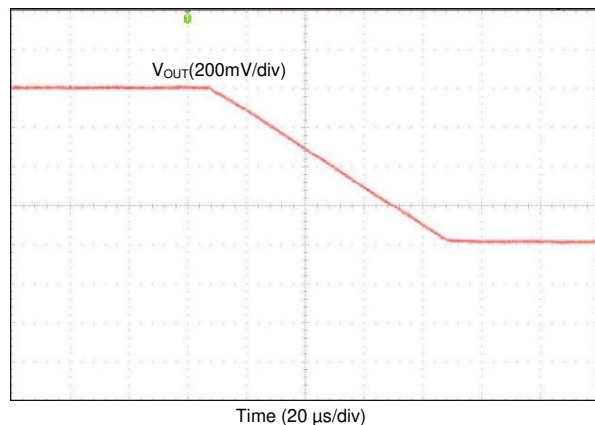
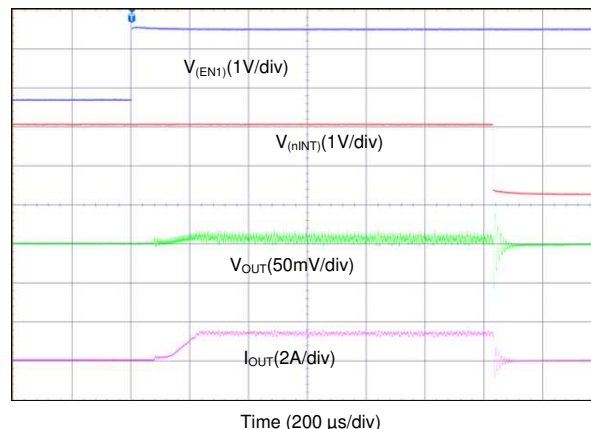
Figure 85. V_{OUT} Transition from 1.4 V to 0.6 V

Figure 86. Start-up With Short on Output (1-Phase Output)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.8 V and 5.5 V. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high drop in the LP87524B/J/P-Q1 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP87524B/J/P-Q1 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high frequency and large switching currents of the LP87524B/J/P-Q1 make the choice of layout important. Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to 10 A, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} as close as possible to the VIN_Bx pin and the PGND_Bxx pin. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the positive node of the input capacitor and the VIN_Bx pin(s) of LP87524B/J/P-Q1, as well as the trace between the negative node of the input capacitor and power PGND_Bxx pin(s), must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor — parasitic inductance on these traces must be kept as small as possible for proper device operation. The parasitic inductance can be reduced by using a ground plane as close as possible to top layer by using thin dielectric layer between top layer and ground plane.
2. The output filter, consisting of COUT and L, converts the switching signal at SW_Bx to the noiseless output voltage. It must be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP87524B/J/P-Q1 output capacitors and the load direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) must be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
4. If the processor load supports remote voltage sensing, connect the feedback pins FB_Bx of the LP87524B/J/P-Q1 device to the respective sense pins on the processor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bxx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I²C. Avoid both capacitive and inductive coupling by keeping the sense lines short, direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. If series resistors are used for load current measurement, place them after connection of the voltage feedback.
5. PGND_Bxx, VIN_Bx and SW_Bx must be routed on thick layers. They must not surround inner signal layers, which are not able to withstand interference from noisy PGND_Bxx, VIN_Bx and SW_Bx.
6. If the input voltage is above 4 V, place snubber components (capacitor and resistor) between SW_Bx and ground on all four phases. The components can be also placed to the other side of the board if there are area limitations and the routing traces can be kept short.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent parameters such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide and thick power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances and thereby reduces the device junction temperature, T_J . TI strongly recommends to perform of a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process, by using a thermal modeling analysis software.

**LP87524B-Q1
LP87524J-Q1, LP87524P-Q1**

SNVSAW2B – APRIL 2017 – REVISED DECEMBER 2018

www.ti.com

10.2 Layout Example

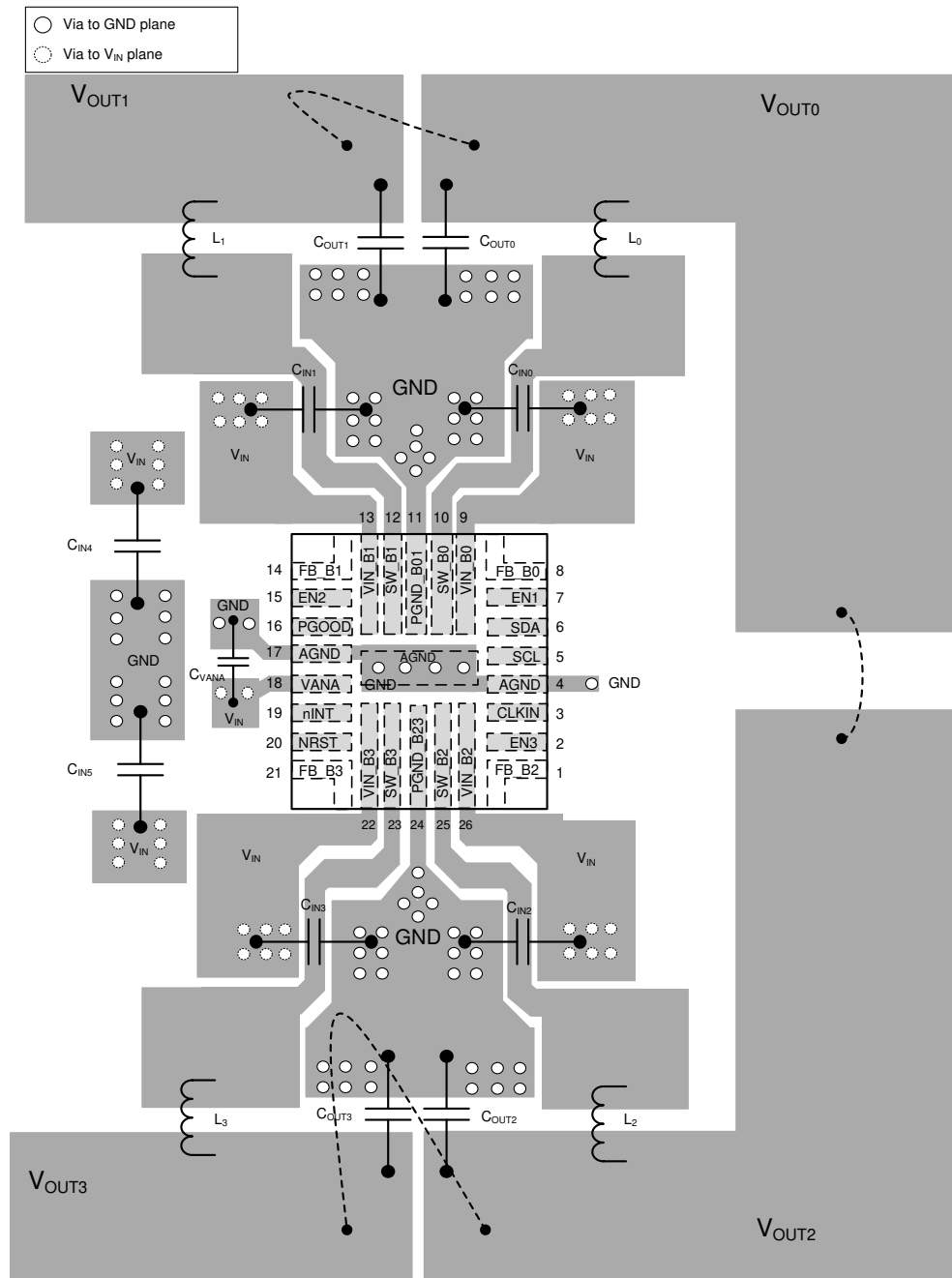


Figure 87. LP87524B/J/P-Q1 Board Layout

The output voltage rails are shorted together based on the configuration as shown in [Typical Application](#).

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 58. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| LP87524B-Q1 | Click here | Click here | Click here | Click here | Click here |
| LP87524J-Q1 | Click here | Click here | Click here | Click here | Click here |
| LP87524P-Q1 | Click here | Click here | Click here | Click here | Click here |

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

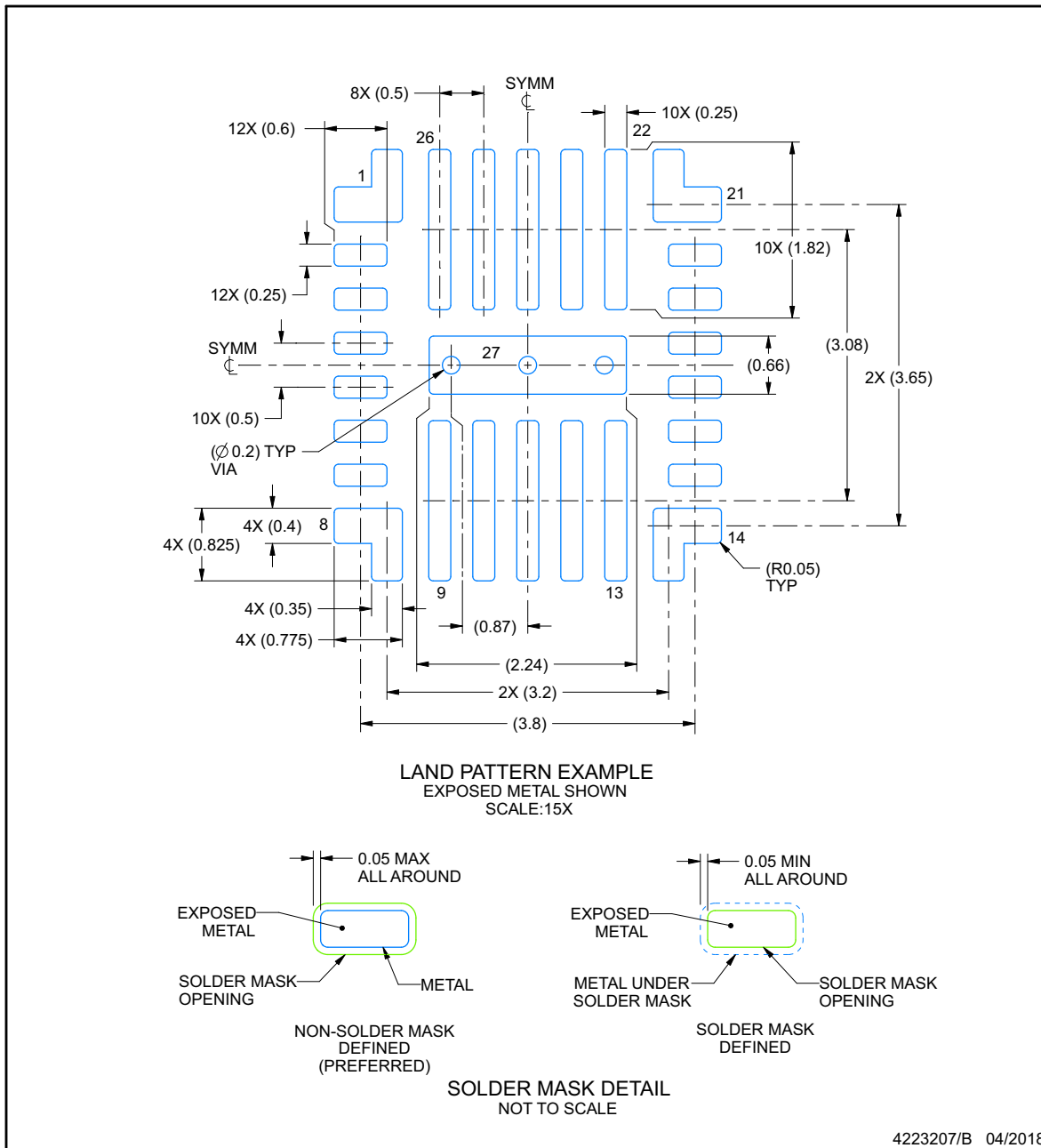
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

EXAMPLE BOARD LAYOUT

RNF0026C

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|--------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LP87524BRNFRQ1 | Active | Production | VQFN-HR (RNF) 26 | 3000 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4B-Q1 |
| LP87524BRNFRQ1.A | Active | Production | VQFN-HR (RNF) 26 | 3000 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4B-Q1 |
| LP87524BRNFTQ1 | Active | Production | VQFN-HR (RNF) 26 | 250 SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4B-Q1 |
| LP87524BRNFTQ1.A | Active | Production | VQFN-HR (RNF) 26 | 250 SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4B-Q1 |
| LP87524JRNFRQ1 | Active | Production | VQFN-HR (RNF) 26 | 3000 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4J-Q1 |
| LP87524JRNFRQ1.A | Active | Production | VQFN-HR (RNF) 26 | 3000 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4J-Q1 |
| LP87524JRNFTQ1 | Active | Production | VQFN-HR (RNF) 26 | 250 SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4J-Q1 |
| LP87524JRNFTQ1.A | Active | Production | VQFN-HR (RNF) 26 | 250 SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4J-Q1 |
| LP87524PRNFRQ1 | Active | Production | VQFN-HR (RNF) 26 | 3000 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4P-Q1 |
| LP87524PRNFRQ1.A | Active | Production | VQFN-HR (RNF) 26 | 3000 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4P-Q1 |
| LP87524PRNFTQ1 | Active | Production | VQFN-HR (RNF) 26 | 250 SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4P-Q1 |
| LP87524PRNFTQ1.A | Active | Production | VQFN-HR (RNF) 26 | 250 SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -40 to 125 | LP8752 4P-Q1 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

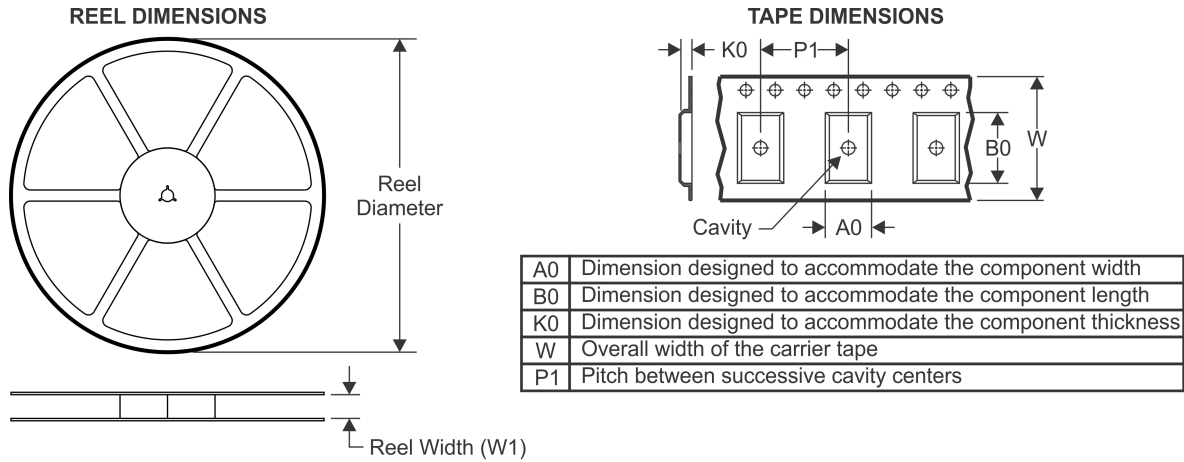
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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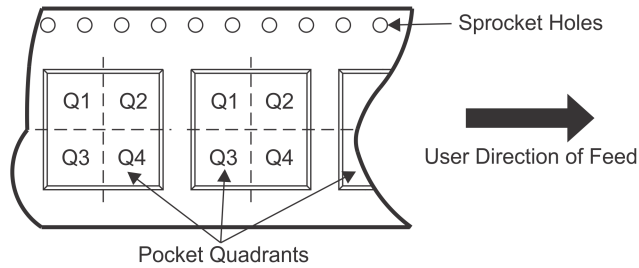
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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION



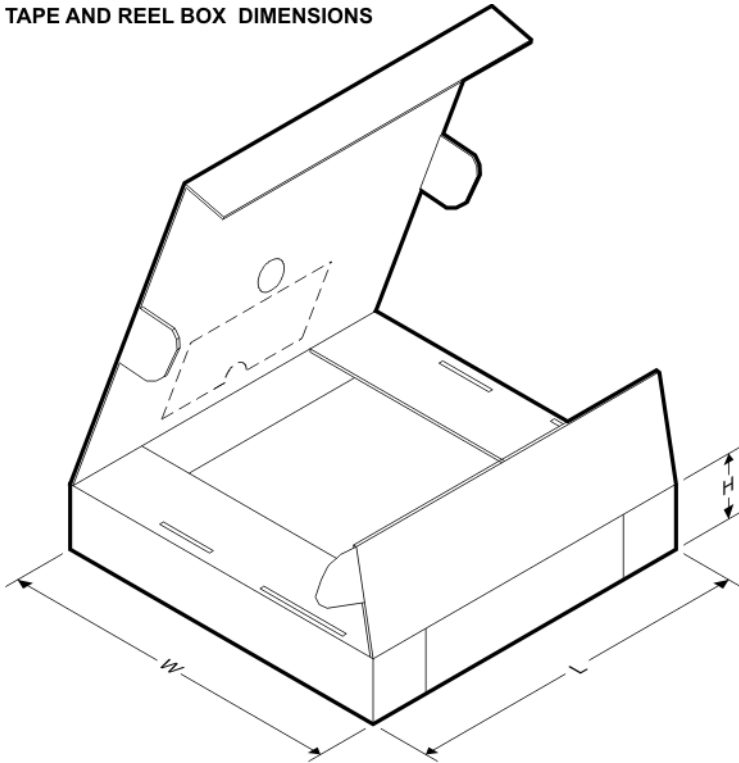
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP87524BRNFRQ1 | VQFN-HR | RNF | 26 | 3000 | 330.0 | 12.4 | 4.25 | 4.75 | 1.2 | 8.0 | 12.0 | Q1 |
| LP87524BRNFTQ1 | VQFN-HR | RNF | 26 | 250 | 180.0 | 12.4 | 4.25 | 4.75 | 1.2 | 8.0 | 12.0 | Q1 |
| LP87524JRNFRQ1 | VQFN-HR | RNF | 26 | 3000 | 330.0 | 12.4 | 4.25 | 4.75 | 1.2 | 8.0 | 12.0 | Q1 |
| LP87524JRNFTQ1 | VQFN-HR | RNF | 26 | 250 | 180.0 | 12.4 | 4.25 | 4.75 | 1.2 | 8.0 | 12.0 | Q1 |
| LP87524PRNFRQ1 | VQFN-HR | RNF | 26 | 3000 | 330.0 | 12.4 | 4.25 | 4.75 | 1.2 | 8.0 | 12.0 | Q1 |
| LP87524PRNFTQ1 | VQFN-HR | RNF | 26 | 250 | 180.0 | 12.4 | 4.25 | 4.75 | 1.2 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP87524BRNFRQ1 | VQFN-HR | RNF | 26 | 3000 | 346.0 | 346.0 | 35.0 |
| LP87524BRNFTQ1 | VQFN-HR | RNF | 26 | 250 | 200.0 | 183.0 | 25.0 |
| LP87524JRNFRQ1 | VQFN-HR | RNF | 26 | 3000 | 346.0 | 346.0 | 35.0 |
| LP87524JRNFTQ1 | VQFN-HR | RNF | 26 | 250 | 200.0 | 183.0 | 25.0 |
| LP87524PRNFRQ1 | VQFN-HR | RNF | 26 | 3000 | 346.0 | 346.0 | 35.0 |
| LP87524PRNFTQ1 | VQFN-HR | RNF | 26 | 250 | 200.0 | 183.0 | 25.0 |

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