MAX3232EIDR Datasheet

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DiGi Electronics Part Number	MAX3232EIDR-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	MAX3232EIDR
Description	IC TRANSCEIVER FULL 2/2 16SOIC
Detailed Description	2/2 Transceiver Full RS232 16-SOIC

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MAX3232EIDR	Texas Instruments
Series:	Product Status:
-	Active
Type:	Protocol:
Transceiver	RS232
Number of Drivers/Receivers:	Duplex:
2/2	Full
Receiver Hysteresis:	Data Rate:
300 mV	250kbps
Voltage - Supply:	Operating Temperature:
3V ~ 5.5V	-40°C ~ 85°C
Mounting Type:	Package / Case:
Surface Mount	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package:	Base Product Number:
16-SOIC	MAX3232

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

MAX3232E 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ±15-kV IEC ESD Protection

1 Features

- ESD protection for RS-232 bus pins
  - ±15 kV (HBM)
  - ±8 kV (IEC61000-4-2, Contact discharge)
  - ±15 kV (IEC61000-4-2, Air-gap discharge)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU V.28 standards
- Operates with 3-V to 5.5-V V_{CC} supply
- Operates up to 250 kbit/s
- Two drivers and two receivers
- Low supply current: 300 µA (typical)
- External capacitors: 4 × 0.1 µF
- Accepts 5-V logic input with 3.3-V supply
- Pin compatible to alternative high-speed devices (1 Mbit/s)
  - SN65C3232E (–40°C to +85°C)
  - SN75C3232E (0°C to 70°C)

2 Applications

- Industrial PCs
- Wired networking
- Data center and enterprise computing
- Battery-powered systems
- Notebooks
- Palmtop PCs
- Hand-held equipment

3 Description

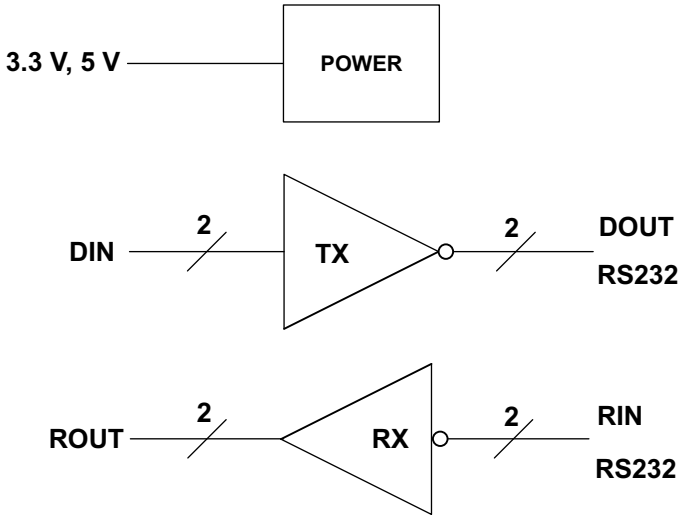
The MAX3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND).

The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MAX3232E	SOIC (D) (16)	9.90 mm × 3.91 mm
	SSOP (DB) (16)	6.20 mm × 5.30 mm
	SOIC (DW) (16)	10.30 mm × 7.50 mm
	TSSOP (PW) (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2017) to Revision E (June 2021) **Page**

- Added *Applications*: Industrial PCs, Wired networking, and Data center and enterprise computing....1
- Added the *ESD Ratings - IEC Specifications* table. Added a table note about 1-uF capacitor requirement between V_{CC} and GND for D, DB and PW packages....4
- Changed the thermal parameter values for D, DB and PW packages in the *Thermal Information* table....5

Changes from Revision C (June 2015) to Revision D (May 2017) **Page**

- Changed 3 V ± 5.5 V to 3 V to 5.5 V in the V_{CC} column of Table 9-1 11

Changes from Revision B (December 2013) to Revision C (May 2015) **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision A (April 2007) to Revision B (December 2013) **Page**

- Updated document to new TI data sheet format....1
- Deleted *Ordering Information* table....1
- Added *Thermal Information* table.... 5

5 Pin Configuration and Functions

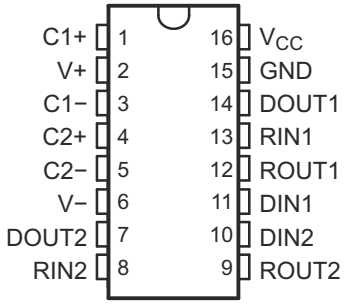


Figure 5-1. D, DW, DB and PW Package, 16-Pin SOIC, SSOP and TSSOP, Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
V+	2	O	Positive charge pump output for storage capacitor only
C1–	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2–	5	—	Negative lead of C2 capacitor
V–	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 3-V to 5.5-V power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
V+	Positive output supply voltage(2)		–0.3	7	V
V–	Negative output supply voltage(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage	Drivers	–0.3	6	V
		Receivers	–25	25	V
V_O	Output voltage	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	V
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except RIN and DOUT	±2000	V
			RIN and DOUT Pins	±15,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC61000-4-2, Contact Discharge(1)	RS232 port pins (RIN, DOUT)	±8000	V
		IEC61000-4-2, Air-Gap Discharge(1)	RS232 port pins (RIN, DOUT)	±15,000	

(1) For D, DB and PW packages only: Minimum of 1-µF capacitor is required between V_{CC} and GND to meet the specified IEC 16000-4-2 rating.

6.4 Recommended Operating Conditions(1)

See Typical Operating Circuit and Capacitor Values.

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2		5.5	V
			V_{CC} = 5 V	2.4		5.5	
V_{IL}	Driver low-level input voltage	DIN		0		0.8	V
V_I	Receiver input voltage	RIN		–25		25	V

6.4 Recommended Operating Conditions(1) (continued)

See Typical Operating Circuit and Capacitor Values.

			MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	MAX3232EC	0		70	°C
		MAX3232EI	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.5 Thermal Information

THERMAL METRIC(1)		MAX3232E				UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.2	85.9	72.3	103.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	39.0	43.1	33.5	49.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	44.5	37.1	54.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.3	10.1	7.5	12	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.8	44.1	37.1	54.1	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics — Device(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values).

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.7 Electrical Characteristics — Driver(1)

over operating free-air temperature range (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values).

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS} (3)	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V				
r_O	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Electrical Characteristics — Receiver[2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values).

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.3		V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

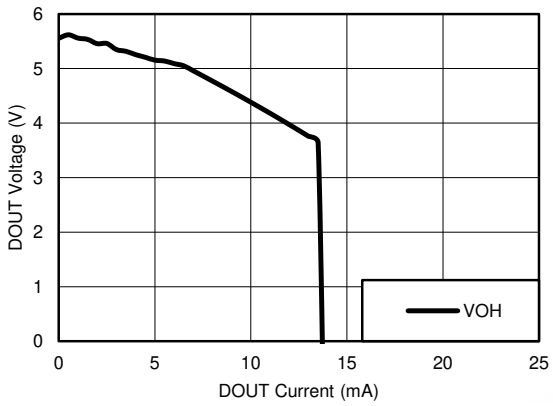
6.9 Switching Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ, One DOUT switching,	C_L = 1000 pF, see Driver Slew Rate	150	250		kbit/s
$t_{sk(p)}$	Driver pulse skew[3]	R_L = 3 kΩ to 7 kΩ, see Driver Pulse Skew	C_L = 150 pF to 2500 pF,		300		ns
SR(tr)	Driver slew rate, transition region (see Driver Slew Rate)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	
t_{PLH}	Receiver propagation delay time, low- to high-level output	C_L = 150 pF, see Receiver Propagation Delay Times			300		ns
t_{PHL}	Receiver propagation delay time, high- to low-level output				300		ns
$t_{sk(p)}$	Receiver pulse skew[3]				300		ns

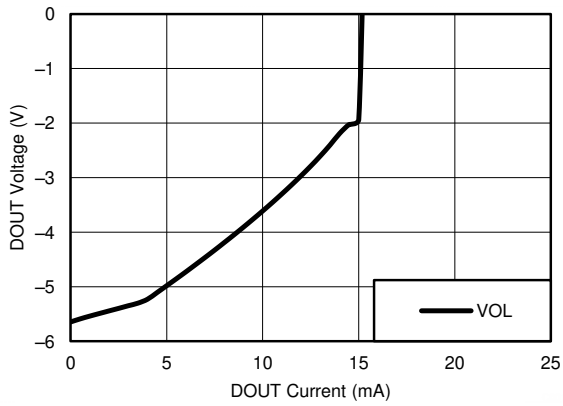
(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

6.10 Typical Characteristics



V_{CC} = 3.3 V

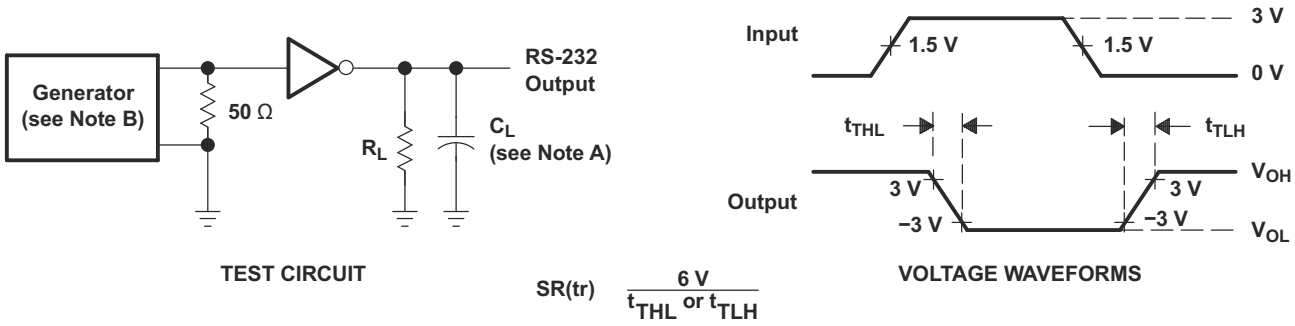
Figure 6-1. DOUT V_{OH} vs Load Current, Both Drivers Loaded



V_{CC} = 3.3 V

Figure 6-2. DOUT V_{OL} vs Load Current, Both Drivers Loaded

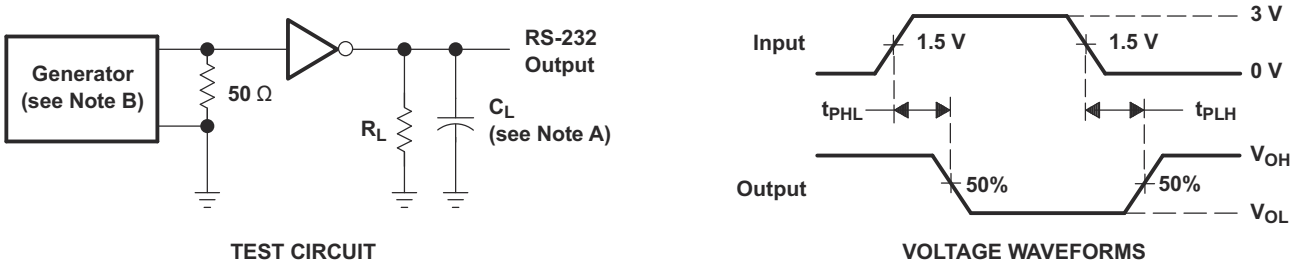
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns

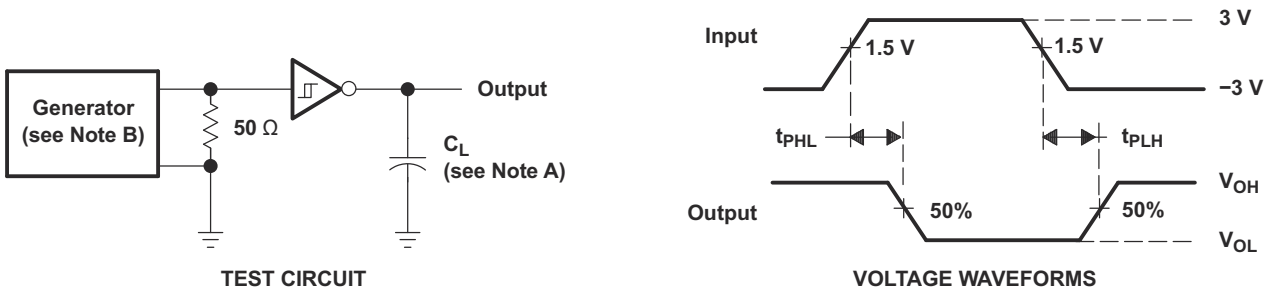
Figure 7-1. Driver Slew Rate



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns

Figure 7-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns

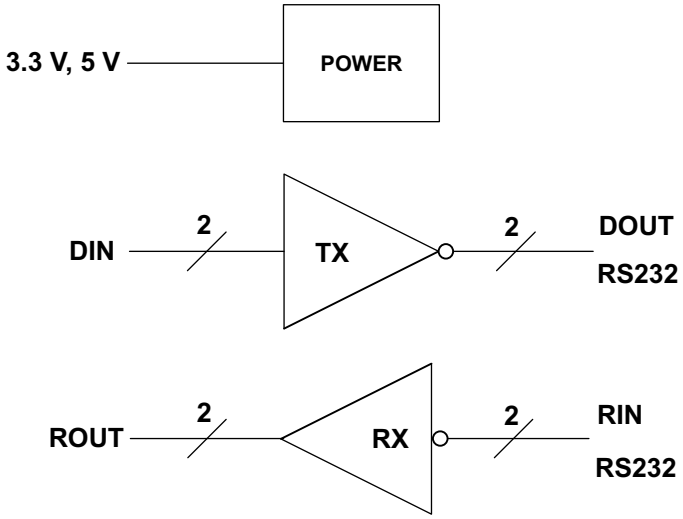
Figure 7-3. Receiver Propagation Delay Times

8 Detailed Description

8.1 Overview

The MAX3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.4 Device Functional Modes

Table 8-1 and Table 8-2 list the functional modes of the drivers and receivers of MAX3232E.

Table 8-1. Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 8-2. Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

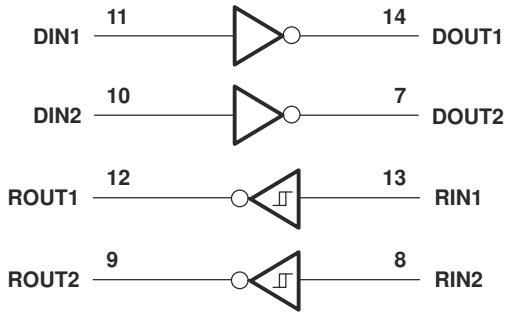


Figure 8-1. Logic Diagram

8.4.1 V_{CC} Powered by 3 V to 5.5 V

The device is in normal operation.

8.4.2 V_{CC} Unpowered, V_{CC} = 0 V

When MAX3232E is unpowered, it can be safely connected to an active remote RS232 device.

9 Application and Implementation

Note

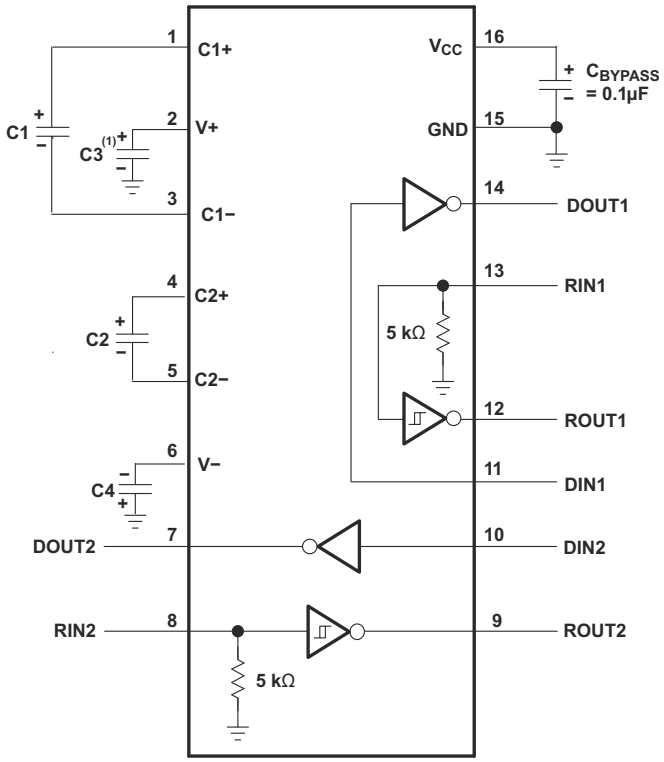
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

For proper operation, add capacitors as shown in Table 9-1.

9.2 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



A. C3 can be connected to V_{CC} or GND

A. Resistor values shown are nominal.

B. Nonpolorized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 9-1. Typical Operating Circuit and Capacitor Values

Table 9-1. VCC vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

9.2.1 Design Requirements

The recommended V_{CC} is 3.3 V or 5 V. 3 V to 5.5 V is also possible

The maximum recommended bit rate is 250 kbit/s.

9.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

Figure 9-2 curves are for 3.3-V VCC and 250-kbit/s alternative bit data stream.

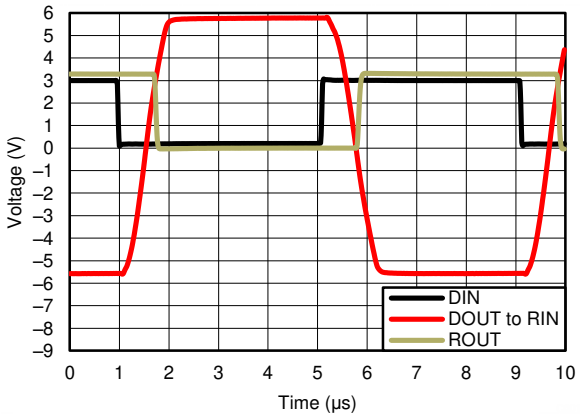


Figure 9-2. 250 kbit/s Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3 V

10 Power Supply Recommendations

The supply voltage, V_{CC}, should be between 3 V and 5.5 V. Select the values of the charge-pump capacitors using Table 9-1.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

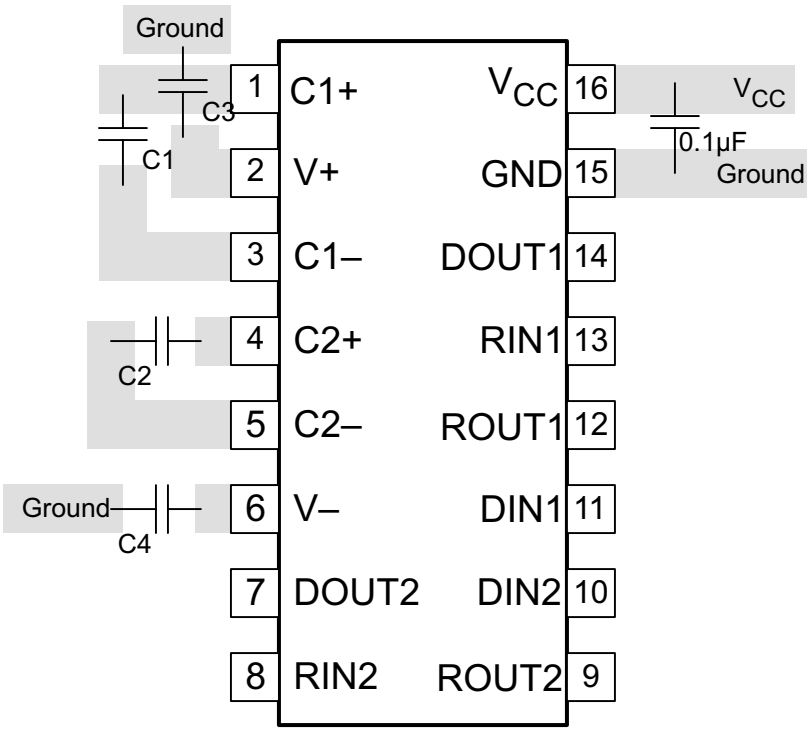


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3232ECD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	MAX3232EC
MAX3232ECDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC
MAX3232ECDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC
MAX3232ECDBRG4	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EC
MAX3232ECDBRG4.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EC
MAX3232ECDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC
MAX3232ECDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC
MAX3232ECDRE4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC
MAX3232ECDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	MAX3232EC
MAX3232ECDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC
MAX3232ECDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC
MAX3232ECPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	MP232EC
MAX3232ECPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC
MAX3232ECPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EC
MAX3232ECPWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EC
MAX3232EID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	MAX3232EI
MAX3232EIDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI
MAX3232EIDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI
MAX3232EIDBRE4	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI
MAX3232EIDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI
MAX3232EIDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI
MAX3232EIDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI
MAX3232EIDRG4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI
MAX3232EIDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	MAX3232EI
MAX3232EIDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI
MAX3232EIDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI
MAX3232EIPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	MP232EI
MAX3232EIPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI
MAX3232EIPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI

TEXAS INSTRUMENTS

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3232EIPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF MAX3232E :

- Automotive : MAX3232E-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

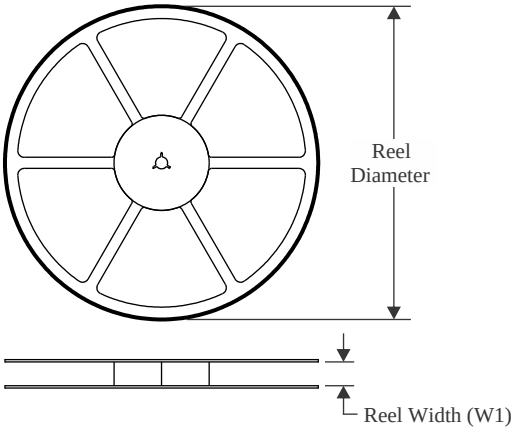
PACKAGE MATERIALS INFORMATION

www.ti.com

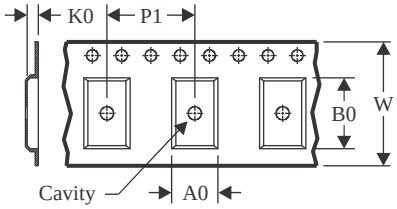
13-Dec-2025

TAPE AND REEL INFORMATION

REEL DIMENSIONS

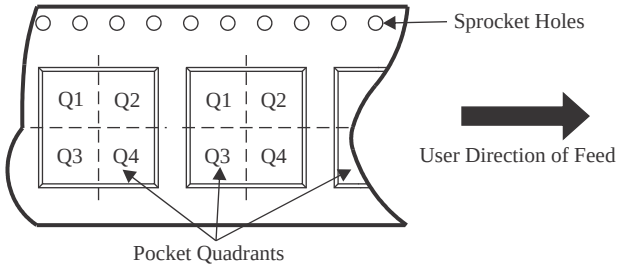


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

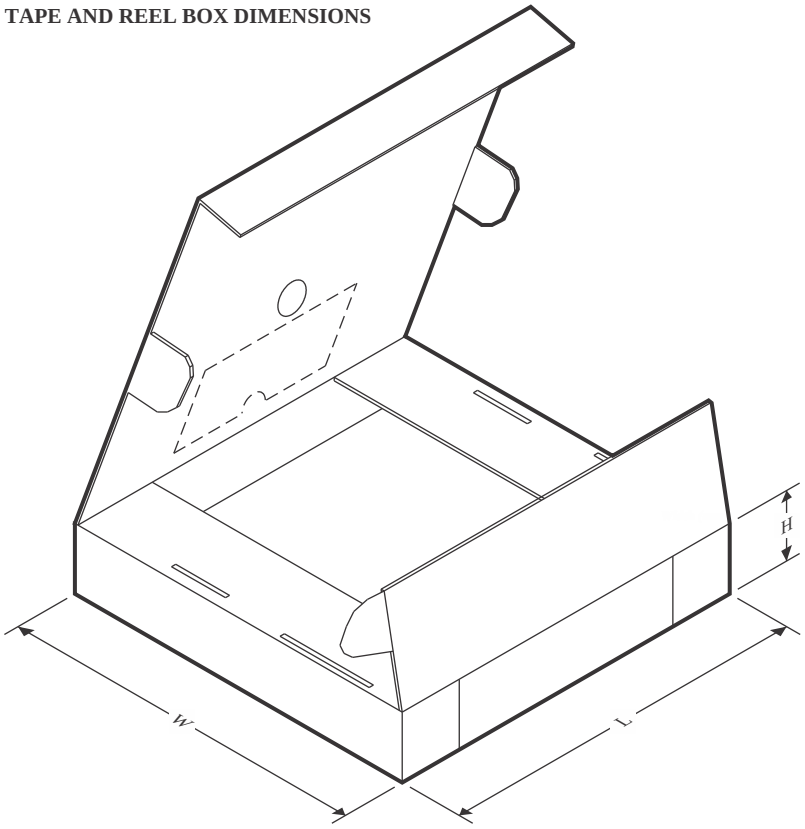
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3232ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3232ECDBRG4	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232ECPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232ECPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232EIDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com

13-Dec-2025

TAPE AND REEL BOX DIMENSIONS

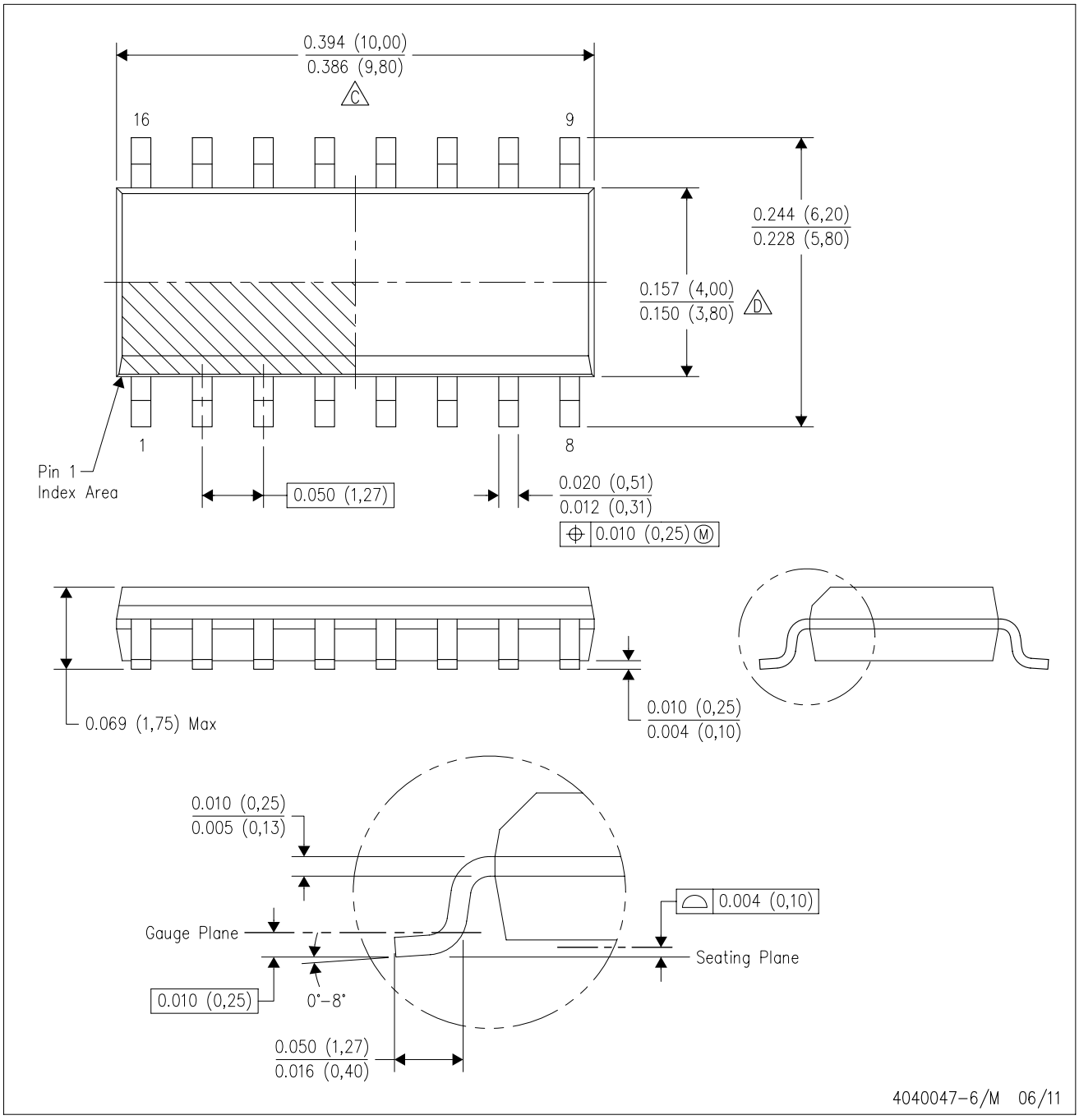


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3232ECDBR	SSOP	DB	16	2000	353.0	353.0	32.0
MAX3232ECDBRG4	SSOP	DB	16	2000	353.0	353.0	32.0
MAX3232ECDR	SOIC	D	16	2500	353.0	353.0	32.0
MAX3232ECDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX3232ECPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3232ECPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3232ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3232ECPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3232ECPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3232EIDBR	SSOP	DB	16	2000	353.0	353.0	32.0
MAX3232EIDR	SOIC	D	16	2500	353.0	353.0	32.0
MAX3232EIDRG4	SOIC	D	16	2500	353.0	353.0	32.0
MAX3232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX3232EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

MECHANICAL DATA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



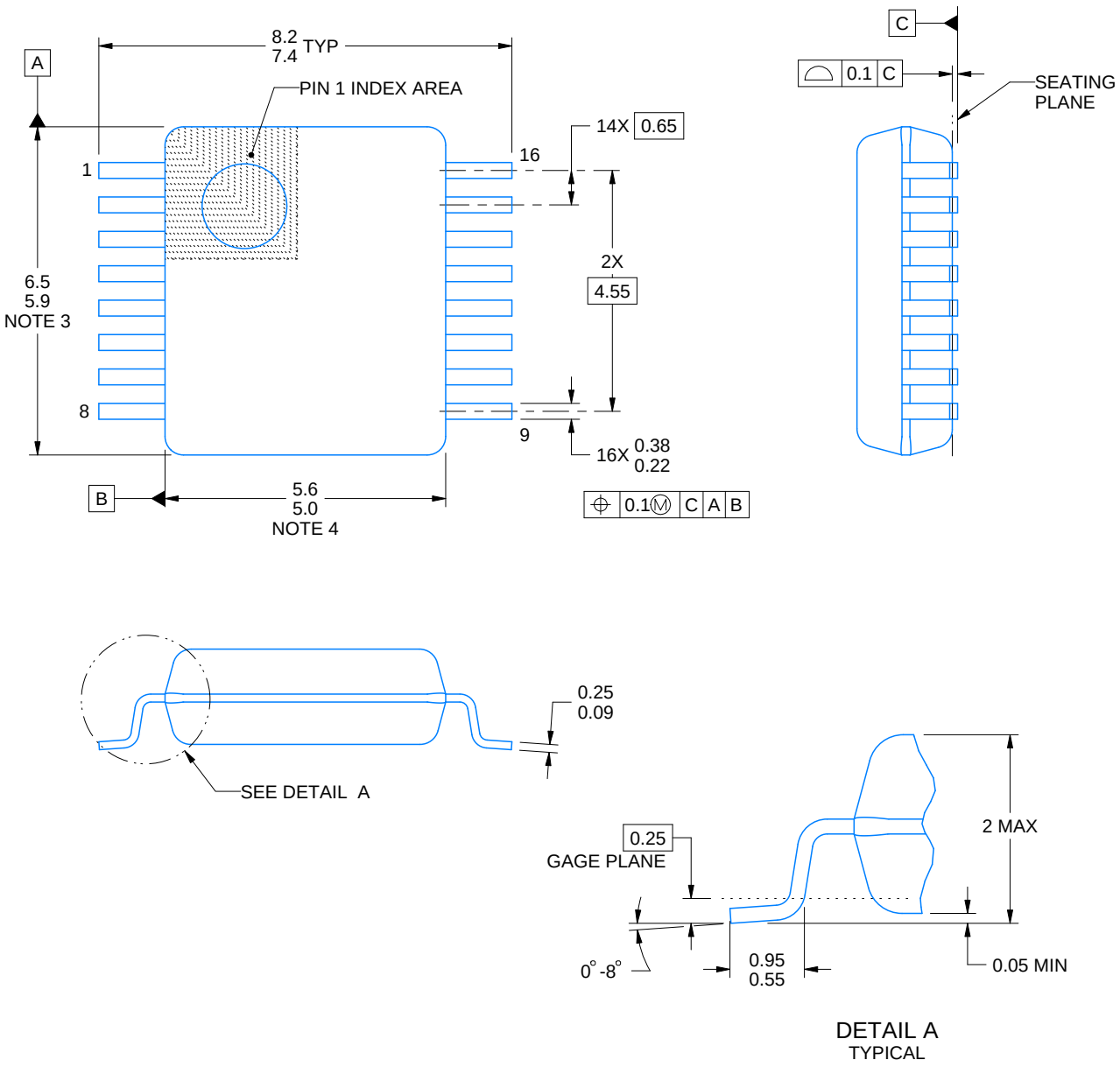
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

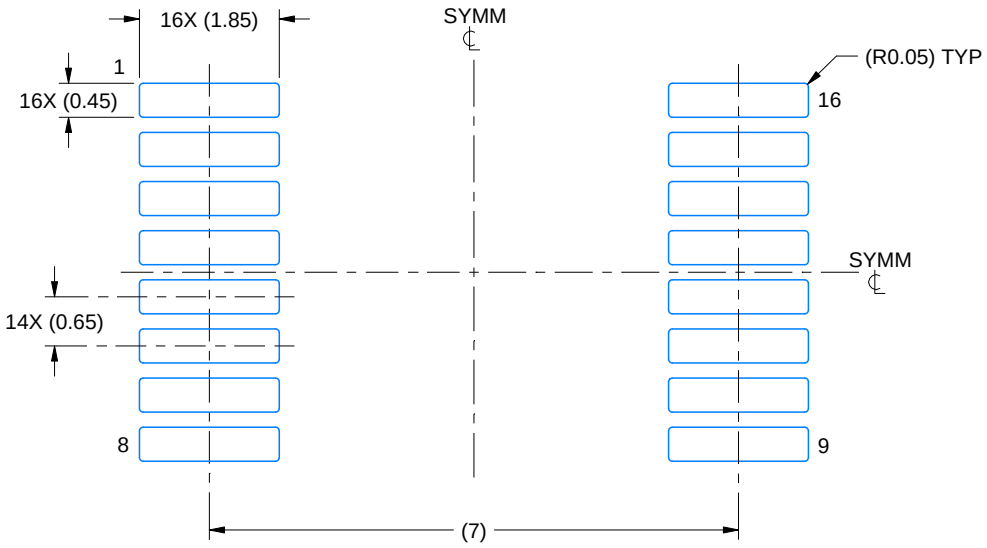
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

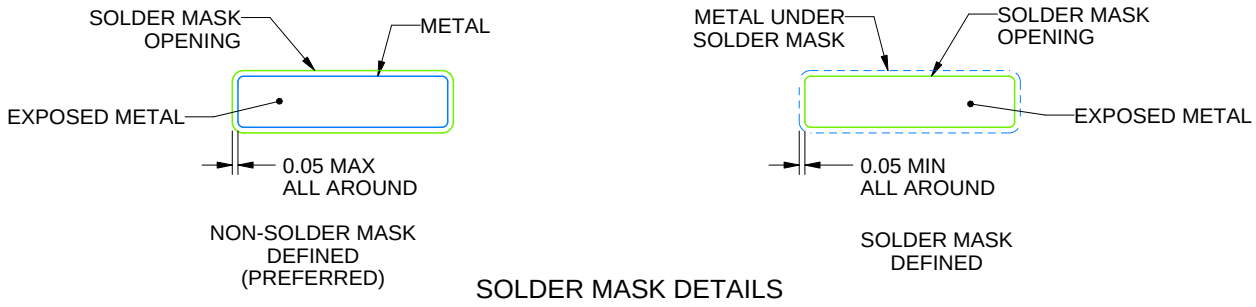
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

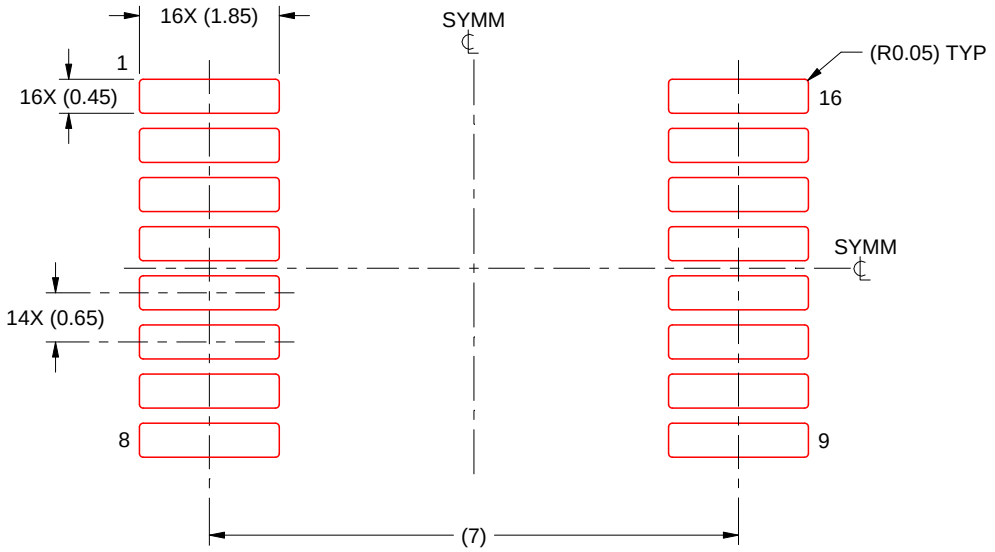
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

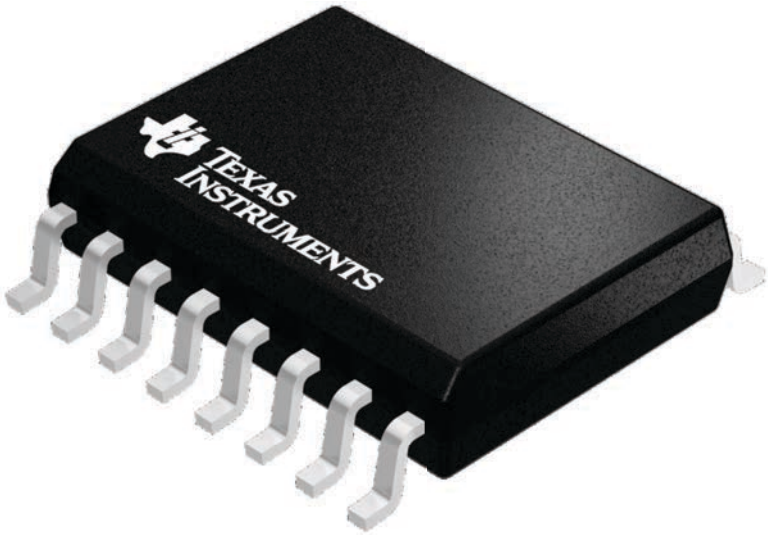
DW 16

SOIC - 2.65 mm max height

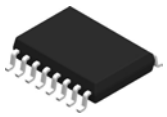
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

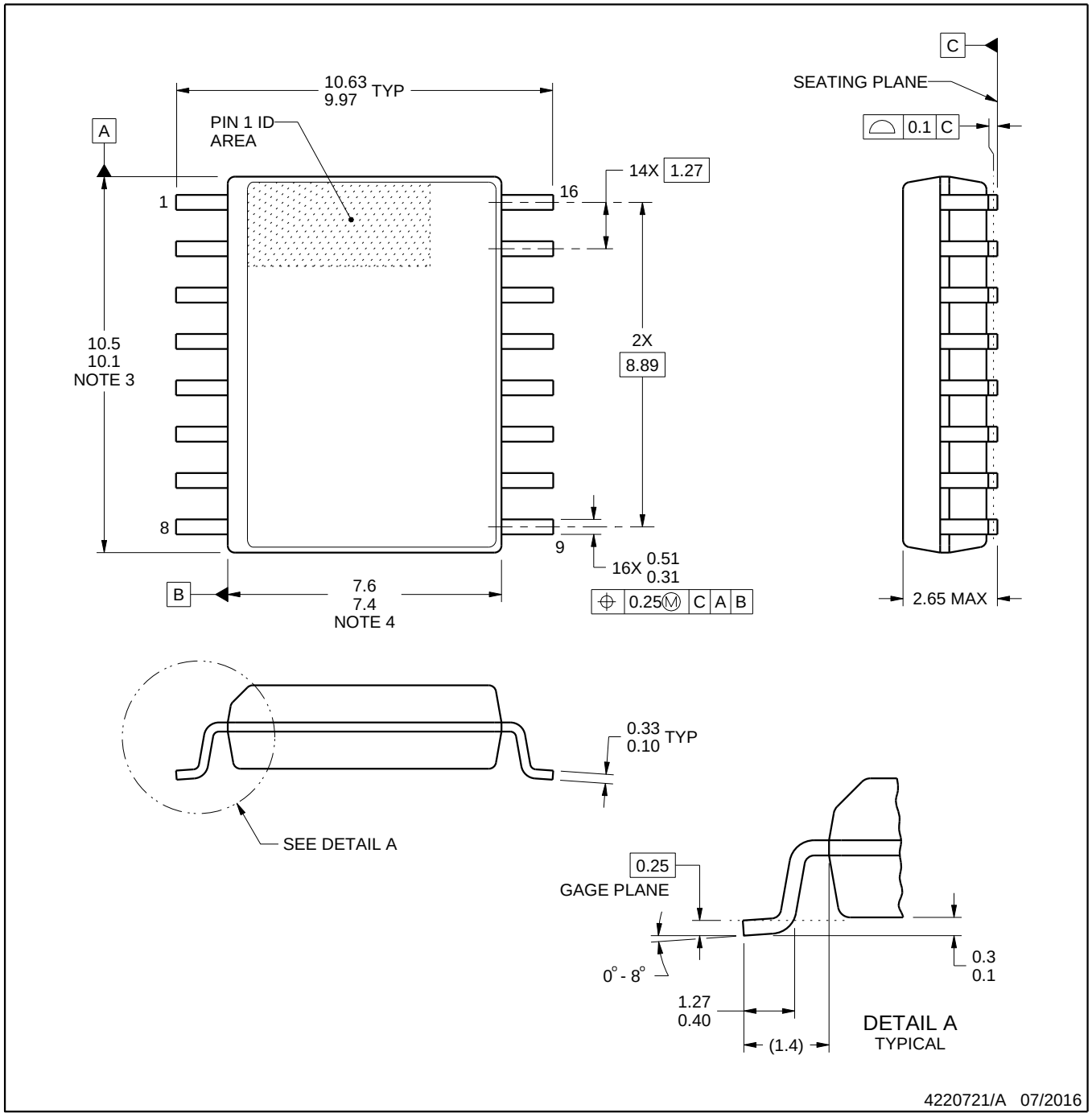


PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

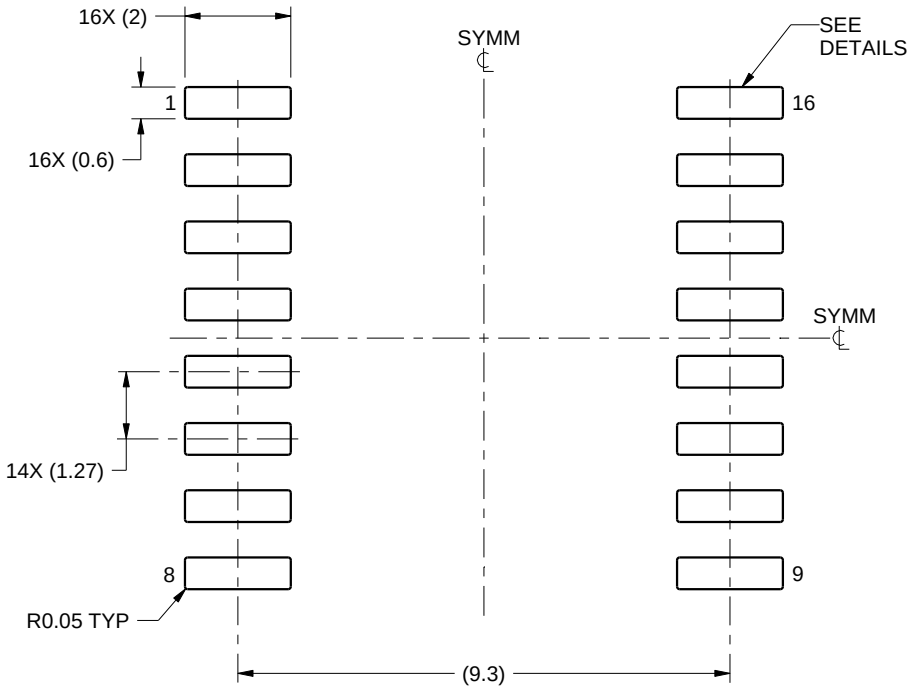
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

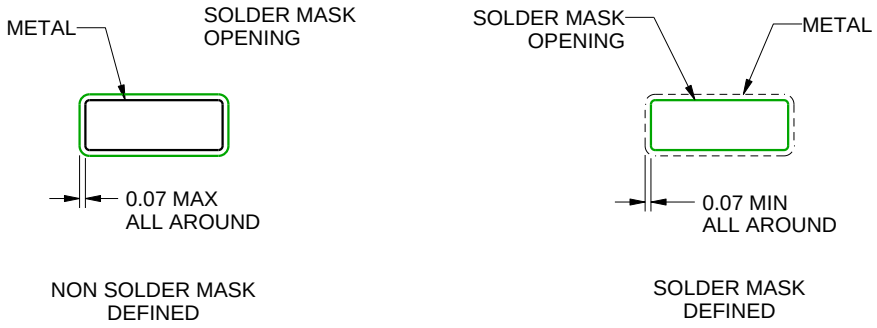
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

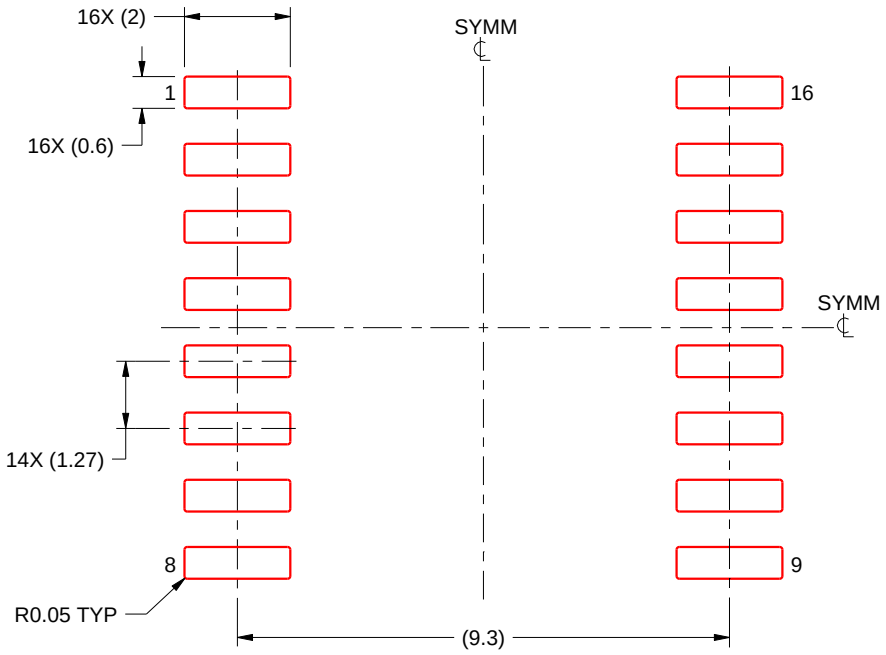
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC

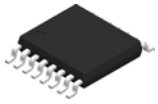


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

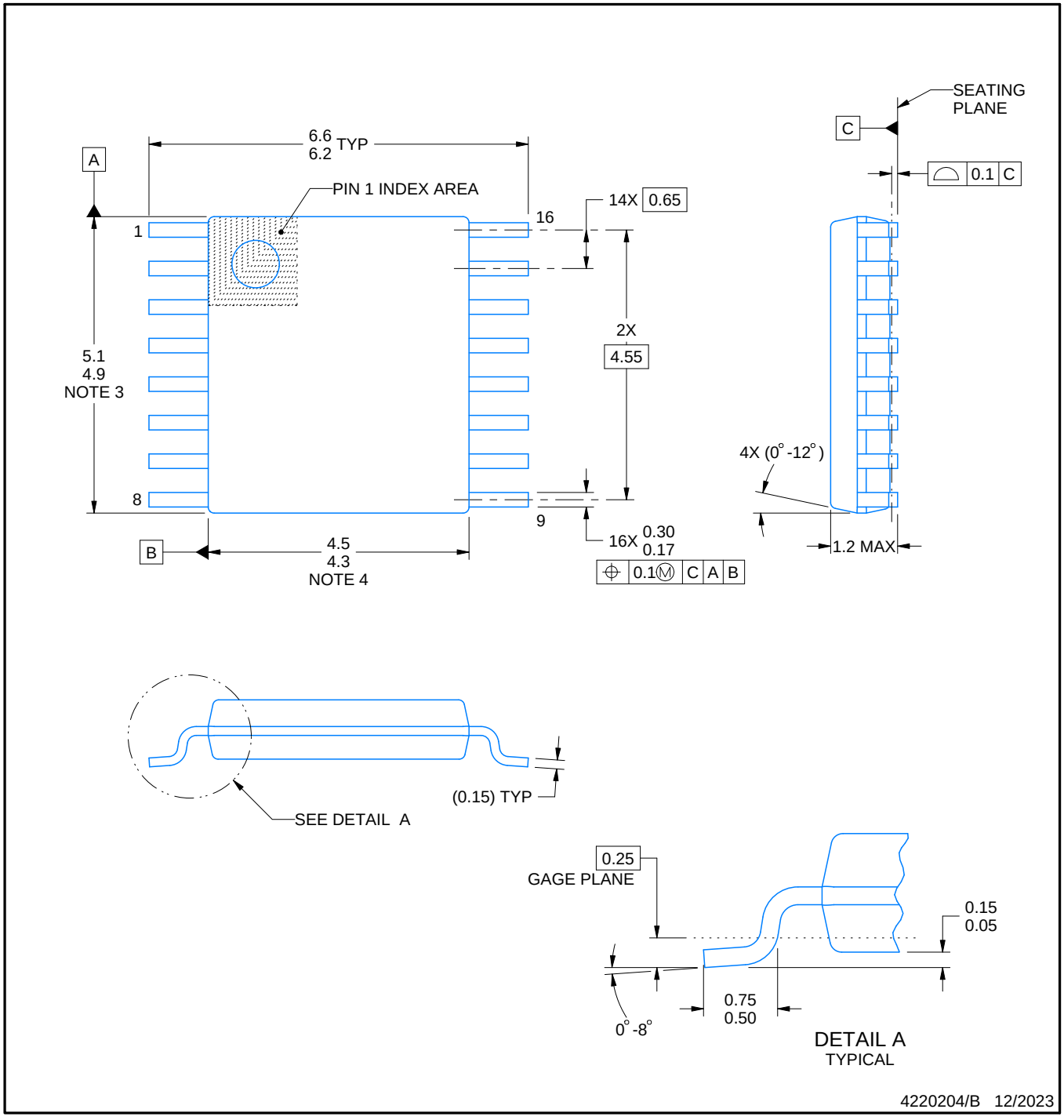


PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

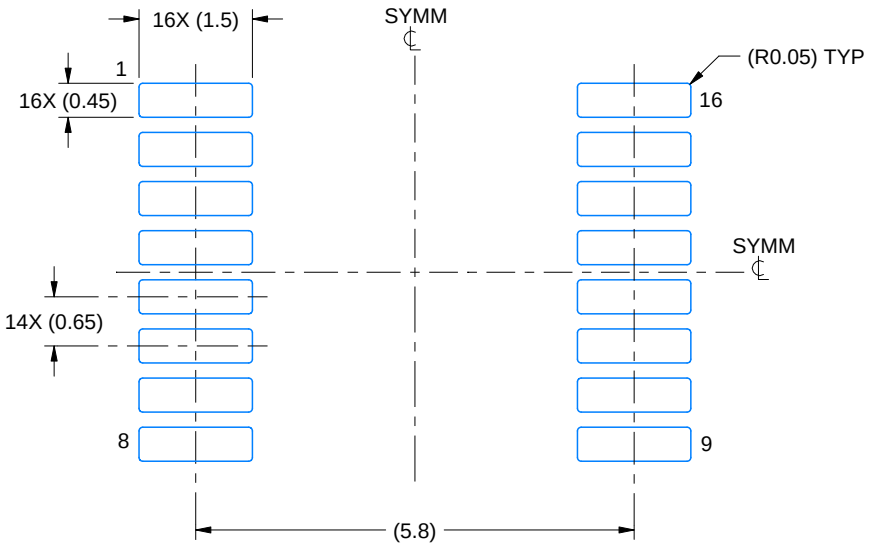
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

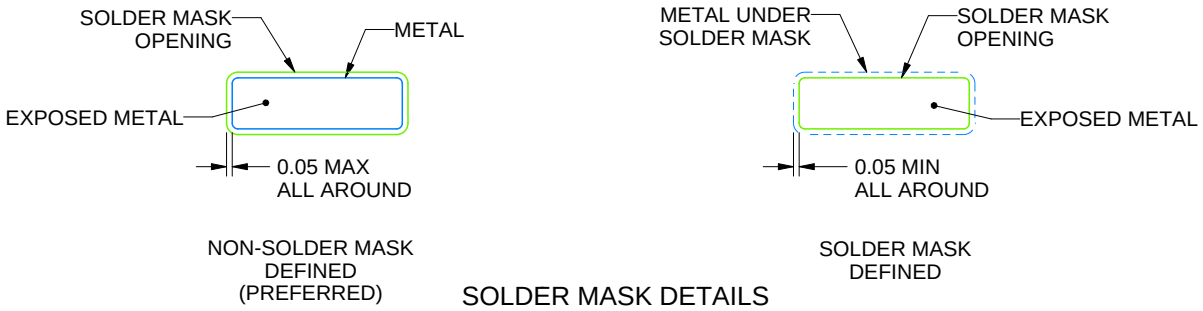
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

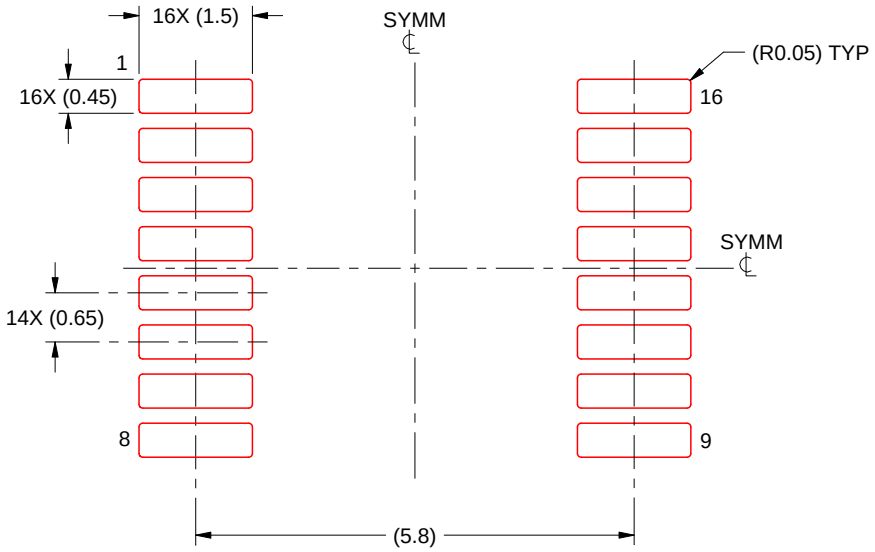
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025

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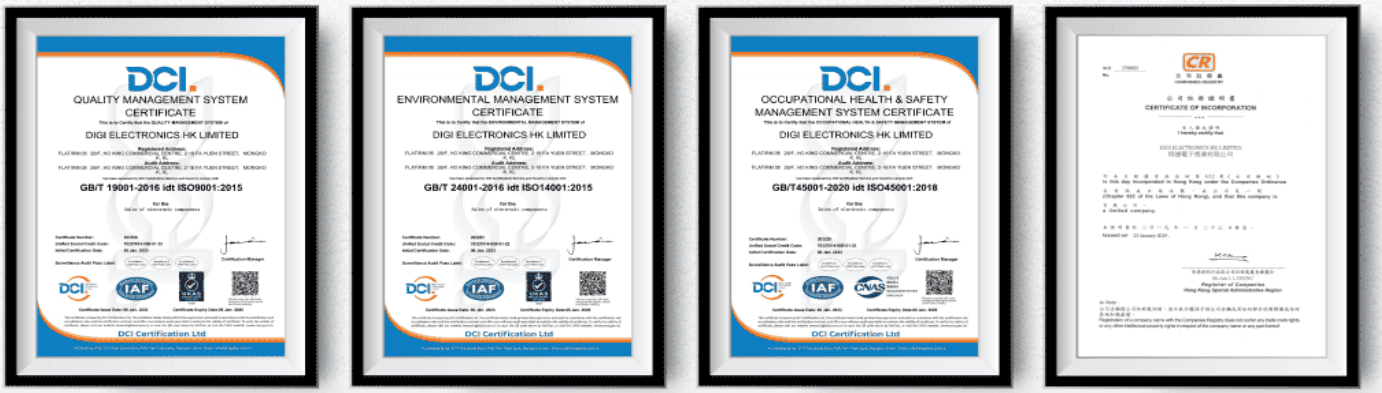

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