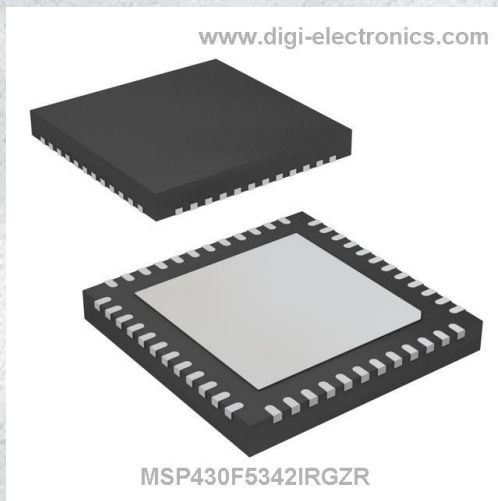


# MSP430F5342IRGZR Datasheet



<https://www.DiGi-Electronics.com>

|                              |                                                                                               |
|------------------------------|-----------------------------------------------------------------------------------------------|
| DiGi Electronics Part Number | MSP430F5342IRGZR-DG                                                                           |
| Manufacturer                 | <a href="#">Texas Instruments</a>                                                             |
| Manufacturer Product Number  | MSP430F5342IRGZR                                                                              |
| Description                  | IC MCU 16BIT 128KB FLASH 48VQFN                                                               |
| Detailed Description         | MSP430 CPUXV2 MSP430F5xx Microcontroller IC 16-Bit 25MHz 128KB (128K x 8) FLASH 48-VQFN (7x7) |



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

MSP430F5342IRGZR

Series:

MSP430F5xx

DiGi-Electronics Programmable:

Not Verified

Core Size:

16-Bit

Connectivity:

I2C, IrDA, SCI, SPI, UART/USART

Number of I/O:

38

Program Memory Type:

FLASH

RAM Size:

10K x 8

Data Converters:

A/D 9x12b

Operating Temperature:

-40°C ~ 85°C (TA)

Supplier Device Package:

48-VQFN (7x7)

Base Product Number:

MSP430F5342

Manufacturer:

Texas Instruments

Product Status:

Active

Core Processor:

MSP430 CPUXV2

Speed:

25MHz

Peripherals:

Brown-out Detect/Reset, DMA, POR, PWM, WDT

Program Memory Size:

128KB (128K x 8)

EEPROM Size:

-

Voltage - Supply (Vcc/Vdd):

1.8V ~ 3.6V

Oscillator Type:

Internal

Mounting Type:

Surface Mount

Package / Case:

48-VFQFN Exposed Pad

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.31.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99

## MSP430F534x Mixed-Signal Microcontrollers

### 1 Device Overview

#### 1.1 Features

- Low Supply-Voltage Range:  
3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
  - Active Mode (AM): All System Clocks Active
    - 290  $\mu$ A/MHz at 8 MHz, 3 V, Flash Program Execution (Typical)
    - 150  $\mu$ A/MHz at 8 MHz, 3 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3):
    - Real-Time Clock (RTC) With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:  
1.9  $\mu$ A at 2.2 V, 2.1  $\mu$ A at 3 V (Typical)
    - Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:  
1.4  $\mu$ A at 3 V (Typical)
  - Off Mode (LPM4):
    - Full RAM Retention, Supply Supervisor Operational, Fast Wakeup:  
1.1  $\mu$ A at 3 V (Typical)
  - Shutdown Mode (LPM4.5):
    - 0.18  $\mu$ A at 3 V (Typical)
- Wake up From Standby Mode in 3.5  $\mu$ s (Typical)
- 16-Bit RISC Architecture, Extended Memory, up to 25-MHz System Clock
- Flexible Power-Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Watch Crystals (XT1)
  - High-Frequency Crystals up to 32 MHz (XT2)
- 16-Bit Timer TA0, Timer\_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer TA2, Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer\_B With Seven Capture/Compare Shadow Registers
- Two Universal Serial Communication Interfaces (USCIs)
  - USCI\_A0 and USCI\_A1 Each Support:
    - Enhanced UART With Automatic Baud-Rate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI\_B0 and USCI\_B1 Each Support:
    - I<sup>2</sup>C
    - Synchronous SPI
- 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold, and Autoscan Feature
- Comparator
- Hardware Multiplier Supports 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- 3-Channel Internal DMA
- Basic Timer With RTC Feature
- [Device Comparison](#) Summarizes the Available Family Members

#### 1.2 Applications

- Analog Sensor Systems
- Digital Sensor Systems
- Data Loggers
- General-Purpose Applications



**MSP430F5342, MSP430F5341, MSP430F5340**

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### 1.3 Description

The TI MSP family of ultra-low-power microcontrollers consists of several devices that feature different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The microcontroller features a powerful 16-bit RISC CPU, 16-bit registers, and a constant generator that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the microcontroller to wake up from low-power modes to active mode in 3.5  $\mu$ s (typical).

The MSP430F534x MCU configurations feature four 16-bit timers, a high-performance 12-bit ADC, two USCIs, a hardware multiplier, DMA, an RTC module with alarm capabilities, and 38 I/O pins.

For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

**Device Information<sup>(1)</sup>**

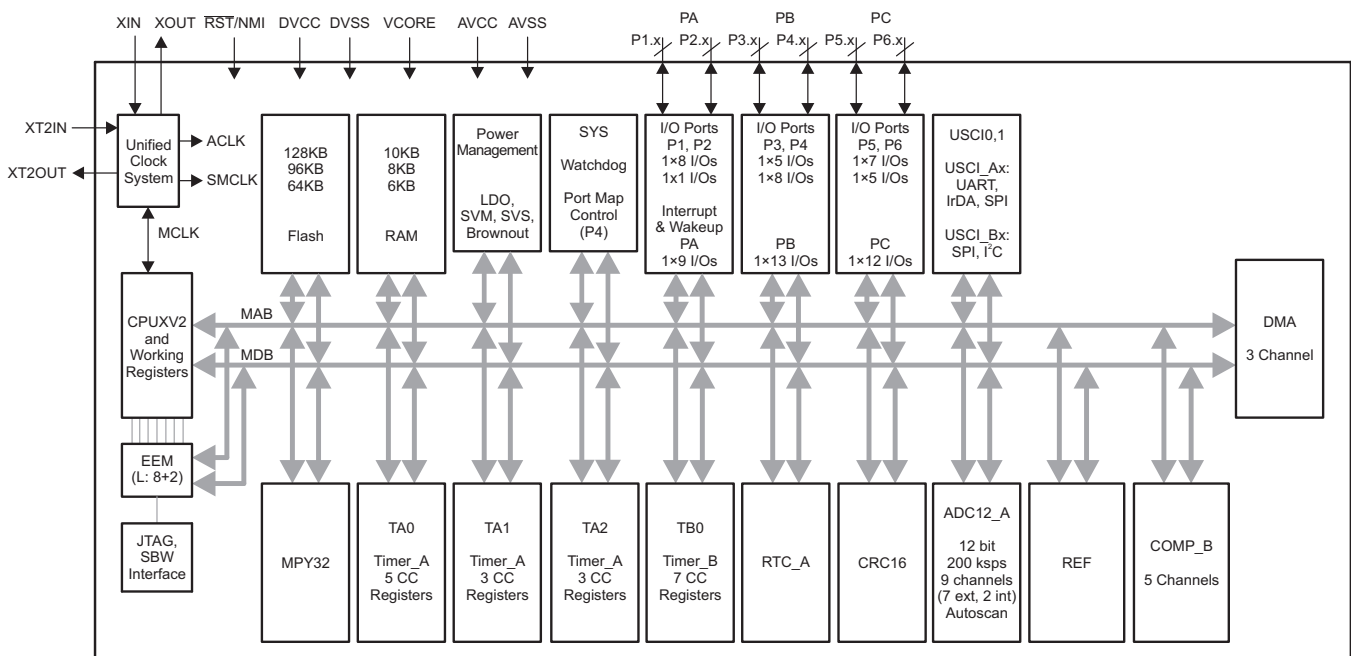
| PART NUMBER     | PACKAGE   | BODY SIZE <sup>(2)</sup> |
|-----------------|-----------|--------------------------|
| MSP430F5342IRGZ | VQFN (48) | 7 mm × 7 mm              |
| MSP430F5341IRGZ | VQFN (48) | 7 mm × 7 mm              |
| MSP430F5340IRGZ | VQFN (48) | 7 mm × 7 mm              |

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in [Section 8](#), or see the TI website at [www.ti.com](http://www.ti.com).

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 8](#).

### 1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.



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**Figure 1-1. MSP430F534x Block Diagram**

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from October 1, 2013 to September 26, 2018                                                                                                                                                                                                          | Page               |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| • Document format and organization changes throughout document, including addition of section numbering .....                                                                                                                                               | <a href="#">1</a>  |
| • Added <i>Device Information</i> table .....                                                                                                                                                                                                               | <a href="#">2</a>  |
| • Moved functional block diagram to <a href="#">Section 1.4</a> .....                                                                                                                                                                                       | <a href="#">2</a>  |
| • Added <a href="#">Section 3.1</a> , <i>Related Products</i> .....                                                                                                                                                                                         | <a href="#">5</a>  |
| • Added typical conditions statements at the beginning of <a href="#">Section 5</a> , <i>Specifications</i> .....                                                                                                                                           | <a href="#">11</a> |
| • Added <a href="#">Section 5.2</a> , <i>ESD Ratings</i> .....                                                                                                                                                                                              | <a href="#">11</a> |
| • Added note to C <sub>VCORE</sub> in <a href="#">Section 5.3</a> , <i>Recommended Operating Conditions</i> .....                                                                                                                                           | <a href="#">11</a> |
| • Moved <a href="#">Section 5.6</a> , <i>Thermal Resistance Characteristics</i> .....                                                                                                                                                                       | <a href="#">13</a> |
| • Changed the TYP value of the C <sub>L,eff</sub> parameter with Test Conditions of "XTS = 0, XCAPx = 0" from 2 pF to 1 pF in <a href="#">Section 5.15</a> , <i>Crystal Oscillator, XT1, Low-Frequency Mode</i> .....                                       | <a href="#">18</a> |
| • Changed the MIN value of V <sub>(DVCC_BOR_hys)</sub> from 60 mV to 50 mV in <a href="#">Section 5.20</a> , <i>PMM, Brownout Reset (BOR)</i> .....                                                                                                         | <a href="#">22</a> |
| • Updated notes (1) and (2) and added note (3) in <a href="#">Section 5.26</a> , <i>Wake-up Times From Low-Power Modes and Reset</i> .....                                                                                                                  | <a href="#">25</a> |
| • Removed ADC12DIV from the formula for the TYP value in the second row of the t <sub>CONVERT</sub> parameter in <a href="#">Section 5.36</a> , <i>12-Bit ADC, Timing Parameters</i> , because ADC12CLK is after division .....                             | <a href="#">31</a> |
| • Added second row for the t <sub>EN_CMP</sub> parameter with Test Conditions of "CBPWRMD = 10" and MAX value of 100 µs and removed option for "CBPWRMD = 10" from first row of Test Conditions in <a href="#">Section 5.42</a> , <i>Comparator_B</i> ..... | <a href="#">36</a> |
| • Changed all instances of "bootstrap loader" to "bootloader" throughout document .....                                                                                                                                                                     | <a href="#">42</a> |
| • Added <a href="#">Section 7</a> and moved <i>Tools Support</i> , <i>Device Nomenclature</i> , <i>ESD Caution</i> , and <i>Trademarks</i> sections to it ...                                                                                               | <a href="#">84</a> |
| • Replaced former Tools Support section with <a href="#">Section 7.3</a> , <i>Tools and Software</i> .....                                                                                                                                                  | <a href="#">86</a> |
| • Added <a href="#">Section 8</a> , <i>Mechanical, Packaging, and Orderable Information</i> .....                                                                                                                                                           | <a href="#">90</a> |

### 3 Device Comparison

Table 3-1 summarizes the available family members.

**Table 3-1. Device Comparison<sup>(1)(2)</sup>**

| DEVICE      | FLASH<br>(KB) | SRAM<br>(KB) | Timer_A <sup>(3)</sup>                 | Timer_B <sup>(4)</sup> | USCI                             |                                     | ADC12_A<br>(Ch) | Comp_B<br>(Ch) | I/Os | PACKAGE |
|-------------|---------------|--------------|----------------------------------------|------------------------|----------------------------------|-------------------------------------|-----------------|----------------|------|---------|
|             |               |              |                                        |                        | CHANNEL A:<br>UART, IrDA,<br>SPI | CHANNEL B:<br>SPI, I <sup>2</sup> C |                 |                |      |         |
| MSP430F5342 | 128           | 10           | 5, 3 <sup>(5)</sup> , 3 <sup>(6)</sup> | 7                      | 2                                | 2                                   | 7 ext, 2 int    | 5              | 38   | 48 RGZ  |
| MSP430F5341 | 96            | 8            | 5, 3 <sup>(5)</sup> , 3 <sup>(6)</sup> | 7                      | 2                                | 2                                   | 7 ext, 2 int    | 5              | 38   | 48 RGZ  |
| MSP430F5340 | 64            | 6            | 5, 3 <sup>(5)</sup> , 3 <sup>(6)</sup> | 7                      | 2                                | 2                                   | 7 ext, 2 int    | 5              | 38   | 48 RGZ  |

- (1) For the most current package and ordering information, see the *Package Option Addendum* in [Section 8](#), or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) Each number in the sequence represents an instantiation of Timer\_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (4) Each number in the sequence represents an instantiation of Timer\_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (5) Only one PWM output and one external capture input available at pin.
- (6) No PWM outputs or external capture inputs available at pins.

#### 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**Products for TI Microcontrollers** TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

**Products for MSP430 Ultra-Low-Power Microcontrollers** One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

**Companion Products for MSP430F5342** Review products that are frequently purchased or used in conjunction with this product.

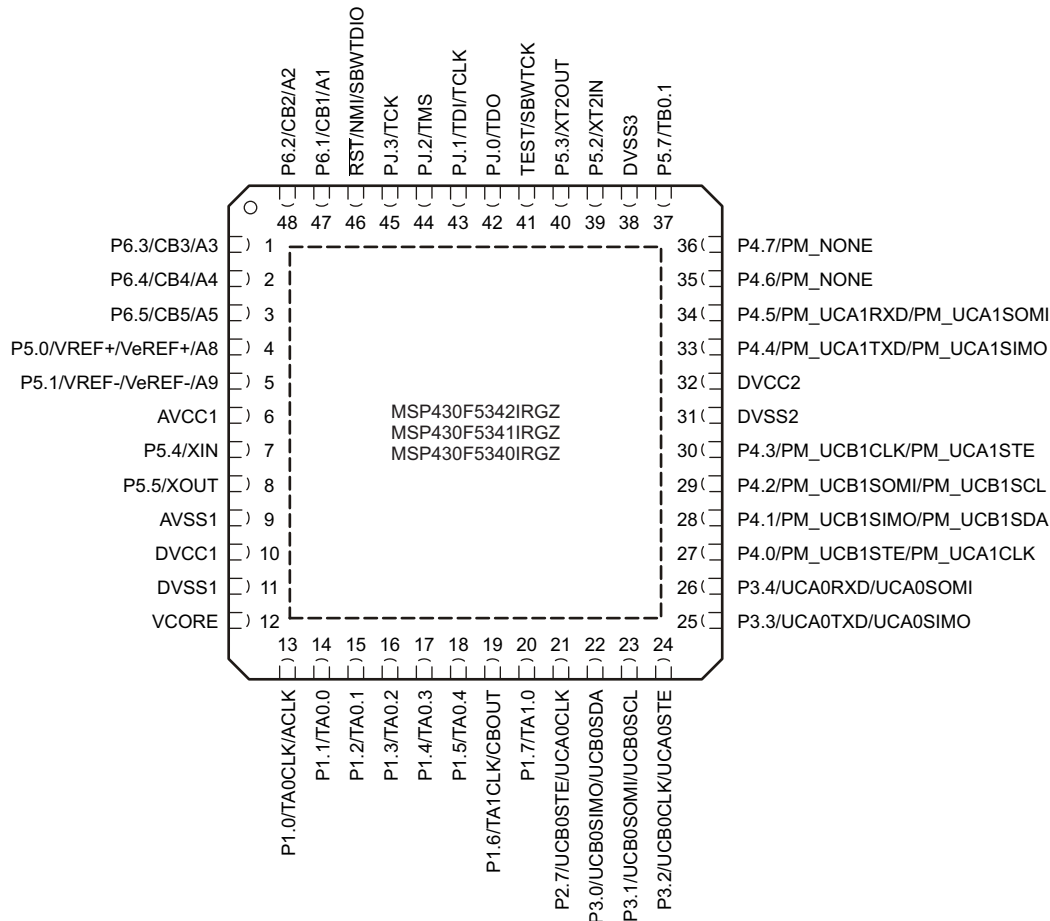
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**MSP430F5342, MSP430F5341, MSP430F5340**

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[www.ti.com](http://www.ti.com)**4 Terminal Configuration and Functions****4.1 Pin Diagram**

Figure 4-1 shows the pinout of the 48-pin RGZ package.



NOTE: TI recommends connecting the exposed thermal pad connection to V<sub>SS</sub>.

**Figure 4-1. 48-Pin RGZ Package (Top View)**

## 4.2 Signal Descriptions

Table 4-1 describes the signals.

**Table 4-1. Signal Descriptions**

| TERMINAL             |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                              |
|----------------------|-----|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                 | NO. |                    |                                                                                                                                                                                                          |
| P6.3/CB3/A3          | 1   | I/O                | General-purpose digital I/O<br>Comparator_B input CB3<br>Analog input A3 for the ADC                                                                                                                     |
| P6.4/CB4/A4          | 2   | I/O                | General-purpose digital I/O<br>Comparator_B input CB4<br>Analog input A4 for the ADC                                                                                                                     |
| P6.5/CB5/A5          | 3   | I/O                | General-purpose digital I/O<br>Comparator_B input CB5<br>Analog input A5 for the ADC                                                                                                                     |
| P5.0/A8/VREF+/VeREF+ | 4   | I/O                | General-purpose digital I/O<br>Analog input A8 for the ADC<br>Output of reference voltage to the ADC<br>Input for an external reference voltage to the ADC                                               |
| P5.1/A9/VREF-/VeREF- | 5   | I/O                | General-purpose digital I/O<br>Analog input A9 for the ADC<br>Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage |
| AVCC1                | 6   |                    | Analog power supply                                                                                                                                                                                      |
| P5.4/XIN             | 7   | I/O                | General-purpose digital I/O<br>Input terminal for crystal oscillator XT1                                                                                                                                 |
| P5.5/XOUT            | 8   | I/O                | General-purpose digital I/O<br>Output terminal of crystal oscillator XT1                                                                                                                                 |
| AVSS1                | 9   |                    | Analog ground supply                                                                                                                                                                                     |
| DVCC1                | 10  |                    | Digital power supply                                                                                                                                                                                     |
| DVSS1                | 11  |                    | Digital ground supply                                                                                                                                                                                    |
| VCORE <sup>(2)</sup> | 12  |                    | Regulated core power supply output (internal use only, no external current loading)                                                                                                                      |
| P1.0/TA0CLK/ACLK     | 13  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 clock signal TA0CLK input<br>ACLK output (divided by 1, 2, 4, 8, 16, or 32)                                                                       |
| P1.1/TA0.0           | 14  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>BSL transmit output                                                                            |
| P1.2/TA0.1           | 15  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>BSL receive input                                                                              |
| P1.3/TA0.2           | 16  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR2 capture: CCI2A input, compare: Out2 output                                                                                                   |

(1) I = input, O = output, N/A = not available

(2) VCore is for internal use only. No external current loading is possible. VCore should be connected to only the recommended capacitor value, C<sub>VCore</sub>.

**MSP430F5342, MSP430F5341, MSP430F5340**

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[www.ti.com](http://www.ti.com)**Table 4-1. Signal Descriptions (continued)**

| TERMINAL                        |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                          |
|---------------------------------|-----|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                            | NO. |                    |                                                                                                                                                                                                                                                                                      |
| P1.4/TA0.3                      | 17  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR3 capture: CCI3A input compare: Out3 output                                                                                                                                                                                |
| P1.5/TA0.4                      | 18  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR4 capture: CCI4A input, compare: Out4 output                                                                                                                                                                               |
| P1.6/TA1CLK/CBOUT               | 19  | I/O                | General-purpose digital I/O with port interrupt<br>TA1 clock signal TA1CLK input<br>Comparator_B output                                                                                                                                                                              |
| P1.7/TA1.0                      | 20  | I/O                | General-purpose digital I/O with port interrupt<br>TA1 CCR0 capture: CCI0A input, compare: Out0 output                                                                                                                                                                               |
| P2.7/UCB0STE/UCA0CLK            | 21  | I/O                | General-purpose digital I/O with port interrupt<br>Slave transmit enable for USCI_B0 SPI mode<br>Clock signal input for USCI_A0 SPI slave mode<br>Clock signal output for USCI_A0 SPI master mode                                                                                    |
| P3.0/UCB0SIMO/UCB0SDA           | 22  | I/O                | General-purpose digital I/O<br>Slave in, master out for USCI_B0 SPI mode<br>I <sup>2</sup> C data for USCI_B0 I <sup>2</sup> C mode                                                                                                                                                  |
| P3.1/UCB0SOMI/UCB0SCL           | 23  | I/O                | General-purpose digital I/O<br>Slave out, master in for USCI_B0 SPI mode<br>I <sup>2</sup> C clock for USCI_B0 I <sup>2</sup> C mode                                                                                                                                                 |
| P3.2/UCB0CLK/UCA0STE            | 24  | I/O                | General-purpose digital I/O<br>Clock signal input for USCI_B0 SPI slave mode<br>Clock signal output for USCI_B0 SPI master mode<br>Slave transmit enable for USCI_A0 SPI mode                                                                                                        |
| P3.3/UCA0TXD/UCA0SIMO           | 25  | I/O                | General-purpose digital I/O<br>Transmit data for USCI_A0 UART mode<br>Slave in, master out for USCI_A0 SPI mode                                                                                                                                                                      |
| P3.4/UCA0RXD/UCA0SOMI           | 26  | I/O                | General-purpose digital I/O<br>Receive data for USCI_A0 UART mode<br>Slave out, master in for USCI_A0 SPI mode                                                                                                                                                                       |
| P4.0/PM_UCB1STE/<br>PM_UCA1CLK  | 27  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Slave transmit enable for USCI_B1 SPI mode<br>Default mapping: Clock signal input for USCI_A1 SPI slave mode<br>Default mapping: Clock signal output for USCI_A1 SPI master mode |
| P4.1/PM_UCB1SIMO/<br>PM_UCB1SDA | 28  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Slave in, master out for USCI_B1 SPI mode<br>Default mapping: I <sup>2</sup> C data for USCI_B1 I <sup>2</sup> C mode                                                            |
| P4.2/PM_UCB1SOMI/<br>PM_UCB1SCL | 29  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Slave out, master in for USCI_B1 SPI mode<br>Default mapping: I <sup>2</sup> C clock for USCI_B1 I <sup>2</sup> C mode                                                           |

**Table 4-1. Signal Descriptions (continued)**

| TERMINAL                                            |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                          |
|-----------------------------------------------------|-----|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                | NO. |                    |                                                                                                                                                                                                                                                                                      |
| P4.3/PM_UCB1CLK/<br>PM_UCA1STE                      | 30  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Clock signal input for USCI_B1 SPI slave mode<br>Default mapping: Clock signal output for USCI_B1 SPI master mode<br>Default mapping: Slave transmit enable for USCI_A1 SPI mode |
| DVSS2                                               | 31  |                    | Digital ground supply                                                                                                                                                                                                                                                                |
| DVCC2                                               | 32  |                    | Digital power supply                                                                                                                                                                                                                                                                 |
| P4.4/PM_UCA1TXD/<br>PM_UCA1SIMO                     | 33  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Transmit data for USCI_A1 UART mode<br>Default mapping: Slave in, master out for USCI_A1 SPI mode                                                                                |
| P4.5/PM_UCA1RXD/<br>PM_UCA1SOMI                     | 34  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Receive data for USCI_A1 UART mode<br>Default mapping: Slave out, master in for USCI_A1 SPI mode                                                                                 |
| P4.6/PM_NONE                                        | 35  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: no secondary function.                                                                                                                                                           |
| P4.7/PM_NONE                                        | 36  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: no secondary function.                                                                                                                                                           |
| P5.7/TB0.1                                          | 37  | I/O                | General-purpose digital I/O<br>TB0 CCR1 capture: CCI1A input, compare: Out1 output                                                                                                                                                                                                   |
| DVSS3                                               | 38  |                    | Digital ground supply                                                                                                                                                                                                                                                                |
| P5.2/XT2IN                                          | 39  | I/O                | General-purpose digital I/O<br>Input terminal for crystal oscillator XT2                                                                                                                                                                                                             |
| P5.3/XT2OUT                                         | 40  | I/O                | General-purpose digital I/O<br>Output terminal of crystal oscillator XT2                                                                                                                                                                                                             |
| TEST/SBWTK <sup>(3)</sup>                           | 41  | I                  | Test mode pin – Selects 4-wire JTAG operation.<br>Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated                                                                                                                                                                       |
| PJ.0/TDO <sup>(4)</sup>                             | 42  | I/O                | General-purpose digital I/O<br>JTAG test data output port                                                                                                                                                                                                                            |
| PJ.1/TDI/TCLK <sup>(4)</sup>                        | 43  | I/O                | General-purpose digital I/O<br>JTAG test data input or test clock input                                                                                                                                                                                                              |
| PJ.2/TMS <sup>(4)</sup>                             | 44  | I/O                | General-purpose digital I/O<br>JTAG test mode select                                                                                                                                                                                                                                 |
| PJ.3/TCK <sup>(4)</sup>                             | 45  | I/O                | General-purpose digital I/O<br>JTAG test clock                                                                                                                                                                                                                                       |
| $\overline{\text{RST}}$ /NMI/SBWTDIO <sup>(3)</sup> | 46  | I/O                | Reset input active low <sup>(5)</sup><br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated.                                                                                                                                          |
| P6.1/CB1/A1                                         | 47  | I/O                | General-purpose digital I/O<br>Comparator_B input CB1<br>Analog input A1 for the ADC                                                                                                                                                                                                 |

(3) See [Section 6.5](#) and [Section 6.6](#) for use with BSL and JTAG functions

(4) See [Section 6.6](#) for use with JTAG function.

(5) When this pin is configured as reset, the internal pullup resistor is enabled by default.

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[www.ti.com](http://www.ti.com)**Table 4-1. Signal Descriptions (continued)**

| TERMINAL    |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                          |
|-------------|-----|--------------------|--------------------------------------------------------------------------------------|
| NAME        | NO. |                    |                                                                                      |
| P6.2/CB2/A2 | 48  | I/O                | General-purpose digital I/O<br>Comparator_B input CB2<br>Analog input A2 for the ADC |
| Thermal Pad |     |                    | QFN package pad. TI recommends connecting to V <sub>SS</sub> .                       |

## 5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                                   | MIN  | MAX            | UNIT |
|-------------------------------------------------------------------|------|----------------|------|
| Voltage applied at $V_{CC}$ to $V_{SS}$                           | −0.3 | 4.1            | V    |
| Voltage applied to any pin (excluding $V_{CORE}$ ) <sup>(2)</sup> | −0.3 | $V_{CC} + 0.3$ | V    |
| Diode current at any device pin                                   |      | ±2             | mA   |
| Storage temperature, $T_{stg}$ <sup>(3)</sup>                     | −55  | 150            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ .  $V_{CORE}$  is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### 5.2 ESD Ratings

|                                     | VALUE                                                                          | UNIT  |
|-------------------------------------|--------------------------------------------------------------------------------|-------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

### 5.3 Recommended Operating Conditions

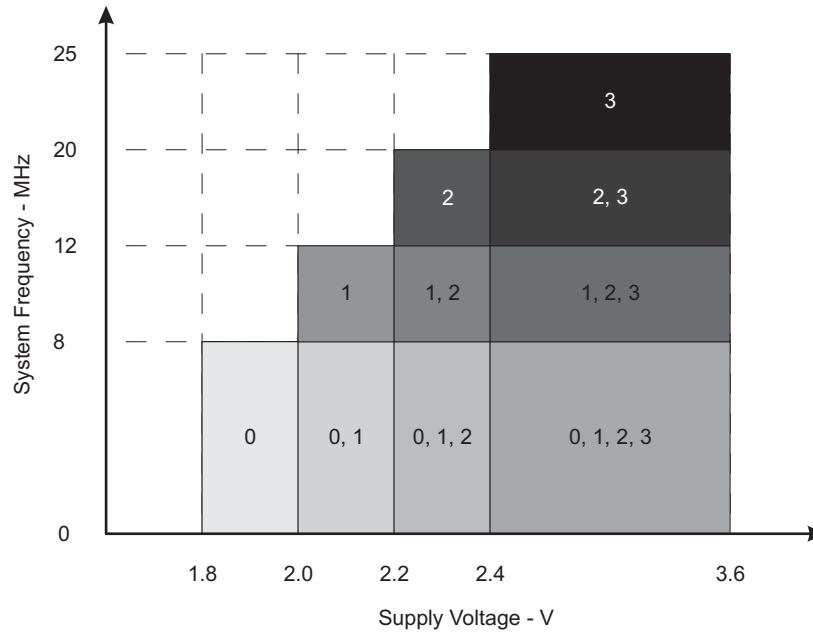
|                         |                                                                                                              | MIN | NOM | MAX  | UNIT |
|-------------------------|--------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| $V_{CC}$                | Supply voltage during program execution and flash programming ( $AVCCx = DVCCx = V_{CC}$ ) <sup>(1)(2)</sup> | 1.8 |     | 3.6  | V    |
|                         | PMMCOREVx = 0                                                                                                | 1.8 |     | 3.6  |      |
|                         | PMMCOREVx = 0, 1                                                                                             | 2.0 |     | 3.6  |      |
|                         | PMMCOREVx = 0, 1, 2                                                                                          | 2.2 |     | 3.6  |      |
|                         | PMMCOREVx = 0, 1, 2, 3                                                                                       | 2.4 |     | 3.6  |      |
| $V_{SS}$                | Supply voltage ( $AVSSx = DVSSx = V_{SS}$ )                                                                  |     | 0   |      | V    |
| $T_A$                   | Operating free-air temperature                                                                               | −40 |     | 85   | °C   |
| $T_J$                   | Operating junction temperature                                                                               | −40 |     | 85   | °C   |
| $C_{V_{CORE}}$          | Recommended capacitor at $V_{CORE}$ <sup>(3)</sup>                                                           |     | 470 |      | nF   |
| $C_{DVCC}/C_{V_{CORE}}$ | Capacitor ratio of DVCC to $V_{CORE}$                                                                        | 10  |     |      |      |
| $f_{SYSTEM}$            | Processor frequency (maximum MCLK frequency) <sup>(4)</sup> (see <a href="#">Figure 5-1</a> )                | 0   |     | 8.0  | MHz  |
|                         | PMMCOREVx = 0, 1.8 V ≤ $V_{CC}$ ≤ 3.6 V (default condition)                                                  | 0   |     | 8.0  |      |
|                         | PMMCOREVx = 1, 2.0 V ≤ $V_{CC}$ ≤ 3.6 V                                                                      | 0   |     | 12.0 |      |
|                         | PMMCOREVx = 2, 2.2 V ≤ $V_{CC}$ ≤ 3.6 V                                                                      | 0   |     | 20.0 |      |
|                         | PMMCOREVx = 3, 2.4 V ≤ $V_{CC}$ ≤ 3.6 V                                                                      | 0   |     | 25.0 |      |

- (1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [Section 5.22](#) threshold parameters for the exact values and further details.
- (3) A capacitor tolerance of ±20% or better is required.
- (4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

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NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

**Figure 5-1. Maximum System Frequency****5.4 Active Mode Supply Current Into  $V_{CC}$  Excluding External Current**over recommended operating free-air temperature (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

| PARAMETER              | EXECUTION MEMORY | V <sub>CC</sub> | PMMCOREVx | FREQUENCY (f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> ) |      |       |      |        |     |        |     |        |      | UNIT |
|------------------------|------------------|-----------------|-----------|------------------------------------------------------------------------|------|-------|------|--------|-----|--------|-----|--------|------|------|
|                        |                  |                 |           | 1 MHz                                                                  |      | 8 MHz |      | 12 MHz |     | 20 MHz |     | 25 MHz |      |      |
|                        |                  |                 |           | TYP                                                                    | MAX  | TYP   | MAX  | TYP    | MAX | TYP    | MAX | TYP    | MAX  |      |
| I <sub>AM, Flash</sub> | Flash            | 3 V             | 0         | 0.36                                                                   | 0.47 | 2.32  | 2.60 |        |     |        |     |        |      | mA   |
|                        |                  |                 | 1         | 0.40                                                                   |      | 2.65  |      | 4.0    | 4.4 |        |     |        |      |      |
|                        |                  |                 | 2         | 0.44                                                                   |      | 2.90  |      | 4.3    |     | 7.1    | 7.7 |        |      |      |
|                        |                  |                 | 3         | 0.46                                                                   |      | 3.10  |      | 4.6    |     | 7.6    |     | 10.1   | 11.0 |      |
| I <sub>AM, RAM</sub>   | RAM              | 3 V             | 0         | 0.20                                                                   | 0.24 | 1.20  | 1.30 |        |     |        |     |        |      | mA   |
|                        |                  |                 | 1         | 0.22                                                                   |      | 1.35  |      | 2.0    | 2.2 |        |     |        |      |      |
|                        |                  |                 | 2         | 0.24                                                                   |      | 1.50  |      | 2.2    |     | 3.7    | 4.2 |        |      |      |
|                        |                  |                 | 3         | 0.26                                                                   |      | 1.60  |      | 2.4    |     | 3.9    |     | 5.3    | 6.2  |      |

- (1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing.  
 $f_{ACLK} = 32786$  Hz,  $f_{DCO} = f_{MCLK} = f_{SMCLK}$  at specified frequency.  
 XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

## 5.5 Low-Power Mode Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER               |                                                   | V <sub>CC</sub> | PMMCOREVx | TEMPERATURE (T <sub>A</sub> ) |     |      |      |      |     |      |     | UNIT |
|-------------------------|---------------------------------------------------|-----------------|-----------|-------------------------------|-----|------|------|------|-----|------|-----|------|
|                         |                                                   |                 |           | –40°C                         |     | 25°C |      | 60°C |     | 85°C |     |      |
|                         |                                                   |                 |           | TYP                           | MAX | TYP  | MAX  | TYP  | MAX | TYP  | MAX |      |
| I <sub>LPM0,1MHz</sub>  | Low-power mode 0 <sup>(3)</sup> (4)               | 2.2 V           | 0         | 73                            |     | 77   | 85   | 80   |     | 85   | 97  | μA   |
|                         |                                                   | 3 V             | 3         | 79                            |     | 83   | 92   | 88   |     | 95   | 105 |      |
| I <sub>LPM2</sub>       | Low-power mode 2 <sup>(5)</sup> (4)               | 2.2 V           | 0         | 6.5                           |     | 6.5  | 12   | 10   |     | 11   | 17  | μA   |
|                         |                                                   | 3 V             | 3         | 7.0                           |     | 7.0  | 13   | 11   |     | 12   | 18  |      |
| I <sub>LPM3,XT1LF</sub> | Low-power mode 3, crystal mode <sup>(6)</sup> (4) | 2.2 V           | 0         | 1.60                          |     | 1.90 |      | 2.6  |     | 5.6  |     | μA   |
|                         |                                                   |                 | 1         | 1.65                          |     | 2.00 |      | 2.7  |     |      |     |      |
|                         |                                                   |                 | 2         | 1.75                          |     | 2.15 |      | 2.9  |     |      |     |      |
|                         |                                                   | 3 V             | 0         | 1.8                           |     | 2.1  | 2.9  | 2.8  |     | 5.8  | 8.3 |      |
|                         |                                                   |                 | 1         | 1.9                           |     | 2.3  |      | 2.9  |     | 6.1  |     |      |
|                         |                                                   |                 | 2         | 2.0                           |     | 2.4  |      | 3.0  |     | 6.3  |     |      |
|                         |                                                   |                 | 3         | 2.0                           |     | 2.5  | 3.9  | 3.1  |     | 6.4  | 9.3 |      |
| I <sub>LPM3,VLO</sub>   | Low-power mode 3, VLO mode <sup>(7)</sup> (4)     | 3 V             | 0         | 1.1                           |     | 1.4  | 2.7  | 1.9  |     | 4.9  | 7.4 | μA   |
|                         |                                                   |                 | 1         | 1.1                           |     | 1.4  |      | 2.0  |     | 5.2  |     |      |
|                         |                                                   |                 | 2         | 1.2                           |     | 1.5  |      | 2.1  |     | 5.3  |     |      |
|                         |                                                   |                 | 3         | 1.3                           |     | 1.6  | 3.0  | 2.2  |     | 5.4  | 8.5 |      |
| I <sub>LPM4</sub>       | Low-power mode 4 <sup>(8)</sup> (4)               | 3 V             | 0         | 0.9                           |     | 1.1  | 1.5  | 1.8  |     | 4.8  | 7.3 | μA   |
|                         |                                                   |                 | 1         | 1.1                           |     | 1.2  |      | 2.0  |     | 5.1  |     |      |
|                         |                                                   |                 | 2         | 1.2                           |     | 1.2  |      | 2.1  |     | 5.2  |     |      |
|                         |                                                   |                 | 3         | 1.3                           |     | 1.3  | 1.6  | 2.2  |     | 5.3  | 8.1 |      |
| I <sub>LPM4.5</sub>     | Low-power mode 4.5 <sup>(9)</sup>                 | 3 V             |           | 0.15                          |     | 0.18 | 0.35 | 0.26 |     | 0.5  | 1.0 | μA   |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).

CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0),  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  = 0 MHz,  $f_{SMCLK}$  =  $f_{DCO}$  = 1 MHz

(4) Current for brownout, high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM<sub>L</sub>) disabled. High-side monitor (SVM<sub>H</sub>) disabled. RAM retention enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).

CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2),  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  = 0 MHz,  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz, DCO setting = 1-MHz operation, DCO bias generator enabled.)

(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3),  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz

(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3),  $f_{ACLK}$  =  $f_{VLO}$ ,  $f_{MCLK}$  =  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4),  $f_{DCO}$  =  $f_{ACLK}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

(9) Internal regulator disabled. No data retention.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5),  $f_{DCO}$  =  $f_{ACLK}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

## 5.6 Thermal Resistance Characteristics, VQFN (RGZ) Package

| THERMAL METRIC |                                                   |                         | VALUE | UNIT |
|----------------|---------------------------------------------------|-------------------------|-------|------|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air | High-K board (JESD51-7) | 27.8  | °C/W |
| $R\theta_{JC}$ | Junction-to-case thermal resistance               |                         | 13.6  | °C/W |
| $R\theta_{JB}$ | Junction-to-board thermal resistance              |                         | 4.7   | °C/W |

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## 5.7 Schmitt-Trigger Inputs – General-Purpose I/O<sup>(1)</sup>

(P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7)  
(P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                        | TEST CONDITIONS                                                                                  | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------|------|-----|------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                          |                                                                                                  | 1.8 V           | 0.80 |     | 1.40 | V    |
|                                                                                  |                                                                                                  | 3 V             | 1.50 |     | 2.10 |      |
| V <sub>IT-</sub> Negative-going input threshold voltage                          |                                                                                                  | 1.8 V           | 0.45 |     | 1.00 | V    |
|                                                                                  |                                                                                                  | 3 V             | 0.75 |     | 1.65 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> ) |                                                                                                  | 1.8 V           | 0.3  |     | 0.8  | V    |
|                                                                                  |                                                                                                  | 3 V             | 0.4  |     | 1.0  |      |
| R <sub>Pull</sub> Pullup/pulldown resistor <sup>(2)</sup>                        | For pullup: V <sub>IN</sub> = V <sub>SS</sub><br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I</sub> Input capacitance                                                 | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                             |                 |      | 5   |      | pF   |

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

(2) Also applies to RST pin when pullup or pulldown resistor is enabled.

## 5.8 Inputs – Ports P1 and P2<sup>(1)</sup>

(P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                   | TEST CONDITIONS                                       | V <sub>CC</sub> | MIN | MAX | UNIT |
|-------------------------------------------------------------|-------------------------------------------------------|-----------------|-----|-----|------|
| t <sub>(int)</sub> External interrupt timing <sup>(2)</sup> | External trigger pulse duration to set interrupt flag | 2.2 V, 3 V      | 20  |     | ns   |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.

## 5.9 Leakage Current – General-Purpose I/O

(P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7)  
(P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                             | TEST CONDITIONS | V <sub>CC</sub> | MIN | MAX | UNIT |
|-------------------------------------------------------|-----------------|-----------------|-----|-----|------|
| I <sub>lkg(Px.y)</sub> High-impedance leakage current | (1) (2)         | 1.8 V, 3 V      |     | ±50 | nA   |

(1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## 5.10 Outputs – General-Purpose I/O (Full Drive Strength) (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Section 5.14](#))

| PARAMETER                                 | TEST CONDITIONS                              | V <sub>CC</sub> | MIN                    | MAX                    | UNIT |
|-------------------------------------------|----------------------------------------------|-----------------|------------------------|------------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = –3 mA <sup>(1)</sup>  | 1.8 V           | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        | V    |
|                                           | I <sub>(OHmax)</sub> = –10 mA <sup>(2)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –5 mA <sup>(1)</sup>  | 3 V             | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –15 mA <sup>(2)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 3 mA <sup>(1)</sup>   | 1.8 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 | V    |
|                                           | I <sub>(OLmax)</sub> = 10 mA <sup>(2)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |
|                                           | I <sub>(OLmax)</sub> = 5 mA <sup>(1)</sup>   | 3 V             | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 |      |
|                                           | I <sub>(OLmax)</sub> = 15 mA <sup>(2)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |

- (1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

## 5.11 Outputs – General-Purpose I/O (Reduced Drive Strength) (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup> (see [Section 5.13](#))

| PARAMETER                                 | TEST CONDITIONS                             | V <sub>CC</sub> | MIN                    | MAX                    | UNIT |
|-------------------------------------------|---------------------------------------------|-----------------|------------------------|------------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = –1 mA <sup>(2)</sup> | 1.8 V           | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        | V    |
|                                           | I <sub>(OHmax)</sub> = –3 mA <sup>(3)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –2 mA <sup>(2)</sup> | 3 V             | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –6 mA <sup>(3)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 1 mA <sup>(2)</sup>  | 1.8 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 | V    |
|                                           | I <sub>(OLmax)</sub> = 3 mA <sup>(3)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |
|                                           | I <sub>(OLmax)</sub> = 2 mA <sup>(2)</sup>  | 3 V             | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 |      |
|                                           | I <sub>(OLmax)</sub> = 6 mA <sup>(3)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |

- (1) Selecting reduced drive strength may reduce EMI.
- (2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
- (3) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

## 5.12 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                           | TEST CONDITIONS                                                 | MIN                                    | MAX | UNIT |
|-----------------------------------------------------|-----------------------------------------------------------------|----------------------------------------|-----|------|
| f <sub>Px,y</sub> Port output frequency (with load) | See <sup>(1)</sup> <sup>(2)</sup>                               | V <sub>CC</sub> = 1.8 V, PMMCOREVx = 0 | 16  | MHz  |
|                                                     |                                                                 | V <sub>CC</sub> = 3 V, PMMCOREVx = 3   | 25  |      |
| f <sub>Port_CLK</sub> Clock output frequency        | ACLK, SMCLK, or MCLK ,<br>C <sub>L</sub> = 20 pF <sup>(2)</sup> | V <sub>CC</sub> = 1.8 V, PMMCOREVx = 0 | 16  | MHz  |
|                                                     |                                                                 | V <sub>CC</sub> = 3 V, PMMCOREVx = 3   | 25  |      |

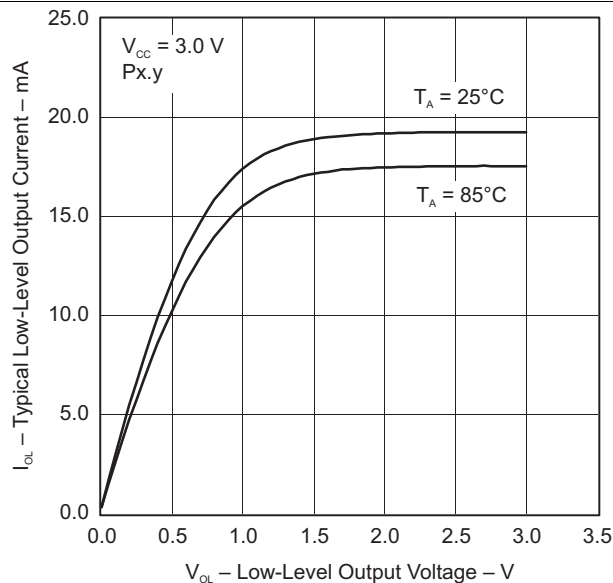
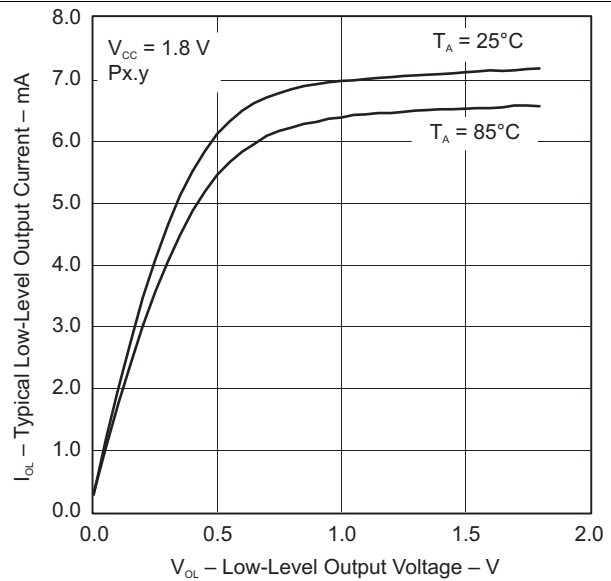
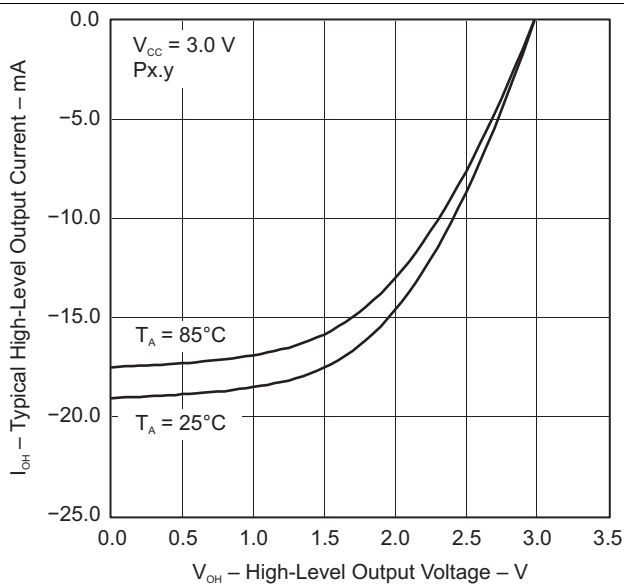
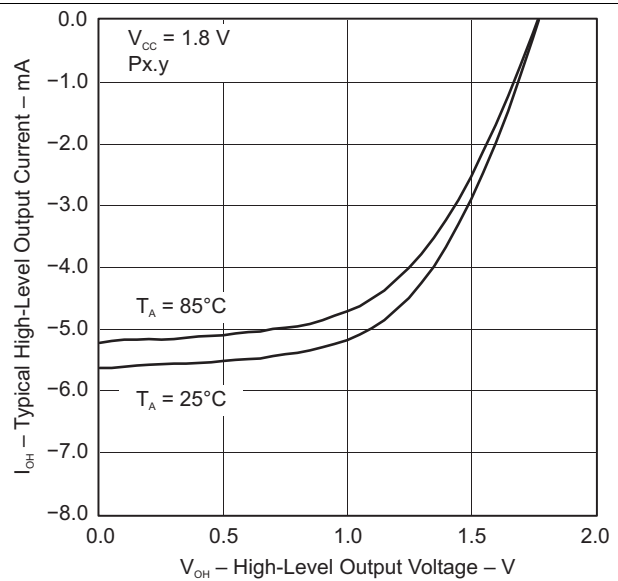
- (1) A resistive divider with 2 × R<sub>1</sub> between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider. For full drive strength, R<sub>1</sub> = 550 Ω. For reduced drive strength, R<sub>1</sub> = 1.6 kΩ. C<sub>L</sub> = 20 pF is connected to the output to V<sub>SS</sub>.
- (2) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

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**5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

**Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage****Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage****Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage****Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage**

## 5.14 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

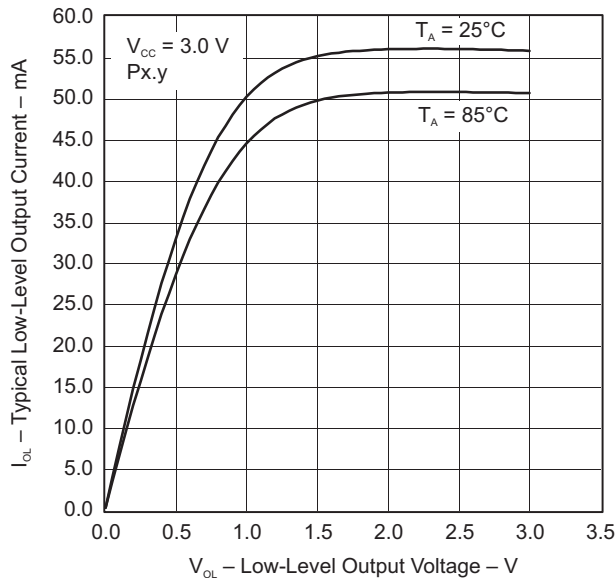


**Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage**

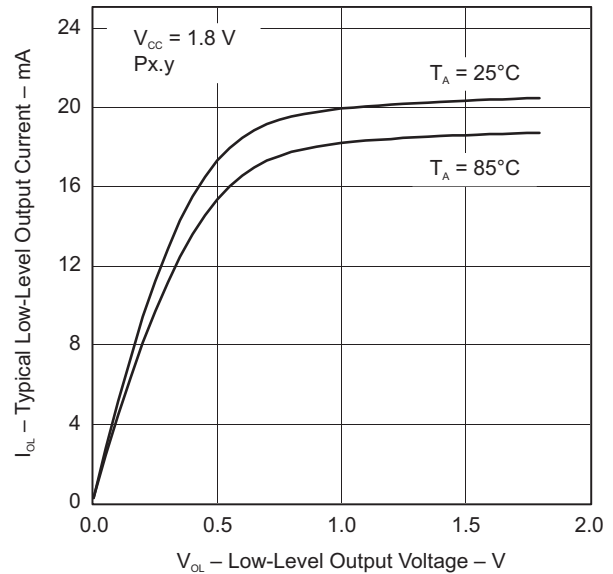


**Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage**

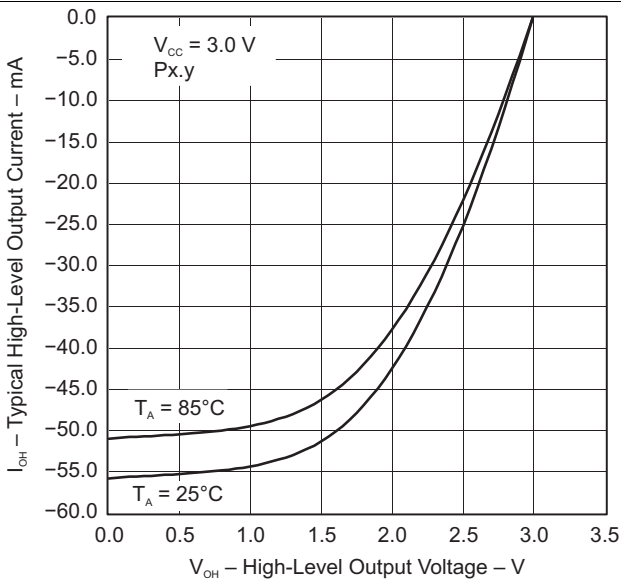


**Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage**

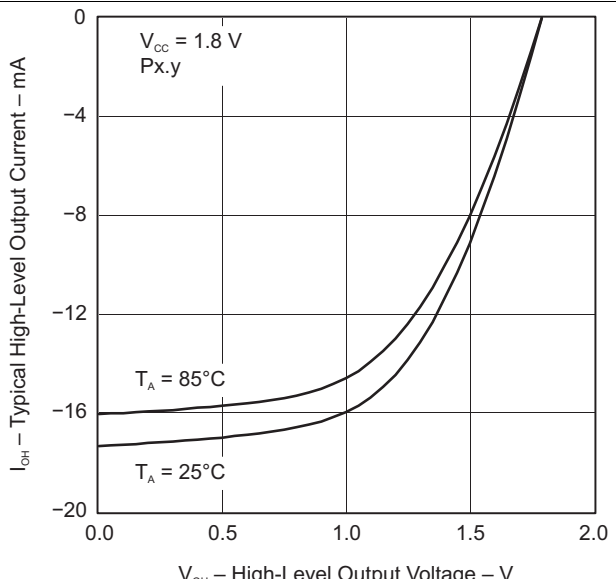


**Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage**

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[www.ti.com](http://www.ti.com)**5.15 Crystal Oscillator, XT1, Low-Frequency Mode<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                                            | TEST CONDITIONS                                                                                                                   | V <sub>CC</sub> | MIN   | TYP    | MAX | UNIT |
|------------------------|--------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|--------|-----|------|
| $\Delta I_{DVCC,LF}$   | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 1, T <sub>A</sub> = 25°C                             | 3 V             | 0.075 |        | μA  |      |
|                        |                                                                                            | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 2, T <sub>A</sub> = 25°C                             |                 | 0.170 |        |     |      |
|                        |                                                                                            | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 3, T <sub>A</sub> = 25°C                             |                 | 0.290 |        |     |      |
| f <sub>XT1,LF0</sub>   | XT1 oscillator crystal frequency, LF mode                                                  | XTS = 0, XT1BYPASS = 0                                                                                                            |                 | 32768 |        | Hz  |      |
| f <sub>XT1,LF,SW</sub> | XT1 oscillator logic-level square-wave input frequency, LF mode                            | XTS = 0, XT1BYPASS = 1 <sup>(2)</sup> <sup>(3)</sup>                                                                              |                 | 10    | 32.768 | 50  | kHz  |
| OA <sub>LF</sub>       | Oscillation allowance for LF crystals <sup>(4)</sup>                                       | XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 0, f <sub>XT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF                      |                 | 210   |        | kΩ  |      |
|                        |                                                                                            | XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 1, f <sub>XT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 12 pF                     |                 | 300   |        |     |      |
| C <sub>L,eff</sub>     | Integrated effective load capacitance, LF mode <sup>(5)</sup>                              | XTS = 0, XCAP <sub>x</sub> = 0 <sup>(6)</sup>                                                                                     |                 | 1     |        | pF  |      |
|                        |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 1                                                                                                    |                 | 5.5   |        |     |      |
|                        |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 2                                                                                                    |                 | 8.5   |        |     |      |
|                        |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 3                                                                                                    |                 | 12.0  |        |     |      |
| Duty cycle, LF mode    |                                                                                            | XTS = 0, Measured at ACLK, f <sub>XT1,LF</sub> = 32768 Hz                                                                         |                 | 30%   | 70%    |     |      |
| f <sub>Fault,LF</sub>  | Oscillator fault frequency, LF mode <sup>(7)</sup>                                         | XTS = 0 <sup>(8)</sup>                                                                                                            |                 | 10    | 10000  |     | Hz   |
| t <sub>START,LF</sub>  | Start-up time, LF mode                                                                     | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 0, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 6 pF  | 3 V             | 1000  |        | ms  |      |
|                        |                                                                                            | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 3, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 12 pF |                 | 500   |        |     |      |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  - Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE<sub>x</sub> settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  - For XT1DRIVE<sub>x</sub> = 0, C<sub>L,eff</sub> ≤ 6 pF.
  - For XT1DRIVE<sub>x</sub> = 1, 6 pF ≤ C<sub>L,eff</sub> ≤ 9 pF.
  - For XT1DRIVE<sub>x</sub> = 2, 6 pF ≤ C<sub>L,eff</sub> ≤ 10 pF.
  - For XT1DRIVE<sub>x</sub> = 3, C<sub>L,eff</sub> ≥ 6 pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

## 5.16 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                                                                                  | TEST CONDITIONS                                                                                                         | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| I <sub>DVCC,XT2</sub> XT2 oscillator crystal current consumption                           | f <sub>OSC</sub> = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>Ex</sub> = 0, T <sub>A</sub> = 25°C                  | 3 V             |     | 200 |     | μA   |
|                                                                                            | f <sub>OSC</sub> = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>Ex</sub> = 1, T <sub>A</sub> = 25°C                 |                 |     | 260 |     |      |
|                                                                                            | f <sub>OSC</sub> = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>Ex</sub> = 2, T <sub>A</sub> = 25°C                 |                 |     | 325 |     |      |
|                                                                                            | f <sub>OSC</sub> = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>Ex</sub> = 3, T <sub>A</sub> = 25°C                 |                 |     | 450 |     |      |
| f <sub>XT2,HF0</sub> XT2 oscillator crystal frequency, mode 0                              | XT2DRIVE <sub>Ex</sub> = 0, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 4   |     | 8   | MHz  |
| f <sub>XT2,HF1</sub> XT2 oscillator crystal frequency, mode 1                              | XT2DRIVE <sub>Ex</sub> = 1, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 8   |     | 16  | MHz  |
| f <sub>XT2,HF2</sub> XT2 oscillator crystal frequency, mode 2                              | XT2DRIVE <sub>Ex</sub> = 2, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 16  |     | 24  | MHz  |
| f <sub>XT2,HF3</sub> XT2 oscillator crystal frequency, mode 3                              | XT2DRIVE <sub>Ex</sub> = 3, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 24  |     | 32  | MHz  |
| f <sub>XT2,HF,SW</sub> XT2 oscillator logic-level square-wave input frequency, bypass mode | XT2BYPASS = 1 <sup>(4) (3)</sup>                                                                                        |                 | 0.7 |     | 32  | MHz  |
| O <sub>AHF</sub> Oscillation allowance for HF crystals <sup>(5)</sup>                      | XT2DRIVE <sub>Ex</sub> = 0, XT2BYPASS = 0, f <sub>XT2,HF0</sub> = 6 MHz, C <sub>L,eff</sub> = 15 pF                     |                 |     | 450 |     | Ω    |
|                                                                                            | XT2DRIVE <sub>Ex</sub> = 1, XT2BYPASS = 0, f <sub>XT2,HF1</sub> = 12 MHz, C <sub>L,eff</sub> = 15 pF                    |                 |     | 320 |     |      |
|                                                                                            | XT2DRIVE <sub>Ex</sub> = 2, XT2BYPASS = 0, f <sub>XT2,HF2</sub> = 20 MHz, C <sub>L,eff</sub> = 15 pF                    |                 |     | 200 |     |      |
|                                                                                            | XT2DRIVE <sub>Ex</sub> = 3, XT2BYPASS = 0, f <sub>XT2,HF3</sub> = 32 MHz, C <sub>L,eff</sub> = 15 pF                    |                 |     | 200 |     |      |
| t <sub>START,HF</sub> Start-up time                                                        | f <sub>OSC</sub> = 6 MHz, XT2BYPASS = 0, XT2DRIVE <sub>Ex</sub> = 0, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 15 pF  | 3 V             |     | 0.5 |     | ms   |
|                                                                                            | f <sub>OSC</sub> = 20 MHz, XT2BYPASS = 0, XT2DRIVE <sub>Ex</sub> = 2, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 15 pF |                 |     | 0.3 |     |      |
| C <sub>L,eff</sub> Integrated effective load capacitance, HF mode <sup>(6) (1)</sup>       |                                                                                                                         |                 |     | 1   |     | pF   |
| Duty cycle                                                                                 | Measured at ACLK, f <sub>XT2,HF2</sub> = 20 MHz                                                                         |                 | 40% | 50% | 60% |      |
| f <sub>Fault,HF</sub> Oscillator fault frequency <sup>(7)</sup>                            | XT2BYPASS = 1 <sup>(8)</sup>                                                                                            |                 | 30  |     | 300 | kHz  |

- (1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.
- (2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
  - Keep the traces between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
  - Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
  - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.
- (4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
- (6) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

**MSP430F5342, MSP430F5341, MSP430F5340**

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[www.ti.com](http://www.ti.com)**5.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub>                    | VLO frequency                      | Measured at ACLK                | 1.8 V to 3.6 V  | 6   | 9.4 | 14  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | Measured at ACLK <sup>(1)</sup> | 1.8 V to 3.6 V  |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | Measured at ACLK <sup>(2)</sup> | 1.8 V to 3.6 V  |     | 4   |     | %/V  |
|                                     | Duty cycle                         | Measured at ACLK                | 1.8 V to 3.6 V  | 40% | 50% | 60% |      |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

**5.18 Internal Reference, Low-Frequency Oscillator (REFO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                            |                                     | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP   | MAX   | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-----|-------|-------|------|
| I <sub>REFO</sub>                    | REFO oscillator current consumption | T <sub>A</sub> = 25°C           | 1.8 V to 3.6 V  |     | 3     |       | μA   |
| f <sub>REFO</sub>                    | REFO frequency calibrated           | Measured at ACLK                | 1.8 V to 3.6 V  |     | 32768 |       | Hz   |
|                                      | REFO absolute tolerance calibrated  | Full temperature range          | 1.8 V to 3.6 V  |     |       | ±3.5% |      |
|                                      |                                     | T <sub>A</sub> = 25°C           | 3 V             |     |       | ±1.5% |      |
| df <sub>REFO</sub> /dT               | REFO frequency temperature drift    | Measured at ACLK <sup>(1)</sup> | 1.8 V to 3.6 V  |     | 0.01  |       | %/°C |
| df <sub>REFO</sub> /dV <sub>CC</sub> | REFO frequency supply voltage drift | Measured at ACLK <sup>(2)</sup> | 1.8 V to 3.6 V  |     | 1.0   |       | %/V  |
|                                      | Duty cycle                          | Measured at ACLK                | 1.8 V to 3.6 V  | 40% | 50%   | 60%   |      |
| t <sub>START</sub>                   | REFO start-up time                  | 40%/60% duty cycle              | 1.8 V to 3.6 V  |     | 25    |       | μs   |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

## 5.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                        | TEST CONDITIONS                                              | MIN                                                                                                           | TYP  | MAX  | UNIT    |
|----------------------------------|--------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|------|------|---------|
| $f_{\text{DCO}(0,0)}$            | DCO frequency (0, 0) <sup>(1)</sup>                          | DCORSELx = 0, DCOx = 0, MODx = 0                                                                              | 0.07 | 0.20 | MHz     |
| $f_{\text{DCO}(0,31)}$           | DCO frequency (0, 31) <sup>(1)</sup>                         | DCORSELx = 0, DCOx = 31, MODx = 0                                                                             | 0.70 | 1.70 | MHz     |
| $f_{\text{DCO}(1,0)}$            | DCO frequency (1, 0) <sup>(1)</sup>                          | DCORSELx = 1, DCOx = 0, MODx = 0                                                                              | 0.15 | 0.36 | MHz     |
| $f_{\text{DCO}(1,31)}$           | DCO frequency (1, 31) <sup>(1)</sup>                         | DCORSELx = 1, DCOx = 31, MODx = 0                                                                             | 1.47 | 3.45 | MHz     |
| $f_{\text{DCO}(2,0)}$            | DCO frequency (2, 0) <sup>(1)</sup>                          | DCORSELx = 2, DCOx = 0, MODx = 0                                                                              | 0.32 | 0.75 | MHz     |
| $f_{\text{DCO}(2,31)}$           | DCO frequency (2, 31) <sup>(1)</sup>                         | DCORSELx = 2, DCOx = 31, MODx = 0                                                                             | 3.17 | 7.38 | MHz     |
| $f_{\text{DCO}(3,0)}$            | DCO frequency (3, 0) <sup>(1)</sup>                          | DCORSELx = 3, DCOx = 0, MODx = 0                                                                              | 0.64 | 1.51 | MHz     |
| $f_{\text{DCO}(3,31)}$           | DCO frequency (3, 31) <sup>(1)</sup>                         | DCORSELx = 3, DCOx = 31, MODx = 0                                                                             | 6.07 | 14.0 | MHz     |
| $f_{\text{DCO}(4,0)}$            | DCO frequency (4, 0) <sup>(1)</sup>                          | DCORSELx = 4, DCOx = 0, MODx = 0                                                                              | 1.3  | 3.2  | MHz     |
| $f_{\text{DCO}(4,31)}$           | DCO frequency (4, 31) <sup>(1)</sup>                         | DCORSELx = 4, DCOx = 31, MODx = 0                                                                             | 12.3 | 28.2 | MHz     |
| $f_{\text{DCO}(5,0)}$            | DCO frequency (5, 0) <sup>(1)</sup>                          | DCORSELx = 5, DCOx = 0, MODx = 0                                                                              | 2.5  | 6.0  | MHz     |
| $f_{\text{DCO}(5,31)}$           | DCO frequency (5, 31) <sup>(1)</sup>                         | DCORSELx = 5, DCOx = 31, MODx = 0                                                                             | 23.7 | 54.1 | MHz     |
| $f_{\text{DCO}(6,0)}$            | DCO frequency (6, 0) <sup>(1)</sup>                          | DCORSELx = 6, DCOx = 0, MODx = 0                                                                              | 4.6  | 10.7 | MHz     |
| $f_{\text{DCO}(6,31)}$           | DCO frequency (6, 31) <sup>(1)</sup>                         | DCORSELx = 6, DCOx = 31, MODx = 0                                                                             | 39.0 | 88.0 | MHz     |
| $f_{\text{DCO}(7,0)}$            | DCO frequency (7, 0) <sup>(1)</sup>                          | DCORSELx = 7, DCOx = 0, MODx = 0                                                                              | 8.5  | 19.6 | MHz     |
| $f_{\text{DCO}(7,31)}$           | DCO frequency (7, 31) <sup>(1)</sup>                         | DCORSELx = 7, DCOx = 31, MODx = 0                                                                             | 60   | 135  | MHz     |
| $S_{\text{DCORSEL}}$             | Frequency step (ratio) between range DCORSEL and DCORSEL + 1 | $S_{\text{RSEL}} = f_{\text{DCO}(\text{DCORSEL}+1, \text{DCO})} / f_{\text{DCO}(\text{DCORSEL}, \text{DCO})}$ |      | 1.2  | 2.3     |
| $S_{\text{DCO}}$                 | Frequency step (ratio) between tap DCO and DCO + 1           | $S_{\text{DCO}} = f_{\text{DCO}(\text{DCORSEL}, \text{DCO}+1)} / f_{\text{DCO}(\text{DCORSEL}, \text{DCO})}$  |      | 1.02 | 1.12    |
|                                  | Duty cycle                                                   | Measured at SMCLK                                                                                             |      | 40%  | 50% 60% |
| $df_{\text{DCO}}/dT$             | DCO frequency temperature drift <sup>(2)</sup>               | $f_{\text{DCO}} = 1 \text{ MHz}$                                                                              |      | 0.1  | %/°C    |
| $df_{\text{DCO}}/dV_{\text{CC}}$ | DCO frequency voltage drift <sup>(3)</sup>                   | $f_{\text{DCO}} = 1 \text{ MHz}$                                                                              |      | 1.9  | %/V     |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency,  $f_{\text{DCO}}$ , should be set to reside within the range of  $f_{\text{DCO}(n, 0), \text{MAX}} \leq f_{\text{DCO}} \leq f_{\text{DCO}(n, 31), \text{MIN}}$ , where  $f_{\text{DCO}(n, 0), \text{MAX}}$  represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and  $f_{\text{DCO}(n, 31), \text{MIN}}$  represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. If the actual  $f_{\text{DCO}}$  frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.
- (2) Calculated using the box method:  $(\text{MAX}(-40^\circ\text{C to } 85^\circ\text{C}) - \text{MIN}(-40^\circ\text{C to } 85^\circ\text{C})) / \text{MIN}(-40^\circ\text{C to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$
- (3) Calculated using the box method:  $(\text{MAX}(1.8 \text{ V to } 3.6 \text{ V}) - \text{MIN}(1.8 \text{ V to } 3.6 \text{ V})) / \text{MIN}(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

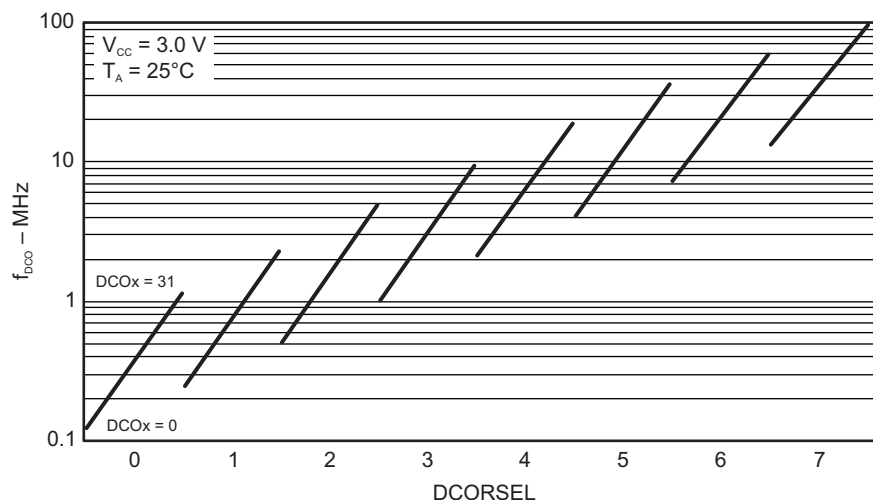


**Figure 5-10. Typical DCO Frequency**

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[www.ti.com](http://www.ti.com)**5.20 PMM, Brownout Reset (BOR)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                                  | TEST CONDITIONS                 | MIN  | TYP  | MAX  | UNIT |
|------------------------|----------------------------------------------------------------------------------|---------------------------------|------|------|------|------|
| $V_{(DVCC\_BOR\_IT-)}$ | BOR <sub>H</sub> on voltage, DV <sub>CC</sub> falling level                      | $ dDV_{CC}/dt  < 3 \text{ V/s}$ |      |      | 1.45 | V    |
| $V_{(DVCC\_BOR\_IT+)}$ | BOR <sub>H</sub> off voltage, DV <sub>CC</sub> rising level                      | $ dDV_{CC}/dt  < 3 \text{ V/s}$ | 0.80 | 1.30 | 1.50 | V    |
| $V_{(DVCC\_BOR\_hys)}$ | BOR <sub>H</sub> hysteresis                                                      |                                 | 50   |      | 250  | mV   |
| $t_{\text{RESET}}$     | Pulse duration required at the $\overline{\text{RST/NMI}}$ pin to accept a reset |                                 | 2    |      |      | μs   |

**5.21 PMM, Core Voltage**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               |                                              | TEST CONDITIONS                                 | MIN | TYP  | MAX | UNIT |
|-------------------------|----------------------------------------------|-------------------------------------------------|-----|------|-----|------|
| $V_{\text{CORE3(AM)}}$  | Core voltage, active mode, PMMCOREV = 3      | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.90 |     | V    |
| $V_{\text{CORE2(AM)}}$  | Core voltage, active mode, PMMCOREV = 2      | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.80 |     | V    |
| $V_{\text{CORE1(AM)}}$  | Core voltage, active mode, PMMCOREV = 1      | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.60 |     | V    |
| $V_{\text{CORE0(AM)}}$  | Core voltage, active mode, PMMCOREV = 0      | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.40 |     | V    |
| $V_{\text{CORE3(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 3 | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.94 |     | V    |
| $V_{\text{CORE2(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 2 | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.84 |     | V    |
| $V_{\text{CORE1(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 1 | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.64 |     | V    |
| $V_{\text{CORE0(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 0 | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ |     | 1.44 |     | V    |

## 5.22 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER         |                                                   | TEST CONDITIONS                                                       | MIN  | TYP  | MAX  | UNIT          |
|-------------------|---------------------------------------------------|-----------------------------------------------------------------------|------|------|------|---------------|
| $I_{(SVSH)}$      | SVS current consumption                           | SVSHE = 0, $DV_{CC} = 3.6\text{ V}$                                   |      | 0    |      | nA            |
|                   |                                                   | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$ , SVSHFP = 0                      |      | 200  |      |               |
|                   |                                                   | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$ , SVSHFP = 1                      |      | 1.5  |      | $\mu\text{A}$ |
| $V_{(SVSH\_IT-)}$ | SVS <sub>H</sub> on voltage level <sup>(1)</sup>  | SVSHE = 1, SVSHRVL = 0                                                | 1.57 | 1.68 | 1.78 | V             |
|                   |                                                   | SVSHE = 1, SVSHRVL = 1                                                | 1.79 | 1.88 | 1.98 |               |
|                   |                                                   | SVSHE = 1, SVSHRVL = 2                                                | 1.98 | 2.08 | 2.21 |               |
|                   |                                                   | SVSHE = 1, SVSHRVL = 3                                                | 2.10 | 2.18 | 2.31 |               |
| $V_{(SVSH\_IT+)}$ | SVS <sub>H</sub> off voltage level <sup>(1)</sup> | SVSHE = 1, SVSMHRRRL = 0                                              | 1.62 | 1.74 | 1.85 | V             |
|                   |                                                   | SVSHE = 1, SVSMHRRRL = 1                                              | 1.88 | 1.94 | 2.07 |               |
|                   |                                                   | SVSHE = 1, SVSMHRRRL = 2                                              | 2.07 | 2.14 | 2.28 |               |
|                   |                                                   | SVSHE = 1, SVSMHRRRL = 3                                              | 2.20 | 2.30 | 2.42 |               |
|                   |                                                   | SVSHE = 1, SVSMHRRRL = 4                                              | 2.32 | 2.40 | 2.55 |               |
|                   |                                                   | SVSHE = 1, SVSMHRRRL = 5                                              | 2.52 | 2.70 | 2.88 |               |
|                   |                                                   | SVSHE = 1, SVSMHRRRL = 6                                              | 2.90 | 3.10 | 3.23 |               |
|                   |                                                   | SVSHE = 1, SVSMHRRRL = 7                                              | 2.90 | 3.10 | 3.23 |               |
| $t_{pd(SVSH)}$    | SVS <sub>H</sub> propagation delay                | SVSHE = 1, $dV_{DVCC}/dt = 10\text{ mV}/\mu\text{s}$ , SVSHFP = 1     |      | 2.5  |      | $\mu\text{s}$ |
|                   |                                                   | SVSHE = 1, $dV_{DVCC}/dt = 1\text{ mV}/\mu\text{s}$ , SVSHFP = 0      |      | 20   |      |               |
| $t_{(SVSH)}$      | SVS <sub>H</sub> on or off delay time             | SVSHE = 0 → 1, $dV_{DVCC}/dt = 10\text{ mV}/\mu\text{s}$ , SVSHFP = 1 |      | 12.5 |      | $\mu\text{s}$ |
|                   |                                                   | SVSHE = 0 → 1, $dV_{DVCC}/dt = 1\text{ mV}/\mu\text{s}$ , SVSHFP = 0  |      | 100  |      |               |
| $dV_{DVCC}/dt$    | $DV_{CC}$ rise time                               |                                                                       | 0    |      | 1000 | V/s           |

(1) The SVS<sub>H</sub> settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) on recommended settings and use.

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**5.23 PMM, SVM High Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                            | TEST CONDITIONS                                              | MIN  | TYP  | MAX  | UNIT |
|----------------------------------------------------------------------|--------------------------------------------------------------|------|------|------|------|
| $I_{(SVMH)}$ SVM <sub>H</sub> current consumption                    | SVMHE = 0, DV <sub>CC</sub> = 3.6 V                          |      | 0    |      | nA   |
|                                                                      | SVMHE = 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 0              |      | 200  |      |      |
|                                                                      | SVMHE = 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 1              |      | 1.5  |      | μA   |
| $V_{(SVMH)}$ SVM <sub>H</sub> on or off voltage level <sup>(1)</sup> | SVMHE = 1, SVSMHRRRL = 0                                     | 1.62 | 1.74 | 1.85 | V    |
|                                                                      | SVMHE = 1, SVSMHRRRL = 1                                     | 1.88 | 1.94 | 2.07 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 2                                     | 2.07 | 2.14 | 2.28 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 3                                     | 2.20 | 2.30 | 2.42 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 4                                     | 2.32 | 2.40 | 2.55 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 5                                     | 2.52 | 2.70 | 2.88 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 6                                     | 2.90 | 3.10 | 3.23 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 7                                     | 2.90 | 3.10 | 3.23 |      |
| $t_{pd(SVMH)}$ SVM <sub>H</sub> propagation delay                    | SVMHE = 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVMHFP = 1     |      | 2.5  |      | μs   |
|                                                                      | SVMHE = 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVMHFP = 0      |      | 20   |      |      |
| $t_{(SVMH)}$ SVM <sub>H</sub> on or off delay time                   | SVMHE = 0 → 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVMHFP = 1 |      | 12.5 |      | μs   |
|                                                                      | SVMHE = 0 → 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVMHFP = 0  |      | 100  |      |      |

(1) The SVM<sub>H</sub> settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) on recommended settings and use.

**5.24 PMM, SVS Low Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                          | TEST CONDITIONS                                              | MIN | TYP  | MAX | UNIT |
|----------------------------------------------------|--------------------------------------------------------------|-----|------|-----|------|
| $I_{(SVSL)}$ SVS <sub>L</sub> current consumption  | SVSLE = 0, PMMCOREV = 2                                      |     | 0    |     | nA   |
|                                                    | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0                          |     | 200  |     |      |
|                                                    | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1                          |     | 1.5  |     | μA   |
| $t_{pd(SVSL)}$ SVS <sub>L</sub> propagation delay  | SVSLE = 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVSLFP = 1     |     | 2.5  |     | μs   |
|                                                    | SVSLE = 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVSLFP = 0      |     | 20   |     |      |
| $t_{(SVSL)}$ SVS <sub>L</sub> on or off delay time | SVSLE = 0 → 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVSLFP = 1 |     | 12.5 |     | μs   |
|                                                    | SVSLE = 0 → 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVSLFP = 0  |     | 100  |     |      |

**5.25 PMM, SVM Low Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                          | TEST CONDITIONS                                              | MIN | TYP  | MAX | UNIT |
|----------------------------------------------------|--------------------------------------------------------------|-----|------|-----|------|
| $I_{(SVML)}$ SVM <sub>L</sub> current consumption  | SVMLE = 0, PMMCOREV = 2                                      |     | 0    |     | nA   |
|                                                    | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0                          |     | 200  |     |      |
|                                                    | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1                          |     | 1.5  |     | μA   |
| $t_{pd(SVML)}$ SVM <sub>L</sub> propagation delay  | SVMLE = 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVMLFP = 1     |     | 2.5  |     | μs   |
|                                                    | SVMLE = 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVMLFP = 0      |     | 20   |     |      |
| $t_{(SVML)}$ SVM <sub>L</sub> on or off delay time | SVMLE = 0 → 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVMLFP = 1 |     | 12.5 |     | μs   |
|                                                    | SVMLE = 0 → 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVMLFP = 0  |     | 100  |     |      |

## 5.26 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                  |                                                                                      | TEST CONDITIONS                                               | MIN                                                   | TYP | MAX | UNIT          |
|----------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------|-------------------------------------------------------|-----|-----|---------------|
| $t_{\text{WAKE-UP-FAST}}$  | Wake-up time from LPM2, LPM3, or LPM4 to active mode <sup>(1)</sup>                  | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | $f_{\text{MCLK}} \geq 4.0 \text{ MHz}$                | 3.5 | 7.5 | $\mu\text{s}$ |
|                            |                                                                                      |                                                               | $1.0 \text{ MHz} < f_{\text{MCLK}} < 4.0 \text{ MHz}$ | 4.5 | 9   |               |
| $t_{\text{WAKE-UP-SLOW}}$  | Wake-up time from LPM2, LPM3, or LPM4 to active mode <sup>(2)(3)</sup>               | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 |                                                       | 150 | 165 | $\mu\text{s}$ |
| $t_{\text{WAKE-UP-LPM5}}$  | Wake-up time from LPM4.5 to active mode <sup>(4)</sup>                               |                                                               |                                                       | 2   | 3   | ms            |
| $t_{\text{WAKE-UP-RESET}}$ | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode <sup>(4)</sup> |                                                               |                                                       | 2   | 3   | ms            |

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVSL) and low-side monitor (SVM<sub>L</sub>).  $t_{\text{WAKE-UP-FAST}}$  is possible with SVSL and SVM<sub>L</sub> in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVSL) and low-side monitor (SVM<sub>L</sub>).  $t_{\text{WAKE-UP-SLOW}}$  is set with SVSL and SVM<sub>L</sub> in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
- (4) This value represents the time from the wake-up event to the reset vector execution.

## 5.27 Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                               | TEST CONDITIONS                                                      | V <sub>CC</sub> | MIN | MAX | UNIT |
|---------------------|-------------------------------|----------------------------------------------------------------------|-----------------|-----|-----|------|
| $f_{\text{TA}}$     | Timer_A input clock frequency | Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% $\pm$ 10% | 1.8 V, 3 V      |     | 25  | MHz  |
| $t_{\text{TA,cap}}$ | Timer_A capture timing        | All capture inputs, minimum pulse duration required for capture      | 1.8 V, 3 V      | 20  |     | ns   |

## 5.28 Timer\_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                               | TEST CONDITIONS                                                      | V <sub>CC</sub> | MIN | MAX | UNIT |
|---------------------|-------------------------------|----------------------------------------------------------------------|-----------------|-----|-----|------|
| $f_{\text{TB}}$     | Timer_B input clock frequency | Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% $\pm$ 10% | 1.8 V, 3 V      |     | 25  | MHz  |
| $t_{\text{TB,cap}}$ | Timer_B capture timing        | All capture inputs, minimum pulse duration required for capture      | 1.8 V, 3 V      | 20  |     | ns   |

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**5.29 USCI (UART Mode) Clock Frequency**

| PARAMETER                                                       | TEST CONDITIONS                                                           | MIN | MAX          | UNIT |
|-----------------------------------------------------------------|---------------------------------------------------------------------------|-----|--------------|------|
| $f_{USCI}$ USCI input clock frequency                           | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% $\pm$ 10% |     | $f_{SYSTEM}$ | MHz  |
| $f_{BITCLK}$ BITCLK clock frequency (equals baud rate in MBaud) |                                                                           |     | 1            | MHz  |

**5.30 USCI (UART Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                       | $V_{CC}$ | MIN | MAX | UNIT |
|-------------------------------------------------|----------|-----|-----|------|
| $t_r$ UART receive deglitch time <sup>(1)</sup> | 2.2 V    | 50  | 600 | ns   |
|                                                 | 3 V      | 50  | 600 |      |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

**5.31 USCI (SPI Master Mode) Clock Frequency**

| PARAMETER                             | TEST CONDITIONS                                        | MIN | MAX          | UNIT |
|---------------------------------------|--------------------------------------------------------|-----|--------------|------|
| $f_{USCI}$ USCI input clock frequency | Internal: SMCLK or ACLK,<br>Duty cycle = 50% $\pm$ 10% |     | $f_{SYSTEM}$ | MHz  |

**5.32 USCI (SPI Master Mode)**over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>(see [Figure 5-11](#) and [Figure 5-12](#))

| PARAMETER                                                 | TEST CONDITIONS                                         | $V_{CC}$ | MIN | MAX          | UNIT |
|-----------------------------------------------------------|---------------------------------------------------------|----------|-----|--------------|------|
| $f_{USCI}$ USCI input clock frequency                     | SMCLK or ACLK,<br>Duty cycle = 50% $\pm$ 10%            |          |     | $f_{SYSTEM}$ | MHz  |
| $t_{SU,MI}$ SOMI input data setup time                    | PMMCOREV = 0                                            | 1.8 V    | 55  | ns           |      |
|                                                           |                                                         | 3 V      | 38  |              |      |
|                                                           | PMMCOREV = 3                                            | 2.4 V    | 30  |              |      |
|                                                           |                                                         | 3 V      | 25  |              |      |
| $t_{HD,MI}$ SOMI input data hold time                     | PMMCOREV = 0                                            | 1.8 V    | 0   | ns           |      |
|                                                           |                                                         | 3 V      | 0   |              |      |
|                                                           | PMMCOREV = 3                                            | 2.4 V    | 0   |              |      |
|                                                           |                                                         | 3 V      | 0   |              |      |
| $t_{VALID,MO}$ SIMO output data valid time <sup>(2)</sup> | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V    |     | 20           | ns   |
|                                                           |                                                         | 3 V      |     | 18           |      |
|                                                           | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V    |     | 16           |      |
|                                                           |                                                         | 3 V      |     | 15           |      |
| $t_{HD,MO}$ SIMO output data hold time <sup>(3)</sup>     | $C_L$ = 20 pF, PMMCOREV = 0                             | 1.8 V    | –10 | ns           |      |
|                                                           |                                                         | 3 V      | –8  |              |      |
|                                                           | $C_L$ = 20 pF, PMMCOREV = 3                             | 2.4 V    | –10 |              |      |
|                                                           |                                                         | 3 V      | –8  |              |      |

- (1)  $f_{UCxCLK} = 1/2t_{LO/Hi}$  with  $t_{LO/Hi} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$   
For the slave parameters  $t_{SU,SI}(Slave)$  and  $t_{VALID,SO}(Slave)$ , see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-11](#) and [Figure 5-12](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 5-11](#) and [Figure 5-12](#).

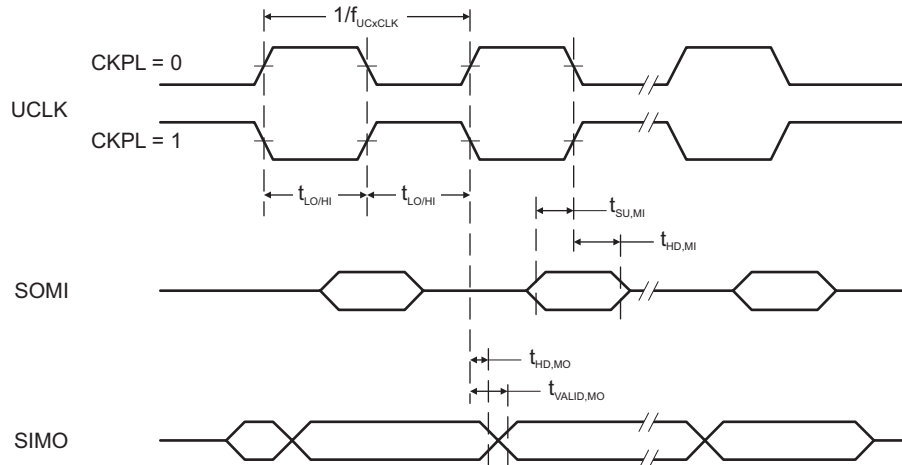


**Figure 5-11. SPI Master Mode, CKPH = 0**

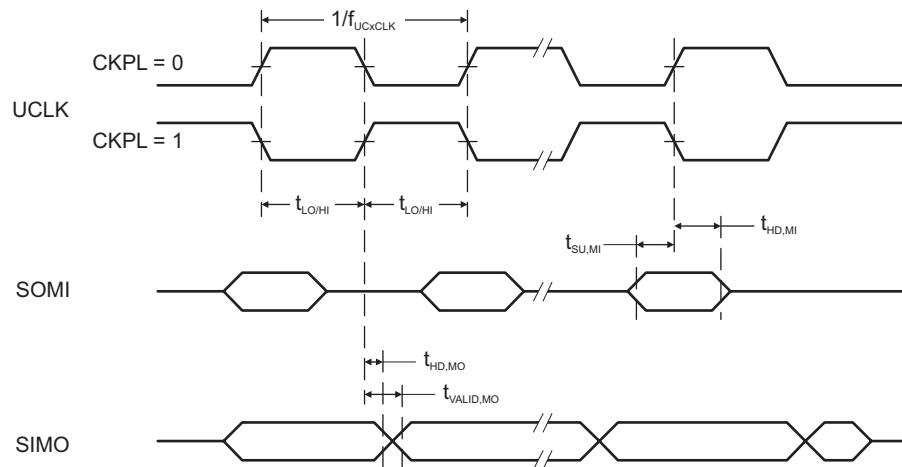


**Figure 5-12. SPI Master Mode, CKPH = 1**

**MSP430F5342, MSP430F5341, MSP430F5340**

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[www.ti.com](http://www.ti.com)**5.33 USCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>  
(see [Figure 5-13](#) and [Figure 5-14](#))

| PARAMETER             |                                                   | TEST CONDITIONS                                                  | V <sub>CC</sub> | MIN | MAX | UNIT |
|-----------------------|---------------------------------------------------|------------------------------------------------------------------|-----------------|-----|-----|------|
| t <sub>STE,LEAD</sub> | STE lead time, STE low to clock                   | PMMCOREV = 0                                                     | 1.8 V           | 11  |     | ns   |
|                       |                                                   |                                                                  | 3 V             | 8   |     |      |
|                       |                                                   | PMMCOREV = 3                                                     | 2.4 V           | 7   |     |      |
|                       |                                                   |                                                                  | 3 V             | 6   |     |      |
| t <sub>STE,LAG</sub>  | STE lag time, last clock to STE high              | PMMCOREV = 0                                                     | 1.8 V           | 3   |     | ns   |
|                       |                                                   |                                                                  | 3 V             | 3   |     |      |
|                       |                                                   | PMMCOREV = 3                                                     | 2.4 V           | 3   |     |      |
|                       |                                                   |                                                                  | 3 V             | 3   |     |      |
| t <sub>STE,ACC</sub>  | STE access time, STE low to SOMI data out         | PMMCOREV = 0                                                     | 1.8 V           |     | 66  | ns   |
|                       |                                                   |                                                                  | 3 V             |     | 50  |      |
|                       |                                                   | PMMCOREV = 3                                                     | 2.4 V           |     | 36  |      |
|                       |                                                   |                                                                  | 3 V             |     | 30  |      |
| t <sub>STE,DIS</sub>  | STE disable time, STE high to SOMI high impedance | PMMCOREV = 0                                                     | 1.8 V           |     | 30  | ns   |
|                       |                                                   |                                                                  | 3 V             |     | 23  |      |
|                       |                                                   | PMMCOREV = 3                                                     | 2.4 V           |     | 16  |      |
|                       |                                                   |                                                                  | 3 V             |     | 13  |      |
| t <sub>SU,SI</sub>    | SIMO input data setup time                        | PMMCOREV = 0                                                     | 1.8 V           | 5   |     | ns   |
|                       |                                                   |                                                                  | 3 V             | 5   |     |      |
|                       |                                                   | PMMCOREV = 3                                                     | 2.4 V           | 2   |     |      |
|                       |                                                   |                                                                  | 3 V             | 2   |     |      |
| t <sub>HD,SI</sub>    | SIMO input data hold time                         | PMMCOREV = 0                                                     | 1.8 V           | 5   |     | ns   |
|                       |                                                   |                                                                  | 3 V             | 5   |     |      |
|                       |                                                   | PMMCOREV = 3                                                     | 2.4 V           | 5   |     |      |
|                       |                                                   |                                                                  | 3 V             | 5   |     |      |
| t <sub>VALID,SO</sub> | SOMI output data valid time <sup>(2)</sup>        | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF, PMMCOREV = 0 | 1.8 V           |     | 76  | ns   |
|                       |                                                   |                                                                  | 3 V             |     | 60  |      |
|                       |                                                   | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF, PMMCOREV = 3 | 2.4 V           |     | 44  |      |
|                       |                                                   |                                                                  | 3 V             |     | 40  |      |
| t <sub>HD,SO</sub>    | SOMI output data hold time <sup>(3)</sup>         | C <sub>L</sub> = 20 pF, PMMCOREV = 0                             | 1.8 V           | 18  |     | ns   |
|                       |                                                   |                                                                  | 3 V             | 12  |     |      |
|                       |                                                   | C <sub>L</sub> = 20 pF, PMMCOREV = 3                             | 2.4 V           | 10  |     |      |
|                       |                                                   |                                                                  | 3 V             | 8   |     |      |

(1)  $f_{UCXCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$

For the master parameters  $t_{SU,MI(Master)}$  and  $t_{VALID,MO(Master)}$ , see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).

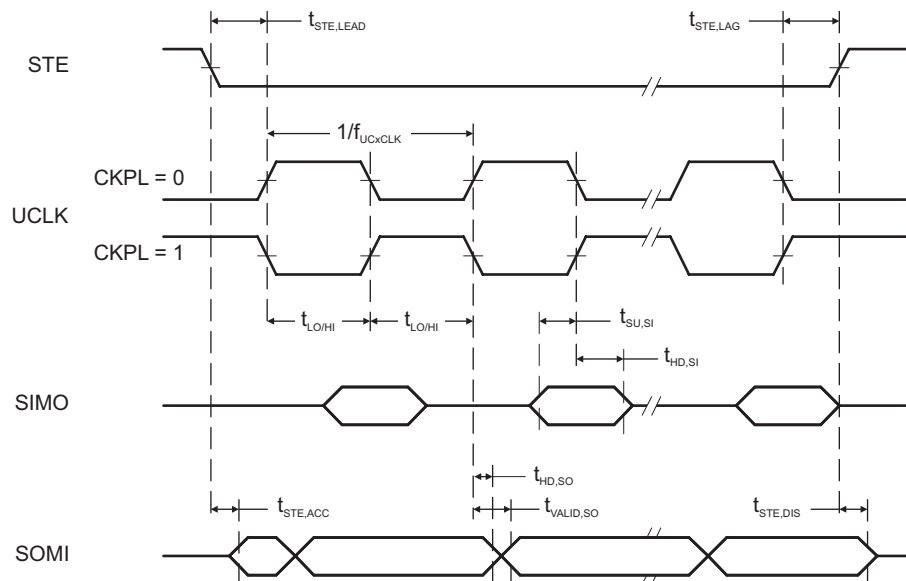


**Figure 5-13. SPI Slave Mode, CKPH = 0**

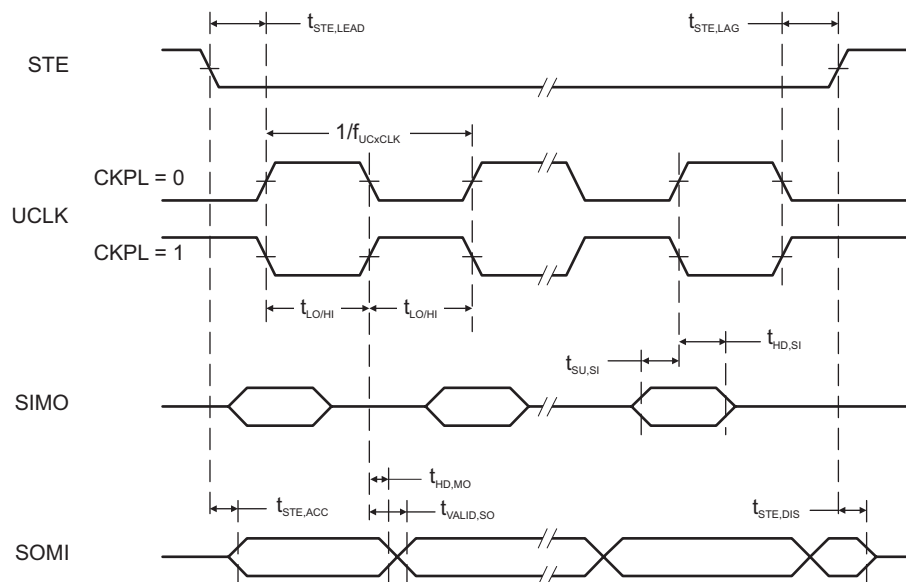


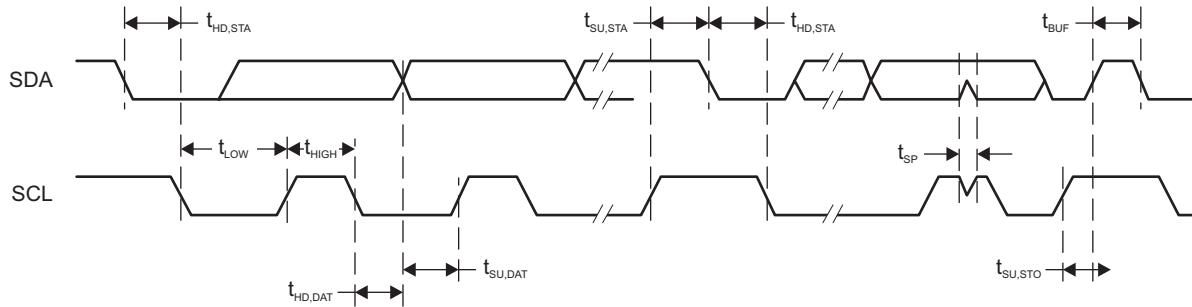
**Figure 5-14. SPI Slave Mode, CKPH = 1**

**MSP430F5342, MSP430F5341, MSP430F5340**

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[www.ti.com](http://www.ti.com)**5.34 USCI (I<sup>2</sup>C Mode)**over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-15](#))

| PARAMETER                                                           | TEST CONDITIONS                                                      | V <sub>CC</sub> | MIN                 | MAX | UNIT |
|---------------------------------------------------------------------|----------------------------------------------------------------------|-----------------|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                        | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% |                 | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>SCL</sub> SCL clock frequency                                |                                                                      | 2.2 V, 3 V      | 0                   | 400 | kHz  |
| t <sub>HD,STA</sub> Hold time (repeated) START                      | f <sub>SCL</sub> ≤ 100 kHz                                           | 2.2 V, 3 V      | 4.0                 |     | μs   |
|                                                                     | f <sub>SCL</sub> > 100 kHz                                           |                 | 0.6                 |     |      |
| t <sub>SU,STA</sub> Setup time for a repeated START                 | f <sub>SCL</sub> ≤ 100 kHz                                           | 2.2 V, 3 V      | 4.7                 |     | μs   |
|                                                                     | f <sub>SCL</sub> > 100 kHz                                           |                 | 0.6                 |     |      |
| t <sub>HD,DAT</sub> Data hold time                                  |                                                                      | 2.2 V, 3 V      | 0                   |     | ns   |
| t <sub>SU,DAT</sub> Data setup time                                 |                                                                      | 2.2 V, 3 V      | 250                 |     | ns   |
| t <sub>SU,STO</sub> Setup time for STOP                             | f <sub>SCL</sub> ≤ 100 kHz                                           | 2.2 V, 3 V      | 4.0                 |     | μs   |
|                                                                     | f <sub>SCL</sub> > 100 kHz                                           |                 | 0.6                 |     |      |
| t <sub>SP</sub> Pulse duration of spikes suppressed by input filter |                                                                      | 2.2 V           | 50                  | 600 | ns   |
|                                                                     |                                                                      | 3 V             | 50                  | 600 |      |

**Figure 5-15. I<sup>2</sup>C Mode Timing**

### 5.35 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                       | TEST CONDITIONS                                                                                                             | V <sub>CC</sub> | MIN | TYP | MAX              | UNIT |
|---------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|------------------|------|
| AV <sub>CC</sub> Analog supply voltage                                          | AVCC and DVCC are connected together, AVSS and DVSS are connected together, V <sub>(AVSS)</sub> = V <sub>(DVSS)</sub> = 0 V |                 | 2.2 |     | 3.6              | V    |
| V <sub>(Ax)</sub> Analog input voltage range <sup>(2)</sup>                     | All ADC12 analog input pins Ax                                                                                              |                 | 0   |     | AV <sub>CC</sub> | V    |
| I <sub>ADC12_A</sub> Operating supply current into AVCC terminal <sup>(3)</sup> | f <sub>ADC12CLK</sub> = 5.0 MHz <sup>(4)</sup>                                                                              | 2.2 V           |     | 125 | 155              | μA   |
|                                                                                 |                                                                                                                             | 3 V             |     | 150 | 220              |      |
| C <sub>I</sub> Input capacitance                                                | Only one terminal Ax can be selected at one time                                                                            | 2.2 V           |     | 20  | 25               | pF   |
| R <sub>I</sub> Input MUX ON resistance                                          | 0 V ≤ V <sub>Ax</sub> ≤ AVCC                                                                                                |                 | 10  | 200 | 1900             | Ω    |

(1) The leakage current is specified by the digital I/O input leakage.

(2) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See [Section 5.40](#) and [Section 5.41](#).

(3) The internal reference supply current is not included in current consumption parameter I<sub>ADC12\_A</sub>.

(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

### 5.36 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                      | TEST CONDITIONS                                                                                                                                 | V <sub>CC</sub> | MIN  | TYP                               | MAX | UNIT |
|----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----------------------------------|-----|------|
| f <sub>ADC12CLK</sub> ADC conversion clock                     | For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference <sup>(1)</sup>                 | 2.2 V, 3 V      | 0.45 | 4.8                               | 5.0 | MHz  |
|                                                                | For specified performance of ADC12 linearity parameters using the internal reference <sup>(2)</sup>                                             |                 | 0.45 | 2.4                               | 4.0 |      |
|                                                                | For specified performance of ADC12 linearity parameters using the internal reference <sup>(3)</sup>                                             |                 | 0.45 | 2.4                               | 2.7 |      |
| f <sub>ADC12OSC</sub> Internal ADC12 oscillator <sup>(4)</sup> | ADC12DIV = 0, f <sub>ADC12CLK</sub> = f <sub>ADC12OSC</sub>                                                                                     | 2.2 V, 3 V      | 4.2  | 4.8                               | 5.4 | MHz  |
| t <sub>CONVERT</sub> Conversion time                           | REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock                                                                          | 2.2 V, 3 V      | 2.4  |                                   | 3.1 | μs   |
|                                                                | External f <sub>ADC12CLK</sub> from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0                                                                         |                 |      | 13 ×<br>1 / f <sub>ADC12CLK</sub> |     |      |
| t <sub>Sample</sub> Sampling time                              | R <sub>S</sub> = 400 Ω, R <sub>I</sub> = 1000 Ω, C <sub>I</sub> = 20 pF, τ = (R <sub>S</sub> + R <sub>I</sub> ) × C <sub>I</sub> <sup>(5)</sup> | 2.2 V, 3 V      | 1000 |                                   |     | ns   |

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The performance of the ADC12 linearity is specified when using the ADC12OSC. For other clock sources, the performance of the ADC12 linearity is specified with f<sub>ADC12CLK</sub> maximum of 5.0 MHz.

(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1

(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.

(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.

(5) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:

t<sub>Sample</sub> = ln(2<sup>n+1</sup>) × (R<sub>S</sub> + R<sub>I</sub>) × C<sub>I</sub> + 800 ns, where n = ADC resolution = 12, R<sub>S</sub> = external source resistance

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**5.37 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER      |                                             | TEST CONDITIONS                      | V <sub>CC</sub> | MIN | TYP  | MAX  | UNIT |
|----------------|---------------------------------------------|--------------------------------------|-----------------|-----|------|------|------|
| E <sub>I</sub> | Integral linearity error <sup>(1)</sup>     | 1.4 V ≤ dVREF ≤ 1.6 V <sup>(2)</sup> | 2.2 V, 3 V      |     |      | ±2.0 | LSB  |
|                |                                             | 1.6 V < dVREF <sup>(2)</sup>         |                 |     |      | ±1.7 |      |
| E <sub>D</sub> | Differential linearity error <sup>(1)</sup> | See <sup>(2)</sup>                   | 2.2 V, 3 V      |     |      | ±1.0 | LSB  |
| E <sub>O</sub> | Offset error <sup>(3)</sup>                 | dVREF ≤ 2.2 V <sup>(2)</sup>         | 2.2 V, 3 V      |     | ±1.0 | ±2.0 | LSB  |
|                |                                             | dVREF > 2.2 V <sup>(2)</sup>         | 2.2 V, 3 V      |     | ±1.0 | ±2.0 |      |
| E <sub>G</sub> | Gain error <sup>(3)</sup>                   | See <sup>(2)</sup>                   | 2.2 V, 3 V      |     | ±1.0 | ±2.0 | LSB  |
| E <sub>T</sub> | Total unadjusted error                      | dVREF ≤ 2.2 V <sup>(2)</sup>         | 2.2 V, 3 V      |     | ±1.4 | ±3.5 | LSB  |
|                |                                             | dVREF > 2.2 V <sup>(2)</sup>         | 2.2 V, 3 V      |     | ±1.4 | ±3.5 |      |

(1) Parameters are derived using the histogram method.

(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = V<sub>R+</sub> - V<sub>R-</sub>. V<sub>R+</sub> < AVCC, V<sub>R-</sub> > AVSS. Unless otherwise noted, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current. Also see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

(3) Parameters are derived using a best fit curve.

**5.38 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER      |                                             | TEST CONDITIONS <sup>(1)</sup>                           | V <sub>CC</sub> | MIN  | TYP  | MAX                  | UNIT |
|----------------|---------------------------------------------|----------------------------------------------------------|-----------------|------|------|----------------------|------|
| E <sub>I</sub> | Integral linearity error <sup>(2)</sup>     | ADC12SR = 0, REFOUT = 1, f <sub>ADC12CLK</sub> ≤ 4.0 MHz | 2.2 V, 3 V      |      |      | ±1.7                 | LSB  |
|                |                                             | ADC12SR = 0, REFOUT = 0, f <sub>ADC12CLK</sub> ≤ 2.7 MHz |                 |      |      | ±2.5                 |      |
| E <sub>D</sub> | Differential linearity error <sup>(2)</sup> | ADC12SR = 0, REFOUT = 1, f <sub>ADC12CLK</sub> ≤ 4.0 MHz | 2.2 V, 3 V      | -1.0 |      | +2.0                 | LSB  |
|                |                                             | ADC12SR = 0, REFOUT = 1, f <sub>ADC12CLK</sub> ≤ 2.7 MHz |                 | -1.0 |      | +1.5                 |      |
|                |                                             | ADC12SR = 0, REFOUT = 0, f <sub>ADC12CLK</sub> ≤ 2.7 MHz |                 | -1.0 |      | +2.5                 |      |
| E <sub>O</sub> | Offset error <sup>(3)</sup>                 | ADC12SR = 0, REFOUT = 1, f <sub>ADC12CLK</sub> ≤ 4.0 MHz | 2.2 V, 3 V      |      | ±1.0 | ±2.0                 | LSB  |
|                |                                             | ADC12SR = 0, REFOUT = 0, f <sub>ADC12CLK</sub> ≤ 2.7 MHz |                 |      | ±1.0 | ±2.0                 |      |
| E <sub>G</sub> | Gain error <sup>(3)</sup>                   | ADC12SR = 0, REFOUT = 1, f <sub>ADC12CLK</sub> ≤ 4.0 MHz | 2.2 V, 3 V      |      | ±1.0 | ±2.0                 | LSB  |
|                |                                             | ADC12SR = 0, REFOUT = 0, f <sub>ADC12CLK</sub> ≤ 2.7 MHz |                 |      |      | ±1.5% <sup>(4)</sup> | VREF |
| E <sub>T</sub> | Total unadjusted error                      | ADC12SR = 0, REFOUT = 1, f <sub>ADC12CLK</sub> ≤ 4.0 MHz | 2.2 V, 3 V      |      | ±1.4 | ±3.5                 | LSB  |
|                |                                             | ADC12SR = 0, REFOUT = 0, f <sub>ADC12CLK</sub> ≤ 2.7 MHz |                 |      |      | ±1.5% <sup>(4)</sup> | VREF |

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = V<sub>R+</sub> - V<sub>R-</sub>.

(2) Parameters are derived using the histogram method.

(3) Parameters are derived using a best fit curve.

(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode, the reference voltage used by the ADC12\_A is not available on a pin.

### 5.39 12-Bit ADC, Temperature Sensor and Built-In $V_{MID}$ <sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                                     | TEST CONDITIONS                                                     | $V_{CC}$   | MIN  | TYP  | MAX  | UNIT                 |
|----------------------|---------------------------------------------------------------------|---------------------------------------------------------------------|------------|------|------|------|----------------------|
| $V_{SENSOR}$         | See <sup>(2)</sup> and Figure 5-16                                  | ADC12ON = 1, INCH = 0Ah,<br>$T_A = 0^\circ\text{C}$                 | 2.2 V      |      | 680  |      | mV                   |
|                      |                                                                     |                                                                     | 3 V        |      | 680  |      |                      |
| $TC_{SENSOR}$        |                                                                     | ADC12ON = 1, INCH = 0Ah                                             | 2.2 V      |      | 2.25 |      | mV/ $^\circ\text{C}$ |
|                      |                                                                     |                                                                     | 3 V        |      | 2.25 |      |                      |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected <sup>(3)</sup>       | ADC12ON = 1, INCH = 0Ah,<br>Error of conversion result $\leq 1$ LSB | 2.2 V      |      | 100  |      | $\mu\text{s}$        |
|                      |                                                                     |                                                                     | 3 V        |      | 100  |      |                      |
| $V_{MID}$            | AV <sub>CC</sub> divider at channel 11,<br>V <sub>AVCC</sub> factor | ADC12ON = 1, INCH = 0Bh                                             |            | 0.48 | 0.5  | 0.52 | V <sub>AVCC</sub>    |
|                      |                                                                     |                                                                     |            |      |      |      |                      |
|                      | AV <sub>CC</sub> divider at channel 11                              | ADC12ON = 1, INCH = 0Bh                                             | 2.2 V      | 1.06 | 1.1  | 1.14 | V                    |
|                      |                                                                     |                                                                     | 3 V        | 1.44 | 1.5  | 1.56 |                      |
| $t_{VMID(sample)}$   | Sample time required if channel 11 is selected <sup>(4)</sup>       | ADC12ON = 1, INCH = 0Bh,<br>Error of conversion result $\leq 1$ LSB | 2.2 V, 3 V | 1000 |      |      | ns                   |

- (1) The temperature sensor is provided by the REF module. See the REF module parametric,  $I_{REF+}$ , regarding the current consumption of the temperature sensor.
- (2) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for  $30^\circ\text{C} \pm 3^\circ\text{C}$  and  $85^\circ\text{C} \pm 3^\circ\text{C}$  for each of the available reference voltage levels. The sensor voltage can be computed as  $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature}, ^\circ\text{C}) + V_{SENSOR}$ , where  $TC_{SENSOR}$  and  $V_{SENSOR}$  can be computed from the calibration values for higher accuracy. Also see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (3) The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor on-time  $t_{SENSOR(on)}$ .
- (4) The on-time  $t_{VMID(on)}$  is included in the sampling time  $t_{VMID(sample)}$ ; no additional on time is needed.

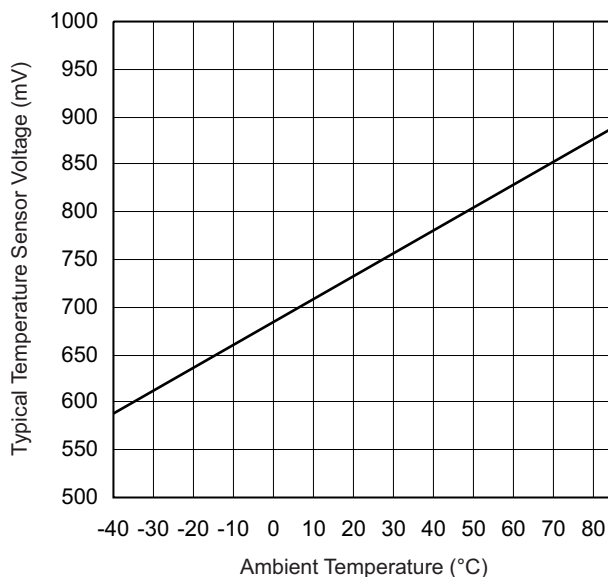


**Figure 5-16. Typical Temperature Sensor Voltage**

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[www.ti.com](http://www.ti.com)**5.40 REF, External Reference**over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                    |                                               | TEST CONDITIONS                                                                                                                                              | V <sub>CC</sub> | MIN               | MAX              | UNIT |
|--------------------------------------------------------------|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------------------|------------------|------|
| V <sub>eREF+</sub>                                           | Positive external reference voltage input     | V <sub>eREF+</sub> > V <sub>REF</sub> /V <sub>eREF-</sub> <sup>(2)</sup>                                                                                     |                 | 1.4               | AV <sub>CC</sub> | V    |
| V <sub>REF</sub> /V <sub>eREF-</sub>                         | Negative external reference voltage input     | V <sub>eREF+</sub> > V <sub>REF</sub> /V <sub>eREF-</sub> <sup>(3)</sup>                                                                                     |                 | 0                 | 1.2              | V    |
| (V <sub>eREF+</sub> – V <sub>REF</sub> /V <sub>eREF-</sub> ) | Differential external reference voltage input | V <sub>eREF+</sub> > V <sub>REF</sub> /V <sub>eREF-</sub> <sup>(4)</sup>                                                                                     |                 | 1.4               | AV <sub>CC</sub> | V    |
| I <sub>VeREF+</sub> ,<br>I <sub>VREF-/VeREF-</sub>           | Static input current                          | 1.4 V ≤ V <sub>eREF+</sub> ≤ V <sub>AVCC</sub> ,<br>V <sub>eREF-</sub> = 0 V, f <sub>ADC12CLK</sub> = 5 MHz,<br>ADC12SHTx = 1h,<br>Conversion rate 200 ksp/s | 2.2 V, 3 V      | –26               | 26               | μA   |
|                                                              |                                               | 1.4 V ≤ V <sub>eREF+</sub> ≤ V <sub>AVCC</sub> ,<br>V <sub>eREF-</sub> = 0 V, f <sub>ADC12CLK</sub> = 5 MHz,<br>ADC12SHTx = 8h,<br>Conversion rate 20 ksp/s  | 2.2 V, 3 V      | –1                | 1                |      |
| C <sub>VREF+/-</sub>                                         | Capacitance at VREF+ or VREF- terminal        |                                                                                                                                                              |                 | <sup>(5)</sup> 10 |                  | μF   |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C<sub>i</sub>, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12\_A. Also see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

## 5.41 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER             | TEST CONDITIONS                                                                                                                                                                           | V <sub>CC</sub> | MIN    | TYP  | MAX    | UNIT       |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------|------|--------|------------|
| V <sub>REF+</sub>     | REFVSEL = {2} for 2.5 V,<br>REFON = REFOUT = 1, I <sub>VREF+</sub> = 0 A                                                                                                                  | 3 V             | 2.4625 | 2.50 | 2.5375 | V          |
|                       | REFVSEL = {1} for 2.0 V,<br>REFON = REFOUT = 1, I <sub>VREF+</sub> = 0 A                                                                                                                  | 3 V             | 1.9503 | 1.98 | 2.0097 |            |
|                       | REFVSEL = {0} for 1.5 V,<br>REFON = REFOUT = 1, I <sub>VREF+</sub> = 0 A                                                                                                                  | 2.2 V, 3 V      | 1.4677 | 1.49 | 1.5124 |            |
| AV <sub>CC(min)</sub> | REFVSEL = {0} for 1.5 V                                                                                                                                                                   |                 | 2.2    |      |        | V          |
|                       | REFVSEL = {1} for 2.0 V                                                                                                                                                                   |                 | 2.3    |      |        |            |
|                       | REFVSEL = {2} for 2.5 V                                                                                                                                                                   |                 | 2.8    |      |        |            |
| I <sub>REF+</sub>     | ADC12SR = 1 <sup>(4)</sup> , REFON = 1,<br>REFOUT = 0, REFBURST = 0                                                                                                                       | 3 V             |        | 70   | 100    | μA         |
|                       | ADC12SR = 1 <sup>(4)</sup> , REFON = 1,<br>REFOUT = 1, REFBURST = 0                                                                                                                       |                 |        | 0.45 | 0.75   | mA         |
|                       | ADC12SR = 0 <sup>(4)</sup> , REFON = 1,<br>REFOUT = 0, REFBURST = 0                                                                                                                       |                 |        | 210  | 310    | μA         |
|                       | ADC12SR = 0 <sup>(4)</sup> , REFON = 1,<br>REFOUT = 1, REFBURST = 0                                                                                                                       |                 |        | 0.95 | 1.7    | mA         |
| I <sub>L(VREF+)</sub> | REFVSEL = {0, 1, 2},<br>I <sub>VREF+</sub> = +10 μA or –1000 μA,<br>AV <sub>CC</sub> = AV <sub>CC(min)</sub> for each reference level,<br>REFVSEL = {0, 1, 2}, REFON = REFOUT = 1         |                 |        |      | 2500   | μV/mA      |
| C <sub>VREF+</sub>    | REFON = REFOUT = 1                                                                                                                                                                        |                 | 20     |      | 100    | pF         |
| TC <sub>REF+</sub>    | I <sub>VREF+</sub> = 0 A,<br>REFVSEL = {0, 1, 2}, REFON = 1,<br>REFOUT = 0 or 1                                                                                                           |                 |        | 30   | 50     | ppm/<br>°C |
| PSRR <sub>DC</sub>    | AV <sub>CC</sub> = AV <sub>CC(min)</sub> to AV <sub>CC(max)</sub> ,<br>T <sub>A</sub> = 25°C, REFVSEL = {0, 1, 2},<br>REFON = 1, REFOUT = 0 or 1                                          |                 |        | 120  | 300    | μV/V       |
| PSRR <sub>AC</sub>    | AV <sub>CC</sub> = AV <sub>CC(min)</sub> to AV <sub>CC(max)</sub> ,<br>T <sub>A</sub> = 25°C, f = 1 kHz, ΔV <sub>pp</sub> = 100 mV,<br>REFVSEL = {0, 1, 2}, REFON = 1,<br>REFOUT = 0 or 1 |                 |        | 6.4  |        | mV/V       |
| t <sub>SETTLE</sub>   | AV <sub>CC</sub> = AV <sub>CC(min)</sub> to AV <sub>CC(max)</sub> ,<br>REFVSEL = {0, 1, 2}, REFOUT = 0,<br>REFON = 0 → 1                                                                  |                 |        | 75   |        | μs         |
|                       | AV <sub>CC</sub> = AV <sub>CC(min)</sub> to AV <sub>CC(max)</sub> ,<br>C <sub>VREF</sub> = C <sub>VREF(max)</sub> ,<br>REFVSEL = {0, 1, 2}, REFOUT = 1,<br>REFON = 0 → 1                  |                 |        | 75   |        |            |

- The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger, for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal and is used as the reference for the conversion and uses the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and uses the smaller buffer.
- The internal reference current is supplied from the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
- The temperature sensor is provided by the REF module. Its current is supplied from the AVCC terminal and is equivalent to I<sub>REF+</sub> with REFON = 1 and REFOUT = 0.
- For devices without the ADC12, the parametric with ADC12SR = 0 are applicable.
- Contribution only due to the reference and buffer including package. This does not include resistance due to factors such as PCB traces.
- Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C)).
- The condition is that the error in a conversion started after t<sub>REFON</sub> is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

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[www.ti.com](http://www.ti.com)**5.42 Comparator\_B**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                                | TEST CONDITIONS                                                | V <sub>CC</sub> | MIN  | TYP                                | MAX                 | UNIT |
|----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|-----------------|------|------------------------------------|---------------------|------|
| V <sub>CC</sub> Supply voltage                                                                           |                                                                |                 | 1.8  |                                    | 3.6                 | V    |
| I <sub>AVCC_COMP</sub> Comparator operating supply current into AVCC, Excludes reference resistor ladder | CBPWRMD = 00                                                   | 1.8 V           |      |                                    | 40                  | μA   |
|                                                                                                          |                                                                | 2.2 V           |      | 30                                 | 50                  |      |
|                                                                                                          |                                                                | 3 V             |      | 40                                 | 65                  |      |
|                                                                                                          | CBPWRMD = 01                                                   | 2.2 V, 3 V      |      | 10                                 | 30                  |      |
|                                                                                                          | CBPWRMD = 10                                                   | 2.2 V, 3 V      |      | 0.1                                | 0.5                 |      |
| I <sub>AVCC_REF</sub> Quiescent current of local reference voltage amplifier into AVCC                   | CBREFACC = 1, CBREFLx = 01                                     |                 |      |                                    | 22                  | μA   |
| V <sub>IC</sub> Common mode input range                                                                  |                                                                |                 | 0    |                                    | V <sub>CC</sub> – 1 | V    |
| V <sub>OFFSET</sub> Input offset voltage                                                                 | CBPWRMD = 00                                                   |                 |      |                                    | ±20                 | mV   |
|                                                                                                          | CBPWRMD = 01, 10                                               |                 |      |                                    | ±10                 |      |
| C <sub>IN</sub> Input capacitance                                                                        |                                                                |                 |      | 5                                  |                     | pF   |
| R <sub>SIN</sub> Series input resistance                                                                 | ON, switch closed                                              |                 |      | 3                                  | 4                   | kΩ   |
|                                                                                                          | OFF, switch opened                                             |                 | 30   |                                    |                     | MΩ   |
| t <sub>PD</sub> Propagation delay, response time                                                         | CBPWRMD = 00, CBF = 0                                          |                 |      |                                    | 450                 | ns   |
|                                                                                                          | CBPWRMD = 01, CBF = 0                                          |                 |      |                                    | 600                 |      |
|                                                                                                          | CBPWRMD = 10, CBF = 0                                          |                 |      |                                    | 50                  | μs   |
| t <sub>PD,filter</sub> Propagation delay with filter active                                              | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 00       |                 | 0.35 | 0.6                                | 1.0                 | μs   |
|                                                                                                          | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 01       |                 | 0.6  | 1.0                                | 1.8                 |      |
|                                                                                                          | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 10       |                 | 1.0  | 1.8                                | 3.4                 |      |
|                                                                                                          | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 11       |                 | 1.8  | 3.4                                | 6.5                 |      |
| t <sub>EN_CMP</sub> Comparator enable time                                                               | CBON = 0 to CBON = 1, CBPWRMD = 00, 01                         |                 |      | 1                                  | 2                   | μs   |
|                                                                                                          | CBON = 0 to CBON = 1, CBPWRMD = 10                             |                 |      |                                    | 100                 |      |
| t <sub>EN_REF</sub> Resistor reference enable time                                                       | CBON = 0 to CBON = 1                                           |                 |      | 1                                  | 1.5                 | μs   |
| V <sub>CB_REF</sub> Reference voltage for a given tap                                                    | V <sub>IN</sub> = reference into resistor ladder (n = 0 to 31) |                 |      | $\frac{V_{IN} \times (n + 1)}{32}$ |                     | V    |

## 5.43 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                               |                                                                                                  | T <sub>J</sub> | MIN             | TYP             | MAX | UNIT   |
|-----------------------------------------|--------------------------------------------------------------------------------------------------|----------------|-----------------|-----------------|-----|--------|
| DV <sub>CC(PGM/ERASE)</sub>             | Program or erase supply voltage                                                                  |                | 1.8             |                 | 3.6 | V      |
| I <sub>PGM</sub>                        | Average supply current from DVCC during program                                                  |                |                 | 3               | 5   | mA     |
| I <sub>ERASE</sub>                      | Average supply current from DVCC during erase                                                    |                |                 | 6               | 11  | mA     |
| I <sub>MERASE</sub> , I <sub>BANK</sub> | Average supply current from DVCC during mass erase or bank erase                                 |                |                 | 6               | 11  | mA     |
| t <sub>CPT</sub>                        | Cumulative program time <sup>(1)</sup>                                                           |                |                 |                 | 16  | ms     |
|                                         | Program and erase endurance                                                                      |                | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles |
| t <sub>Retention</sub>                  | Data retention duration                                                                          | 25°C           | 100             |                 |     | years  |
| t <sub>Word</sub>                       | Word or byte program time <sup>(2)</sup>                                                         |                | 64              |                 | 85  | μs     |
| t <sub>Block, 0</sub>                   | Block program time for first byte or word <sup>(2)</sup>                                         |                | 49              |                 | 65  | μs     |
| t <sub>Block, 1–(N–1)</sub>             | Block program time for each additional byte or word, except for last byte or word <sup>(2)</sup> |                | 37              |                 | 49  | μs     |
| t <sub>Block, N</sub>                   | Block program time for last byte or word <sup>(2)</sup>                                          |                | 55              |                 | 73  | μs     |
| t <sub>Erase</sub>                      | Erase time for segment, mass erase, and bank erase (when available) <sup>(2)</sup>               |                | 23              |                 | 32  | ms     |
| f <sub>MCLK,MGR</sub>                   | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)                          |                | 0               |                 | 1   | MHz    |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) These values are hardwired into the state machine of the flash controller.

## 5.44 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                                                                     | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|-----------------------|-------------------------------------------------------------------------------------|-----------------|-------|-----|-----|------|
| f <sub>SBW</sub>      | Spy-Bi-Wire input frequency                                                         | 2.2 V, 3 V      | 0     |     | 20  | MHz  |
| t <sub>SBW,Low</sub>  | Spy-Bi-Wire low clock pulse duration                                                | 2.2 V, 3 V      | 0.025 |     | 15  | μs   |
| t <sub>SBW,En</sub>   | Spy-Bi-Wire enable time, TEST high to acceptance of first clock edge <sup>(1)</sup> | 2.2 V, 3 V      |       |     | 1   | μs   |
| t <sub>SBW,Rst</sub>  | Spy-Bi-Wire return to normal operation time                                         |                 | 15    |     | 100 | μs   |
| f <sub>TCK</sub>      | TCK input frequency, 4-wire JTAG <sup>(2)</sup>                                     | 2.2 V           | 0     |     | 5   | MHz  |
|                       |                                                                                     | 3 V             | 0     |     | 10  |      |
| R <sub>Internal</sub> | Internal pulldown resistance on TEST                                                | 2.2 V, 3 V      | 45    | 60  | 80  | kΩ   |

(1) Tools that access the Spy-Bi-Wire interface must wait for the t<sub>SBW,En</sub> time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.

## 6 Detailed Description

### 6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [Figure 6-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Figure 6-1. CPU Registers**

## 6.2 Operating Modes

These microcontrollers have one active mode and six software-selectable low-power modes of operation. An interrupt event can wake the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up input from  $\overline{\text{RST}}$ /NMI, P1, and P2

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[www.ti.com](http://www.ti.com)**6.3 Interrupt Vector Addresses**

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-1](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 6-1. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE                                                                                                                                        | INTERRUPT FLAG                                                                                             | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|------------------|--------------|-------------|
| <b>System Reset</b><br>Power up<br>External reset<br>Watchdog time-out, password violation<br>Flash memory password violation<br>PMM password violation | WDTIFG, KEYV (SYSRSTIV) <sup>(1) (2)</sup>                                                                 | Reset            | 0FFFEh       | 63, highest |
| <b>System NMI</b><br>PMM<br>Vacant memory access<br>JTAG mailbox                                                                                        | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBINIFG, JMBOUTIFG (SYSSNIV) <sup>(1)</sup> | (Non)maskable    | 0FFFCh       | 62          |
| <b>User NMI</b><br>NMI<br>Oscillator fault<br>Flash memory access violation                                                                             | NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) <sup>(1) (2)</sup>                                                | (Non)maskable    | 0FFFAh       | 61          |
| Comp_B                                                                                                                                                  | Comparator B interrupt flags (CBIV) <sup>(1) (3)</sup>                                                     | Maskable         | 0FFF8h       | 60          |
| TB0                                                                                                                                                     | TB0CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFF6h       | 59          |
| TB0                                                                                                                                                     | TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV) <sup>(1) (3)</sup>                                        | Maskable         | 0FFF4h       | 58          |
| Watchdog Timer_A interval timer mode                                                                                                                    | WDTIFG                                                                                                     | Maskable         | 0FFF2h       | 57          |
| USCI_A0 receive or transmit                                                                                                                             | UCA0RXIFG, UCA0TXIFG (UCA0IV) <sup>(1) (3)</sup>                                                           | Maskable         | 0FFF0h       | 56          |
| USCI_B0 receive or transmit                                                                                                                             | UCB0RXIFG, UCB0TXIFG (UCB0IV) <sup>(1) (3)</sup>                                                           | Maskable         | 0FFEEh       | 55          |
| ADC12_A                                                                                                                                                 | ADC12IFG0 to ADC12IFG15 (ADC12IV) <sup>(1) (3) (4)</sup>                                                   | Maskable         | 0FFECCh      | 54          |
| TA0                                                                                                                                                     | TA0CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFEAh       | 53          |
| TA0                                                                                                                                                     | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) <sup>(1) (3)</sup>                                        | Maskable         | 0FFE8h       | 52          |
| Reserved                                                                                                                                                | Reserved                                                                                                   | Maskable         | 0FFE6h       | 51          |
| DMA                                                                                                                                                     | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) <sup>(1) (3)</sup>                                                       | Maskable         | 0FFE4h       | 50          |
| TA1                                                                                                                                                     | TA1CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFE2h       | 49          |
| TA1                                                                                                                                                     | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) <sup>(1) (3)</sup>                                        | Maskable         | 0FFE0h       | 48          |
| I/O port P1                                                                                                                                             | P1IFG.0 to P1IFG.7 (P1IV) <sup>(1) (3)</sup>                                                               | Maskable         | 0FFDEh       | 47          |
| USCI_A1 receive or transmit                                                                                                                             | UCA1RXIFG, UCA1TXIFG (UCA1IV) <sup>(1) (3)</sup>                                                           | Maskable         | 0FFDCh       | 46          |
| USCI_B1 receive or transmit                                                                                                                             | UCB1RXIFG, UCB1TXIFG (UCB1IV) <sup>(1) (3)</sup>                                                           | Maskable         | 0FFDAh       | 45          |
| TA2                                                                                                                                                     | TA2CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFD8h       | 44          |
| TA2                                                                                                                                                     | TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) <sup>(1) (3)</sup>                                        | Maskable         | 0FFD6h       | 43          |
| I/O port P2                                                                                                                                             | P2IFG.0 to P2IFG.7 (P2IV) <sup>(1) (3)</sup>                                                               | Maskable         | 0FFD4h       | 42          |
| RTC_A                                                                                                                                                   | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) <sup>(1) (3)</sup>                               | Maskable         | 0FFD2h       | 41          |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.

(3) Interrupt flags are in the module.

(4) Only on devices with ADC, otherwise reserved.

**Table 6-1. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG          | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY  |
|------------------|-------------------------|------------------|--------------|-----------|
| Reserved         | Reserved <sup>(5)</sup> |                  | 0FFD0h       | 40        |
|                  |                         |                  | ⋮            | ⋮         |
|                  |                         |                  | 0FF80h       | 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

## 6.4 Memory Organization

[Table 6-2](#) summarizes the memory map for all device variants.

**Table 6-2. Memory Organization<sup>(1)</sup>**

|                                 |            | MSP430F5340                 | MSP430F5341                 | MSP430F5342                 |
|---------------------------------|------------|-----------------------------|-----------------------------|-----------------------------|
| Memory (flash)                  | Total Size | 64KB<br>00FFFFh to 00FF80h  | 96KB<br>00FFFFh to 00FF80h  | 128KB<br>00FFFFh to 00FF80h |
| Main: code memory               | Bank D     | N/A                         | N/A                         | 32KB<br>0243FFh to 01C400h  |
|                                 | Bank C     | N/A                         | 32KB<br>01C3FFh to 014400h  | 32KB<br>01C3FFh to 014400h  |
|                                 | Bank B     | 32KB<br>0143FFh to 00C400h  | 32KB<br>0143FFh to 00C400h  | 32KB<br>0143FFh to 00C400h  |
|                                 | Bank A     | 32KB<br>00C3FFh to 004400h  | 32KB<br>00C3FFh to 004400h  | 32KB<br>00C3FFh to 004400h  |
| RAM                             | Sector 3   | N/A                         | N/A                         | 2 KB<br>0043FFh to 003C00h  |
|                                 | Sector 2   | N/A                         | 2KB<br>003BFFh to 003400h   | 2KB<br>003BFFh to 003400h   |
|                                 | Sector 1   | 2KB<br>0033FFh to 002C00h   | 2KB<br>0033FFh to 002C00h   | 2KB<br>0033FFh to 002C00h   |
|                                 | Sector 0   | 2KB<br>002BFFh to 002400h   | 2KB<br>002BFFh to 002400h   | 2KB<br>002BFFh to 002400h   |
|                                 | Sector 7   | 2KB<br>0023FFh to 001C00h   | 2KB<br>0023FFh to 001C00h   | 2KB<br>0023FFh to 001C00h   |
| Information memory (flash)      | Info A     | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h |
|                                 | Info B     | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h |
|                                 | Info C     | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h |
|                                 | Info D     | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h |
| Bootloader (BSL) memory (flash) | BSL 3      | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h |
|                                 | BSL 2      | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h |
|                                 | BSL 1      | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h |
|                                 | BSL 0      | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h |
| Peripherals                     | Size       | 4KB<br>000FFFh to 0h        | 4KB<br>000FFFh to 0h        | 4KB<br>000FFFh to 0h        |

(1) N/A = Not available

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**6.5 Bootloader (BSL)**

The BSL lets users program the flash memory or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. [Table 6-3](#) lists the pins that are required to use the BSL. BSL entry requires a specific entry sequence on the  $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$  and  $\text{TEST}/\text{SBWTCK}$  pins. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For complete description of the features of the BSL and its implementation, see [MSP430 Flash Device Bootloader \(BSL\) User's Guide](#).

**Table 6-3. BSL Pin Requirements and Functions**

| DEVICE SIGNAL                                     | BSL FUNCTION          |
|---------------------------------------------------|-----------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| $\text{TEST}/\text{SBWTCK}$                       | Entry sequence signal |
| P1.1                                              | Data transmit         |
| P1.2                                              | Data receive          |
| VCC                                               | Power supply          |
| VSS                                               | Ground supply         |

**6.6 JTAG Operation****6.6.1 JTAG Standard Interface**

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The  $\text{TEST}/\text{SBWTCK}$  pin is used to enable the JTAG signals. In addition to these signals, the  $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$  is required to interface with MSP430 development tools and device programmers. [Table 6-4](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

**Table 6-4. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL                                     | DIRECTION | FUNCTION                    |
|---------------------------------------------------|-----------|-----------------------------|
| PJ.3/TCK                                          | IN        | JTAG clock input            |
| PJ.2/TMS                                          | IN        | JTAG state control          |
| PJ.1/TDI/TCLK                                     | IN        | JTAG data input, TCLK input |
| PJ.0/TDO                                          | OUT       | JTAG data output            |
| $\text{TEST}/\text{SBWTCK}$                       | IN        | Enable JTAG pins            |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN        | External reset              |
| VCC                                               |           | Power supply                |
| VSS                                               |           | Ground supply               |

**6.6.2 Spy-Bi-Wire Interface**

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. [Table 6-5](#) lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

**Table 6-5. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL  | DIRECTION | FUNCTION                      |
|----------------|-----------|-------------------------------|
| TEST/SBWTCK    | IN        | Spy-Bi-Wire clock input       |
| RST/NMI/SBWDIO | IN, OUT   | Spy-Bi-Wire data input/output |
| VCC            |           | Power supply                  |
| VSS            |           | Ground supply                 |

## 6.7 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

## 6.8 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors. See [Section 6.4](#) for the size of a sector.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.

## 6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

### 6.9.1 Digital I/O

Up to eight 8-bit I/O ports are implemented. For 80-pin options, P1, P2, P3, P4, P5, P6, and P7 are complete, and P8 is reduced to 3-bit I/O. For 64-pin options, P3 and P5 are reduced to 5-bit I/O and 6-bit I/O, respectively, and P7 and P8 are completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wake-up input capability available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P8) or word-wise in pairs (PA through PD).

### 6.9.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4 (see [Table 6-6](#)). [Table 6-7](#) lists the default settings for all pins that support port mapping.

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[www.ti.com](http://www.ti.com)**Table 6-6. Port Mapping Mnemonics and Functions**

| VALUE                    | PxMAPy MNEMONIC | INPUT PIN FUNCTION                                                                                                         | OUTPUT PIN FUNCTION          |
|--------------------------|-----------------|----------------------------------------------------------------------------------------------------------------------------|------------------------------|
| 0                        | PM_NONE         | None                                                                                                                       | DVSS                         |
| 1                        | PM_CBOU0        | –                                                                                                                          | Comparator_B output          |
|                          | PM_TB0CLK       | TB0 clock input                                                                                                            | –                            |
| 2                        | PM_ADC12CLK     | –                                                                                                                          | ADC12CLK                     |
|                          | PM_DMAE0        | DMAE0 input                                                                                                                | –                            |
| 3                        | PM_SVMOUT       | –                                                                                                                          | SVM output                   |
|                          | PM_TB0OUTH      | TB0 high-impedance input TB0OUTH                                                                                           | –                            |
| 4                        | PM_TB0CCR0A     | TB0 CCR0 capture input CCI0A                                                                                               | TB0 CCR0 compare output Out0 |
| 5                        | PM_TB0CCR1A     | TB0 CCR1 capture input CCI1A                                                                                               | TB0 CCR1 compare output Out1 |
| 6                        | PM_TB0CCR2A     | TB0 CCR2 capture input CCI2A                                                                                               | TB0 CCR2 compare output Out2 |
| 7                        | PM_TB0CCR3A     | TB0 CCR3 capture input CCI3A                                                                                               | TB0 CCR3 compare output Out3 |
| 8                        | PM_TB0CCR4A     | TB0 CCR4 capture input CCI4A                                                                                               | TB0 CCR4 compare output Out4 |
| 9                        | PM_TB0CCR5A     | TB0 CCR5 capture input CCI5A                                                                                               | TB0 CCR5 compare output Out5 |
| 10                       | PM_TB0CCR6A     | TB0 CCR6 capture input CCI6A                                                                                               | TB0 CCR6 compare output Out6 |
| 11                       | PM_UCA1RXD      | USCI_A1 UART RXD (Direction controlled by USCI – input)                                                                    |                              |
|                          | PM_UCA1SOMI     | USCI_A1 SPI slave out master in (direction controlled by USCI)                                                             |                              |
| 12                       | PM_UCA1TXD      | USCI_A1 UART TXD (Direction controlled by USCI – output)                                                                   |                              |
|                          | PM_UCA1SIMO     | USCI_A1 SPI slave in master out (direction controlled by USCI)                                                             |                              |
| 13                       | PM_UCA1CLK      | USCI_A1 clock input/output (direction controlled by USCI)                                                                  |                              |
|                          | PM_UCB1STE      | USCI_B1 SPI slave transmit enable (direction controlled by USCI)                                                           |                              |
| 14                       | PM_UCB1SOMI     | USCI_B1 SPI slave out master in (direction controlled by USCI)                                                             |                              |
|                          | PM_UCB1SCL      | USCI_B1 I <sup>2</sup> C clock (open drain and direction controlled by USCI)                                               |                              |
| 15                       | PM_UCB1SIMO     | USCI_B1 SPI slave in master out (direction controlled by USCI)                                                             |                              |
|                          | PM_UCB1SDA      | USCI_B1 I <sup>2</sup> C data (open drain and direction controlled by USCI)                                                |                              |
| 16                       | PM_UCB1CLK      | USCI_B1 clock input/output (direction controlled by USCI)                                                                  |                              |
|                          | PM_UCA1STE      | USCI_A1 SPI slave transmit enable (direction controlled by USCI)                                                           |                              |
| 17                       | PM_CBOU1        | None                                                                                                                       | Comparator_B output          |
| 18                       | PM_MCLK         | None                                                                                                                       | MCLK                         |
| 19-30                    | Reserved        | None                                                                                                                       | DVSS                         |
| 31 (0FFh) <sup>(1)</sup> | PM_ANALOG       | Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. |                              |

- (1) The value of the PM\_ANALOG mnemonic is 0FFh. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read out value of 31.

**Table 6-7. Default Mapping**

| PIN         | PxMAPy MNEMONIC        | INPUT PIN FUNCTION                                                                                                                             | OUTPUT PIN FUNCTION |
|-------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| P4.0/P4MAP0 | PM_UCB1STE/PM_UCA1CLK  | USCI_B1 SPI slave transmit enable (direction controlled by USCI)<br>USCI_A1 clock input/output (direction controlled by USCI)                  |                     |
| P4.1/P4MAP1 | PM_UCB1SIMO/PM_UCB1SDA | USCI_B1 SPI slave in master out (direction controlled by USCI)<br>USCI_B1 I <sup>2</sup> C data (open drain and direction controlled by USCI)  |                     |
| P4.2/P4MAP2 | PM_UCB1SOMI/PM_UCB1SCL | USCI_B1 SPI slave out master in (direction controlled by USCI)<br>USCI_B1 I <sup>2</sup> C clock (open drain and direction controlled by USCI) |                     |
| P4.3/P4MAP3 | PM_UCB1CLK/PM_UCA1STE  | USCI_A1 SPI slave transmit enable (direction controlled by USCI)<br>USCI_B1 clock input/output (direction controlled by USCI)                  |                     |
| P4.4/P4MAP4 | PM_UCA1TXD/PM_UCA1SIMO | USCI_A1 UART TXD (Direction controlled by USCI – output)<br>USCI_A1 SPI slave in master out (direction controlled by USCI)                     |                     |
| P4.5/P4MAP5 | PM_UCA1RXD/PM_UCA1SOMI | USCI_A1 UART RXD (Direction controlled by USCI – input)<br>USCI_A1 SPI slave out master in (direction controlled by USCI)                      |                     |
| P4.6/P4MAP6 | PM_NONE                | None                                                                                                                                           | DVSS                |
| P4.7/P4MAP7 | PM_NONE                | None                                                                                                                                           | DVSS                |

### 6.9.3 Oscillator and System Clock

The clock system is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features a digital frequency-locked loop (FLL) that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3.5  $\mu$ s (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by the same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by the same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

### 6.9.4 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

### 6.9.5 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 6.9.6 Real-Time Clock (RTC\_A)

The RTC\_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC\_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer or counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC\_A also supports flexible alarm functions and offset-calibration hardware.

### 6.9.7 Watchdog Timer (WDT\_A)

The primary function of the WDT\_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

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[www.ti.com](http://www.ti.com)**6.9.8 System Module (SYS)**

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, as well as configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. [Table 6-8](#) lists the interrupt vector registers of the SYS module.

**Table 6-8. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT                     | VALUE      | PRIORITY |
|---------------------------|---------|-------------------------------------|------------|----------|
| SYSRSTIV, System Reset    | 019Eh   | No interrupt pending                | 00h        |          |
|                           |         | Brownout (BOR)                      | 02h        | Highest  |
|                           |         | $\overline{\text{RST}}$ /NMI (POR)  | 04h        |          |
|                           |         | PMMSWBOR (BOR)                      | 06h        |          |
|                           |         | Wakeup from LPMx.5                  | 08h        |          |
|                           |         | Security violation (BOR)            | 0Ah        |          |
|                           |         | SVSL (POR)                          | 0Ch        |          |
|                           |         | SVSH (POR)                          | 0Eh        |          |
|                           |         | SVML_OVP (POR)                      | 10h        |          |
|                           |         | SVMH_OVP (POR)                      | 12h        |          |
|                           |         | PMMSWPOR (POR)                      | 14h        |          |
|                           |         | WDT time-out (PUC)                  | 16h        |          |
|                           |         | WDT password violation (PUC)        | 18h        |          |
|                           |         | KEYV flash password violation (PUC) | 1Ah        |          |
|                           |         | Reserved                            | 1Ch        |          |
|                           |         | Peripheral area fetch (PUC)         | 1Eh        |          |
|                           |         | PMM password violation (PUC)        | 20h        |          |
|                           |         | Reserved                            | 22h to 3Eh | Lowest   |
| SYSSNIV, System NMI       | 019Ch   | No interrupt pending                | 00h        |          |
|                           |         | SVMLIFG                             | 02h        | Highest  |
|                           |         | SVMHIFG                             | 04h        |          |
|                           |         | SVSMLDLYIFG                         | 06h        |          |
|                           |         | SVSMHDLYIFG                         | 08h        |          |
|                           |         | VMAIFG                              | 0Ah        |          |
|                           |         | JMBINIFG                            | 0Ch        |          |
|                           |         | JMBOUTIFG                           | 0Eh        |          |
|                           |         | SVMLVLRIFG                          | 10h        |          |
|                           |         | SVMHVLRIFG                          | 12h        |          |
|                           |         | Reserved                            | 14h to 1Eh | Lowest   |
| SYSUNIV, User NMI         | 019Ah   | No interrupt pending                | 00h        |          |
|                           |         | NMIIFG                              | 02h        | Highest  |
|                           |         | OFIFG                               | 04h        |          |
|                           |         | ACCVIFG                             | 06h        |          |
|                           |         | Reserved                            | 08h        |          |
|                           |         | Reserved                            | 0Ah to 1Eh | Lowest   |

### 6.9.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can move data from the ADC12\_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. [Table 6-9](#) lists the available DMA triggers.

**Table 6-9. DMA Trigger Assignments<sup>(1)</sup>**

| TRIGGER | CHANNEL       |               |               |
|---------|---------------|---------------|---------------|
|         | 0             | 1             | 2             |
| 0       | DMAREQ        | DMAREQ        | DMAREQ        |
| 1       | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2       | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3       | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4       | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5       | TA2CCR0 CCIFG | TA2CCR0 CCIFG | TA2CCR0 CCIFG |
| 6       | TA2CCR2 CCIFG | TA2CCR2 CCIFG | TA2CCR2 CCIFG |
| 7       | TB0CCR0 CCIFG | TB0CCR0 CCIFG | TB0CCR0 CCIFG |
| 8       | TB0CCR2 CCIFG | TB0CCR2 CCIFG | TB0CCR2 CCIFG |
| 9       | Reserved      | Reserved      | Reserved      |
| 10      | Reserved      | Reserved      | Reserved      |
| 11      | Reserved      | Reserved      | Reserved      |
| 12      | Reserved      | Reserved      | Reserved      |
| 13      | Reserved      | Reserved      | Reserved      |
| 14      | Reserved      | Reserved      | Reserved      |
| 15      | Reserved      | Reserved      | Reserved      |
| 16      | UCA0RXIFG     | UCA0RXIFG     | UCA0RXIFG     |
| 17      | UCA0TXIFG     | UCA0TXIFG     | UCA0TXIFG     |
| 18      | UCB0RXIFG     | UCB0RXIFG     | UCB0RXIFG     |
| 19      | UCB0TXIFG     | UCB0TXIFG     | UCB0TXIFG     |
| 20      | UCA1RXIFG     | UCA1RXIFG     | UCA1RXIFG     |
| 21      | UCA1TXIFG     | UCA1TXIFG     | UCA1TXIFG     |
| 22      | UCB1RXIFG     | UCB1RXIFG     | UCB1RXIFG     |
| 23      | UCB1TXIFG     | UCB1TXIFG     | UCB1TXIFG     |
| 24      | ADC12IFGx     | ADC12IFGx     | ADC12IFGx     |
| 25      | Reserved      | Reserved      | Reserved      |
| 26      | Reserved      | Reserved      | Reserved      |
| 27      | Reserved      | Reserved      | Reserved      |
| 28      | Reserved      | Reserved      | Reserved      |
| 29      | MPY ready     | MPY ready     | MPY ready     |
| 30      | DMA2IFG       | DMA0IFG       | DMA1IFG       |
| 31      | DMAE0         | DMAE0         | DMAE0         |

(1) If a reserved trigger source is selected, no trigger is generated.

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[www.ti.com](http://www.ti.com)**6.9.10 Universal Serial Communication Interface (USCI)**

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I<sup>2</sup>C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI\_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI\_Bn module provides support for SPI (3- or 4-pin) or I<sup>2</sup>C.

The MSP430F534x MCUs include two complete USCI modules (n = 0, 1).

**6.9.11 TA0**

TA0 is a 16-bit timer/counter (Timer\_A type) with five capture/compare registers. TA0 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-10](#)). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-10. TA0 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL       | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER                   |
|------------------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------------------------|
| 13-P1.0          | TA0CLK              | TACLK                     | Timer        | N/A                  | N/A                  |                                     |
|                  | ACLK (internal)     | ACLK                      |              |                      |                      |                                     |
|                  | SMCLK (internal)    | SMCLK                     |              |                      |                      |                                     |
| 13-P1.0          | TA0CLK              | $\overline{\text{TACLK}}$ |              |                      |                      |                                     |
| 14-P1.1          | TA0.0               | CCI0A                     | CCR0         | TA0                  | TA0.0                | 14-P1.1                             |
|                  | DV <sub>SS</sub>    | CCI0B                     |              |                      |                      |                                     |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                                     |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                                     |
| 15-P1.2          | TA0.1               | CCI1A                     | CCR1         | TA1                  | TA0.1                | 15-P1.2                             |
|                  | CBOUT (internal)    | CCI1B                     |              |                      |                      | ADC12 (internal)<br>ADC12SHSx = {1} |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                                     |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                                     |
| 16-P1.3          | TA0.2               | CCI2A                     | CCR2         | TA2                  | TA0.2                | 16-P1.3                             |
|                  | ACLK (internal)     | CCI2B                     |              |                      |                      |                                     |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                                     |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                                     |
| 17-P1.4          | TA0.3               | CCI3A                     | CCR3         | TA3                  | TA0.3                | 17-P1.4                             |
|                  | DV <sub>SS</sub>    | CCI3B                     |              |                      |                      |                                     |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                                     |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                                     |
| 18-P1.5          | TA0.4               | CCI4A                     | CCR4         | TA4                  | TA0.4                | 18-P1.5                             |
|                  | DV <sub>SS</sub>    | CCI4B                     |              |                      |                      |                                     |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                                     |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                                     |

## 6.9.12 TA1

TA1 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. TA1 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-11](#)). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-11. TA1 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL       | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|------------------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|
| 19-P1.6          | TA1CLK              | TACLK                     | Timer        | N/A                  | N/A                  |                   |
|                  | ACLK (internal)     | ACLK                      |              |                      |                      |                   |
|                  | SMCLK (internal)    | SMCLK                     |              |                      |                      |                   |
| 19-P1.6          | TA1CLK              | $\overline{\text{TACLK}}$ |              |                      |                      |                   |
| 20-P1.7          | TA1.0               | CCI0A                     | CCR0         | TA0                  | TA1.0                | 20-P1.7           |
|                  | DV <sub>SS</sub>    | CCI0B                     |              |                      |                      |                   |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                   |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                   |
| Not available    | TA1.1               | CCI1A                     | CCR1         | TA1                  | TA1.1                | Not available     |
|                  | CBOUT (internal)    | CCI1B                     |              |                      |                      |                   |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                   |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                   |
| Not available    | TA1.2               | CCI2A                     | CCR2         | TA2                  | TA1.2                | Not available     |
|                  | ACLK (internal)     | CCI2B                     |              |                      |                      |                   |
|                  | DV <sub>SS</sub>    | GND                       |              |                      |                      |                   |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>           |              |                      |                      |                   |

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[www.ti.com](http://www.ti.com)**6.9.13 TA2**

TA2 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. TA2 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-12](#)). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-12. TA2 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|------------------|---------------------|---------------------|--------------|----------------------|----------------------|-------------------|
| Not available    | TA2CLK              | TACLK               | Timer        | N/A                  | N/A                  |                   |
|                  | ACLK (internal)     | ACLK                |              |                      |                      |                   |
|                  | SMCLK (internal)    | SMCLK               |              |                      |                      |                   |
| Not available    | TA2CLK              | TACLK               |              |                      |                      |                   |
| Not available    | TA2.0               | CCI0A               | CCR0         | TA0                  | TA2.0                | Not available     |
|                  | DV <sub>SS</sub>    | CCI0B               |              |                      |                      |                   |
|                  | DV <sub>SS</sub>    | GND                 |              |                      |                      |                   |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>     |              |                      |                      |                   |
| Not available    | TA2.1               | CCI1A               | CCR1         | TA1                  | TA2.1                | Not available     |
|                  | CBOUT (internal)    | CCI1B               |              |                      |                      |                   |
|                  | DV <sub>SS</sub>    | GND                 |              |                      |                      |                   |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>     |              |                      |                      |                   |
| Not available    | TA2.2               | CCI2A               | CCR2         | TA2                  | TA2.2                | Not available     |
|                  | ACLK (internal)     | CCI2B               |              |                      |                      |                   |
|                  | DV <sub>SS</sub>    | GND                 |              |                      |                      |                   |
|                  | DV <sub>CC</sub>    | V <sub>CC</sub>     |              |                      |                      |                   |

## 6.9.14 TB0

TB0 is a 16-bit timer/counter (Timer\_B type) with seven capture/compare registers. TB0 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-13](#)). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-13. TB0 Signal Connections**

| INPUT PIN NUMBER <sup>(1)</sup> | DEVICE INPUT SIGNAL          | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER <sup>(1)</sup>    |
|---------------------------------|------------------------------|---------------------|--------------|----------------------|----------------------|-------------------------------------|
|                                 | TB0CLK                       | TBCLK               | Timer        | N/A                  | N/A                  |                                     |
|                                 | ACLK (internal)              | ACLK                |              |                      |                      |                                     |
|                                 | SMCLK (internal)             | SMCLK               |              |                      |                      |                                     |
|                                 | TB0CLK                       | TBCLK               |              |                      |                      |                                     |
|                                 | TB0.0                        | CCI0A               | CCR0         | TB0                  | TB0.0                |                                     |
|                                 | TB0.0                        | CCI0B               |              |                      |                      | ADC12 (internal)<br>ADC12SHSx = {2} |
|                                 | DV <sub>SS</sub>             | GND                 |              |                      |                      |                                     |
|                                 | DV <sub>CC</sub>             | V <sub>CC</sub>     |              |                      |                      |                                     |
| 37-P5.7                         | TB0.1                        | CCI1A               | CCR1         | TB1                  | TB0.1                | 37-P5.7                             |
|                                 | CBOU <sub>T</sub> (internal) | CCI1B               |              |                      |                      | ADC12 (internal)<br>ADC12SHSx = {3} |
|                                 | DV <sub>SS</sub>             | GND                 |              |                      |                      |                                     |
|                                 | DV <sub>CC</sub>             | V <sub>CC</sub>     |              |                      |                      |                                     |
|                                 | TB0.2                        | CCI2A               | CCR2         | TB2                  | TB0.2                |                                     |
|                                 | TB0.2                        | CCI2B               |              |                      |                      |                                     |
|                                 | DV <sub>SS</sub>             | GND                 |              |                      |                      |                                     |
|                                 | DV <sub>CC</sub>             | V <sub>CC</sub>     |              |                      |                      |                                     |
|                                 | TB0.3                        | CCI3A               | CCR3         | TB3                  | TB0.3                |                                     |
|                                 | TB0.3                        | CCI3B               |              |                      |                      |                                     |
|                                 | DV <sub>SS</sub>             | GND                 |              |                      |                      |                                     |
|                                 | DV <sub>CC</sub>             | V <sub>CC</sub>     |              |                      |                      |                                     |
|                                 | TB0.4                        | CCI4A               | CCR4         | TB4                  | TB0.4                |                                     |
|                                 | TB0.4                        | CCI4B               |              |                      |                      |                                     |
|                                 | DV <sub>SS</sub>             | GND                 |              |                      |                      |                                     |
|                                 | DV <sub>CC</sub>             | V <sub>CC</sub>     |              |                      |                      |                                     |
|                                 | TB0.5                        | CCI5A               | CCR5         | TB5                  | TB0.5                |                                     |
|                                 | TB0.5                        | CCI5B               |              |                      |                      |                                     |
|                                 | DV <sub>SS</sub>             | GND                 |              |                      |                      |                                     |
|                                 | DV <sub>CC</sub>             | V <sub>CC</sub>     |              |                      |                      |                                     |
|                                 | TB0.6                        | CCI6A               | CCR6         | TB6                  | TB0.6                |                                     |
|                                 | ACLK (internal)              | CCI6B               |              |                      |                      |                                     |
|                                 | DV <sub>SS</sub>             | GND                 |              |                      |                      |                                     |
|                                 | DV <sub>CC</sub>             | V <sub>CC</sub>     |              |                      |                      |                                     |

(1) Timer functions selectable through the port mapping controller.

### **6.9.15 Comparator\_B**

The primary function of the Comparator\_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### **6.9.16 ADC12\_A**

The ADC12\_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

### **6.9.17 CRC16**

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

### **6.9.18 Reference (REF) Module Voltage Reference**

The REF module generates all critical reference voltages that can be used by the various analog peripherals in the device.

### **6.9.19 Embedded Emulation Module (EEM)**

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware trigger or breakpoint on CPU register write access
- Up to 10 hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

## 6.9.20 Peripheral File Map

Table 6-14 lists the base address for all of the peripherals that are available. Table 6-15 through Table 6-41 list the registers available in each peripheral.

**Table 6-14. Peripherals**

| MODULE NAME                                 | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---------------------------------------------|--------------|----------------------|
| Special Functions (see Table 6-15)          | 0100h        | 000h to 01Fh         |
| PMM (see Table 6-16)                        | 0120h        | 000h to 010h         |
| Flash Control (see Table 6-17)              | 0140h        | 000h to 00Fh         |
| CRC16 (see Table 6-18)                      | 0150h        | 000h to 007h         |
| RAM Control (see Table 6-19)                | 0158h        | 000h to 001h         |
| Watchdog (see Table 6-20)                   | 015Ch        | 000h to 001h         |
| UCS (see Table 6-21)                        | 0160h        | 000h to 01Fh         |
| SYS (see Table 6-22)                        | 0180h        | 000h to 01Fh         |
| Shared Reference (see Table 6-23)           | 01B0h        | 000h to 001h         |
| Port Mapping Control (see Table 6-24)       | 01C0h        | 000h to 002h         |
| Port Mapping Port P4 (see Table 6-24)       | 01E0h        | 000h to 007h         |
| Port P1 and P2 (see Table 6-25)             | 0200h        | 000h to 01Fh         |
| Port P3 and P4 (see Table 6-26)             | 0220h        | 000h to 00Bh         |
| Port P5 and P6 (see Table 6-27)             | 0240h        | 000h to 00Bh         |
| Port PJ (see Table 6-28)                    | 0320h        | 000h to 01Fh         |
| TA0 (see Table 6-29)                        | 0340h        | 000h to 02Eh         |
| TA1 (see Table 6-30)                        | 0380h        | 000h to 02Eh         |
| TB0 (see Table 6-31)                        | 03C0h        | 000h to 02Eh         |
| TA2 (see Table 6-32)                        | 0400h        | 000h to 02Eh         |
| Real-Time Clock (RTC_A) (see Table 6-33)    | 04A0h        | 000h to 01Bh         |
| 32-Bit Hardware Multiplier (see Table 6-34) | 04C0h        | 000h to 02Fh         |
| DMA General Control (see Table 6-35)        | 0500h        | 000h to 00Fh         |
| DMA Channel 0 (see Table 6-35)              | 0510h        | 000h to 00Ah         |
| DMA Channel 1 (see Table 6-35)              | 0520h        | 000h to 00Ah         |
| DMA Channel 2 (see Table 6-35)              | 0530h        | 000h to 00Ah         |
| USCI_A0 (see Table 6-36)                    | 05C0h        | 000h to 01Fh         |
| USCI_B0 (see Table 6-37)                    | 05E0h        | 000h to 01Fh         |
| USCI_A1 (see Table 6-38)                    | 0600h        | 000h to 01Fh         |
| USCI_B1 (see Table 6-39)                    | 0620h        | 000h to 01Fh         |
| ADC12_A (see Table 6-40)                    | 0700h        | 000h to 03Eh         |
| Comparator_B (see Table 6-41)               | 08C0h        | 000h to 00Fh         |

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[www.ti.com](http://www.ti.com)**Table 6-15. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION  | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable  | SFRIE1   | 00h    |
| SFR interrupt flag    | SFRIFG1  | 02h    |
| SFR reset pin control | SFRRPCR  | 04h    |

**Table 6-16. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| PMM control 0            | PMMCTL0  | 00h    |
| PMM control 1            | PMMCTL1  | 02h    |
| SVS high-side control    | SVSMHCTL | 04h    |
| SVS low-side control     | SVSMLCTL | 06h    |
| PMM interrupt flags      | PMMIFG   | 0Ch    |
| PMM interrupt enable     | PMMIE    | 0Eh    |
| PMM power mode 5 control | PM5CTL0  | 10h    |

**Table 6-17. Flash Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1      | FCTL1    | 00h    |
| Flash control 3      | FCTL3    | 04h    |
| Flash control 4      | FCTL4    | 06h    |

**Table 6-18. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input                | CRC16DI   | 00h    |
| CRC data input reverse byte   | CRCDIRB   | 02h    |
| CRC initialization and result | CRCINIRES | 04h    |
| CRC result reverse byte       | CRCRESR   | 06h    |

**Table 6-19. RAM Control Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0        | RCCTL0   | 00h    |

**Table 6-20. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION   | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL   | 00h    |

**Table 6-21. UCS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0        | UCSCTL0  | 00h    |
| UCS control 1        | UCSCTL1  | 02h    |
| UCS control 2        | UCSCTL2  | 04h    |
| UCS control 3        | UCSCTL3  | 06h    |
| UCS control 4        | UCSCTL4  | 08h    |
| UCS control 5        | UCSCTL5  | 0Ah    |
| UCS control 6        | UCSCTL6  | 0Ch    |
| UCS control 7        | UCSCTL7  | 0Eh    |
| UCS control 8        | UCSCTL8  | 10h    |

**Table 6-22. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| System control                | SYSCTL    | 00h    |
| Bootloader configuration area | SYSBSLC   | 02h    |
| JTAG mailbox control          | SYSJMBC   | 06h    |
| JTAG mailbox input 0          | SYSJMBI0  | 08h    |
| JTAG mailbox input 1          | SYSJMBI1  | 0Ah    |
| JTAG mailbox output 0         | SYSJMBO0  | 0Ch    |
| JTAG mailbox output 1         | SYSJMBO1  | 0Eh    |
| Bus error vector generator    | SYSBERRIV | 18h    |
| User NMI vector generator     | SYSUNIV   | 1Ah    |
| System NMI vector generator   | SYSSNIV   | 1Ch    |
| Reset vector generator        | SYSRSTIV  | 1Eh    |

**Table 6-23. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL   | 00h    |

**Table 6-24. Port Mapping Registers  
(Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)**

| REGISTER DESCRIPTION | REGISTER  | OFFSET |
|----------------------|-----------|--------|
| Port mapping key/ID  | PMAPKEYID | 00h    |
| Port mapping control | PMAPCTL   | 02h    |
| Port P4.0 mapping    | P4MAP0    | 00h    |
| Port P4.1 mapping    | P4MAP1    | 01h    |
| Port P4.2 mapping    | P4MAP2    | 02h    |
| Port P4.3 mapping    | P4MAP3    | 03h    |
| Port P4.4 mapping    | P4MAP4    | 04h    |
| Port P4.5 mapping    | P4MAP5    | 05h    |
| Port P4.6 mapping    | P4MAP6    | 06h    |
| Port P4.7 mapping    | P4MAP7    | 07h    |

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[www.ti.com](http://www.ti.com)**Table 6-25. Port P1 and P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION          | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P1 input                 | P1IN     | 00h    |
| Port P1 output                | P1OUT    | 02h    |
| Port P1 direction             | P1DIR    | 04h    |
| Port P1 resistor enable       | P1REN    | 06h    |
| Port P1 drive strength        | P1DS     | 08h    |
| Port P1 selection             | P1SEL    | 0Ah    |
| Port P1 interrupt vector word | P1IV     | 0Eh    |
| Port P1 interrupt edge select | P1IES    | 18h    |
| Port P1 interrupt enable      | P1IE     | 1Ah    |
| Port P1 interrupt flag        | P1IFG    | 1Ch    |
| Port P2 input                 | P2IN     | 01h    |
| Port P2 output                | P2OUT    | 03h    |
| Port P2 direction             | P2DIR    | 05h    |
| Port P2 resistor enable       | P2REN    | 07h    |
| Port P2 drive strength        | P2DS     | 09h    |
| Port P2 selection             | P2SEL    | 0Bh    |
| Port P2 interrupt vector word | P2IV     | 1Eh    |
| Port P2 interrupt edge select | P2IES    | 19h    |
| Port P2 interrupt enable      | P2IE     | 1Bh    |
| Port P2 interrupt flag        | P2IFG    | 1Dh    |

**Table 6-26. Port P3 and P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P3 input           | P3IN     | 00h    |
| Port P3 output          | P3OUT    | 02h    |
| Port P3 direction       | P3DIR    | 04h    |
| Port P3 resistor enable | P3REN    | 06h    |
| Port P3 drive strength  | P3DS     | 08h    |
| Port P3 selection       | P3SEL    | 0Ah    |
| Port P4 input           | P4IN     | 01h    |
| Port P4 output          | P4OUT    | 03h    |
| Port P4 direction       | P4DIR    | 05h    |
| Port P4 resistor enable | P4REN    | 07h    |
| Port P4 drive strength  | P4DS     | 09h    |
| Port P4 selection       | P4SEL    | 0Bh    |

**Table 6-27. Port P5 and P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P5 input           | P5IN     | 00h    |
| Port P5 output          | P5OUT    | 02h    |
| Port P5 direction       | P5DIR    | 04h    |
| Port P5 resistor enable | P5REN    | 06h    |
| Port P5 drive strength  | P5DS     | 08h    |
| Port P5 selection       | P5SEL    | 0Ah    |
| Port P6 input           | P6IN     | 01h    |
| Port P6 output          | P6OUT    | 03h    |
| Port P6 direction       | P6DIR    | 05h    |
| Port P6 resistor enable | P6REN    | 07h    |
| Port P6 drive strength  | P6DS     | 09h    |
| Port P6 selection       | P6SEL    | 0Bh    |

**Table 6-28. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port PJ input           | PJIN     | 00h    |
| Port PJ output          | PJOUT    | 02h    |
| Port PJ direction       | PJDIR    | 04h    |
| Port PJ resistor enable | PJREN    | 06h    |
| Port PJ drive strength  | PJDS     | 08h    |

**Table 6-29. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA0 control               | TA0CTL   | 00h    |
| Capture/compare control 0 | TA0CCTL0 | 02h    |
| Capture/compare control 1 | TA0CCTL1 | 04h    |
| Capture/compare control 2 | TA0CCTL2 | 06h    |
| Capture/compare control 3 | TA0CCTL3 | 08h    |
| Capture/compare control 4 | TA0CCTL4 | 0Ah    |
| TA0 counter               | TA0R     | 10h    |
| Capture/compare 0         | TA0CCR0  | 12h    |
| Capture/compare 1         | TA0CCR1  | 14h    |
| Capture/compare 2         | TA0CCR2  | 16h    |
| Capture/compare 3         | TA0CCR3  | 18h    |
| Capture/compare 4         | TA0CCR4  | 1Ah    |
| TA0 expansion 0           | TA0EX0   | 20h    |
| TA0 interrupt vector      | TA0IV    | 2Eh    |

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[www.ti.com](http://www.ti.com)**Table 6-30. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control               | TA1CTL   | 00h    |
| Capture/compare control 0 | TA1CCTL0 | 02h    |
| Capture/compare control 1 | TA1CCTL1 | 04h    |
| Capture/compare control 2 | TA1CCTL2 | 06h    |
| TA1 counter               | TA1R     | 10h    |
| Capture/compare 0         | TA1CCR0  | 12h    |
| Capture/compare 1         | TA1CCR1  | 14h    |
| Capture/compare 2         | TA1CCR2  | 16h    |
| TA1 expansion 0           | TA1EX0   | 20h    |
| TA1 interrupt vector      | TA1IV    | 2Eh    |

**Table 6-31. TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB0 control               | TB0CTL   | 00h    |
| Capture/compare control 0 | TB0CCTL0 | 02h    |
| Capture/compare control 1 | TB0CCTL1 | 04h    |
| Capture/compare control 2 | TB0CCTL2 | 06h    |
| Capture/compare control 3 | TB0CCTL3 | 08h    |
| Capture/compare control 4 | TB0CCTL4 | 0Ah    |
| Capture/compare control 5 | TB0CCTL5 | 0Ch    |
| Capture/compare control 6 | TB0CCTL6 | 0Eh    |
| TB0 counter               | TB0R     | 10h    |
| Capture/compare 0         | TB0CCR0  | 12h    |
| Capture/compare 1         | TB0CCR1  | 14h    |
| Capture/compare 2         | TB0CCR2  | 16h    |
| Capture/compare 3         | TB0CCR3  | 18h    |
| Capture/compare 4         | TB0CCR4  | 1Ah    |
| Capture/compare 5         | TB0CCR5  | 1Ch    |
| Capture/compare 6         | TB0CCR6  | 1Eh    |
| TB0 expansion 0           | TB0EX0   | 20h    |
| TB0 interrupt vector      | TB0IV    | 2Eh    |

**Table 6-32. TA2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA2 control               | TA2CTL   | 00h    |
| Capture/compare control 0 | TA2CCTL0 | 02h    |
| Capture/compare control 1 | TA2CCTL1 | 04h    |
| Capture/compare control 2 | TA2CCTL2 | 06h    |
| TA2 counter               | TA2R     | 10h    |
| Capture/compare 0         | TA2CCR0  | 12h    |
| Capture/compare 1         | TA2CCR1  | 14h    |
| Capture/compare 2         | TA2CCR2  | 16h    |
| TA2 expansion 0           | TA2EX0   | 20h    |
| TA2 interrupt vector      | TA2IV    | 2Eh    |

**Table 6-33. Real-Time Clock Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION           | REGISTER        | OFFSET |
|--------------------------------|-----------------|--------|
| RTC control 0                  | RTCCTL0         | 00h    |
| RTC control 1                  | RTCCTL1         | 01h    |
| RTC control 2                  | RTCCTL2         | 02h    |
| RTC control 3                  | RTCCTL3         | 03h    |
| RTC prescaler 0 control        | RTCPSEL0CTL     | 08h    |
| RTC prescaler 1 control        | RTCPSEL1CTL     | 0Ah    |
| RTC prescaler 0                | RTCPSEL0        | 0Ch    |
| RTC prescaler 1                | RTCPSEL1        | 0Dh    |
| RTC interrupt vector word      | RTCIV           | 0Eh    |
| RTC seconds, RTC counter 1     | RTCSEC, RTCNT1  | 10h    |
| RTC minutes, RTC counter 2     | RTCMIN, RTCNT2  | 11h    |
| RTC hours, RTC counter 3       | RTCHOUR, RTCNT3 | 12h    |
| RTC day of week, RTC counter 4 | RTCDOW, RTCNT4  | 13h    |
| RTC days                       | RTCDAY          | 14h    |
| RTC month                      | RTCMON          | 15h    |
| RTC year low                   | RTCYEARL        | 16h    |
| RTC year high                  | RTCYEARH        | 17h    |
| RTC alarm minutes              | RTCAMIN         | 18h    |
| RTC alarm hours                | RTCAHOUR        | 19h    |
| RTC alarm day of week          | RTCADOW         | 1Ah    |
| RTC alarm days                 | RTCADAY         | 1Bh    |

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[www.ti.com](http://www.ti.com)**Table 6-34. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION                                    | REGISTER  | OFFSET |
|---------------------------------------------------------|-----------|--------|
| 16-bit operand 1 – multiply                             | MPY       | 00h    |
| 16-bit operand 1 – signed multiply                      | MPYS      | 02h    |
| 16-bit operand 1 – multiply accumulate                  | MAC       | 04h    |
| 16-bit operand 1 – signed multiply accumulate           | MACS      | 06h    |
| 16-bit operand 2                                        | OP2       | 08h    |
| 16 × 16 result low word                                 | RESLO     | 0Ah    |
| 16 × 16 result high word                                | RESHI     | 0Ch    |
| 16 × 16 sum extension                                   | SUMEXT    | 0Eh    |
| 32-bit operand 1 – multiply low word                    | MPY32L    | 10h    |
| 32-bit operand 1 – multiply high word                   | MPY32H    | 12h    |
| 32-bit operand 1 – signed multiply low word             | MPYS32L   | 14h    |
| 32-bit operand 1 – signed multiply high word            | MPYS32H   | 16h    |
| 32-bit operand 1 – multiply accumulate low word         | MAC32L    | 18h    |
| 32-bit operand 1 – multiply accumulate high word        | MAC32H    | 1Ah    |
| 32-bit operand 1 – signed multiply accumulate low word  | MACS32L   | 1Ch    |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H   | 1Eh    |
| 32-bit operand 2 – low word                             | OP2L      | 20h    |
| 32-bit operand 2 – high word                            | OP2H      | 22h    |
| 32 × 32 result 0 – least significant word               | RES0      | 24h    |
| 32 × 32 result 1                                        | RES1      | 26h    |
| 32 × 32 result 2                                        | RES2      | 28h    |
| 32 × 32 result 3 – most significant word                | RES3      | 2Ah    |
| MPY32 control 0                                         | MPY32CTL0 | 2Ch    |

**Table 6-35. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

| REGISTER DESCRIPTION                   | REGISTER | OFFSET |
|----------------------------------------|----------|--------|
| DMA channel 0 control                  | DMA0CTL  | 00h    |
| DMA channel 0 source address low       | DMA0SAL  | 02h    |
| DMA channel 0 source address high      | DMA0SAH  | 04h    |
| DMA channel 0 destination address low  | DMA0DAL  | 06h    |
| DMA channel 0 destination address high | DMA0DAH  | 08h    |
| DMA channel 0 transfer size            | DMA0SZ   | 0Ah    |
| DMA channel 1 control                  | DMA1CTL  | 00h    |
| DMA channel 1 source address low       | DMA1SAL  | 02h    |
| DMA channel 1 source address high      | DMA1SAH  | 04h    |
| DMA channel 1 destination address low  | DMA1DAL  | 06h    |
| DMA channel 1 destination address high | DMA1DAH  | 08h    |
| DMA channel 1 transfer size            | DMA1SZ   | 0Ah    |
| DMA channel 2 control                  | DMA2CTL  | 00h    |
| DMA channel 2 source address low       | DMA2SAL  | 02h    |
| DMA channel 2 source address high      | DMA2SAH  | 04h    |
| DMA channel 2 destination address low  | DMA2DAL  | 06h    |
| DMA channel 2 destination address high | DMA2DAH  | 08h    |
| DMA channel 2 transfer size            | DMA2SZ   | 0Ah    |
| DMA module control 0                   | DMACTL0  | 00h    |
| DMA module control 1                   | DMACTL1  | 02h    |
| DMA module control 2                   | DMACTL2  | 04h    |
| DMA module control 3                   | DMACTL3  | 06h    |
| DMA module control 4                   | DMACTL4  | 08h    |
| DMA interrupt vector                   | DMAIV    | 0Eh    |

**Table 6-36. USCI\_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION       | REGISTER   | OFFSET |
|----------------------------|------------|--------|
| USCI control 1             | UCA0CTL1   | 00h    |
| USCI control 0             | UCA0CTL0   | 01h    |
| USCI baud rate 0           | UCA0BR0    | 06h    |
| USCI baud rate 1           | UCA0BR1    | 07h    |
| USCI modulation control    | UCA0MCTL   | 08h    |
| USCI status                | UCA0STAT   | 0Ah    |
| USCI receive buffer        | UCA0RXBUF  | 0Ch    |
| USCI transmit buffer       | UCA0TXBUF  | 0Eh    |
| USCI LIN control           | UCA0ABCTL  | 10h    |
| USCI IrDA transmit control | UCA0IRTCTL | 12h    |
| USCI IrDA receive control  | UCA0IRRCTL | 13h    |
| USCI interrupt enable      | UCA0IE     | 1Ch    |
| USCI interrupt flags       | UCA0IFG    | 1Dh    |
| USCI interrupt vector word | UCA0IV     | 1Eh    |

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[www.ti.com](http://www.ti.com)**Table 6-37. USCI\_B0 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION             | REGISTER  | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1       | UCB0CTL1  | 00h    |
| USCI synchronous control 0       | UCB0CTL0  | 01h    |
| USCI synchronous bit rate 0      | UCB0BR0   | 06h    |
| USCI synchronous bit rate 1      | UCB0BR1   | 07h    |
| USCI synchronous status          | UCB0STAT  | 0Ah    |
| USCI synchronous receive buffer  | UCB0RXBUF | 0Ch    |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh    |
| USCI I2C own address             | UCB0I2COA | 10h    |
| USCI I2C slave address           | UCB0I2CSA | 12h    |
| USCI interrupt enable            | UCB0IE    | 1Ch    |
| USCI interrupt flags             | UCB0IFG   | 1Dh    |
| USCI interrupt vector word       | UCB0IV    | 1Eh    |

**Table 6-38. USCI\_A1 Registers (Base Address: 0600h)**

| REGISTER DESCRIPTION       | REGISTER   | OFFSET |
|----------------------------|------------|--------|
| USCI control 1             | UCA1CTL1   | 00h    |
| USCI control 0             | UCA1CTL0   | 01h    |
| USCI baud rate 0           | UCA1BR0    | 06h    |
| USCI baud rate 1           | UCA1BR1    | 07h    |
| USCI modulation control    | UCA1MCTL   | 08h    |
| USCI status                | UCA1STAT   | 0Ah    |
| USCI receive buffer        | UCA1RXBUF  | 0Ch    |
| USCI transmit buffer       | UCA1TXBUF  | 0Eh    |
| USCI LIN control           | UCA1ABCTL  | 10h    |
| USCI IrDA transmit control | UCA1IRTCTL | 12h    |
| USCI IrDA receive control  | UCA1IRRCTL | 13h    |
| USCI interrupt enable      | UCA1IE     | 1Ch    |
| USCI interrupt flags       | UCA1IFG    | 1Dh    |
| USCI interrupt vector word | UCA1IV     | 1Eh    |

**Table 6-39. USCI\_B1 Registers (Base Address: 0620h)**

| REGISTER DESCRIPTION             | REGISTER  | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1       | UCB1CTL1  | 00h    |
| USCI synchronous control 0       | UCB1CTL0  | 01h    |
| USCI synchronous bit rate 0      | UCB1BR0   | 06h    |
| USCI synchronous bit rate 1      | UCB1BR1   | 07h    |
| USCI synchronous status          | UCB1STAT  | 0Ah    |
| USCI synchronous receive buffer  | UCB1RXBUF | 0Ch    |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh    |
| USCI I2C own address             | UCB1I2COA | 10h    |
| USCI I2C slave address           | UCB1I2CSA | 12h    |
| USCI interrupt enable            | UCB1IE    | 1Ch    |
| USCI interrupt flags             | UCB1IFG   | 1Dh    |
| USCI interrupt vector word       | UCB1IV    | 1Eh    |

**Table 6-40. ADC12\_A Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION      | REGISTER    | OFFSET |
|---------------------------|-------------|--------|
| ADC control 0             | ADC12CTL0   | 00h    |
| ADC control 1             | ADC12CTL1   | 02h    |
| ADC control 2             | ADC12CTL2   | 04h    |
| ADC interrupt flag        | ADC12IFG    | 0Ah    |
| ADC interrupt enable      | ADC12IE     | 0Ch    |
| ADC interrupt vector word | ADC12IV     | 0Eh    |
| ADC memory control 0      | ADC12MCTL0  | 10h    |
| ADC memory control 1      | ADC12MCTL1  | 11h    |
| ADC memory control 2      | ADC12MCTL2  | 12h    |
| ADC memory control 3      | ADC12MCTL3  | 13h    |
| ADC memory control 4      | ADC12MCTL4  | 14h    |
| ADC memory control 5      | ADC12MCTL5  | 15h    |
| ADC memory control 6      | ADC12MCTL6  | 16h    |
| ADC memory control 7      | ADC12MCTL7  | 17h    |
| ADC memory control 8      | ADC12MCTL8  | 18h    |
| ADC memory control 9      | ADC12MCTL9  | 19h    |
| ADC memory control 10     | ADC12MCTL10 | 1Ah    |
| ADC memory control 11     | ADC12MCTL11 | 1Bh    |
| ADC memory control 12     | ADC12MCTL12 | 1Ch    |
| ADC memory control 13     | ADC12MCTL13 | 1Dh    |
| ADC memory control 14     | ADC12MCTL14 | 1Eh    |
| ADC memory control 15     | ADC12MCTL15 | 1Fh    |
| Conversion memory 0       | ADC12MEM0   | 20h    |
| Conversion memory 1       | ADC12MEM1   | 22h    |
| Conversion memory 2       | ADC12MEM2   | 24h    |
| Conversion memory 3       | ADC12MEM3   | 26h    |
| Conversion memory 4       | ADC12MEM4   | 28h    |
| Conversion memory 5       | ADC12MEM5   | 2Ah    |
| Conversion memory 6       | ADC12MEM6   | 2Ch    |
| Conversion memory 7       | ADC12MEM7   | 2Eh    |
| Conversion memory 8       | ADC12MEM8   | 30h    |
| Conversion memory 9       | ADC12MEM9   | 32h    |
| Conversion memory 10      | ADC12MEM10  | 34h    |
| Conversion memory 11      | ADC12MEM11  | 36h    |
| Conversion memory 12      | ADC12MEM12  | 38h    |
| Conversion memory 13      | ADC12MEM13  | 3Ah    |
| Conversion memory 14      | ADC12MEM14  | 3Ch    |
| Conversion memory 15      | ADC12MEM15  | 3Eh    |

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[www.ti.com](http://www.ti.com)**Table 6-41. Comparator\_B Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION         | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Comp_B control 0             | CBCTL0   | 00h    |
| Comp_B control 1             | CBCTL1   | 02h    |
| Comp_B control 2             | CBCTL2   | 04h    |
| Comp_B control 3             | CBCTL3   | 06h    |
| Comp_B interrupt             | CBINT    | 0Ch    |
| Comp_B interrupt vector word | CBIV     | 0Eh    |

## 6.10 Input/Output Diagrams

### 6.10.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-42 summarizes the selection of the pin functions.

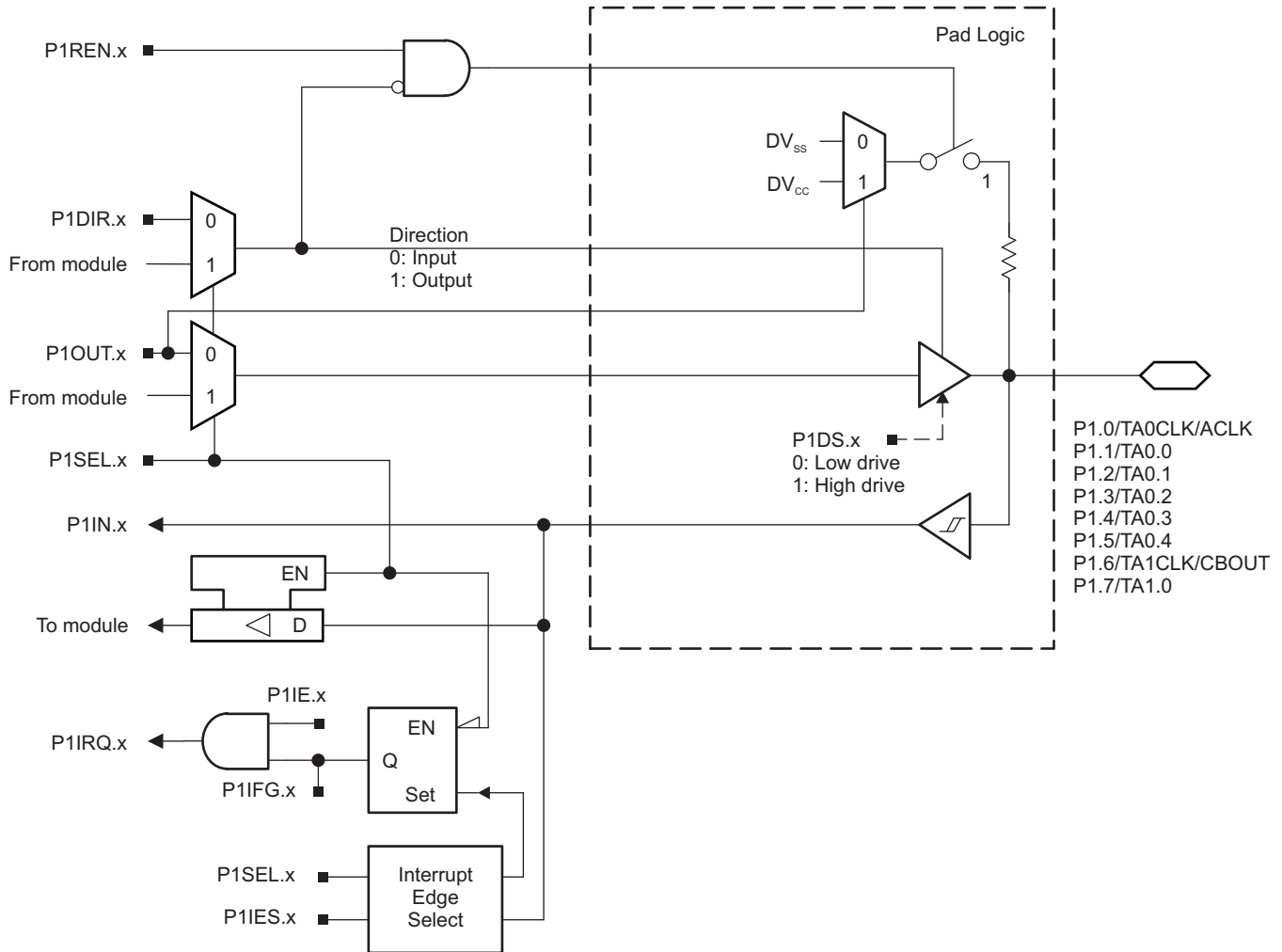


Figure 6-2. Port P1 (P1.0 to P1.7) Diagram

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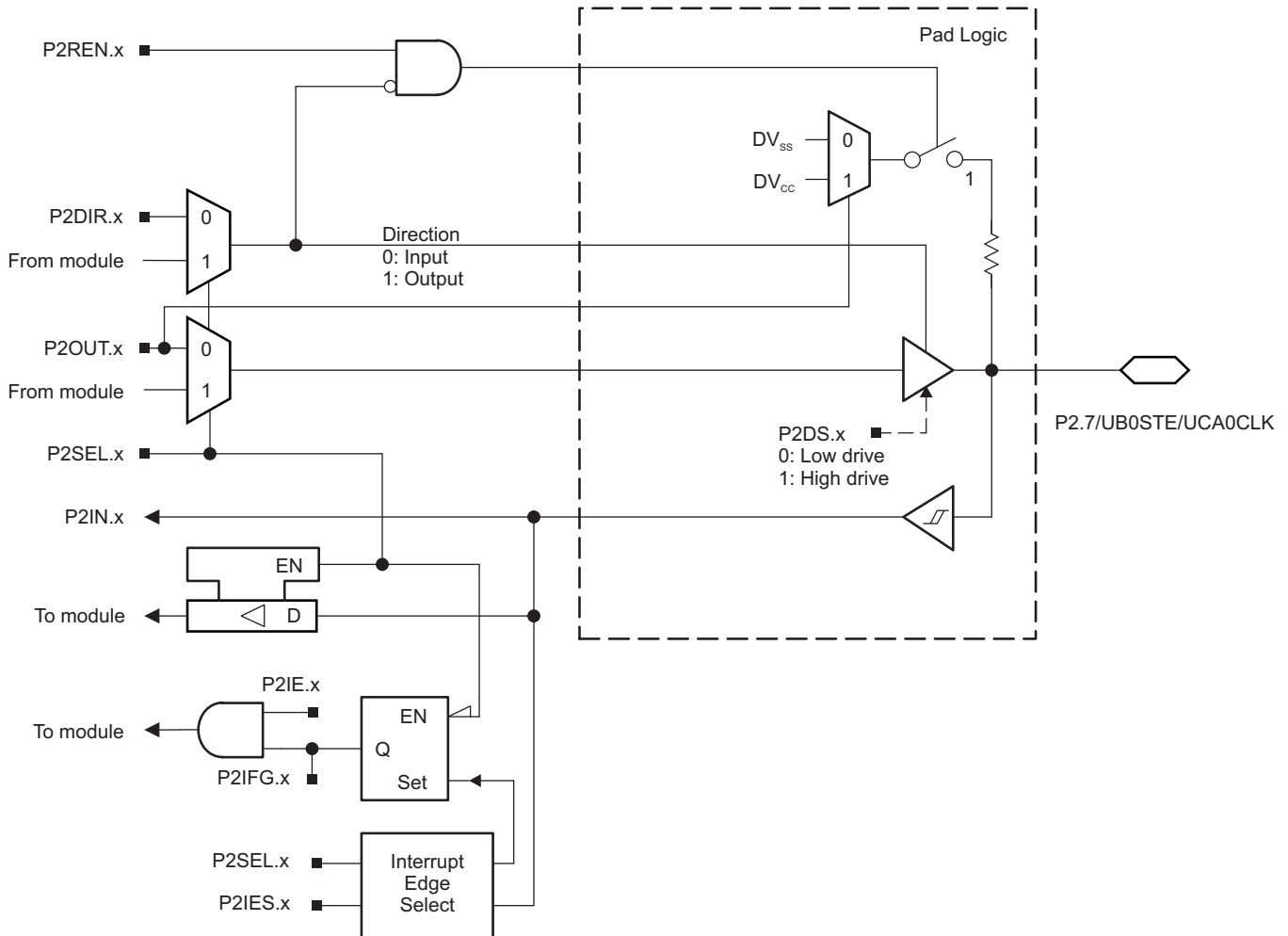
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[www.ti.com](http://www.ti.com)**Table 6-42. Port P1 (P1.0 to P1.7) Pin Functions**

| PIN NAME (P1.x)   | x | FUNCTION           | CONTROL BITS OR SIGNALS |         |
|-------------------|---|--------------------|-------------------------|---------|
|                   |   |                    | P1DIR.x                 | P1SEL.x |
| P1.0/TA0CLK/ACLK  | 0 | P1.0 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA0CLK             | 0                       | 1       |
|                   |   | ACLK               | 1                       | 1       |
| P1.1/TA0.0        | 1 | P1.1 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA0.CCI0A          | 0                       | 1       |
|                   |   | TA0.0              | 1                       | 1       |
| P1.2/TA0.1        | 2 | P1.2 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA0.CCI1A          | 0                       | 1       |
|                   |   | TA0.1              | 1                       | 1       |
| P1.3/TA0.2        | 3 | P1.3 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA0.CCI2A          | 0                       | 1       |
|                   |   | TA0.2              | 1                       | 1       |
| P1.4/TA0.3        | 4 | P1.4 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA0.CCI3A          | 0                       | 1       |
|                   |   | TA0.3              | 1                       | 1       |
| P1.5/TA0.4        | 5 | P1.5 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA0.CCI4A          | 0                       | 1       |
|                   |   | TA0.4              | 1                       | 1       |
| P1.6/TA1CLK/CBOUT | 6 | P1.6 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA1CLK             | 0                       | 1       |
|                   |   | CBOUT comparator B | 1                       | 1       |
| P1.7/TA1.0        | 7 | P1.7 (I/O)         | I: 0; O: 1              | 0       |
|                   |   | TA1.CCI0A          | 0                       | 1       |
|                   |   | TA1.0              | 1                       | 1       |

### 6.10.2 Port P2 (P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-43 summarizes the selection of the pin functions.



### Figure 6-3. Port P2 (P2.7) Diagram

### Table 6-43. Port P2 (P2.7) Pin Functions

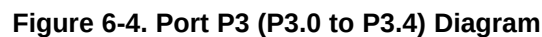
| PIN NAME (P2.x)      | x | FUNCTION                           | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |
|----------------------|---|------------------------------------|----------------------------------------|---------|
|                      |   |                                    | P2DIR.x                                | P2SEL.x |
| P2.7/UCB0STE/UCA0CLK | 7 | P2.7 (I/O)                         | I: 0; O: 1                             | 0       |
|                      |   | UCB0STE/UCA0CLK <sup>(2) (3)</sup> | X                                      | 1       |

(1)  $X = \text{Don't care}$

(2) The pin direction is controlled by the USCI module.

(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USC1\_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Figure 6-4 shows the port diagram. Table 6-44 summarizes the selection of the pin functions.



| PIN NAME (P3.x)       | x | FUNCTION                            | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |
|-----------------------|---|-------------------------------------|----------------------------------------|---------|
|                       |   |                                     | P3DIR.x                                | P3SEL.x |
| P3.0/UCB0SIMO/UCB0SDA | 0 | P3.0 (I/O)                          | I: 0; O: 1                             | 0       |
|                       |   | UCB0SIMO/UCB0SDA <sup>(2) (3)</sup> | X                                      | 1       |
| P3.1/UCB0SOMI/UCB0SCL | 1 | P3.1 (I/O)                          | I: 0; O: 1                             | 0       |
|                       |   | UCB0SOMI/UCB0SCL <sup>(2) (3)</sup> | X                                      | 1       |
| P3.2/UCB0CLK/UCA0STE  | 2 | P3.2 (I/O)                          | I: 0; O: 1                             | 0       |
|                       |   | UCB0CLK/UCA0STE <sup>(2) (4)</sup>  | X                                      | 1       |
| P3.3/UCA0TXD/UCA0SIMO | 3 | P3.3 (I/O)                          | I: 0; O: 1                             | 0       |
|                       |   | UCA0TXD/UCA0SIMO <sup>(2)</sup>     | X                                      | 1       |
| P3.4/UCA0RXD/UCA0SOMI | 4 | P3.4 (I/O)                          | I: 0; O: 1                             | 0       |
|                       |   | UCA0RXD/UCA0SOMI <sup>(2)</sup>     | X                                      | 1       |

- (1) X = Don't care
- (2) The pin direction is controlled by the USCI module.
- (3) If the I<sup>2</sup>C functionality is selected, the output drives only the logical 0 to V<sub>SS</sub> level.
- (4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI\_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

#### 6.10.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-45 summarizes the selection of the pin functions.

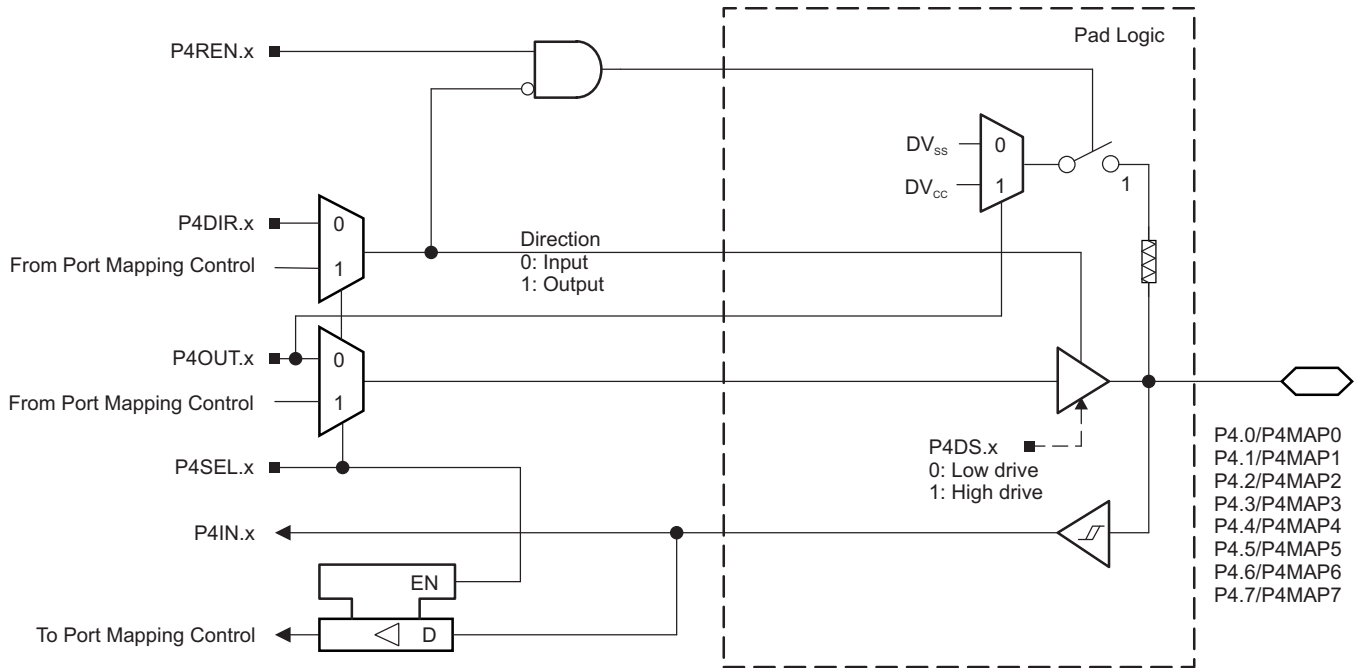


Figure 6-5. Port P4 (P4.0 to P4.7) Diagram

Table 6-45. Port P4 (P4.0 to P4.7) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION                          | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |        |
|-----------------|---|-----------------------------------|----------------------------------------|---------|--------|
|                 |   |                                   | P4DIR.x <sup>(2)</sup>                 | P4SEL.x | P4MAPx |
| P4.0/P4MAP0     | 0 | P4.0 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |
| P4.1/P4MAP1     | 1 | P4.1 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |
| P4.2/P4MAP2     | 2 | P4.2 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |
| P4.3/P4MAP3     | 3 | P4.3 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |
| P4.4/P4MAP4     | 4 | P4.4 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |
| P4.5/P4MAP5     | 5 | P4.5 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |
| P4.6/P4MAP6     | 6 | P4.6 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |
| P4.7/P4MAP7     | 7 | P4.7 (I/O)                        | I: 0; O: 1                             | 0       | X      |
|                 |   | Mapped secondary digital function | X                                      | 1       | ≤ 30   |

(1) X = Don't care

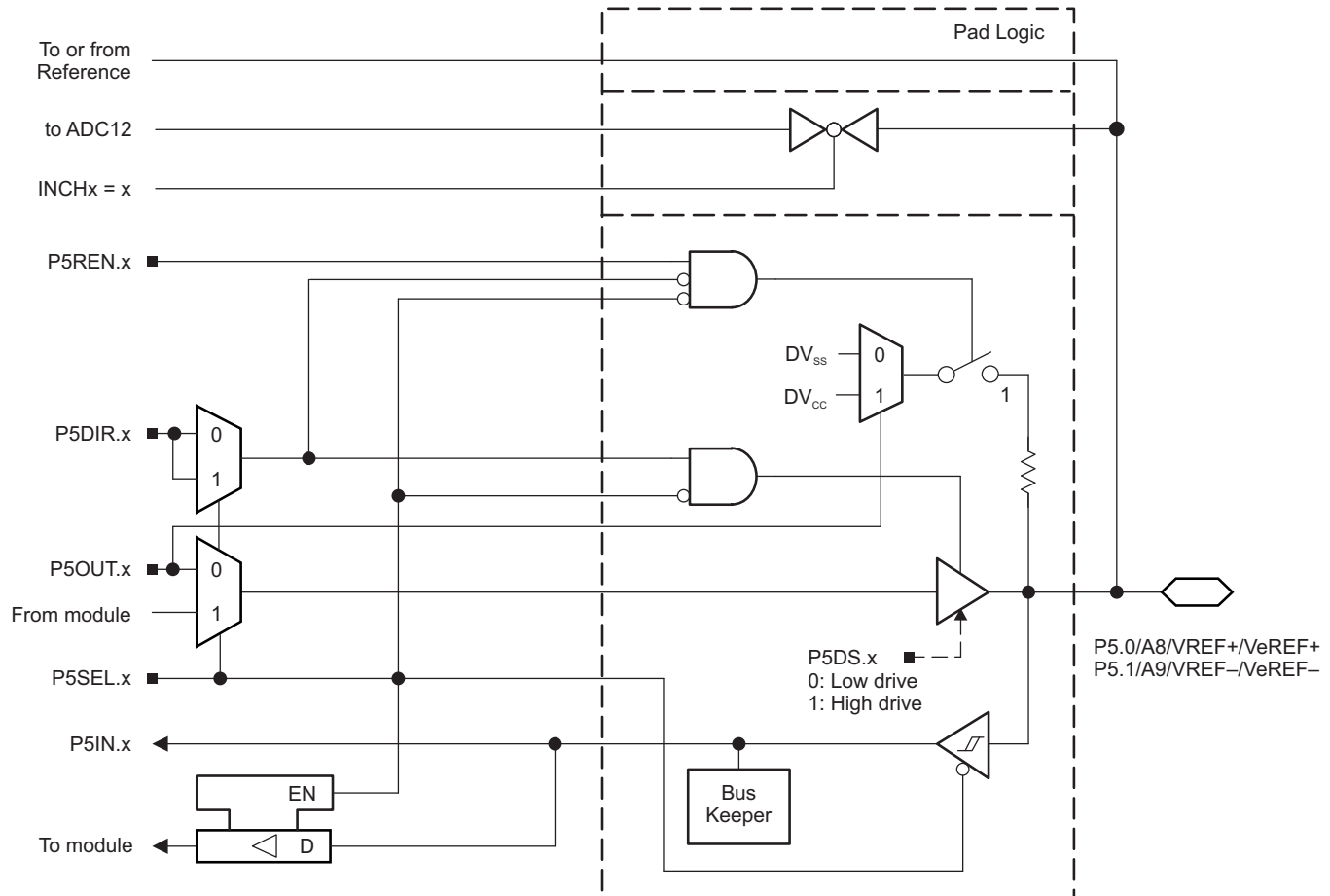
(2) The direction of some mapped secondary functions are controlled directly by the module. See Table 6-6 for specific direction control information of mapped secondary functions.

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[www.ti.com](http://www.ti.com)**6.10.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger**

Figure 6-6 shows the port diagram. Table 6-46 summarizes the selection of the pin functions.

**Figure 6-6. Port P5 (P5.0 and P5.1) Diagram****Table 6-46. Port P5 (P5.0 and P5.1) Pin Functions**

| PIN NAME (P5.x)      | x | FUNCTION                  | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |        |
|----------------------|---|---------------------------|----------------------------------------|---------|--------|
|                      |   |                           | P5DIR.x                                | P5SEL.x | REFOUT |
| P5.0/A8/VREF+/VeREF+ | 0 | P5.0 (I/O) <sup>(2)</sup> | I: 0; O: 1                             | 0       | X      |
|                      |   | A8/VeREF+ <sup>(3)</sup>  | X                                      | 1       | 0      |
|                      |   | A8/VREF+ <sup>(4)</sup>   | X                                      | 1       | 1      |

(1) X = Don't care

(2) Default condition

(3) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12\_A. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.

(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF+ reference is available at the pin. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.

**Table 6-46. Port P5 (P5.0 and P5.1) Pin Functions (continued)**

| PIN NAME (P5.x)      | x | FUNCTION                  | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |        |
|----------------------|---|---------------------------|----------------------------------------|---------|--------|
|                      |   |                           | P5DIR.x                                | P5SEL.x | REFOUT |
| P5.1/A9/VREF-/VeREF- | 1 | P5.1 (I/O) <sup>(2)</sup> | I: 0; O: 1                             | 0       | X      |
|                      |   | A9/VeREF- <sup>(5)</sup>  | X                                      | 1       | 0      |
|                      |   | A9/VREF- <sup>(6)</sup>   | X                                      | 1       | 1      |

(5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12\_A. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

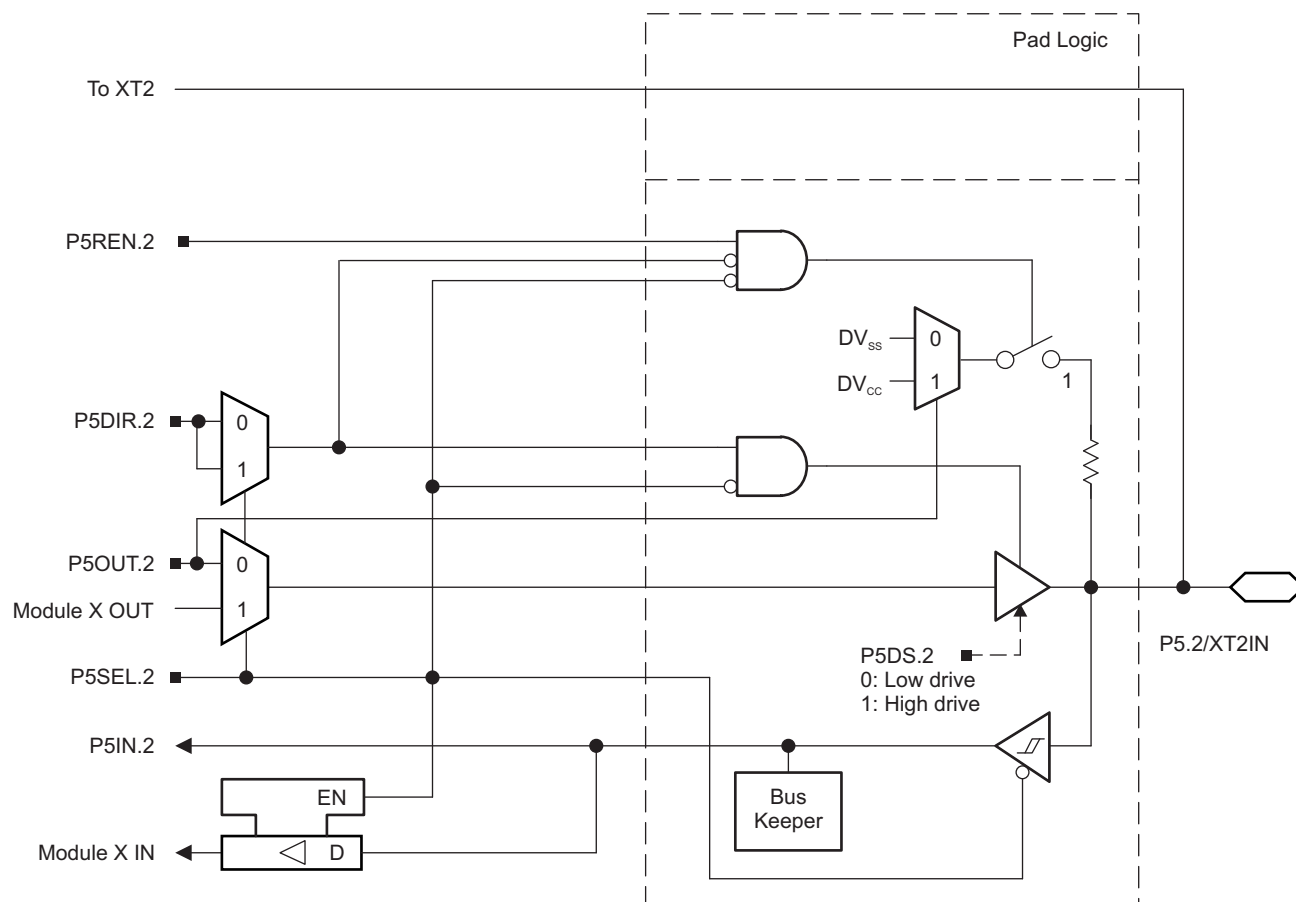
(6) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF- reference is available at the pin. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

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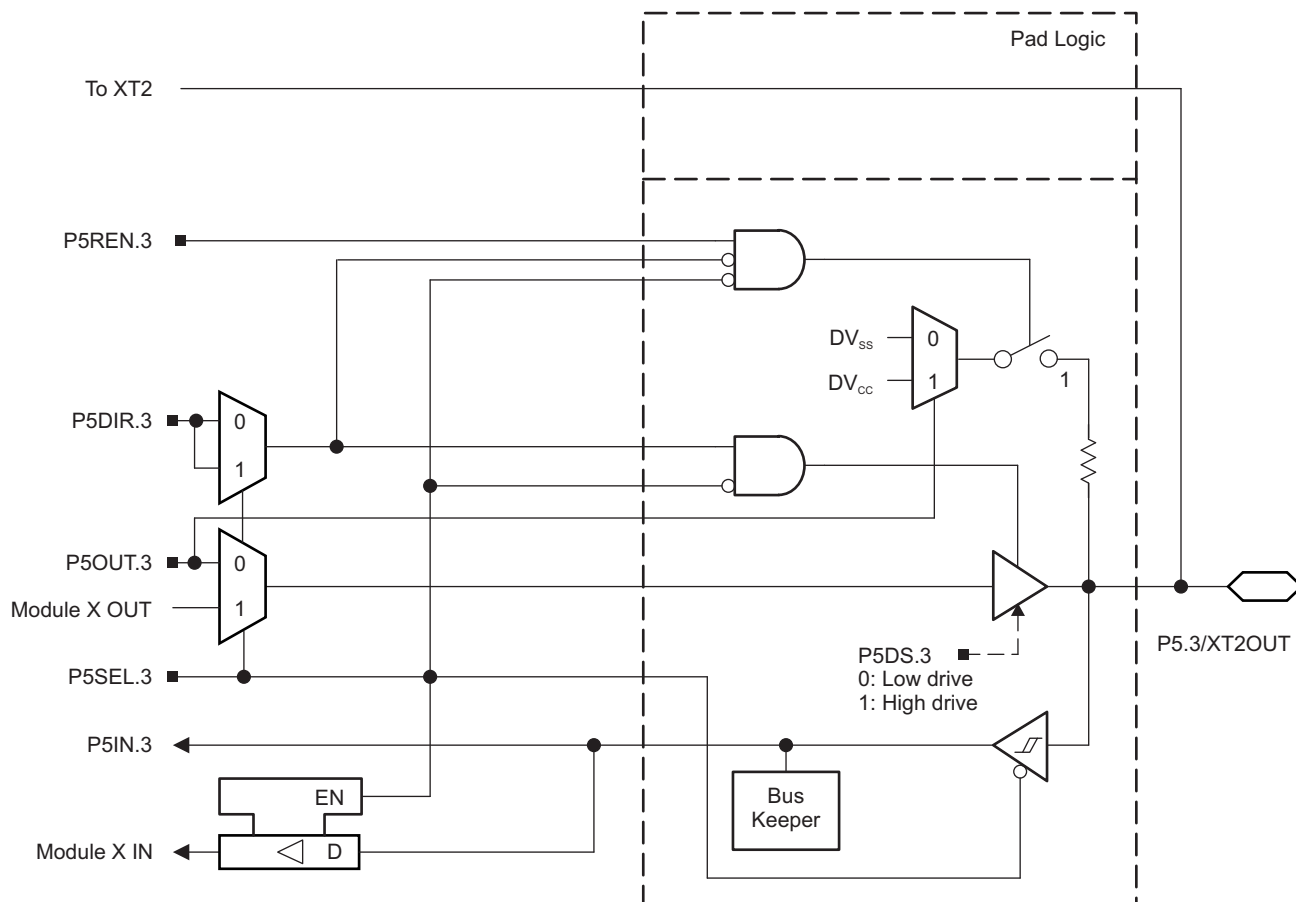
[www.ti.com](http://www.ti.com)**6.10.6 Port P5 (P5.2) Input/Output With Schmitt Trigger**

Figure 6-7 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.

**Figure 6-7. Port P5 (P5.2) Diagram**

### 6.10.7 Port P5 (P5.3) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.



### Figure 6-8. Port P5 (P5.3) Diagram

### Table 6-47. Port P5 (P5.2 and 5.3) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION                           | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |         |           |
|-----------------|---|------------------------------------|----------------------------------------|---------|---------|-----------|
|                 |   |                                    | P5DIR.x                                | P5SEL.2 | P5SEL.3 | XT2BYPASS |
| P5.2/XT2IN      | 2 | P5.2 (I/O)                         | I: 0; O: 1                             | 0       | X       | X         |
|                 |   | XT2IN crystal mode <sup>(2)</sup>  | X                                      | 1       | X       | 0         |
|                 |   | XT2IN bypass mode <sup>(2)</sup>   | X                                      | 1       | X       | 1         |
| P5.3/XT2OUT     | 3 | P5.3 (I/O)                         | I: 0; O: 1                             | 0       | X       | X         |
|                 |   | XT2OUT crystal mode <sup>(3)</sup> | X                                      | 1       | X       | 0         |
|                 |   | P5.3 (I/O) <sup>(3)</sup>          | X                                      | 1       | X       | 1         |

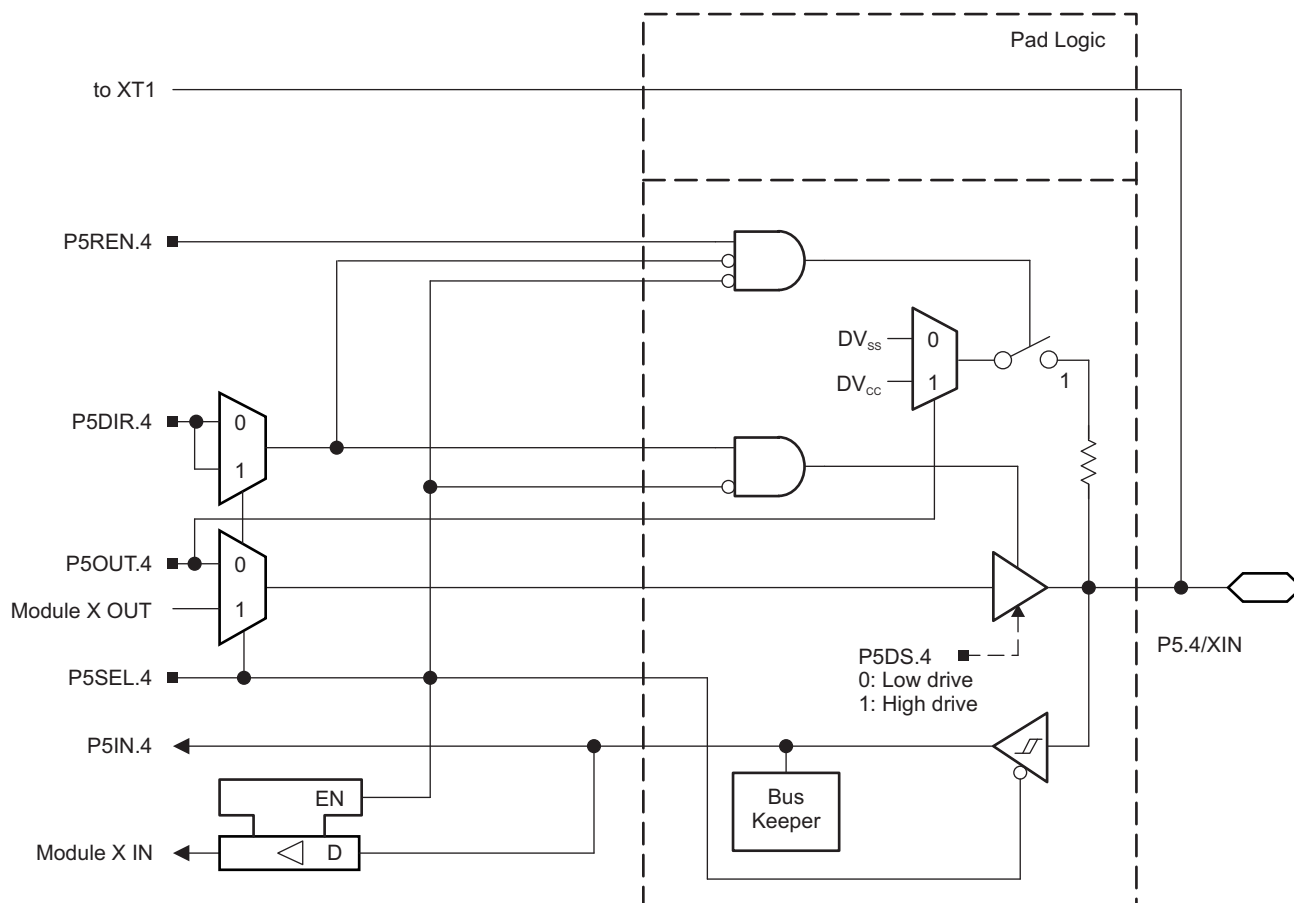
(1) X = Don't care

(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

**6.10.8 Port P5 (P5.4 and P5.5) Input/Output With Schmitt Trigger**

Figure 6-9 and Figure 6-10 show the port diagrams. Table 6-48 summarizes the selection of the pin functions.

**Figure 6-9. Port P5 (P5.4) Diagram**



### Table 6-48. Port P5 (P5.4 and P5.5) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION                         | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |         |           |
|-----------------|---|----------------------------------|----------------------------------------|---------|---------|-----------|
|                 |   |                                  | P5DIR.x                                | P5SEL.4 | P5SEL.5 | XT1BYPASS |
| P5.4/XIN        | 4 | P5.4 (I/O)                       | I: 0; O: 1                             | 0       | X       | X         |
|                 |   | XIN crystal mode <sup>(2)</sup>  | X                                      | 1       | X       | 0         |
|                 |   | XIN bypass mode <sup>(2)</sup>   | X                                      | 1       | X       | 1         |
| P5.5/XOUT       | 5 | P5.5 (I/O)                       | I: 0; O: 1                             | 0       | X       | X         |
|                 |   | XOUT crystal mode <sup>(3)</sup> | X                                      | 1       | X       | 0         |
|                 |   | P5.5 (I/O) <sup>(3)</sup>        | X                                      | 1       | X       | 1         |

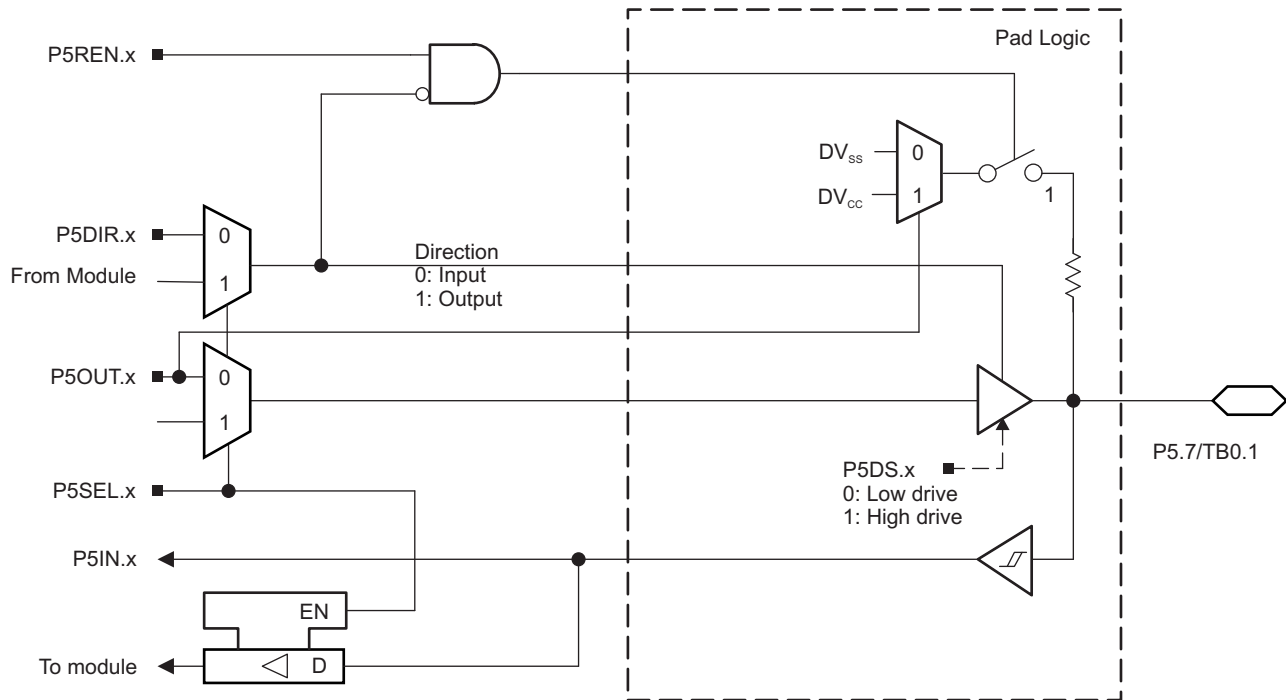
(3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

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[www.ti.com](http://www.ti.com)**6.10.9 Port P5 (P5.7) Input/Output With Schmitt Trigger**

Figure 6-11 shows the port diagram. Table 6-49 summarizes the selection of the pin functions.

**Figure 6-11. Port P5 (P5.7) Diagram****Table 6-49. Port P5 (P5.7) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION  | CONTROL BITS OR SIGNALS |         |
|-----------------|---|-----------|-------------------------|---------|
|                 |   |           | P5DIR.x                 | P5SEL.x |
| P5.7/TB0.1      | 7 | TB0.CCI1A | 0                       | 1       |
|                 |   | TB0.1     | 1                       | 1       |

### 6.10.10 Port P6 (P6.1 to P6.5) Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 6-50 summarizes the selection of the pin functions.

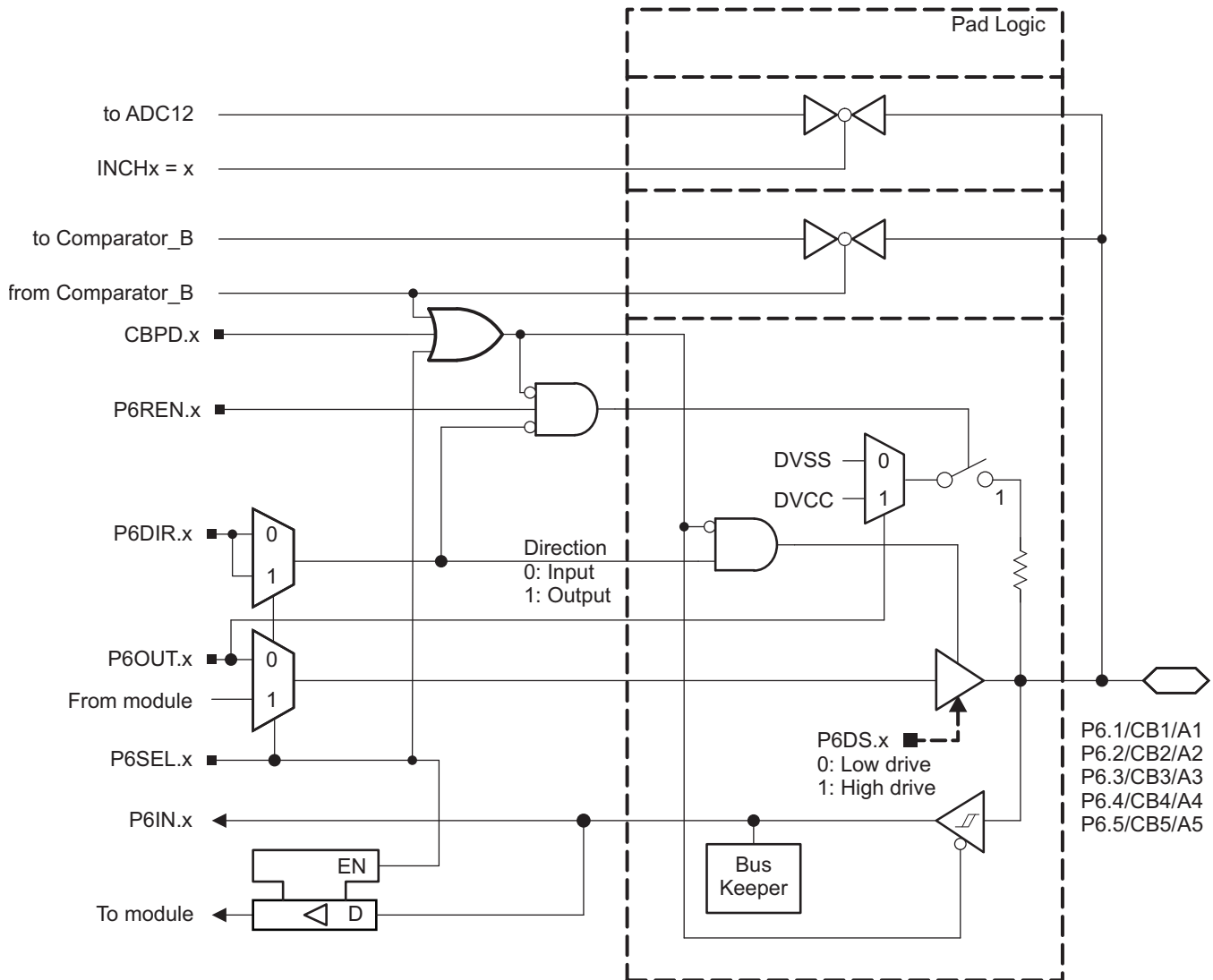


Figure 6-12. Port P6 (P6.1 to P6.5) Diagram

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[www.ti.com](http://www.ti.com)**Table 6-50. Port P6 (P6.1 to P6.5) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION           | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |       |
|-----------------|---|--------------------|----------------------------------------|---------|-------|
|                 |   |                    | P6DIR.x                                | P6SEL.x | CBPDx |
| P6.1/CB1/A1     | 1 | P6.1 (I/O)         | I: 0; O: 1                             | 0       | 0     |
|                 |   | A1                 | X                                      | 1       | X     |
|                 |   | CB1 <sup>(2)</sup> | X                                      | X       | 1     |
| P6.2/CB2/A2     | 2 | P6.2 (I/O)         | I: 0; O: 1                             | 0       | 0     |
|                 |   | A2                 | X                                      | 1       | X     |
|                 |   | CB2 <sup>(2)</sup> | X                                      | X       | 1     |
| P6.3/CB3/A3     | 3 | P6.3 (I/O)         | I: 0; O: 1                             | 0       | 0     |
|                 |   | A3                 | X                                      | 1       | X     |
|                 |   | CB3 <sup>(2)</sup> | X                                      | X       | 1     |
| P6.4/CB4/A4     | 4 | P6.4 (I/O)         | I: 0; O: 1                             | 0       | 0     |
|                 |   | A4                 | X                                      | 1       | X     |
|                 |   | CB4 <sup>(2)</sup> | X                                      | X       | 1     |
| P6.5/CB5/A5     | 5 | P6.5 (I/O)         | I: 0; O: 1                             | 0       | 0     |
|                 |   | A5                 | X                                      | 1       | X     |
|                 |   | CB5 <sup>(2)</sup> | X                                      | X       | 1     |

(1) X = Don't care

(2) Setting the CBPDx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPDx bit.

### 6.10.11 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-13 shows the port diagram. Table 6-51 summarizes the selection of the pin functions.

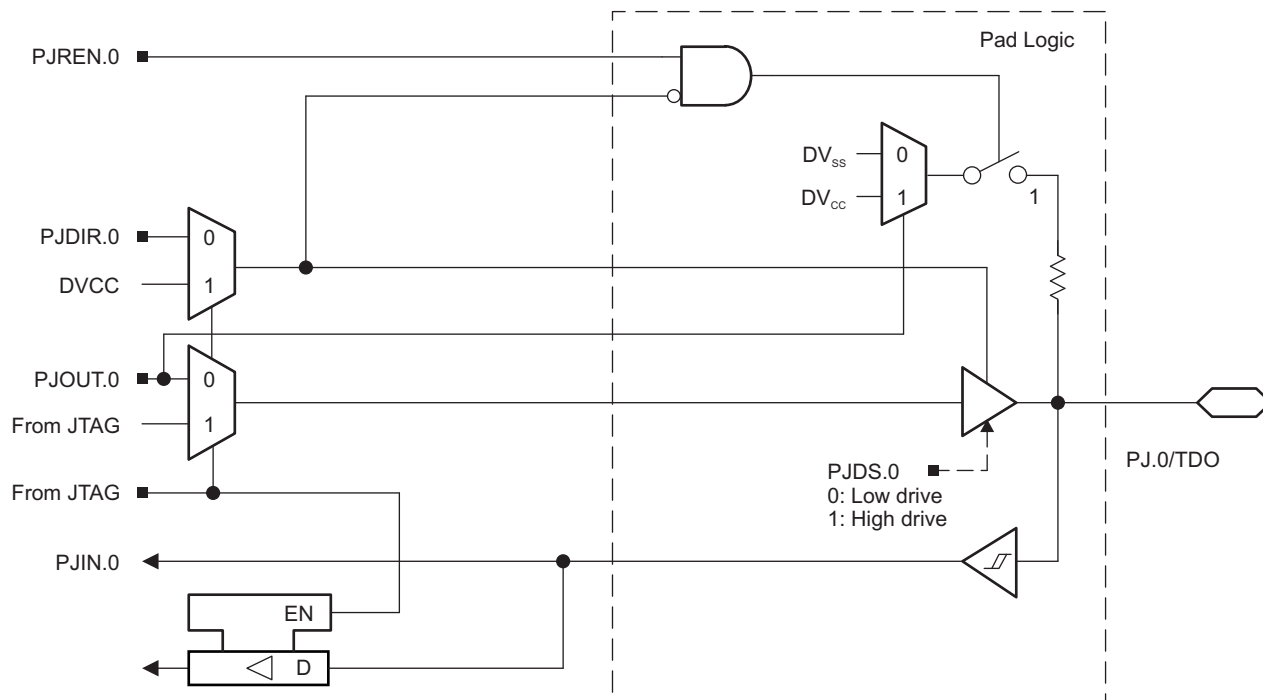


**Figure 6-13. Port PJ (PJ.0) Diagram**



## 6.11 Device Descriptors

Table 6-52 lists the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

**Table 6-52. Device Descriptor Table<sup>(1)</sup>**

| DESCRIPTION       |                                             | ADDRESS | SIZE<br>(bytes) | VALUE    |          |          |
|-------------------|---------------------------------------------|---------|-----------------|----------|----------|----------|
|                   |                                             |         |                 | F5342    | F5341    | F5340    |
| Info Block        | Info length                                 | 01A00h  | 1               | 06h      | 06h      | 06h      |
|                   | CRC length                                  | 01A01h  | 1               | 06h      | 06h      | 06h      |
|                   | CRC value                                   | 01A02h  | 2               | Per unit | Per unit | Per unit |
|                   | Device ID                                   | 01A04h  | 1               | 1Eh      | 1Dh      | 1Ch      |
|                   | Device ID                                   | 01A05h  | 1               | 81h      | 81h      | 81h      |
|                   | Hardware revision                           | 01A06h  | 1               | Per unit | Per unit | Per unit |
|                   | Firmware revision                           | 01A07h  | 1               | Per unit | Per unit | Per unit |
| Die Record        | Die record tag                              | 01A08h  | 1               | 08h      | 08h      | 08h      |
|                   | Die record length                           | 01A09h  | 1               | 0Ah      | 0Ah      | 0Ah      |
|                   | Lot/wafer ID                                | 01A0Ah  | 4               | Per unit | Per unit | Per unit |
|                   | Die X position                              | 01A0Eh  | 2               | Per unit | Per unit | Per unit |
|                   | Die Y position                              | 01A10h  | 2               | Per unit | Per unit | Per unit |
|                   | Test results                                | 01A12h  | 2               | Per unit | Per unit | Per unit |
| ADC12 Calibration | ADC12 calibration tag                       | 01A14h  | 1               | 11h      | 11h      | 11h      |
|                   | ADC12 calibration length                    | 01A15h  | 1               | 10h      | 10h      | 10h      |
|                   | ADC gain factor                             | 01A16h  | 2               | Per unit | Per unit | Per unit |
|                   | ADC offset                                  | 01A18h  | 2               | Per unit | Per unit | Per unit |
|                   | ADC 1.5-V reference temperature sensor 30°C | 01A1Ah  | 2               | Per unit | Per unit | Per unit |
|                   | ADC 1.5-V reference temperature sensor 85°C | 01A1Ch  | 2               | Per unit | Per unit | Per unit |
|                   | ADC 2.0-V reference temperature sensor 30°C | 01A1Eh  | 2               | Per unit | Per unit | Per unit |
|                   | ADC 2.0-V reference temperature sensor 85°C | 01A20h  | 2               | Per unit | Per unit | Per unit |
|                   | ADC 2.5-V reference temperature sensor 30°C | 01A22h  | 2               | Per unit | Per unit | Per unit |
|                   | ADC 2.5-V reference temperature sensor 85°C | 01A24h  | 2               | Per unit | Per unit | Per unit |
| REF Calibration   | REF calibration tag                         | 01A26h  | 1               | 12h      | 12h      | 12h      |
|                   | REF calibration length                      | 01A27h  | 1               | 06h      | 06h      | 06h      |
|                   | REF 1.5-V reference factor                  | 01A28h  | 2               | Per unit | Per unit | Per unit |
|                   | REF 2.0-V reference factor                  | 01A2Ah  | 2               | Per unit | Per unit | Per unit |
|                   | REF 2.5-V reference factor                  | 01A2Ch  | 2               | Per unit | Per unit | Per unit |

(1) N/A = Not applicable, blank = unused and reads FFh

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[www.ti.com](http://www.ti.com)**Table 6-52. Device Descriptor Table<sup>(1)</sup> (continued)**

| DESCRIPTION           |                              | ADDRESS | SIZE<br>(bytes) | VALUE      |            |            |
|-----------------------|------------------------------|---------|-----------------|------------|------------|------------|
|                       |                              |         |                 | F5342      | F5341      | F5340      |
| Peripheral Descriptor | Peripheral descriptor tag    | 01A2Eh  | 1               | 02h        | 02h        | 02h        |
|                       | Peripheral descriptor length | 01A2Fh  | 1               | 5Eh        | 5Eh        | 5Eh        |
|                       | Memory 1                     |         | 2               | 08h<br>8Ah | 08h<br>8Ah | 08h<br>8Ah |
|                       | Memory 2                     |         | 2               | 0Ch<br>86h | 0Ch<br>86h | 0Ch<br>86h |
|                       | Memory 3                     |         | 2               | 0Eh<br>2Fh | 0Eh<br>2Eh | 0Eh<br>2Dh |
|                       | Memory 4                     |         | 2               | 2Ah<br>22h | 22h<br>95h | 2Ah<br>22h |
|                       | Memory 5                     |         | 1               | 96h        | 92h        | 94h        |
|                       | Delimiter                    |         | 1               | 00h        | 00h        | 00h        |
|                       | Peripheral count             |         | 1               | 1Fh        | 1Fh        | 1Fh        |
|                       | MSP430CPUXV2                 |         | 2               | 00h<br>23h | 00h<br>23h | 00h<br>23h |
|                       | JTAG                         |         | 2               | 00h<br>09h | 00h<br>09h | 00h<br>09h |
|                       | SBW                          |         | 2               | 00h<br>0Fh | 00h<br>0Fh | 00h<br>0Fh |
|                       | EEM-L                        |         | 2               | 00h<br>05h | 00h<br>05h | 00h<br>05h |
|                       | TI BSL                       |         | 2               | 00h<br>FCh | 00h<br>FCh | 00h<br>FCh |
|                       | SFR                          |         | 2               | 10h<br>41h | 10h<br>41h | 10h<br>41h |
|                       | PMM                          |         | 2               | 02h<br>30h | 02h<br>30h | 02h<br>30h |
|                       | FCTL                         |         | 2               | 02h<br>38h | 02h<br>38h | 02h<br>38h |
|                       | CRC16                        |         | 2               | 01h<br>3Ch | 01h<br>3Ch | 01h<br>3Ch |
|                       | CRC16_RB                     |         | 2               | 00h<br>3Dh | 00h<br>3Dh | 00h<br>3Dh |
|                       | RAMCTL                       |         | 2               | 00h<br>44h | 00h<br>44h | 00h<br>44h |
|                       | WDT_A                        |         | 2               | 00h<br>40h | 00h<br>40h | 00h<br>40h |
|                       | UCS                          |         | 2               | 01h<br>48h | 01h<br>48h | 01h<br>48h |
|                       | SYS                          |         | 2               | 02h<br>42h | 02h<br>42h | 02h<br>42h |
|                       | REF                          |         | 2               | 03h<br>A0h | 03h<br>A0h | 03h<br>A0h |
|                       | Port Mapping                 |         | 2               | 01h<br>10h | 01h<br>10h | 01h<br>10h |
|                       | Port 1 and 2                 |         | 2               | 04h<br>51h | 04h<br>51h | 04h<br>51h |
|                       | Port 3 and 4                 |         | 2               | 02h<br>52h | 02h<br>52h | 02h<br>52h |
|                       | Port 5 and 6                 |         | 2               | 02h<br>53h | 02h<br>53h | 02h<br>53h |

**Table 6-52. Device Descriptor Table<sup>(1)</sup> (continued)**

| DESCRIPTION                          | ADDRESS        | SIZE<br>(bytes) | VALUE      |            |            |
|--------------------------------------|----------------|-----------------|------------|------------|------------|
|                                      |                |                 | F5342      | F5341      | F5340      |
| Peripheral Descriptor<br>(continued) | JTAG           | 2               | 0Eh<br>5Fh | 0Eh<br>5Fh | 0Eh<br>5Fh |
|                                      | TA0            | 2               | 02h<br>62h | 02h<br>62h | 02h<br>62h |
|                                      | TA1            | 2               | 04h<br>61h | 04h<br>61h | 04h<br>61h |
|                                      | TB0            | 2               | 04h<br>67h | 04h<br>67h | 04h<br>67h |
|                                      | TA2            | 2               | 04h<br>61h | 04h<br>61h | 04h<br>61h |
|                                      | RTC            | 2               | 0Ah<br>68h | 0Ah<br>68h | 0Ah<br>68h |
|                                      | MPY32          | 2               | 02h<br>85h | 02h<br>85h | 02h<br>85h |
|                                      | DMA-3          | 2               | 04h<br>47h | 04h<br>47h | 04h<br>47h |
|                                      | USCI_A, USCI_B | 2               | 0Ch<br>90h | 0Ch<br>90h | 0Ch<br>90h |
|                                      | USCI_A, USCI_B | 2               | 04h<br>90h | 04h<br>90h | 04h<br>90h |
|                                      | ADC12_A        | 2               | 10h<br>D1h | 10h<br>D1h | 10h<br>D1h |
|                                      | COMP_B         | 2               | 1Ch<br>A8h | 1Ch<br>A8h | 1Ch<br>A8h |
| Interrupts                           | COMP_B         | 1               | A8h        | A8h        | A8h        |
|                                      | TB0.CCIFG0     | 1               | 64h        | 64h        | 64h        |
|                                      | TB0.CCIFG1..6  | 1               | 65h        | 65h        | 65h        |
|                                      | WDTIFG         | 1               | 40h        | 40h        | 40h        |
|                                      | USCI_A0        | 1               | 90h        | 90h        | 90h        |
|                                      | USCI_B0        | 1               | 91h        | 91h        | 91h        |
|                                      | ADC12_A        | 1               | D0h        | D0h        | D0h        |
|                                      | TA0.CCIFG0     | 1               | 60h        | 60h        | 60h        |
|                                      | TA0.CCIFG1..4  | 1               | 61h        | 61h        | 61h        |
|                                      | Reserved       | 1               | 01h        | 01h        | 01h        |
|                                      | DMA            | 1               | 46h        | 46h        | 46h        |
|                                      | TA1.CCIFG0     | 1               | 62h        | 62h        | 62h        |
|                                      | TA1.CCIFG1..2  | 1               | 63h        | 63h        | 63h        |
|                                      | P1             | 1               | 50h        | 50h        | 50h        |
|                                      | USCI_A1        | 1               | 92h        | 92h        | 92h        |
|                                      | USCI_B1        | 1               | 93h        | 93h        | 93h        |
|                                      | TA1.CCIFG0     | 1               | 66h        | 66h        | 66h        |
|                                      | TA1.CCIFG1..2  | 1               | 67h        | 67h        | 67h        |
|                                      | P2             | 1               | 51h        | 51h        | 51h        |
|                                      | RTC_A          | 1               | 68h        | 68h        | 68h        |
|                                      | Delimiter      | 1               | 00h        | 00h        | 00h        |

## 7 Device and Documentation Support

### 7.1 Getting Started

For an introduction to the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the [MSP430 ultra-low-power sensing and measurement MCUs overview](#).

### 7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

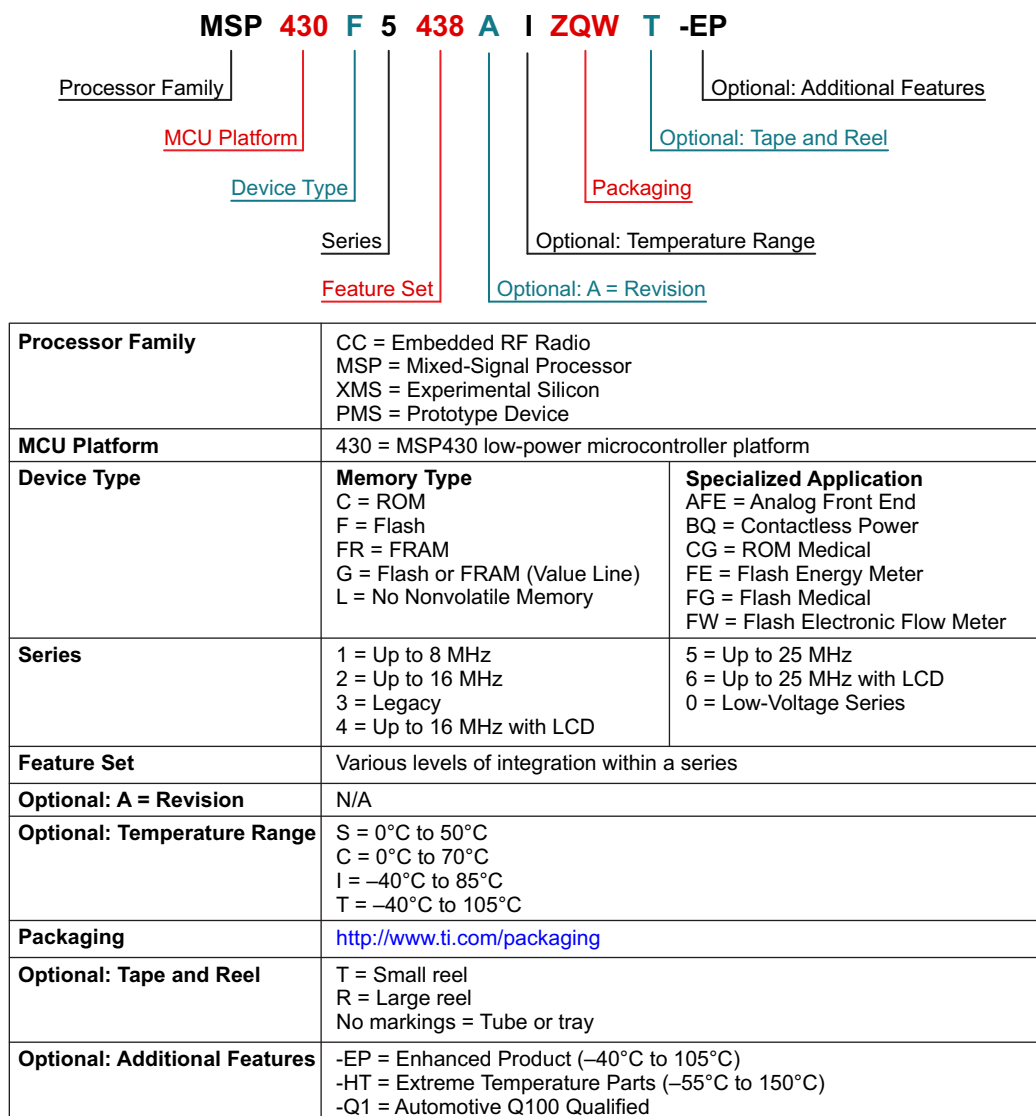
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 7-1](#) provides a legend for reading the complete device name.


**Figure 7-1. Device Nomenclature**

## 7.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at [MSP430 Ultra-Low-Power MCUs – Tools & software](#).

Table 7-1 lists the debug features of the MSP430F532x MCUs. See the [Code Composer Studio for MSP430 User's Guide](#) for details on the available features.

**Table 7-1. Hardware Debug Features**

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|
| MSP430Xv2           | Yes         | Yes         | 8                | Yes                | Yes           | Yes             | Yes          | No                       |

### Design Kits and Evaluation Modules

**MSP430F534x 48-Pin Target board only** The MSP-TS430RGZ48B is a standalone 48-pin ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

**48-pin Target Development Board and MSP-FET Programmer Bundle for MSP430F5x MCUs** The MSP-FET430U48B is a powerful flash emulation tool to quickly begin application development on the MSP430 MCU. It includes USB debugging interface used to program and debug the MSP430 in-system through the JTAG interface or the pin saving Spy Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and since the MSP430 flash is ultra-low power, no external power supply is required.

### Software

**MSP430Ware™ Software** MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 MCU design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

**MSP430F534x Code Examples** C code examples that configure each of the integrated peripherals for various application needs.

**MSP Driver Library** Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

**MSP EnergyTrace™ Technology** EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

**ULP (Ultra-Low Power) Advisor** ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

**IEC60730 Software Package** The IEC60730 MSP430 software package was developed to be useful in assisting customers in complying with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

**Fixed Point Math Library for MSP** The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

**Floating Point Math Library for MSP430** Continuing to innovate in the low power and low cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs. Read the user's guide for an in depth look at the math library and relevant benchmarks.

## Development Tools

**Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers** Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar utilities and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. When using Code Composer Studio IDE with an MSP MCU, a unique and powerful set of plugins and embedded software utilities are made available to fully leverage the MSP microcontroller.

**Command-Line Programmer** MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) files directly to the MSP microcontroller without an IDE.

**MSP MCU Programmer and Debugger** The MSP-FET is a powerful emulation development tool – often called a debug probe – which allows users to quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a Backchannel UART connection between the computer's USB interface and the MSP UART. This affords the MSP programmer a convenient method for communicating serially between the MSP and a terminal running on the computer. It also supports loading programs (often called firmware) to the MSP target using the BSL (bootloader) through the UART and I<sup>2</sup>C communication protocols.

**MSP-GANG Production Programmer** The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 Flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices. Eight cables are provided that connect the expansion board to eight target devices (through JTAG or Spy-Bi-Wire connectors). The programming can be done with a PC or as a stand-alone device. A PC-side graphical user interface is also available and is DLL-based.

## 7.4 Documentation Support

The following documents describe the MSP430F532x MCUs. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com).

### Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://ti.com) (for links to the product folders, see [Section 7.5](#)). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### Errata

**MSP430F5342 Device Erratasheet** Describes the known exceptions to the functional specifications for all silicon revisions of this device.

**MSP430F5341 Device Erratasheet** Describes the known exceptions to the functional specifications for all silicon revisions of this device.

**MSP430F5340 Device Erratasheet** Describes the known exceptions to the functional specifications for all silicon revisions of this device.

### User's Guides

**MSP430F5xx and MSP430F6xx Family User's Guide** Detailed information on the modules and peripherals available in this device family.

**MSP430 Flash Device Bootloader (BSL) User's Guide** The MSP430 bootloader (BSL) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

**MSP430 Programming With the JTAG Interface** This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

**MSP430 Hardware Tools User's Guide** This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

### Application Reports

**MSP430 32-kHz Crystal Oscillators** Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

**MSP430 System-Level ESD Considerations** System-Level ESD has become increasingly demanding as silicon technology scales to lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three ESD topics to help board designers and OEMs understand and design robust system-level designs: (1) Component-level ESD testing and system-level ESD testing; (2) General design guidelines for system-level ESD protection; (3) Introduction to System Efficient ESD Design (SEED), a co-design methodology of on-board and on-chip ESD protection. A few real-world system-level ESD protection design examples and their results are discussed.

## 7.5 Related Links

[Table 7-2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 7-2. Related Links**

| PARTS       | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430F5342 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430F5341 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430F5340 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

## 7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### [TI E2E™ Community](#)

*TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

### [TI Embedded Processors Wiki](#)

*Texas Instruments Embedded Processors Wiki.* Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 7.7 Trademarks

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## 7.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.9 Export Control Notice

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## 7.10 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430F5340IRGZR</a> | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| MSP430F5340IRGZR.A               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| MSP430F5340IRGZR.B               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| MSP430F5340IRGZRG4               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| MSP430F5340IRGZRG4.A             | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| MSP430F5340IRGZRG4.B             | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| <a href="#">MSP430F5340IRGZT</a> | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| MSP430F5340IRGZT.A               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| MSP430F5340IRGZT.B               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5340       |
| <a href="#">MSP430F5341IRGZR</a> | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5341       |
| MSP430F5341IRGZR.A               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5341       |
| MSP430F5341IRGZR.B               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5341       |
| <a href="#">MSP430F5341IRGZT</a> | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5341       |
| MSP430F5341IRGZT.A               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5341       |
| MSP430F5341IRGZT.B               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5341       |
| <a href="#">MSP430F5342IRGZR</a> | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| MSP430F5342IRGZR.A               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |
| MSP430F5342IRGZR.B               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |
| MSP430F5342IRGZRG4               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |
| MSP430F5342IRGZRG4.A             | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |
| MSP430F5342IRGZRG4.B             | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |
| <a href="#">MSP430F5342IRGZT</a> | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |
| MSP430F5342IRGZT.A               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |
| MSP430F5342IRGZT.B               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | M430<br>F5342       |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

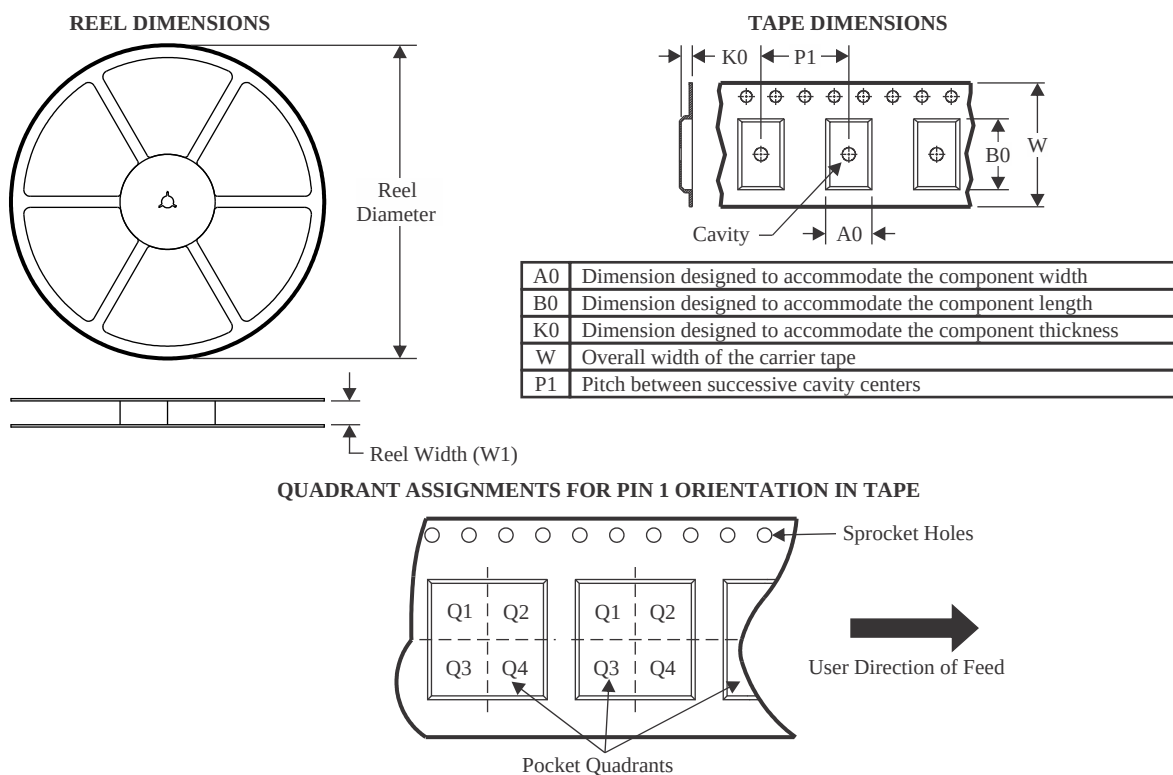
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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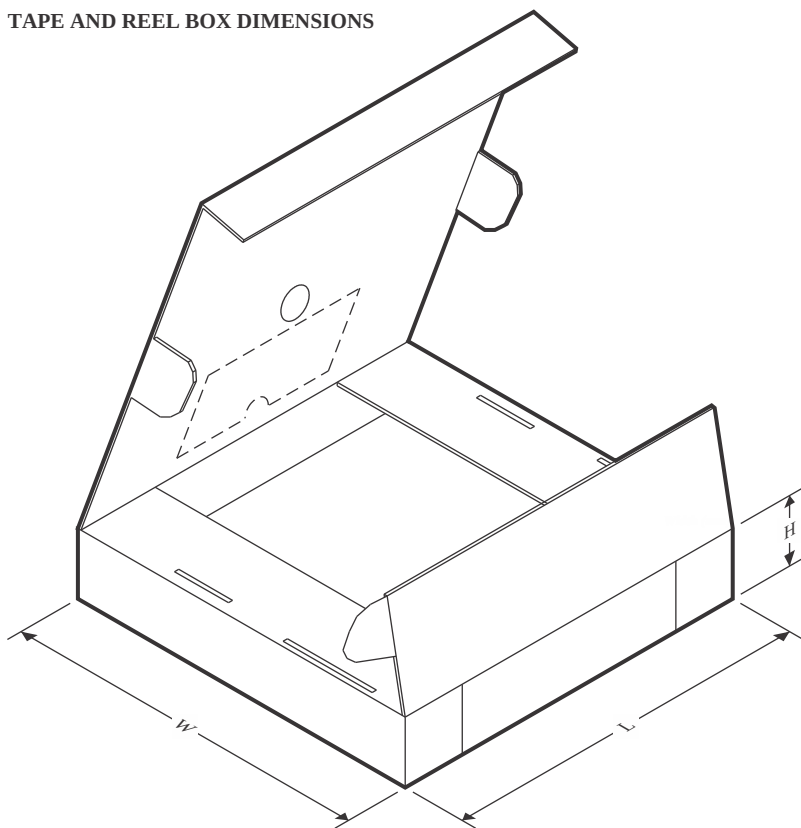
# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F5340IRGZR   | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F5340IRGZRG4 | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F5340IRGZT   | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F5341IRGZR   | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F5341IRGZT   | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F5342IRGZR   | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F5342IRGZRG4 | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F5342IRGZT   | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F5340IRGZR   | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430F5340IRGZRG4 | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430F5340IRGZT   | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F5341IRGZR   | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430F5341IRGZT   | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F5342IRGZR   | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430F5342IRGZRG4 | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430F5342IRGZT   | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |

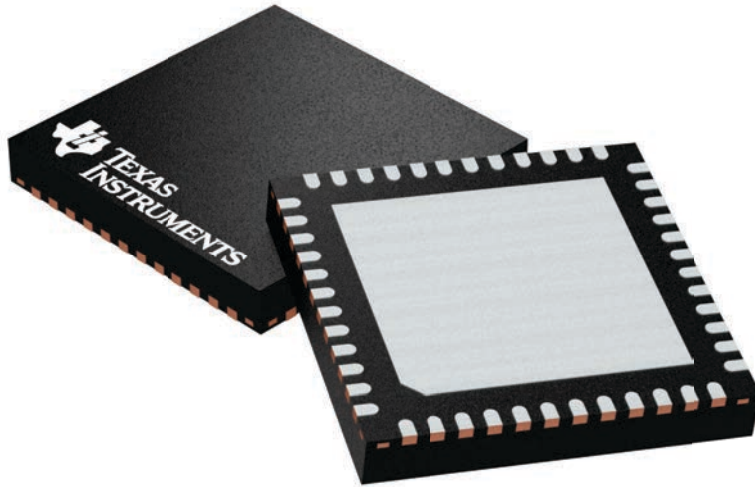
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD

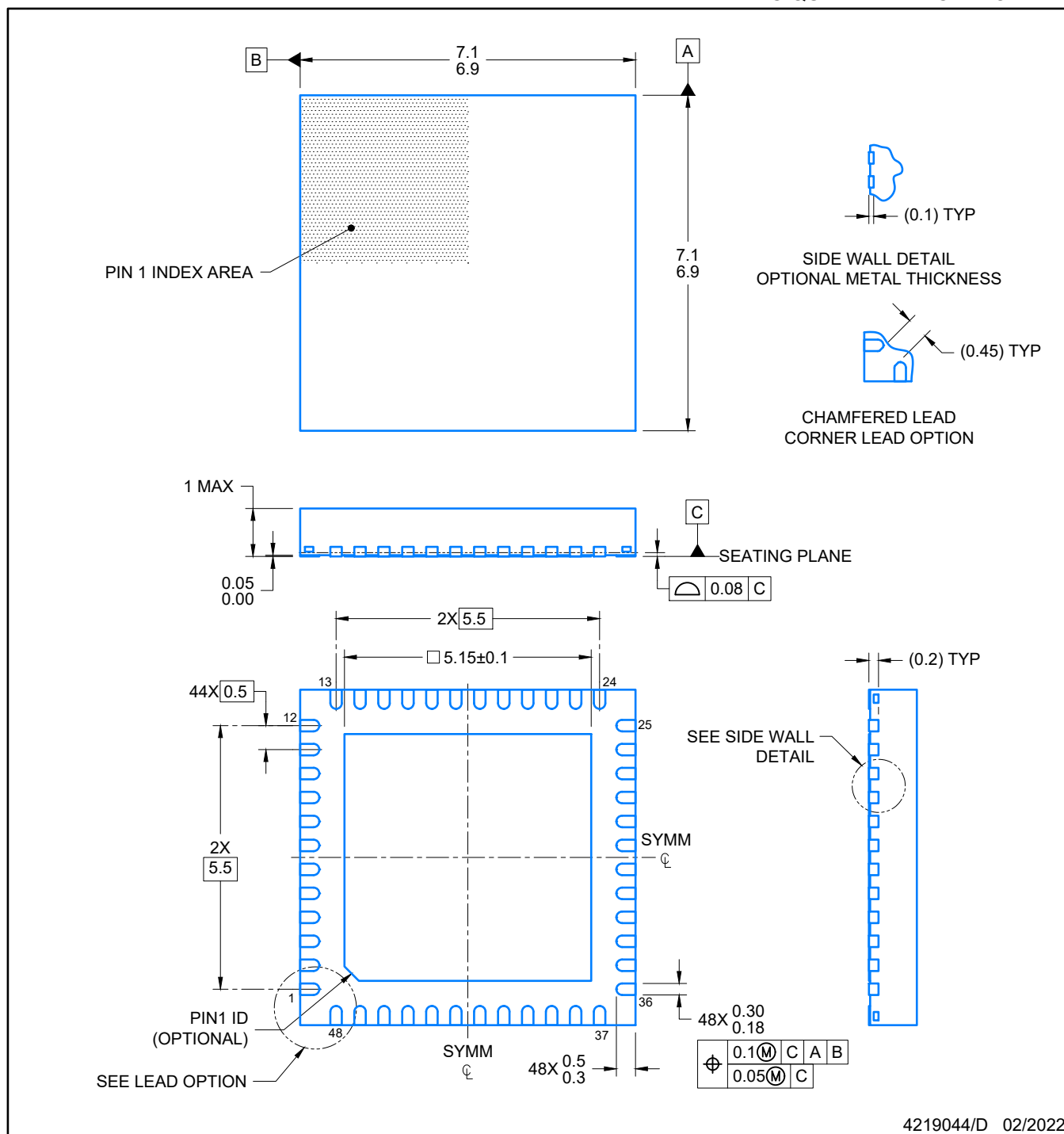


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

## PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD

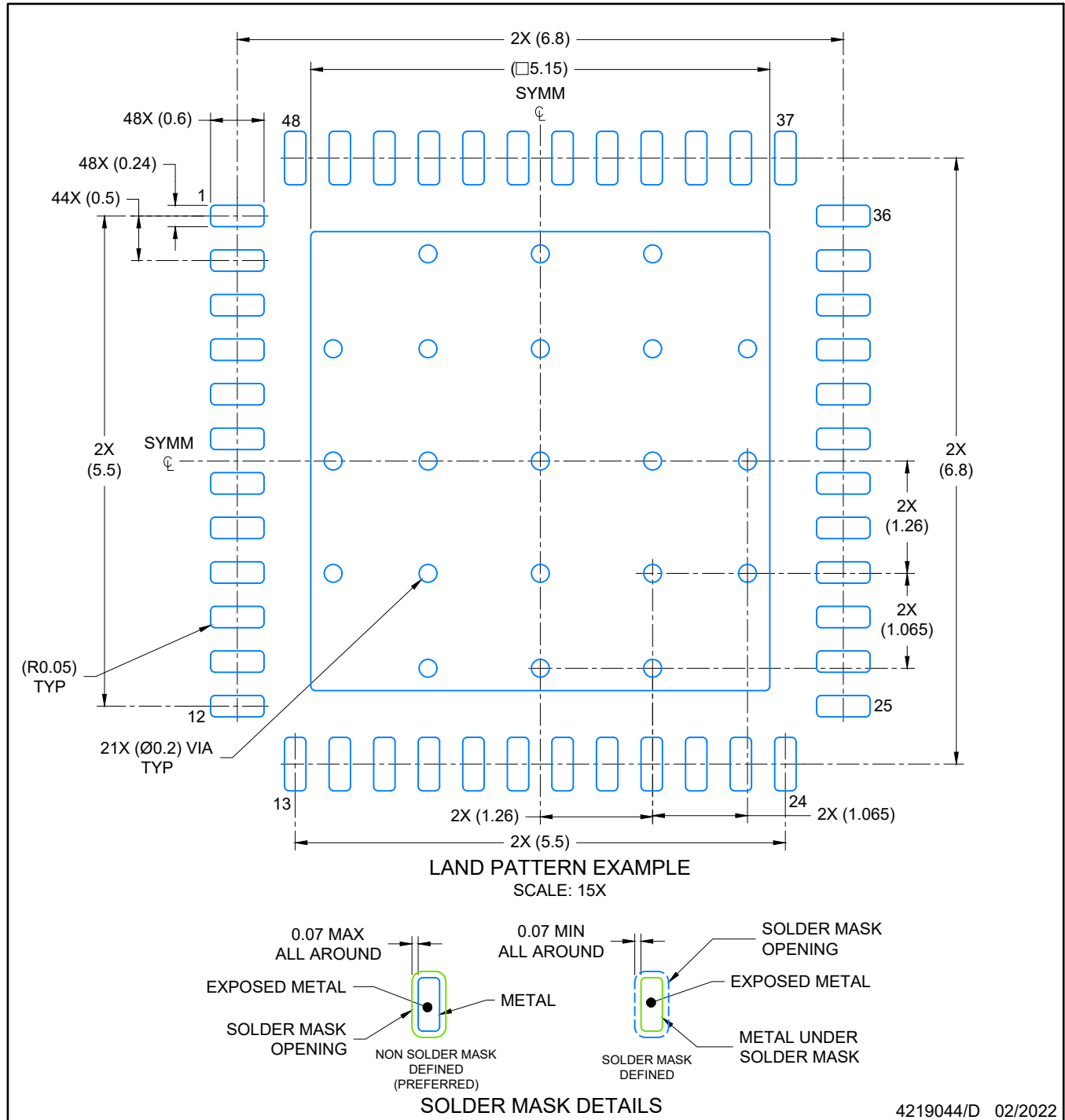


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT****RGZ0048A****VQFN - 1 mm max height**

PLASTIC QUADFLAT PACK- NO LEAD



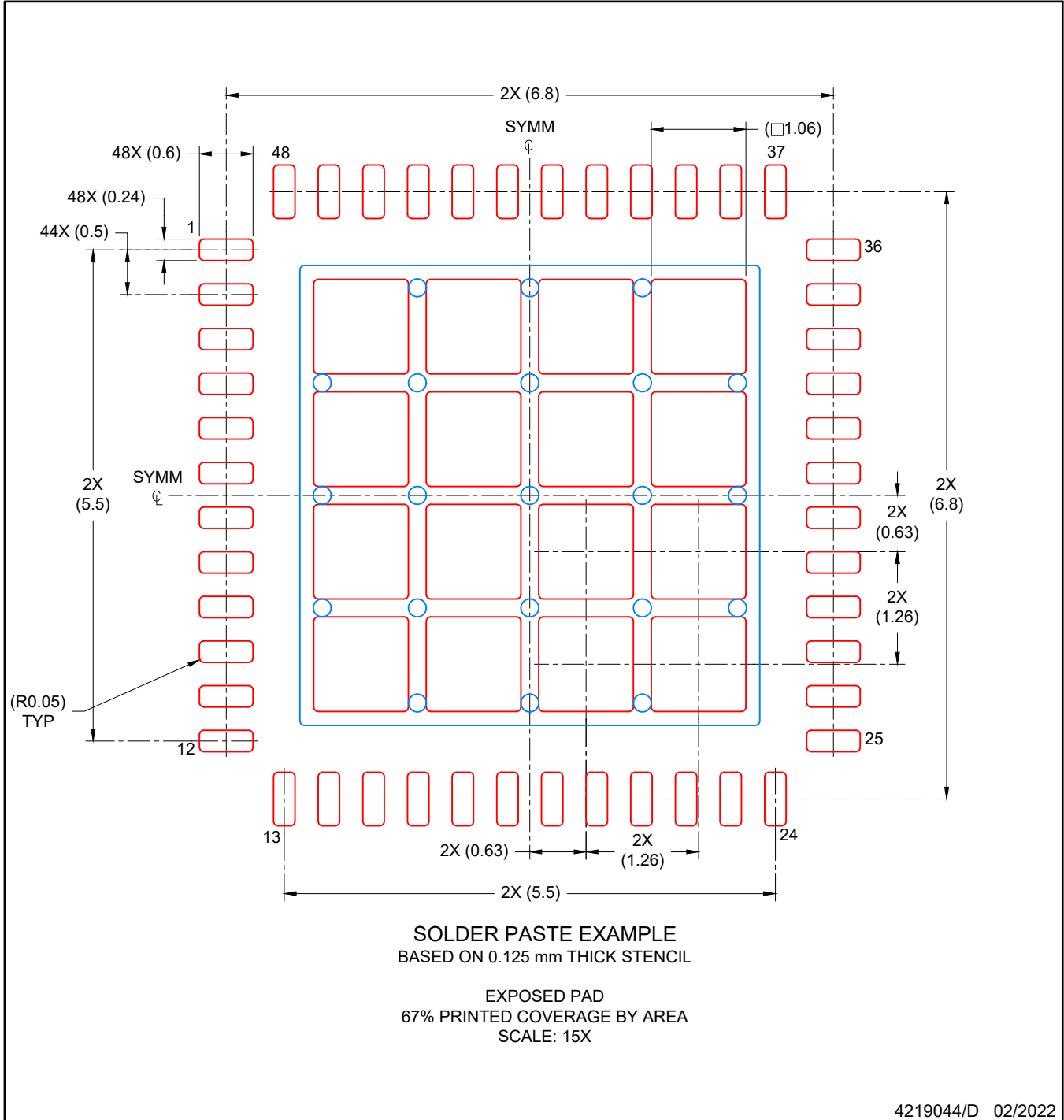
4219044/D 02/2022

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN****RGZ0048A****VQFN - 1 mm max height**

PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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