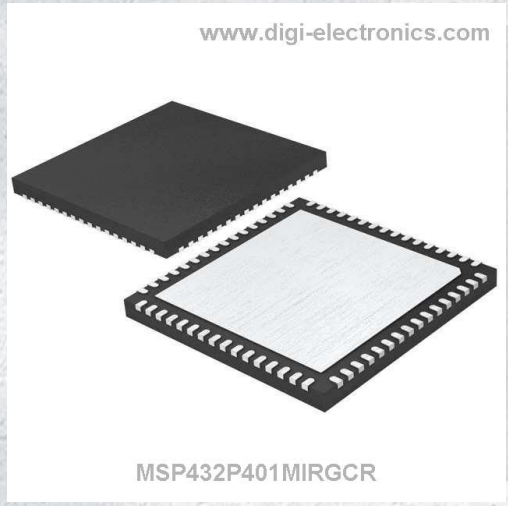
MSP432P401MIRGCR Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	MSP432P401MIRGCR-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	MSP432P401MIRGCR
Description	IC MCU 32BIT 128KB FLASH 64VQFN
Detailed Description	ARM® Cortex®-M4F MSP432™ Microcontroller IC 32-Bit Single-Core 48MHz 128KB (128K x 8) FLASH 64-V QFN (9x9)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MSP432P401MIRGCR	Texas Instruments
Series:	Product Status:
MSP432™	Obsolete
DiGi-Electronics Programmable:	Core Processor:
Not Verified	ARM® Cortex®-M4F
Core Size:	Speed:
32-Bit Single-Core	48MHz
Connectivity:	Peripherals:
I2C, IrDA, SPI, UART/USART	DMA, POR, PWM, WDT
Number of I/O:	Program Memory Size:
48	128KB (128K x 8)
Program Memory Type:	EEPROM Size:
FLASH	-
RAM Size:	Voltage - Supply (Vcc/Vdd):
32K x 8	1.62V ~ 3.7V
Data Converters:	Oscillator Type:
A/D 14x14b	Internal
Operating Temperature:	Mounting Type:
-40°C ~ 85°C (TA)	Surface Mount
Supplier Device Package:	Package / Case:
64-VQFN (9x9)	64-VFQFN Exposed Pad
Base Product Number:	
MSP432P401	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	5A992C
HTSUS:	
8542.31.0001	

MSP432P401R, MSP432P401M Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Core
  - ARM® 32-Bit Cortex®-M4F CPU With Floating-Point Unit and Memory Protection Unit
  - Frequency up to 48 MHz
  - ULPBench™ Benchmark:
    - 192.3 ULPMark™-CP
  - Performance Benchmark:
    - 3.41 CoreMark/MHz
    - 1.22 DMIPS/MHz (Dhrystone 2.1)
- Memories
  - Up to 256KB of Flash Main Memory (Organized Into Two Banks Enabling Simultaneous Read/Execute During Erase)
  - 16KB of Flash Information Memory (Used for BSL, TLV, and Flash Mailbox)
  - Up to 64KB of SRAM (Including 6KB of Backup Memory)
  - 32KB of ROM With MSP432™ Peripheral Driver Libraries
- Operating Characteristics
  - Wide Supply Voltage Range: 1.62 V to 3.7 V
  - Temperature Range (Ambient): –40°C to 85°C
- Ultra-Low-Power Operating Modes
  - Active: 80 µA/MHz
  - Low-Frequency Active: 83 µA at 128 kHz (Typical)
  - LPM3 (With RTC): 660 nA (Typical)
  - LPM3.5 (With RTC): 630 nA (Typical)
  - LPM4: 500 nA (Typical)
  - LPM4.5: 25 nA (Typical)
- Flexible Clocking Features
  - Tunable Internal DCO (up to 48 MHz)
  - 32.768 kHz Low-Frequency Crystal Support (LFXT)
  - High-Frequency Crystal Support (HFXT) up to 48 MHz
  - Low-Frequency Internal Reference Oscillator (REFO)
  - Very Low-Power Low-Frequency Internal Oscillator (VLO)
  - Module Oscillator (MODOSC)
  - System Oscillator (SYSOSC)
- Code Security Features
  - JTAG and SWD Lock
  - IP Protection (up to Four Secure Flash Zones, Each With Configurable Start Address and Size)
- Enhanced System Features
  - Programmable Supervision and Monitoring of Supply Voltage
  - Multiple-Class Resets for Better Control of Application and Debug
  - 8-Channel DMA
  - RTC With Calendar and Alarm Functions
- Timing and Control
  - Up to Four 16-Bit Timers, Each With up to Five Capture, Compare, PWM Capability
  - Two 32-Bit Timers, Each With Interrupt Generation Capability
- Serial Communication
  - Up to Four eUSCI_A Modules
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI (up to 16 Mbps)
  - Up to Four eUSCI_B Modules
    - I^2C (With Multiple-Slave Addressing)
    - SPI (up to 16 Mbps)
- Flexible I/O Features
  - Ultra-Low-Leakage I/Os (±20 nA Maximum)
  - All I/Os With Capacitive-Touch Capability
  - Up to 48 I/Os With Interrupt and Wake-up Capability
  - Up to 24 I/Os With Port Mapping Capability
  - Eight I/Os With Glitch Filtering Capability
- Advanced Low-Power Analog Features
  - 14-Bit 1-MSPS SAR ADC With Differential and Single-Ended Inputs
  - Internal Voltage Reference With 10-ppm/°C Typical Stability
  - Two Analog Comparators
- Encryption and Data Integrity Accelerators
  - 128-, 192-, or 256-Bit AES Encryption and Decryption Accelerator
  - 32-Bit Hardware CRC Engine
- JTAG and Debug Support
  - Support for 4-Pin JTAG and 2-Pin SWD Debug Interfaces
  - Support for Serial Wire Trace
  - Support for Power Debug and Profiling of Applications

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.2 Applications

- Industrial and Automation
  - Home Automation
  - Smoke Detectors
  - Barcode Scanners
  - Access Panels
- Metering
  - Electric Meters
  - Flow Meters
  - Communication Modules
- Health and Fitness
  - Watches
  - Activity Monitors
  - Fitness Accessories
  - Blood Glucose Meters
- Consumer Electronics
  - Mobile Devices
  - Sensor Hubs

1.3 Description

The MSP432P401x microcontroller (MCU) family is TI's latest addition to its portfolio of efficient ultra-low-power mixed-signal MCUs. The MSP432P401x MCUs feature the ARM Cortex-M4 processor in a wide configuration of device options including a rich set of analog, timing, and communication peripherals, thereby catering to a large number of application scenarios where both efficient data processing and enhanced low-power operation are paramount.

Overall, the MSP432P401x is an ideal combination of the TI MSP430™ low-power DNA, advance mixed-signal features, and the processing capabilities of the ARM 32-bit Cortex-M4 RISC engine. The devices ship with bundled peripheral driver libraries and are compatible with standard components of the ARM ecosystem.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE(2)
MSP432P401RIPZ MSP432P401MIPZ	LQFP (100)	14 mm × 14 mm
MSP432P401RIZXH MSP432P401MIZXH	NFBGA (80)	5 mm × 5 mm
MSP432P401RIRGC MSP432P401MIRGC	VQFN (64)	9 mm × 9 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 9, or see the TI website.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 9.

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1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the MSP432P401R and MSP432P401M devices.

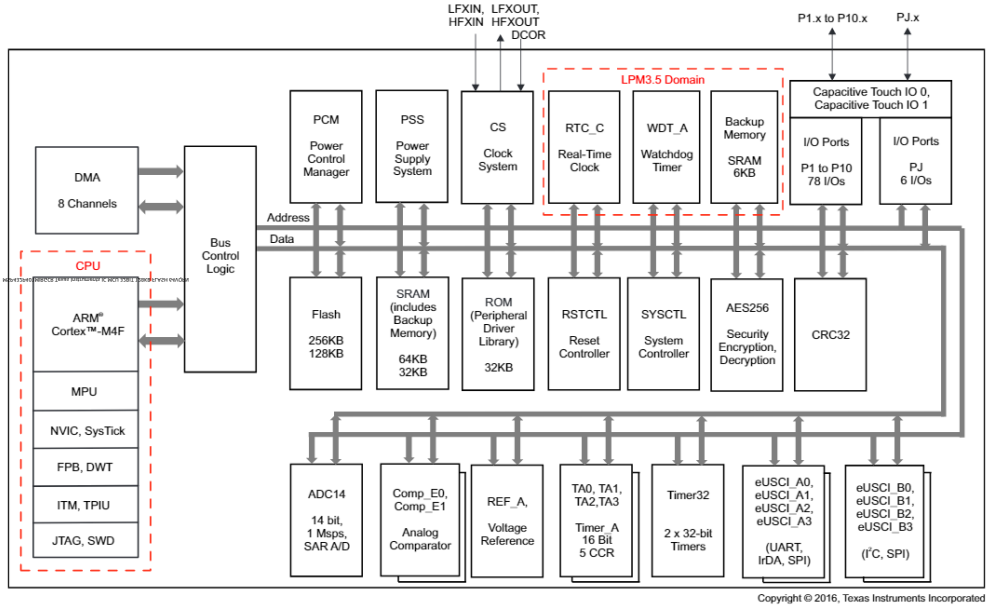


Figure 1-1. MSP432P401R, MSP432P401M Functional Block Diagram

The CPU and all of the peripherals in the device interact with each other through a common AHB matrix. In some cases, there are bridges between the AHB ports and the peripherals. These bridges are transparent to the application from a memory map perspective and, therefore, are not shown in the block diagram.

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 28, 2016 to July 25, 2016	Page
• Corrected C0.7 signal type (changed I/O to I) in Table 4-1, *Pin Attributes*	12
• Corrected C0.7 signal type (changed I/O to I) in Table 4-2, *Signal Descriptions*	18
• Added "HSMCLK, and SMCLK" to note (3) of Section 5.12 , *Current Consumption in Low-Frequency Active Modes – Dhrystone 2.1 Program*	32
• Added "HSMCLK, and SMCLK" to note (3) of Section 5.20 , *Current Consumption in Low-Frequency LPM0 Modes*	38
• Changed the ADC Gain Factor, ADC Offset, REF 1.2V Reference, REF 1.45V Reference, REF 2.5V Reference fields to Reserved in Table 6-86, *Device Descriptor Table*	177
• Added Section 6.14.1, *Revision Identification*	178
• Added Section 6.14.2, *Device Identification*	178

PRODUCT PREVIEW ARM 32-BIT CORTEX-M4F MICROCONTROLLER MSP432P401R, MSP432P401M

3 Device Comparison

Table 3-1 summarizes the features of the MSP432P401x microcontrollers.

Table 3-1. Device Comparison(1)

DEVICE	FLASH (KB)	SRAM (KB)	ADC14 (Channels)	COMP_E0 (Channels)	COMP_E1 (Channels)	Timer_A(2)	eUSCI		20-mA DRIVE I/O	TOTAL I/Os	PACKAGE
							CHANNEL A: UART, IrDA, SPI	CHANNEL B: SPI, I^2C			
MSP432P401RIPZ	256	64	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401MIPZ	128	32	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401RIZXH	256	64	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401MIZXH	128	32	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401RIRGC	256	64	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC
MSP432P401MIRGC	128	32	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 9, or see the TI website at www.ti.com.
(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

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3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for MSP 16-Bit and 32-Bit MCUs Low-power mixed-signal processors with smart analog and digital peripherals for a wide range of industrial and consumer applications.

Products for MSP432 Low Power + Performance MCUs MSP low power and performance microcontrollers from TI provide designers with increased processing capability, smart analog, advanced security, and display and communication peripherals while using less watts than ever before for the development of “always on” embedded applications.

Companion Products for MSP432P401R Review products that are frequently purchased or used with this product.

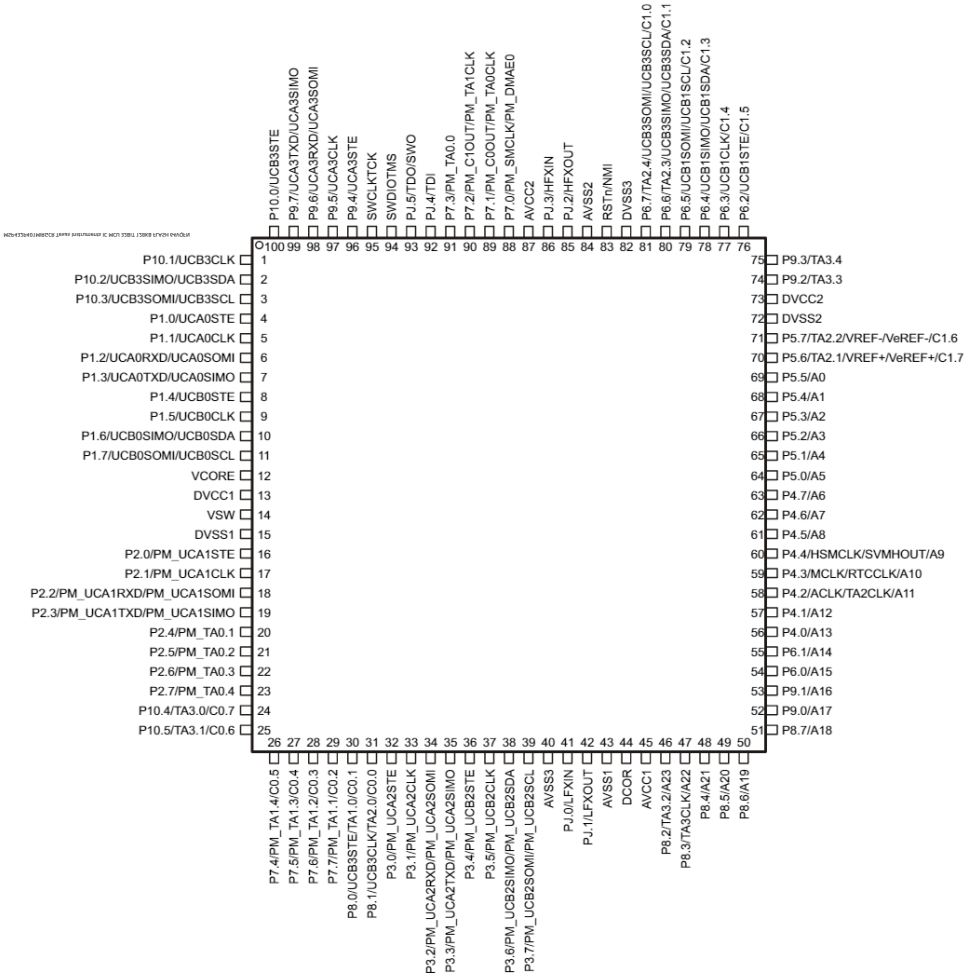
Reference Designs for MSP432P401R The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 100-pin PZ package.

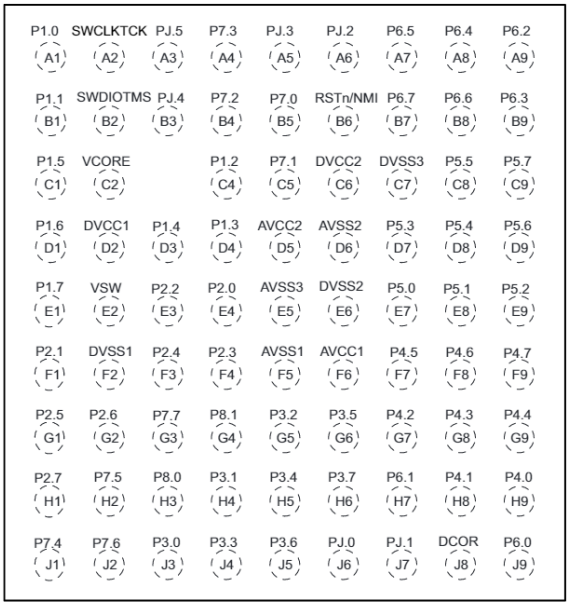


A. The secondary digital functions on Ports P2, P3, and P7 are fully mappable. This pinout shows only the default mapping. See Section 6.9.2 for details.
B. A glitch filter is implemented on these digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.
C. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD
D. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI
E. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-1. 100-Pin PZ Package (Top View)

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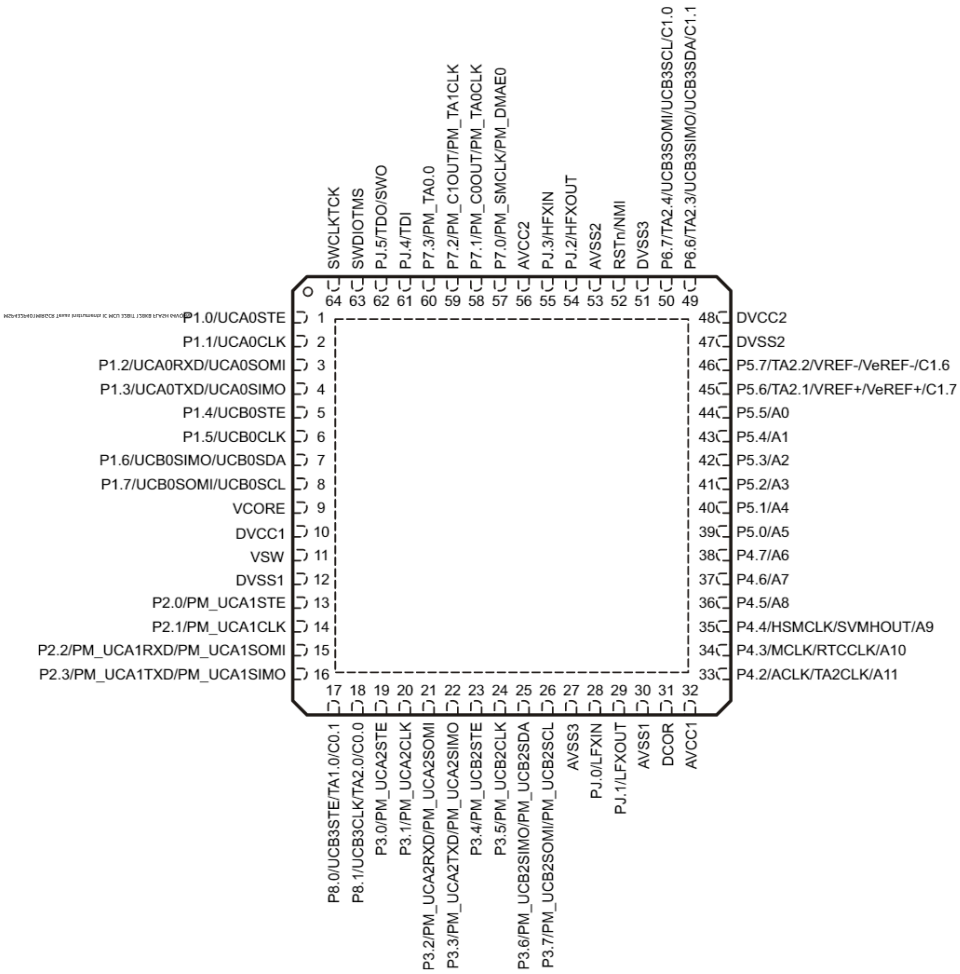
Figure 4-2 shows the pinout of the 80-pin ZXH package.



A. A glitch filter is implemented on these digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.
B. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD
C. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI
D. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-2. 80-Pin ZXH Package (Top View)

Figure 4-3 shows the pinout of the 64-pin RGC package.



A. The secondary digital functions on Ports P2, P3, and P7 are fully mappable. This pinout shows only the default mapping. See Section 6.9.2 for details.
B. A glitch filter is implemented on these digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.
C. TI recommends connecting the thermal pad on the QFN package to DVSS.
D. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD
E. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI
F. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-3. 64-Pin RGC Package (Top View)

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4.2 Pin Attributes

Table 4-1 describes the attributes of the pins.

Table 4-1. Pin Attributes

PIN NO.(1)			SIGNAL NAME(2) (3)	SIGNAL TYPE(4)	BUFFER TYPE(5)	POWER SOURCE(6)	RESET STATE AFTER POR(7)
PZ	ZXH	RGC					
1	N/A	N/A	P10.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB3CLK	I/O	LVCMOS	DVCC	N/A
2	N/A	N/A	P10.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB3SIMO	I/O	LVCMOS	DVCC	N/A
			UCB3SDA	I/O	LVCMOS	DVCC	N/A
3	N/A	N/A	P10.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB3SOMI	I/O	LVCMOS	DVCC	N/A
			UCB3SCL	I/O	LVCMOS	DVCC	N/A
4	A1	1	P1.0 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0STE	I/O	LVCMOS	DVCC	N/A
5	B1	2	P1.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0CLK	I/O	LVCMOS	DVCC	N/A
6	C4	3	P1.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0RXD	I	LVCMOS	DVCC	N/A
			UCA0SOMI	I/O	LVCMOS	DVCC	N/A
7	D4	4	P1.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0TXD	O	LVCMOS	DVCC	N/A
			UCA0SIMO	I/O	LVCMOS	DVCC	N/A
8	D3	5	P1.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0STE	I/O	LVCMOS	DVCC	N/A
9	C1	6	P1.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0CLK	I/O	LVCMOS	DVCC	N/A
10	D1	7	P1.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SIMO	I/O	LVCMOS	DVCC	N/A
			UCB0SDA	I/O	LVCMOS	DVCC	N/A
11	E1	8	P1.7 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SOMI	I/O	LVCMOS	DVCC	N/A
			UCB0SCL	I/O	LVCMOS	DVCC	N/A
12	C2	9	VCORE	–	Power	DVCC	N/A
13	D2	10	DVCC1	–	Power	N/A	N/A
14	E2	11	VSW	–	Power	N/A	N/A
15	F2	12	DVSS1	–	Power	N/A	N/A
16	E4	13	P2.0 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA1STE	I/O	LVCMOS	DVCC	N/A

(1) N/A = not available on this package
(2) (RD) indicates the reset default signal name for that pin.
(3) To determine the pin mux encodings for each pin, see Section 6.12, *Input/Output Diagrams*.
(4) Signal Types: I = Input, O = Output, I/O = Input or Output, P = power
(5) Buffer Types: see Table 4-3 for details
(6) The power source shown in this table is the I/O power source, which may differ from the module power source.
(7) Reset States:
OFF = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled
PD = High-impedance input with pulldown enabled
PU = High-impedance input with pullup enabled
N/A = Not applicable

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Table 4-1. Pin Attributes (continued)

PIN NO.[1]			SIGNAL NAME[2] [3]	SIGNAL TYPE[4]	BUFFER TYPE[5]	POWER SOURCE[6]	RESET STATE AFTER POR[7]
PZ	ZXH	RGC					
17	F1	14	P2.1 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA1CLK	I/O	LVCMOS	DVCC	N/A
18	E3	15	P2.2 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA1RXD	I	LVCMOS	DVCC	N/A
			PM_UCA1SOMI	I/O	LVCMOS	DVCC	N/A
19	F4	16	P2.3 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA1TXD	O	LVCMOS	DVCC	N/A
			PM_UCA1SIMO	I/O	LVCMOS	DVCC	N/A
20	F3	N/A	P2.4 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA0.1	I/O	LVCMOS	DVCC	N/A
21	G1	N/A	P2.5 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA0.2	I/O	LVCMOS	DVCC	N/A
22	G2	N/A	P2.6 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA0.3	I/O	LVCMOS	DVCC	N/A
23	H1	N/A	P2.7 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA0.4	I/O	LVCMOS	DVCC	N/A
24	N/A	N/A	P10.4 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.0	I/O	LVCMOS	DVCC	N/A
			C0.7	I	Analog	DVCC	N/A
25	N/A	N/A	P10.5 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.1	I/O	LVCMOS	DVCC	N/A
			C0.6	I	Analog	DVCC	N/A
26	J1	N/A	P7.4 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA1.4	I/O	LVCMOS	DVCC	N/A
			C0.5	I	Analog	DVCC	N/A
27	H2	N/A	P7.5 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA1.3	I/O	LVCMOS	DVCC	N/A
			C0.4	I	Analog	DVCC	N/A
28	J2	N/A	P7.6 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA1.2	I/O	LVCMOS	DVCC	N/A
			C0.3	I	Analog	DVCC	N/A
29	G3	N/A	P7.7 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA1.1	I/O	LVCMOS	DVCC	N/A
			C0.2	I	Analog	DVCC	N/A
30	H3	17	P8.0 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB3STE	I/O	LVCMOS	DVCC	N/A
			TA1.0	I/O	LVCMOS	DVCC	N/A
			C0.1	I	Analog	DVCC	N/A
31	G4	18	P8.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB3CLK	I/O	LVCMOS	DVCC	N/A
			TA2.0	I/O	LVCMOS	DVCC	N/A
			C0.0	I	Analog	DVCC	N/A
32	J3	19	P3.0 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA2STE	I/O	LVCMOS	DVCC	N/A
33	H4	20	P3.1 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA2CLK	I/O	LVCMOS	DVCC	N/A

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Table 4-1. Pin Attributes (continued)

PIN NO.[1]			SIGNAL NAME[2] [3]	SIGNAL TYPE[4]	BUFFER TYPE[5]	POWER SOURCE[6]	RESET STATE AFTER POR[7]
PZ	ZXH	RGC					
34	G5	21	P3.2 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA2RXD	I	LVCMOS	DVCC	N/A
			PM_UCA2SOMI	I/O	LVCMOS	DVCC	N/A
35	J4	22	P3.3 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCA2TXD	O	LVCMOS	DVCC	N/A
			PM_UCA2SIMO	I/O	LVCMOS	DVCC	N/A
36	H5	23	P3.4 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCB2STE	I/O	LVCMOS	DVCC	N/A
37	G6	24	P3.5 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCB2CLK	I/O	LVCMOS	DVCC	N/A
38	J5	25	P3.6 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCB2SIMO	I/O	LVCMOS	DVCC	N/A
			PM_UCB2SDA	I/O	LVCMOS	DVCC	N/A
39	H6	26	P3.7 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_UCB2SOMI	I/O	LVCMOS	DVCC	N/A
			PM_UCB2SCL	I	LVCMOS	DVCC	N/A
40	E5	27	AVSS3	–	Power	N/A	N/A
41	J6	28	PJ.0 (RD)	I/O	LVCMOS	DVCC	OFF
			LFXIN	I	Analog	DVCC	N/A
42	J7	29	PJ.1 (RD)	I/O	LVCMOS	DVCC	OFF
			LFXOUT	O	Analog	DVCC	N/A
43	F5	30	AVSS1	–	Power	N/A	N/A
44	J8	31	DCOR	–	Analog	N/A	N/A
45	F6	32	AVCC1	–	Power	N/A	N/A
46	N/A	N/A	P8.2 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.2	I/O	LVCMOS	DVCC	N/A
			A23	I	Analog	DVCC	N/A
47	N/A	N/A	P8.3 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3CLK	I	LVCMOS	DVCC	N/A
			A22	I	Analog	DVCC	N/A
48	N/A	N/A	P8.4 (RD)	I/O	LVCMOS	DVCC	OFF
			A21	I	Analog	DVCC	N/A
49	N/A	N/A	P8.5 (RD)	I/O	LVCMOS	DVCC	OFF
			A20	I	Analog	DVCC	N/A
50	N/A	N/A	P8.6 (RD)	I/O	LVCMOS	DVCC	OFF
			A19	I	Analog	DVCC	N/A
51	N/A	N/A	P8.7 (RD)	I/O	LVCMOS	DVCC	OFF
			A18	I	Analog	DVCC	N/A
52	N/A	N/A	P9.0 (RD)	I/O	LVCMOS	DVCC	OFF
			A17	I	Analog	DVCC	N/A
53	N/A	N/A	P9.1 (RD)	I/O	LVCMOS	DVCC	OFF
			A16	I	Analog	DVCC	N/A
54	J9	N/A	P6.0 (RD)	I/O	LVCMOS	DVCC	OFF
			A15	I	Analog	DVCC	N/A
55	H7	N/A	P6.1 (RD)	I/O	LVCMOS	DVCC	OFF
			A14	I	Analog	DVCC	N/A

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Table 4-1. Pin Attributes (continued)

PIN NO.[1]			SIGNAL NAME[2] [3]	SIGNAL TYPE[4]	BUFFER TYPE[5]	POWER SOURCE[6]	RESET STATE AFTER POR[7]
PZ	ZXH	RGC					
56	H9	N/A	P4.0 (RD)	I/O	LVCMOS	DVCC	OFF
			A13	I	Analog	DVCC	N/A
57	H8	N/A	P4.1 (RD)	I/O	LVCMOS	DVCC	OFF
			A12	I	Analog	DVCC	N/A
58	G7	33	P4.2 (RD)	I/O	LVCMOS	DVCC	OFF
			ACLK	O	LVCMOS	DVCC	N/A
			TA2CLK	I	LVCMOS	DVCC	N/A
			A11	I	Analog	DVCC	N/A
59	G8	34	P4.3 (RD)	I/O	LVCMOS	DVCC	OFF
			MCLK	O	LVCMOS	DVCC	N/A
			RTCCLK	O	LVCMOS	DVCC	N/A
			A10	I	Analog	DVCC	N/A
60	G9	35	P4.4 (RD)	I/O	LVCMOS	DVCC	OFF
			HSMCLK	O	LVCMOS	DVCC	N/A
			SVMHOUT	O	LVCMOS	DVCC	N/A
			A9	I	Analog	DVCC	N/A
61	F7	36	P4.5 (RD)	I/O	LVCMOS	DVCC	OFF
			A8	I	Analog	DVCC	N/A
62	F8	37	P4.6 (RD)	I/O	LVCMOS	DVCC	OFF
			A7	I	Analog	DVCC	N/A
63	F9	38	P4.7 (RD)	I/O	LVCMOS	DVCC	OFF
			A6	I	Analog	DVCC	N/A
64	E7	39	P5.0 (RD)	I/O	LVCMOS	DVCC	OFF
			A5	I	Analog	DVCC	N/A
65	E8	40	P5.1 (RD)	I/O	LVCMOS	DVCC	OFF
			A4	I	Analog	DVCC	N/A
66	E9	41	P5.2 (RD)	I/O	LVCMOS	DVCC	OFF
			A3	I	Analog	DVCC	N/A
67	D7	42	P5.3 (RD)	I/O	LVCMOS	DVCC	OFF
			A2	I	Analog	DVCC	N/A
68	D8	43	P5.4 (RD)	I/O	LVCMOS	DVCC	OFF
			A1	I	Analog	DVCC	N/A
69	C8	44	P5.5 (RD)	I/O	LVCMOS	DVCC	OFF
			A0	I	Analog	DVCC	N/A
70	D9	45	P5.6 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.1	I/O	LVCMOS	DVCC	N/A
			VREF+	O	Analog	DVCC	N/A
			VeREF+	I	Analog	DVCC	N/A
			C1.7	I	Analog	DVCC	N/A
71	C9	46	P5.7 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.2	I/O	LVCMOS	DVCC	N/A
			VREF-	O	Analog	DVCC	N/A
			VeREF-	I	Analog	DVCC	N/A
			C1.6	I	Analog	DVCC	N/A
72	E6	47	DVSS2	–	Power	N/A	N/A
73	C6	48	DVCC2	–	Power	N/A	N/A

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Table 4-1. Pin Attributes (continued)

PIN NO.(1)			SIGNAL NAME(2) (3)	SIGNAL TYPE(4)	BUFFER TYPE(5)	POWER SOURCE(6)	RESET STATE AFTER POR(7)
PZ	ZXH	RGC					
74	N/A	N/A	P9.2 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.3	I/O	LVCMOS	DVCC	N/A
75	N/A	N/A	P9.3 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.4	I/O	LVCMOS	DVCC	N/A
76	A9	N/A	P6.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1STE	I/O	LVCMOS	DVCC	N/A
			C1.5	I	Analog	DVCC	N/A
77	B9	N/A	P6.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1CLK	I/O	LVCMOS	DVCC	N/A
			C1.4	I	Analog	DVCC	N/A
78	A8	N/A	P6.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1SIMO	I/O	LVCMOS	DVCC	N/A
			UCB1SDA	I/O	LVCMOS	DVCC	N/A
			C1.3	I	Analog	DVCC	N/A
79	A7	N/A	P6.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1SOMI	I/O	LVCMOS	DVCC	N/A
			UCB1SCL	I/O	LVCMOS	DVCC	N/A
			C1.2	I	Analog	DVCC	N/A
80	B8	49	P6.6 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.3	I/O	LVCMOS	DVCC	N/A
			UCB3SIMO	I/O	LVCMOS	DVCC	N/A
			UCB3SDA	I/O	LVCMOS	DVCC	N/A
			C1.1	I	Analog	DVCC	N/A
81	B7	50	P6.7 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.4	I/O	LVCMOS	DVCC	N/A
			UCB3SOMI	I/O	LVCMOS	DVCC	N/A
			UCB3SCL	I/O	LVCMOS	DVCC	N/A
			C1.0	I	Analog	DVCC	N/A
82	C7	51	DVSS3	–	Power	N/A	N/A
83	B6	52	RSTn (RD)	I	LVCMOS	DVCC	PU
			NMI	I	LVCMOS	DVCC	N/A
84	D6	53	AVSS2	–	Power	N/A	N/A
85	A6	54	PJ.2 (RD)	I/O	LVCMOS	DVCC	OFF
			HFXOUT	O	Analog	DVCC	N/A
86	A5	55	PJ.3 (RD)	I/O	LVCMOS	DVCC	OFF
			HFXIN	I	Analog	DVCC	N/A
87	D5	56	AVCC2	–	Power	N/A	N/A
88	B5	57	P7.0 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_SMCLK	O	LVCMOS	DVCC	N/A
			PM_DMAE0	I	LVCMOS	DVCC	N/A
89	C5	58	P7.1 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_C0OUT	O	LVCMOS	DVCC	N/A
			PM_TA0CLK	I	LVCMOS	DVCC	N/A
90	B4	59	P7.2 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_C1OUT	O	LVCMOS	DVCC	N/A
			PM_TA1CLK	I	LVCMOS	DVCC	N/A

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Table 4-1. Pin Attributes (continued)

PIN NO.[1]			SIGNAL NAME[2] [3]	SIGNAL TYPE[4]	BUFFER TYPE[5]	POWER SOURCE[6]	RESET STATE AFTER POR[7]
PZ	ZXH	RGC					
91	A4	60	P7.3 (RD)	I/O	LVCMOS	DVCC	OFF
			PM_TA0.0	I/O	LVCMOS	DVCC	N/A
92	B3	61	PJ.4	I/O	LVCMOS	DVCC	N/A
			TDI (RD)	I	LVCMOS	DVCC	PU
93	A3	62	PJ.5	I/O	LVCMOS	DVCC	N/A
			TDO (RD)	O	LVCMOS	DVCC	N/A
			SWO	O	LVCMOS	DVCC	N/A
94	B2	63	SWDIOTMS	I/O	LVCMOS	DVCC	PU
95	A2	64	SWCLKTCK	I	LVCMOS	DVCC	PD
96	N/A	N/A	P9.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA3STE	I/O	LVCMOS	DVCC	N/A
97	N/A	N/A	P9.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA3CLK	I/O	LVCMOS	DVCC	N/A
98	N/A	N/A	P9.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA3RXD	I	LVCMOS	DVCC	N/A
			UCA3SOMI	I/O	LVCMOS	DVCC	N/A
99	N/A	N/A	P9.7 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA3TXD	O	LVCMOS	DVCC	N/A
			UCA3SIMO	I/O	LVCMOS	DVCC	N/A
100	N/A	N/A	P10.0 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB3STE	I/O	LVCMOS	DVCC	N/A
N/A	N/A	Pad	QFN Pad	–	–	N/A	–

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4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

Table 4-2. Signal Descriptions

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
ADC	A0	69	C8	44	I	ADC analog input A0
	A1	68	D8	43	I	ADC analog input A1
	A2	67	D7	42	I	ADC analog input A2
	A3	66	E9	41	I	ADC analog input A3
	A4	65	E8	40	I	ADC analog input A4
	A5	64	E7	39	I	ADC analog input A5
	A6	63	F9	38	I	ADC analog input A6
	A7	62	F8	37	I	ADC analog input A7
	A8	61	F7	36	I	ADC analog input A8
	A9	60	G9	35	I	ADC analog input A9
	A10	59	G8	34	I	ADC analog input A10
	A11	58	G7	33	I	ADC analog input A11
	A12	57	H8	N/A	I	ADC analog input A12
	A13	56	H9	N/A	I	ADC analog input A13
	A14	55	H7	N/A	I	ADC analog input A14
	A15	54	J9	N/A	I	ADC analog input A15
	A16	53	N/A	N/A	I	ADC analog input A16
	A17	52	N/A	N/A	I	ADC analog input A17
	A18	51	N/A	N/A	I	ADC analog input A18
	A19	50	N/A	N/A	I	ADC analog input A19
	A20	49	N/A	N/A	I	ADC analog input A20
	A21	48	N/A	N/A	I	ADC analog input A21
	A22	47	N/A	N/A	I	ADC analog input A22
	A23	46	N/A	N/A	I	ADC analog input A23
Clock	ACLK	58	G7	33	O	ACLK clock output
	DCOR	44	J8	31	–	DCO external resistor pin
	HFXIN	86	A5	55	I	Input for high-frequency crystal oscillator HFXT
	HFXOUT	85	A6	54	O	Output for high-frequency crystal oscillator HFXT
	HSMCLK	60	G9	35	O	HSMCLK clock output
	LFXIN	41	J6	28	I	Input for low-frequency crystal oscillator LFXT
	LFXOUT	42	J7	29	O	Output of low-frequency crystal oscillator LFXT
	MCLK	59	G8	34	O	MCLK clock output

(1) N/A = not available
(2) I = input, O = output

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
Comparator	C0.0	31	G4	18	I	Comparator_E0 input 0
	C0.1	30	H3	17	I	Comparator_E0 input 1
	C0.2	29	G3	N/A	I	Comparator_E0 input 2
	C0.3	28	J2	N/A	I	Comparator_E0 input 3
	C0.4	27	H2	N/A	I	Comparator_E0 input 4
	C0.5	26	J1	N/A	I	Comparator_E0 input 5
	C0.6	25	N/A	N/A	I	Comparator_E0 input 6
	C0.7	24	N/A	N/A	I	Comparator_E0 input 7
	C1.0	81	B7	50	I	Comparator_E1 input 0
	C1.1	80	B8	49	I	Comparator_E1 input 1
	C1.2	79	A7	N/A	I	Comparator_E1 input 2
	C1.3	78	A8	N/A	I	Comparator_E1 input 3
	C1.4	77	B9	N/A	I	Comparator_E1 input 4
	C1.5	76	A9	N/A	I	Comparator_E1 input 5
	C1.6	71	C9	46	I	Comparator_E1 input 6
	C1.7	70	D9	45	I	Comparator_E1 input 7
Debug	SWCLKTCK	95	A2	64	I	Serial wire clock input (SWCLK)/JTAG clock input (TCK)
	SWDIOTMS	94	B2	63	I/O	Serial wire data input/output (SWDIO)/JTAG test mode select (TMS)
	SWO	93	A3	62	O	Serial wire trace output
	TDI	92	B3	61	I	JTAG test data input
	TDO	93	A3	62	O	JTAG test data output
GPIO	P1.0	4	A1	1	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.1	5	B1	2	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.2	6	C4	3	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.3	7	D4	4	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.4	8	D3	5	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.5	9	C1	6	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.6	10	D1	7	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.7	11	E1	8	I/O	General-purpose digital I/O with port interrupt and wake-up capability

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
GPIO (continued)	P2.0	16	E4	13	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
	P2.1	17	F1	14	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
	P2.2	18	E3	15	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
	P2.3	19	F4	16	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
	P2.4	20	F3	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P2.5	21	G1	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P2.6	22	G2	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P2.7	23	H1	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.0	32	J3	19	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
	P3.1	33	H4	20	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.2	34	G5	21	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.3	35	J4	22	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.4	36	H5	23	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
	P3.5	37	G6	24	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
	P3.6	38	J5	25	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.7	39	H6	26	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
GPIO (continued)	P4.0	56	H9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.1	57	H8	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.2	58	G7	33	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.3	59	G8	34	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.4	60	G9	35	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.5	61	F7	36	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.6	62	F8	37	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.7	63	F9	38	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.0	64	E7	39	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.1	65	E8	40	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.2	66	E9	41	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.3	67	D7	42	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.4	68	D8	43	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.5	69	C8	44	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.6	70	D9	45	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.7	71	C9	46	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.0	54	J9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.1	55	H7	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.2	76	A9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.3	77	B9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.4	78	A8	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.5	79	A7	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.6	80	B8	49	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P6.7	81	B7	50	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
GPIO (continued)	P7.0	88	B5	57	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.1	89	C5	58	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.2	90	B4	59	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.3	91	A4	60	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.4	26	J1	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.5	27	H2	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.6	28	J2	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.7	29	G3	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P8.0	30	H3	17	I/O	General-purpose digital I/O
	P8.1	31	G4	18	I/O	General-purpose digital I/O
	P8.2	46	N/A	N/A	I/O	General-purpose digital I/O
	P8.3	47	N/A	N/A	I/O	General-purpose digital I/O
	P8.4	48	N/A	N/A	I/O	General-purpose digital I/O
	P8.5	49	N/A	N/A	I/O	General-purpose digital I/O
	P8.6	50	N/A	N/A	I/O	General-purpose digital I/O
	P8.7	51	N/A	N/A	I/O	General-purpose digital I/O
	P9.0	52	N/A	N/A	I/O	General-purpose digital I/O
	P9.1	53	N/A	N/A	I/O	General-purpose digital I/O
	P9.2	74	N/A	N/A	I/O	General-purpose digital I/O
	P9.3	75	N/A	N/A	I/O	General-purpose digital I/O
	P9.4	96	N/A	N/A	I/O	General-purpose digital I/O
	P9.5	97	N/A	N/A	I/O	General-purpose digital I/O
	P9.6	98	N/A	N/A	I/O	General-purpose digital I/O
	P9.7	99	N/A	N/A	I/O	General-purpose digital I/O
	P10.0	100	N/A	N/A	I/O	General-purpose digital I/O
	P10.1	1	N/A	N/A	I/O	General-purpose digital I/O
	P10.2	2	N/A	N/A	I/O	General-purpose digital I/O
	P10.3	3	N/A	N/A	I/O	General-purpose digital I/O
	P10.4	24	N/A	N/A	I/O	General-purpose digital I/O
	P10.5	25	N/A	N/A	I/O	General-purpose digital I/O
	PJ.0	41	J6	28	I/O	General-purpose digital I/O
	PJ.1	42	J7	29	I/O	General-purpose digital I/O
	PJ.2	85	A6	54	I/O	General-purpose digital I/O
	PJ.3	86	A5	55	I/O	General-purpose digital I/O
	PJ.4	92	B3	61	I/O	General-purpose digital I/O
	PJ.5	93	A3	62	I/O	General-purpose digital I/O

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
I²C	UCB0SCL	11	E1	8	I/O	I²C clock – eUSCI_B0 I²C mode
	UCB0SDA	10	D1	7	I/O	I²C data – eUSCI_B0 I²C mode
	UCB1SCL	79	A7	N/A	I/O	I²C clock – eUSCI_B1 I²C mode
	UCB1SDA	78	A8	N/A	I/O	I²C data – eUSCI_B1 I²C mode
	UCB3SCL	3	N/A	N/A	I/O	I²C clock – eUSCI_B3 I²C mode
	UCB3SCL	81	B7	50	I/O	I²C clock – eUSCI_B3 I²C mode
	UCB3SDA	2	N/A	N/A	I/O	I²C data – eUSCI_B3 I²C mode
	UCB3SDA	80	B8	49	I/O	I²C data – eUSCI_B3 I²C mode

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
Port Mapper	PM_C0OUT	89	C5	58	O	Default mapping: Comparator_E0 output
	PM_C1OUT	90	B4	59	O	Default mapping: Comparator_E1 output
	PM_DMAE0	88	B5	57	I	Default mapping: DMA external trigger input
	PM_SMCLK	88	B5	57	O	Default mapping: SMCLK clock output
	PM_TA0.0	91	A4	60	I/O	Default mapping: TA0 CCR0 capture: CCI0A input, compare: Out0
	PM_TA0.1	20	F3	N/A	I/O	Default mapping: TA0 CCR1 capture: CCI1A input, compare: Out1
	PM_TA0.2	21	G1	N/A	I/O	Default mapping: TA0 CCR2 capture: CCI2A input, compare: Out2
	PM_TA0.3	22	G2	N/A	I/O	Default mapping: TA0 CCR3 capture: CCI3A input, compare: Out3
	PM_TA0.4	23	H1	N/A	I/O	Default mapping: TA0 CCR4 capture: CCI4A input, compare: Out4
	PM_TA0CLK	89	C5	58	I	Default mapping: TA0 input clock
	PM_TA1.2	28	J2	N/A	I/O	Default mapping: TA1 CCR2 capture: CCI2A input, compare: Out2
	PM_TA1.3	27	H2	N/A	I/O	Default mapping: TA1 CCR3 capture: CCI3A input, compare: Out3
	PM_TA1.4	26	J1	N/A	I/O	Default mapping: TA1 CCR4 capture: CCI4A input, compare: Out4
	PM_TA1CLK	90	B4	59	I	Default mapping: TA1 input clock
	PM_UCA1CLK	17	F1	14	I/O	Default mapping: Clock signal input – eUSCI_A1 SPI slave mode Clock signal output – eUSCI_A1 SPI master mode
	PM_UCA1RXD	18	E3	15	I	Default mapping: Receive data – eUSCI_A1 UART mode
	PM_UCA1SIMO	19	F4	16	I/O	Default mapping: Slave in, master out – eUSCI_A1 SPI mode
	PM_UCA1SOMI	18	E3	15	I/O	Default mapping: Slave out, master in – eUSCI_A1 SPI mode
	PM_UCA1STE	16	E4	13	I/O	Default mapping: Slave transmit enable – eUSCI_A1 SPI mode
	PM_UCA1TXD	19	F4	16	O	Default mapping: Transmit data – eUSCI_A1 UART mode
	PM_UCA2CLK	33	H4	20	I/O	Default mapping: Clock signal input – eUSCI_A2 SPI slave mode Clock signal output – eUSCI_A2 SPI master mode
	PM_UCA2RXD	34	G5	21	I	Default mapping: Receive data – eUSCI_A2 UART mode
	PM_UCA2SIMO	35	J4	22	I/O	Default mapping: Slave in, master out – eUSCI_A2 SPI mode
	PM_UCA2SOMI	34	G5	21	I/O	Default mapping: Slave out, master in – eUSCI_A2 SPI mode
	PM_UCA2STE	32	J3	19	I/O	Default mapping: Slave transmit enable – eUSCI_A2 SPI mode
	PM_UCA2TXD	35	J4	22	O	Default mapping: Transmit data – eUSCI_A2 UART mode

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
Port Mapper (continued)	PM_UCB2CLK	37	G6	24	I/O	Default mapping: Clock signal input – eUSCI_B2 SPI slave mode Clock signal output – eUSCI_B2 SPI master mode
	PM_UCB2SCL	39	H6	26	I	Default mapping: I^2C clock – eUSCI_B2 I^2C mode
	PM_UCB2SDA	38	J5	25	I/O	Default mapping: I^2C data – eUSCI_B2 I^2C mode
	PM_UCB2SIMO	38	J5	25	I/O	Default mapping: Slave in, master out – eUSCI_B2 SPI mode
	PM_UCB2SOMI	39	H6	26	I/O	Default mapping: Slave out, master in – eUSCI_B2 SPI mode
	PM_UCB2STE	36	H5	23	I/O	Default mapping: Slave transmit enable – eUSCI_B2 SPI mode
Power	AVCC1	45	F6	32	–	Analog power supply
	AVCC2	87	D5	56	–	Analog power supply
	AVSS1	43	F5	30	–	Analog ground supply
	AVSS2	84	D6	53	–	Analog ground supply
	AVSS3	40	E5	27	–	Analog ground supply
	DVCC1	13	D2	10	–	Digital power supply
	DVCC2	73	C6	48	–	Digital power supply
	DVSS1	15	F2	12	–	Digital ground supply
	DVSS2	72	E6	47	–	Digital ground supply
	DVSS3	82	C7	51	–	Must be connected to ground
	VCORE(3)	12	C2	9	–	Regulated core power supply (internal use only, no external current loading)
	VSW	14	E2	11	–	DC-to-DC converter switching output
RTC	RTCCLK	59	G8	34	O	RTC_C clock calibration output
Reference	VREF+	70	D9	45	O	Internal shared reference voltage positive terminal
	VREF-	71	C9	46	O	Internal shared reference voltage negative terminal
	VeREF+	70	D9	45	I	Positive terminal of external reference voltage to ADC
	VeREF-	71	C9	46	I	Negative terminal of external reference voltage to ADC (recommended to connect to onboard ground)

(3) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
SPI	UCA0CLK	5	B1	2	I/O	Clock signal input – eUSCI_A0 SPI slave mode Clock signal output – eUSCI_A0 SPI master mode
	UCA0SIMO	7	D4	4	I/O	Slave in, master out – eUSCI_A0 SPI mode
	UCA0SOMI	6	C4	3	I/O	Slave out, master in – eUSCI_A0 SPI mode
	UCA0STE	4	A1	1	I/O	Slave transmit enable – eUSCI_A0 SPI mode
	UCA3CLK	97	N/A	N/A	I/O	Clock signal input – eUSCI_A3 SPI slave mode Clock signal output – eUSCI_A3 SPI master mode
	UCA3SIMO	99	N/A	N/A	I/O	Slave in, master out – eUSCI_A3 SPI mode
	UCA3SOMI	98	N/A	N/A	I/O	Slave out, master in – eUSCI_A3 SPI mode
	UCA3STE	96	N/A	N/A	I/O	Slave transmit enable – eUSCI_A3 SPI mode
	UCB0CLK	9	C1	6	I/O	Clock signal input – eUSCI_B0 SPI slave mode Clock signal output – eUSCI_B0 SPI master mode
	UCB0SIMO	10	D1	7	I/O	Slave in, master out – eUSCI_B0 SPI mode
	UCB0SOMI	11	E1	8	I/O	Slave out, master in – eUSCI_B0 SPI mode
	UCB0STE	8	D3	5	I/O	Slave transmit enable – eUSCI_B0 SPI mode
	UCB1CLK	77	B9	N/A	I/O	Clock signal input – eUSCI_B1 SPI slave mode Clock signal output – eUSCI_B1 SPI master mode
	UCB1SIMO	78	A8	N/A	I/O	Slave in, master out – eUSCI_B1 SPI mode
	UCB1SOMI	79	A7	N/A	I/O	Slave out, master in – eUSCI_B1 SPI mode
	UCB1STE	76	A9	N/A	I/O	Slave transmit enable – eUSCI_B1 SPI mode
	UCB3CLK	1	N/A	N/A	I/O	Clock signal input – eUSCI_B3 SPI slave mode Clock signal output – eUSCI_B3 SPI master mode
	UCB3CLK	31	G4	18	I/O	Clock signal input – eUSCI_B3 SPI slave mode Clock signal output – eUSCI_B3 SPI master mode
	UCB3SIMO	2	N/A	N/A	I/O	Slave in, master out – eUSCI_B3 SPI mode
	UCB3SIMO	80	B8	49	I/O	Slave in, master out – eUSCI_B3 SPI mode
	UCB3SOMI	3	N/A	N/A	I/O	Slave out, master in – eUSCI_B3 SPI mode
	UCB3SOMI	81	B7	50	I/O	Slave out, master in – eUSCI_B3 SPI mode
	UCB3STE	30	H3	17	I/O	Slave transmit enable – eUSCI_B3 SPI mode
	UCB3STE	100	N/A	N/A	I/O	Slave transmit enable – eUSCI_B3 SPI mode
System	NMI	83	B6	52	I	External nonmaskable interrupt
	RSTn	83	B6	52	I	External reset (active low)
	SVMHOUT	60	G9	35	O	SVMH output
Thermal	QFN Pad	N/A	N/A	Pad	–	QFN package exposed thermal pad. TI recommends connection to VSS.

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)			SIGNAL TYPE(2)	DESCRIPTION
		PZ	ZXH	RGC		
Timer	PM_TA1.1	29	G3	N/A	I/O	Default mapping: TA1 CCR1 capture: CCI1A input, compare: Out1
	TA1.0	30	H3	17	I/O	TA1 CCR0 capture: CCI0A input, compare: Out0
	TA2.0	31	G4	18	I/O	TA2 CCR0 capture: CCI0A input, compare: Out0
	TA2.1	70	D9	45	I/O	TA2 CCR1 capture: CCI1A input, compare: Out1
	TA2.2	71	C9	46	I/O	TA2 CCR2 capture: CCI2A input, compare: Out2
	TA2.3	80	B8	49	I/O	TA2 CCR3 capture: CCI3A input, compare: Out3
	TA2.4	81	B7	50	I/O	TA2 CCR4 capture: CCI4A input, compare: Out4
	TA2CLK	58	G7	33	I	TA2 input clock
	TA3.0	24	N/A	N/A	I/O	TA3 CCR0 capture: CCI0A input, compare: Out0
	TA3.1	25	N/A	N/A	I/O	TA3 CCR1 capture: CCI1A input, compare: Out1
	TA3.2	46	N/A	N/A	I/O	TA3 CCR2 capture: CCI2A input, compare: Out2
	TA3.3	74	N/A	N/A	I/O	TA3 CCR3 capture: CCI3A input, compare: Out3
	TA3.4	75	N/A	N/A	I/O	TA3 CCR4 capture: CCI4A input, compare: Out4
	TA3CLK	47	N/A	N/A	I	TA3 input clock
UART	UCA0RXD	6	C4	3	I	Receive data – eUSCI_A0 UART mode
	UCA0TXD	7	D4	4	O	Transmit data – eUSCI_A0 UART mode
	UCA3RXD	98	N/A	N/A	I	Receive data – eUSCI_A3 UART mode
	UCA3TXD	99	N/A	N/A	O	Transmit data – eUSCI_A3 UART mode

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4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see Section 6.12.

4.5 Buffer Types

Table 4-3 describes the buffer types that are referenced in Table 4-1.

Table 4-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
Analog(1)	3.0 V	N	N/A	N/A	N/A	See analog modules in *Specifications* for details
HVCMOS	13.0 V	Y	N/A	N/A	See *Typical Characteristics*	
LVCMOS	3.0 V	Y(2)	Programmable	See *General-Purpose I/Os*	See *Typical Characteristics*	
Power (DVCC)(3)	3.0 V	N	N/A	N/A	N/A	SVSMH enables hysteresis on DVCC
Power (AVCC)(3)	3.0 V	N	N/A	N/A	N/A	
Power (DVSS and AVSS)(3)	0 V	N	N/A	N/A	N/A	

(1) This is a switch, not a buffer.
(2) Only for input pins
(3) This is supply input, not a buffer.

4.6 Connection for Unused Pins

Table 4-4 lists the correct termination of all unused pins.

Table 4-4. Connection for Unused Pins(1)

PIN	POTENTIAL	COMMENT
AVCC	DV_{CC}	
AVSS	DV_{SS}	
Px.0 to Px.7	Open	Set to port function, output direction, and leave unconnected on the PC board
RSTn/NMI	DV_{CC} or V_{CC}	47-kΩ pullup with 1.1-nF pulldown.
PJ.4/TDI	Open	The JTAG TDI pin is shared with general-purpose I/O function (PJ.4). If not being used, this pin should be set to port function, output direction. When used as JTAG TDI pin, it should remain open.
PJ.5/TDO/SWO	DV_{CC} or V_{CC}	The JTAG TDO/SWO pin is shared with general-purpose I/O function (PJ.5). If not being used, this pin should be set to port function, output direction. When used as JTAG TDO/SWO pin, it should be pulled down externally.
SWDIOTMS	DV_{CC} or V_{CC}	This pin should be pulled up externally.
SWCLKTCK	DV_{SS} or V_{SS}	This pin should be pulled down externally.

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 pins.

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3	4.17	V
Voltage difference between DVCC and AVCC pins(2)		±0.3	V
Voltage applied to any pin(3)	–0.3	V_{CC} + 0.3 V (4.17 V MAX)	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} (4)	–40	125	°C
Maximum junction temperature, T_J		95	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device.
(3) All voltages referenced to V_{SS}.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (2)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) All pins except DVSS3 pass HBM up to ±1000 V. The DVSS3 pin is used for TI internal test purposes. Connect the DVSS3 pin to supply ground on the customer application board.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical data are based on V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range at all DVCC and AVCC pins (1) (2) (3)	At power-up (with internal V_{CC} supervision)	1.71		3.7	V
		Normal operation with internal V_{CC} supervision	1.71		3.7	
		Normal operation without internal V_{CC} supervision	1.62		3.7	
V_{SS}	Supply voltage on all DVSS and AVSS pins			0		V
I_{INRUSH}	Inrush current into the V_{CC} pins(4)				100	mA
f_{MCLK}	Frequency of the CPU and AHB clock in the system(5)		0		48	MHz
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of ±0.1 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation. See Section 5.4 for decoupling capacitor recommendations.
(2) Supply voltage must not change faster than 1 V/ms. Faster changes can cause the VCCDET to trigger a reset even within the recommended supply voltage range.
(3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(4) Does not include I/O currents (driven by application requirements).
(5) Operating frequency may require the flash to be accessed with wait states. See Section 5.8 for further details.

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5.4 Recommended External Components(1) (2) (3)

			MIN	TYP	MAX	UNIT
C_{DVCC}	Capacitor on DVCC pin	For DC-DC operation(4)	3.3	4.7		µF
		For LDO-only operation	3.3	4.7		
C_{VCORE}	Capacitor on VCORE pin	For DC-DC operation, including capacitor tolerance	1.54	4.7	9	µF
		For LDO-only operation, including capacitor tolerance	70	100	9000	nF
C_{AVCC}	Capacitor on AVCC pin		3.3	4.7		µF
L_{VSW}	Inductor between VSW and VCORE pins for DC-DC		3.3	4.7	13	µH
$R_{LVSW-DCR}$	Allowed DCR for L_{VSW}			150	350	mΩ
$I_{SAT-LVSW}$	L_{VSW} saturation current		700			mA

(1) For optimum performance, select the component value to match the typical value given in the table.
(2) See the section on board guidelines for further details on component selection, placement as well as related PCB design guidelines.
(3) Tolerance of the capacitance and inductance values should be taken into account when choosing a component, to ensure that the MIN and MAX limits are never exceeded.
(4) C_{DVCC} should not be smaller than C_{VCORE}.

5.5 Operating Mode V_{CC} Ranges

over operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC_LDO} (1) (2)	AM_LDO_VCORE0 AM_LF_VCORE0 LPM0_LDO_VCORE0 LPM0_LF_VCORE0 LPM3_VCORE0 LPM4_VCORE0 LPM3.5 AM_LDO_VCORE1 AM_LF_VCORE1 LPM0_LDO_VCORE1 LPM0_LF_VCORE1 LPM3_VCORE1 LPM4_VCORE1	LDO active, SVSMH disabled	1.62	3.7	V
		LDO active, SVSMH enabled	1.71	3.7	
$V_{CC_DCDC_DF0}$	AM_DCDC_VCORE0 LPM0_DCDC_VCORE0 AM_DCDC_VCORE1 LPM0_DCDC_VCORE1	DC-DC active, DC-DC operation not forced (DCDC_FORCE = 0), SVSMH enabled or disabled(3)	2.0	3.7	V
$V_{CC_DCDC_DF1}$	AM_DCDC_VCORE0 LPM0_DCDC_VCORE0 AM_DCDC_VCORE1 LPM0_DCDC_VCORE1	DC-DC active, DC-DC operation forced (DCDC_FORCE = 1), SVSMH enabled or disabled	1.8	3.7	V
$V_{CC_VCORE_OFF}$ (4)	LPM4.5	LDO disabled, SVSMH disabled	1.62	3.7	V
		LDO disabled, SVSMH enabled	1.71	3.7	

(1) Flash remains active **only** in active modes and LPM0 modes.
(2) Low-frequency active, low-frequency LPM0, LPM3, LPM4, and LPM3.5 modes are based on LDO **only**.
(3) When V_{CC} falls below the specified MIN value, the DC-DC operation switches to LDO automatically, as long as the V_{CC} drop is slower than the rate that is reliably detected. See Table 5-19 for more details.
(4) Core voltage is off in LPM4.5 mode.

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5.6 Operating Mode CPU Frequency Ranges(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	f_{MCLK}		UNIT
			MIN	MAX	
$f_{AM_LDO_VCORE0}$	AM_LDO_VCORE0	Normal performance mode with LDO as the active regulator	0	24	MHz
$f_{AM_LDO_VCORE1}$	AM_LDO_VCORE1	High performance mode with LDO as the active regulator	0	48	MHz
$f_{AM_DCDC_VCORE0}$	AM_DCDC_VCORE0	Normal performance mode with DC-DC as the active regulator	0	24	MHz
$f_{AM_DCDC_VCORE1}$	AM_DCDC_VCORE1	High performance mode with DC-DC as the active regulator	0	48	MHz
$f_{AM_LF_VCORE0}$	AM_LF_VCORE0	Low-frequency mode with LDO as the active regulator	0	128	kHz
$f_{AM_LF_VCORE1}$	AM_LF_VCORE1	Low-frequency mode with LDO as the active regulator	0	128	kHz

(1) DMA can be operated at the same frequency as CPU.

5.7 Operating Mode Peripheral Frequency Ranges

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	MIN	MAX	UNIT
$f_{AM_LPM0_VCORE0}$	AM_LDO_VCORE0	Peripheral frequency range in LDO or DC-DC based active or LPM0 modes for VCORE0	0	12	MHz
	AM_DCDC_VCORE0				
	LPM0_LDO_VCORE0				
	LPM0_DCDC_VCORE0				
$f_{AM_LPM0_VCORE1}$	AM_LDO_VCORE1	Peripheral frequency range in LDO or DC-DC based active or LPM0 modes for VCORE1	0	24	MHz
	AM_DCDC_VCORE1				
	LPM0_LDO_VCORE1				
	LPM0_DCDC_VCORE1				
$f_{AM_LPM0_LF}$	AM_LF_VCORE0	Peripheral frequency range in low-frequency active or low frequency LPM0 modes for VCORE0 and VCORE1	0	128	kHz
	AM_LF_VCORE1				
	LPM0_LF_VCORE0				
	LPM0_LF_VCORE1				
f_{LPM3}(1)	LPM3_VCORE0	Peripheral frequency in LPM3 mode for VCORE0 and VCORE1	0	32.768	kHz
	LPM3_VCORE1				
$f_{LPM3.5}$(1)	LPM3.5	Peripheral frequency in LPM3.5 mode	0	32.768	kHz

(1) Only RTC and WDT can be active.

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5.8 Operating Mode Execution Frequency vs Flash Wait-State Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	NUMBER OF FLASH WAIT STATES	FLASH READ MODE	MAXIMUM SUPPORTED MCLK FREQUENCY (1) (2)		UNIT
			AM_LDO_VCORE0, AM_DCDC_VCORE0	AM_LDO_VCORE1, AM_DCDC_VCORE1	
$f_{MAX_NRM_FLWAIT0}$	0	Normal read mode	16	24	MHz
$f_{MAX_NRM_FLWAIT1}$	1	Normal read mode	24	48	MHz
$f_{MAX_ORM_FLWAIT0}$	0	Other read modes (3)	8	12	MHz
$f_{MAX_ORM_FLWAIT1}$	1	Other read modes (3)	16	24	MHz
$f_{MAX_ORM_FLWAIT2}$	2	Other read modes (3)	24	36	MHz
$f_{MAX_ORM_FLWAIT3}$	3	Other read modes (3)	24	48	MHz

(1) Violation of the maximum frequency limitation for a given wait-state configuration results in nondeterministic data or instruction fetches from the flash memory.
(2) In low-frequency active modes, the flash can always be accessed with zero wait states, because the maximum MCLK frequency is limited to 128 kHz.
(3) Other read modes refers to Read Margin 0, Read Margin 1, Program Verify, and Erase Verify.

5.9 Current Consumption During Device Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (2) (3)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
I_{RESET}	Current during device reset	2.2 V		510		µA
		3.0 V		600	850	

(1) Device held in reset through RSTn/NMI pin.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.

5.10 Current Consumption in LDO-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM_LDO_VCORE0,Flash}$ (6) (7) (8)	Flash	3.0 V	490	625	1500	1700	2650	2950	3580	3900							µA
$I_{AM_LDO_VCORE1,Flash}$ (6) (7) (8)	Flash	3.0 V	510	685	1650	1900	2970	3300	4260	4700	5300	5800	6500	7100	7700	8400	µA
$I_{AM_LDO_VCORE0,SRAM}$ (9)	SRAM	3.0 V	435	565	1070	1240	1800	2010	2530	2800							µA
$I_{AM_LDO_VCORE1,SRAM}$ (9)	SRAM	3.0 V	450	620	1160	1370	1980	2250	2800	3120	3650	4020	4470	4900	5280	5760	µA

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) All SRAM banks kept active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 program. Code execution from flash. Stack and data in SRAM.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Flash instruction and data buffers are enabled (BUFI = BUFD = 1).
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

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5.11 Current Consumption in DC-DC-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM_DCDC_VCORE0,Flash}$ (6) (7) (8)	Flash	3.0 V	400	475	925	1050	1530	1720	2060	2300							µA
$I_{AM_DCDC_VCORE1,Flash}$ (6) (7) (8)	Flash	3.0 V	430	550	1100	1280	1880	2140	2650	3000	3290	3700	4020	4500	4720	5300	µA
$I_{AM_DCDC_VCORE0,SRAM}$ (9)	SRAM	3.0 V	370	450	680	780	1040	1180	1410	1600							µA
$I_{AM_DCDC_VCORE1,SRAM}$ (9)	SRAM	3.0 V	390	510	790	940	1250	1440	1720	1960	2200	2480	2670	3000	3050	3420	µA

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) All SRAM banks are active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 program. Code execution from flash. Stack and data in SRAM.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Flash instruction and data buffers are enabled (BUFI = BUFD = 1).
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

5.12 Current Consumption in Low-Frequency Active Modes – Dhrystone 2.1 Program

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

PARAMETER	EXECUTION MEMORY	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM_LF_VCORE0,\ Flash}$ (6) (7) (8)	Flash	2.2 V	75		80		95		115		µA
		3.0 V	78		83	100	98		118	200	
$I_{AM_LF_VCORE1,\ Flash}$ (6) (7) (8)	Flash	2.2 V	78		85		105		125		µA
		3.0 V	81		88	110	108		128	245	
$I_{AM_LF_VCORE0,\ SRAM}$ (9)	SRAM	2.2 V	68		73		90		105		µA
		3.0 V	71		76	92	93		108	190	
$I_{AM_LF_VCORE1,\ SRAM}$ (9)	SRAM	2.2 V	70		77		98		117		µA
		3.0 V	73		90	102	101		120	235	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) MCLK, HSMCLK, and SMCLK sourced by REFO at 128 kHz
(4) All peripherals are inactive.
(5) SRAM banks 0 and 1 enabled for execution from flash, and SRAM banks 0 to 3 enabled for execution from SRAM.
(6) Flash configured to 0 wait states.
(7) Device executing the Dhrystone 2.1 program. Code execution from flash. Stack and data in SRAM.
(8) Flash instruction and data buffers are enabled (BUFI = BUFD = 1).
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

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5.13 Typical Characteristics of Active Mode Currents for CoreMark Program

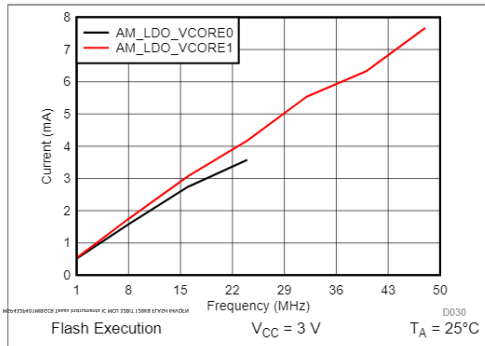


Figure 5-1. Frequency vs Current Consumption

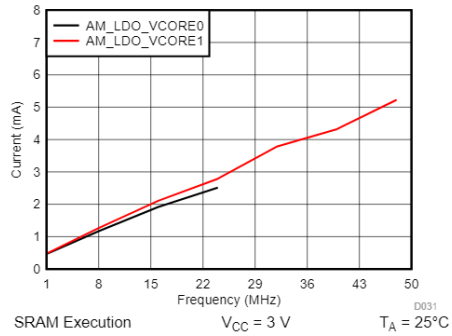


Figure 5-2. Frequency vs Current Consumption

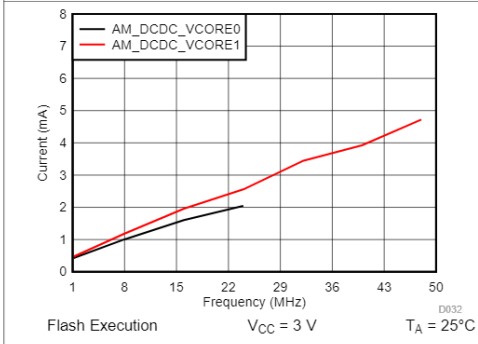


Figure 5-3. Frequency vs Current Consumption

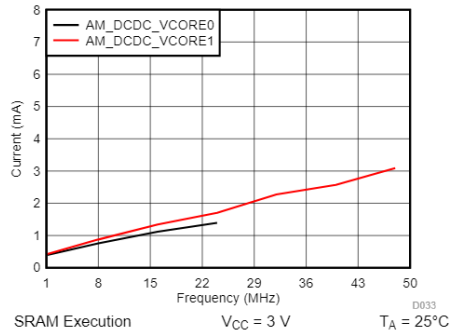


Figure 5-4. Frequency vs Current Consumption

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5.14 Typical Characteristics of Active Mode Currents for Prime Number Program

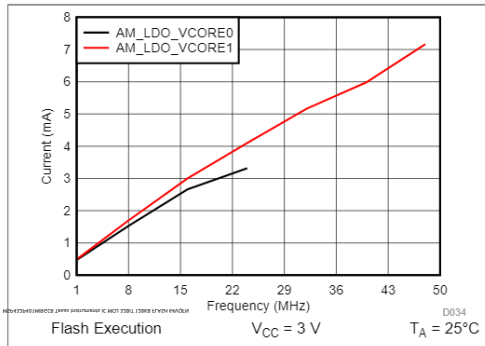


Figure 5-5. Frequency vs Current Consumption

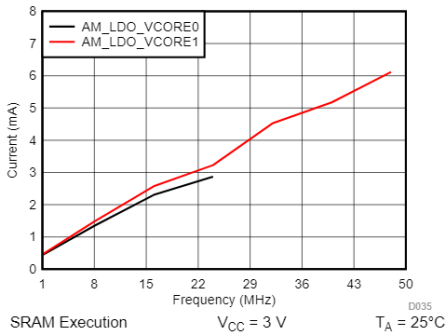


Figure 5-6. Frequency vs Current Consumption

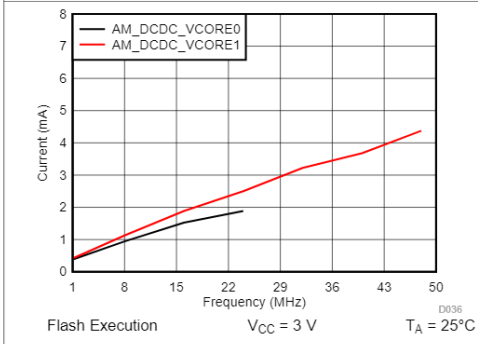


Figure 5-7. Frequency vs Current Consumption

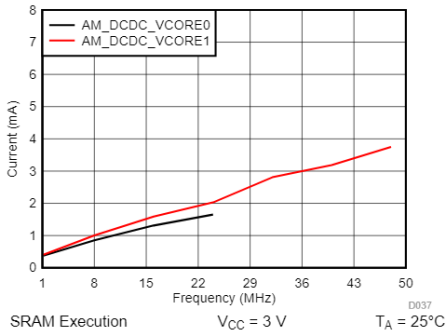


Figure 5-8. Frequency vs Current Consumption

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5.15 Typical Characteristics of Active Mode Currents for Fibonacci Program

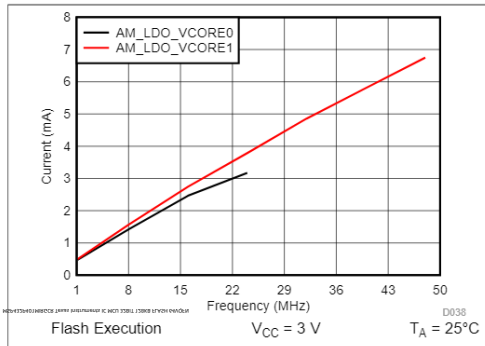


Figure 5-9. Frequency vs Current Consumption

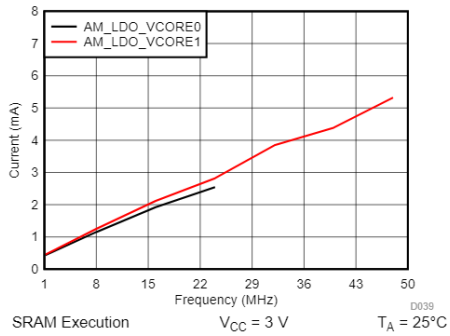


Figure 5-10. Frequency vs Current Consumption

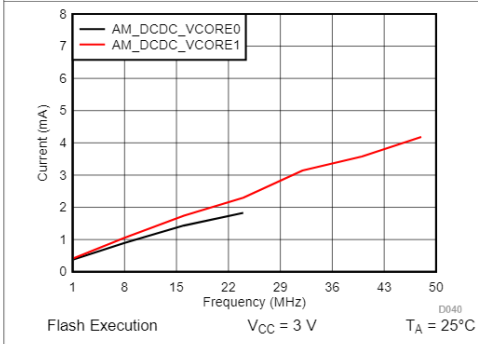


Figure 5-11. Frequency vs Current Consumption

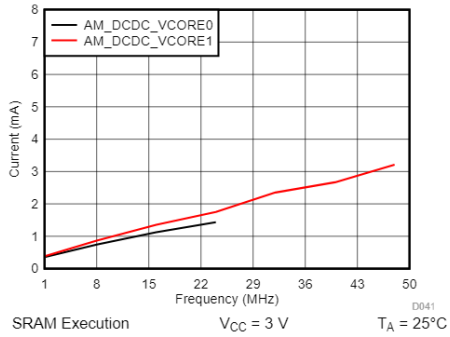


Figure 5-12. Frequency vs Current Consumption

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5.16 Typical Characteristics of Active Mode Currents for While(1) Program

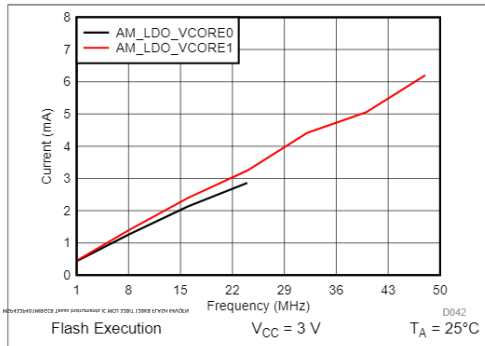


Figure 5-13. Frequency vs Current Consumption

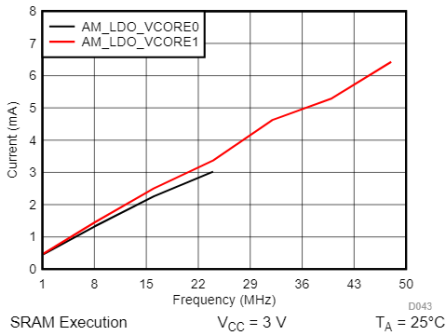


Figure 5-14. Frequency vs Current Consumption

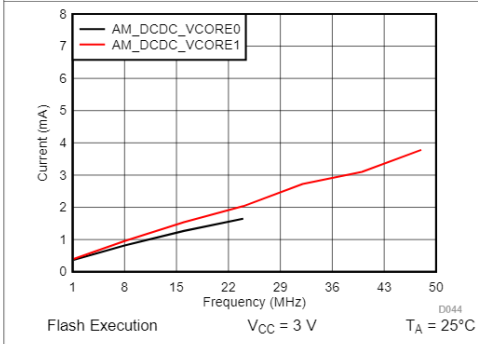


Figure 5-15. Frequency vs Current Consumption

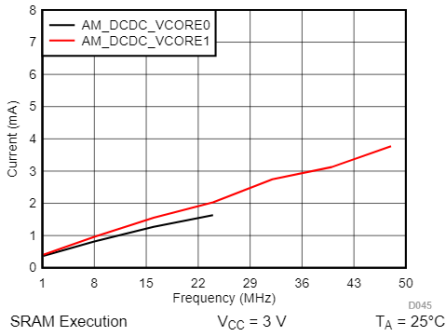


Figure 5-16. Frequency vs Current Consumption

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5.17 Typical Characteristics of Low-Frequency Active Mode Currents for CoreMark Program

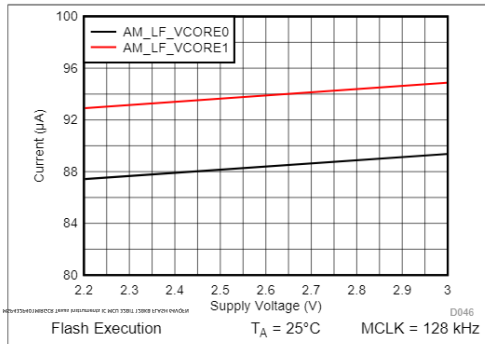


Figure 5-17. Supply Voltage vs Current Consumption

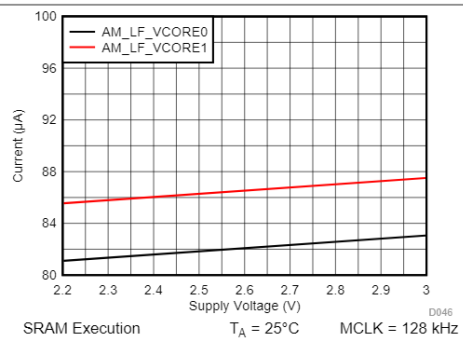


Figure 5-18. Supply Voltage vs Current Consumption

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5.18 Current Consumption in LDO-Based LPM0 Modes

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0_LDO_VCORE0}$	2.2 V	355	485	465	605	590	735	710	860							µA
	3.0 V	355	485	465	605	590	735	710	860							
$I_{LPM0_LDO_VCORE1}$	2.2 V	365	530	495	665	640	820	775	970	965	1160	1130	1330	1235	1450	µA
	3.0 V	365	530	495	665	640	820	775	970	965	1160	1130	1330	1230	1450	

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) CPU is off. Flash and SRAM not accessed.
(5) All SRAM banks are active.
(6) All peripherals are inactive.

5.19 Current Consumption in DC-DC-Based LPM0 Modes

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0_DCDC_VCORE0}$	2.2 V	330	425	400	510	485	600	570	690							µA
	3.0 V	325	400	380	460	440	530	510	610							
$I_{LPM0_DCDC_VCORE1}$	2.2 V	350	485	445	590	555	710	660	820	810	970	935	1110	1020	1200	µA
	3.0 V	345	450	420	530	500	620	585	720	700	830	800	940	870	1020	

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) CPU is off. Flash and SRAM not accessed.
(5) All SRAM banks are active.
(6) All peripherals are inactive.

5.20 Current Consumption in Low-Frequency LPM0 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0_LF_VCORE0}$	2.2 V	58		63		78		94		µA
	3.0 V	61		66	82	81		97	180	
$I_{LPM0_LF_VCORE1}$	2.2 V	60		66		84		104		µA
	3.0 V	63		69	90	87		107	220	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) MCLK, HSMCLK, and SMCLK sourced by REFO at 128 kHz.
(4) All peripherals are inactive.
(5) Bank 0 of SRAM kept active. Rest of the banks are powered down.
(6) CPU is off. Flash and SRAM not accessed.

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5.21 Current Consumption in LPM3, LPM4 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3_VCORE0_RTCLF}$ (7) (8)	2.2 V	0.52		0.64		1.11		2.43		µA
	3.0 V	0.54		0.66	0.85	1.13		2.46	5	
$I_{LPM3_VCORE0_RTCREFO}$ (9) (8)	2.2 V	0.85		1.07		1.55		2.89		µA
	3.0 V	0.95		1.16	1.35	1.64		2.98	5.6	
$I_{LPM3_VCORE1_RTCLF}$ (7) (8)	2.2 V	0.72		0.93		1.47		2.95		µA
	3.0 V	0.75		0.95	1.35	1.5		2.98	6	
$I_{LPM3_VCORE1_RTCREFO}$ (9) (8)	2.2 V	1.04		1.3		1.87		3.34		µA
	3.0 V	1.14		1.4	1.7	1.96		3.44	6.5	
I_{LPM4_VCORE0} (10)	2.2 V	0.37		0.48		0.92		2.19		µA
	3.0 V	0.4		0.5	0.65	0.94		2.2	4.8	
I_{LPM4_VCORE1} (10)	2.2 V	0.54		0.7		1.2		2.58		µA
	3.0 V	0.56		0.72	0.98	1.23		2.6	5.6	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) CPU is off, and flash is powered down.
(4) Bank 0 of SRAM retained, all other banks are powered down.
(5) See Table 5-47 for details on additional current consumed for each extra Bank that is enabled for retention.
(6) SVSMH is disabled.
(7) RTC sourced by LFXT. Effective load capacitance of LF crystal is 3.7 pF.
(8) WDT module is disabled.
(9) RTC sourced by REFO.
(10) RTC and WDT modules disabled.

5.22 Current Consumption in LPM3.5, LPM4.5 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5_RTCLF}$ (3) (4) (5) (6) (7)	2.2 V	0.48		0.6		1.07		2.36		µA
	3.0 V	0.5		0.63	0.81	1.1		2.38	4.9	
$I_{LPM3.5_RTCREFO}$ (3) (4) (8) (6) (7)	2.2 V	0.82		1.03		1.52		2.81		µA
	3.0 V	0.92		1.12	1.3	1.61		2.9	5.5	
$I_{LPM4.5}$ (9) (7)	2.2 V	10		20		45		125		nA
	3.0 V	15		25	35	50		150	300	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) CPU and flash are powered down.
(4) Bank 0 of SRAM retained, all other banks powered down.
(5) RTC sourced by LFXT. Effective load capacitance of LF crystal is 3.7 pF.
(6) WDT module is disabled.
(7) SVSMH is disabled.
(8) RTC sourced by REFO.
(9) No core voltage. CPU, flash, and all banks of SRAM are powered down.

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5.23 Current Consumption of Digital Peripherals

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
I_{TIMER_A}	Timer_A configured as PWM timer with 50% duty cycle	5		µA/MHz
$I_{TIMER32}$	Timer32 enabled	3.5		µA/MHz
I_{UART}	eUSCI_A configured in UART mode	6.5		µA/MHz
I_{SPI}	eUSCI_A configured in SPI master mode	5		µA/MHz
I_{I2C}	eUSCI_B configured in I^2C master mode	5		µA/MHz
I_{WDT_A}	WDT_A configured in interval timer mode	6		µA/MHz
I_{RTC_C}	RTC_C enabled and sourced from 32-kHz LFXT	100		nA
I_{AES256}	AES256 active	19		µA/MHz
I_{CRC32}	CRC32 active	2		µA/MHz

(1) Measured with VCORE = 1.2 V

5.24 Thermal Resistance Characteristics

THERMAL METRICS(1)		PACKAGE	VALUE(2)	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air(3)	LQFP-100 (PZ)	50.9	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(4)		9.7	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance(5)		27.2	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		26.9	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.2	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(6)		N/A	°C/W
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air(3)	NFBGA-80 (ZXH)	58.1	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(4)		26.1	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance(5)		22.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		22.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.5	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(6)		N/A	°C/W
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air(3)	VQFN-64 (RGC)	29.4	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(4)		14.8	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance(5)		8.3	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		8.2	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.2	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(6)		1.0	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) N/A = not applicable
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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5.25 Timing and Switching Characteristics

5.25.1 Reset Timing

Table 5-1 lists the latencies to recover from different types of resets.

Table 5-1. Reset Recovery Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

	PARAMETER	MIN	TYP	MAX	UNIT
t_{SOFT}	Latency from release of soft reset to first CPU instruction fetch		5		MCLK cycles
t_{HARD}	Latency from release of hard reset to release of soft reset		25		MCLK cycles
t_{POR}	Latency from release of device POR to release of hard reset		15	25	µs
$t_{COLDPWR,100\ nF}$	Latency from a cold power-up condition to release of device POR, C_{VCORE} = 100 nF		300	400	µs
$t_{COLDPWR,4.7\ µF}$	Latency from a cold power-up condition to release of device POR, C_{VCORE} = 4.7 µF		400	500	µs

(1) See Section 6.8.1 for details on the various classes of resets on the device

Table 5-2 lists the latencies to recover from an external reset applied on RSTn pin.

Table 5-2. External Reset Recovery Latencies (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{AM_RSTn}	External reset applied when device is in LDO or DC-DC based active modes, MCLK = 1 to 48 MHz		5	ms
$t_{AMLF_RSTn,\ 128\ kHz}$	External reset applied when device is in low-frequency active modes, MCLK = 128 kHz		5.5	ms
$t_{AMLF_RSTn,\ 32\ kHz}$	External reset applied when device is in low-frequency active modes, MCLK = 32.768 kHz		6.5	ms
t_{LPM0_RSTn}	External reset applied when device is in LDO or DC-DC based LPM0 modes, MCLK = 1 to 48 MHz		5	ms
$t_{LPM0LF_RSTn,\ 128\ kHz}$	External reset applied when device is in low-frequency LPM0 modes, MCLK = 128 kHz		5.5	ms
$t_{LPM0LF_RSTn,\ 32\ kHz}$	External reset applied when device is in low-frequency LPM0 modes, MCLK = 32.768 kHz		6.5	ms
$t_{LPM3_LPM4_RSTn}$	External reset applied when device is in LPM3 or LPM4 modes, MCLK = 24 or 48 MHz while entering LPM3 or LPM4 modes		5	ms
$t_{LPMx.5_RSTn}$	External reset applied when device is in LPM3.5 or LPM4.5 modes		5	ms

(1) External reset is applied on RSTn pin, and the latency is measured from release of external reset to start of user application code.

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5.25.2 Mode Transition Timing

Table 5-3 lists the latencies required to change between different active modes.

Table 5-3. Active Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
t_{OFF_AMLDO0}	Power Off	AM_LDO_VCORE0	From V_{CC} reaching 1.71 V to start of user application code		6	ms
t_{AMLDO0_AMLDO1}	AM_LDO_VCORE0	AM_LDO_VCORE1	Transition from AM_LDO_VCORE0 to AM_LDO_VCORE1 MCLK frequency = 24 MHz	300	350	µs
t_{AMLDO1_AMLDO0}	AM_LDO_VCORE1	AM_LDO_VCORE0	Transition from AM_LDO_VCORE1 to AM_LDO_VCORE0 MCLK frequency = 24 MHz	4	5	µs
$t_{AMLDO0_AMDCDC0}$	AM_LDO_VCORE0	AM_DCDC_VCORE0	Transition from AM_LDO_VCORE0 to AM_DCDC_VCORE0 MCLK frequency = 24 MHz	20	30	µs
$t_{AMDCDC0_AMLDO0}$	AM_DCDC_VCORE0	AM_LDO_VCORE0	Transition from AM_DCDC_VCORE0 to AM_LDO_VCORE0 MCLK frequency = 24 MHz	10	15	µs
$t_{AMLDO1_AMDCDC1}$	AM_LDO_VCORE1	AM_DCDC_VCORE1	Transition from AM_LDO_VCORE1 to AM_DCDC_VCORE1 MCLK frequency = 48 MHz	20	30	µs
$t_{AMDCDC1_AMLDO1}$	AM_DCDC_VCORE1	AM_LDO_VCORE1	Transition from AM_DCDC_VCORE1 to AM_LDO_VCORE1 MCLK frequency = 48 MHz	10	15	µs
t_{AMLDO0_AMLF0}	AM_LDO_VCORE0	AM_LF_VCORE0	Transition from AM_LDO_VCORE0 to AM_LF_VCORE0 SELM = 2, REFO frequency = 128 kHz	90	100	µs
t_{AMLF0_AMLDO0}	AM_LF_VCORE0	AM_LDO_VCORE0	Transition from AM_LF_VCORE0 to AM_LDO_VCORE0 SELM = 2, REFO frequency = 128 kHz	50	60	µs
t_{AMLDO1_AMLF1}	AM_LDO_VCORE1	AM_LF_VCORE1	Transition from AM_LDO_VCORE1 to AM_LF_VCORE1 SELM = 2, REFO frequency = 128 kHz	90	100	µs
t_{AMLF1_AMLDO1}	AM_LF_VCORE1	AM_LDO_VCORE1	Transition from AM_LF_VCORE1 to AM_LDO_VCORE1 SELM = 2, REFO frequency = 128 kHz	50	60	µs

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Table 5-4 lists the latencies required to change between different active and LPM0 modes.

Table 5-4. LPM0 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
$t_{AMLDOx_LPM0LDOx}$ (1)	AM_LDO_VCOREx	LPM0_LDO_VCOREx	Transition from AM_LDO_VCORE0 or AM_LDO_VCORE1 to LPM0_LDO_VCORE0 or LPM0_LDO_VCORE1	1		MCLK cycles
$t_{LPM0LDOx_AMLDOx}$ (2)	LPM0_LDO_VCOREx	AM_LDO_VCOREx	Transition from LPM0_LDO_VCORE0 or LPM0_LDO_VCORE1 to AM_LDO_VCORE0 or AM_LDO_VCORE1 through I/O interrupt	3	4	MCLK cycles
$t_{AMDCDCx_LPM0DCDCx}$ (1)	AM_DCDC_VCOREx	LPM0_DCDC_VCOREx	Transition from AM_DCDC_VCORE0 or AM_DCDC_VCORE1 to LPM0_DCDC_VCORE0 or LPM0_DCDC_VCORE1	1		MCLK cycles
$t_{LPM0DCDCx_AMDCDCx}$ (2)	LPM0_DCDC_VCOREx	AM_DCDC_VCOREx	Transition from LPM0_DCDC_VCORE0 or LPM0_DCDC_VCORE1 to AM_DCDC_VCORE0 or AM_DCDC_VCORE1 through I/O interrupt	3	4	MCLK cycles
$t_{AMLFx_LPM0LFx}$ (1)	AM_LF_VCOREx	LPM0_LF_VCOREx	Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM0_LF_VCORE0 or LPM0_LF_VCORE1	1		MCLK cycles
$t_{LPM0LFx_AMLFx}$ (2)	LPM0_LF_VCOREx	AM_LF_VCOREx	Transition from LPM0_LF_VCORE0 or LPM0_LF_VCORE1 to AM_LF_VCORE0 or AM_LF_VCORE1 through I/O interrupt	3	4	MCLK cycles

(1) This is the latency between execution of WFI instruction by CPU to assertion of SLEEPING signal at CPU output.
(2) This is the latency between I/O interrupt event to deassertion of SLEEPING signal at CPU output.

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Table 5-5 lists the latencies required to change between different active modes and LPM3 or LPM4 modes.

Table 5-5. LPM3, LPM4 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS		TYP	MAX	UNIT
t_{AMLDO0_LPMx0} (1)	AM_LDO_VCORE0	LPM3_LPM4_VCORE0	Transition from AM_LDO_VCORE0 to LPM3 or LPM4 at VCORE0	SELM = 3. DCO frequency = 24 MHz	22	24	µs
$t_{LPMx0_AMLDO0_NORIO}$ (2)	LPM3_LPM4_VCORE0	AM_LDO_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from nonglitch filter type I/O	SELM = 3. DCO frequency = 24 MHz	8	9	µs
$t_{LPMx0_AMLDO0_GFLTIO}$ (2)	LPM3_LPM4_VCORE0	AM_LDO_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1	SELM = 3. DCO frequency = 24 MHz	9	10	µs
t_{AMLDO1_LPMx1} (1)	AM_LDO_VCORE1	LPM3_LPM4_VCORE1	Transition from AM_LDO_VCORE1 to LPM3 or LPM4 at VCORE1	SELM = 3. DCO frequency = 48 MHz	21	23	µs
$t_{LPMx1_AMLDO1_NORIO}$ (2)	LPM3_LPM4_VCORE1	AM_LDO_VCORE1	Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from nonglitch filter type I/O	SELM = 3. DCO frequency = 48 MHz	7.5	8	µs
$t_{LPMx1_AMLDO1_GFLTIO}$ (2)	LPM3_LPM4_VCORE1	AM_LDO_VCORE1	Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1	SELM = 3. DCO frequency = 48 MHz	8	9	µs
$t_{AMLFx_LPMx_128k}$ (1)	AM_LF_VCOREx	LPM3_LPM4_VCOREx	Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM3 or LPM4 at VCORE0/1	SELM = 2. REFO frequency = 128 kHz	240	260	µs
$t_{AMLFx_LPMx_32k}$ (1)	AM_LF_VCOREx	LPM3_LPM4_VCOREx	Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM3 or LPM4 at VCORE0/1	SELM = 0. LFXT frequency = 32.768 kHz	880	900	µs
$t_{LPMx_AMLFx_NORIO_128k}$ (2)	LPM3_LPM4_VCOREx	AM_LF_VCOREx	Transition from LPM3 or LPM4 at VCORE0/1 to AM_LF_VCORE0 or AM_LF_VCORE1 through wake-up event from nonglitch filter type I/O	SELM = 2. REFO frequency = 128 kHz	45	50	µs
$t_{LPMx_AMLFx_NORIO_32k}$ (2)	LPM3_LPM4_VCOREx	AM_LF_VCOREx	Transition from LPM3 or LPM4 at VCORE0/1 to AM_LF_VCORE0 or AM_LF_VCORE1 through wake-up event from nonglitch filter type I/O	SELM = 0. LFXT frequency = 32.768 kHz	150	170	µs

(1) This is the latency from WFI instruction execution by CPU to LPM3 or LPM4 entry.
(2) This is the latency from I/O wake-up event to MCLK clock start at device pin.

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Table 5-6 lists the latencies required to change to and from LPM3.5 and LPM4.5 modes.

Table 5-6. LPM3.5, LPM4.5 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
$t_{AMLDOx_LPM3.5}$ (1)	AM_LDO_VCOREx	LPM3.5	Transition from AM_LDO_VCORE0 or AM_LDO_VCORE1 to LPM3.5	25	30	µs
$t_{AMDCDCx_LPM3.5}$ (1)	AM_DCDC_VCOREx	LPM3.5	Transition from AM_DCDC_VCORE0 or AM_DCDC_VCORE1 to LPM3.5	35	50	µs
$t_{AMLFx_LPM3.5}$ (1)	AM_LF_VCOREx	LPM3.5	Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM3.5	225	250	µs
$t_{AMLDOx_LPM4.5}$ (2)	AM_LDO_VCOREx	LPM4.5	Transition from AM_LDO_VCORE0 or AM_LDO_VCORE1 to LPM4.5	25	30	µs
$t_{AMDCDCx_LPM4.5}$ (2)	AM_DCDC_VCOREx	LPM4.5	Transition from AM_DCDC_VCORE0 or AM_DCDC_VCORE1 to LPM4.5	35	50	µs
$t_{AMLFx_LPM4.5}$ (2)	AM_LF_VCOREx	LPM4.5	Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM4.5	250	270	µs
$t_{LPM3.5_AMLDO0}$ (3)	LPM3.5	AM_LDO_VCORE0	Transition from LPM3.5 to AM_LDO_VCORE0	0.7	0.8	ms
$t_{LPM4.5_AMLDO0_SVSMON,\ 100\ nF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, C_{VCORE} = 100 nF	0.8	0.9	ms
$t_{LPM4.5_AMLDO0_SVSMON,\ 4.7\ µF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, C_{VCORE} = 4.7 µF	0.9	1	ms
$t_{LPM4.5_AMLDO0_SVSMOFF,\ 100\ nF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, C_{VCORE} = 100 nF	1	1.1	ms
$t_{LPM4.5_AMLDO0_SVSMOFF,\ 4.7\ µF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, C_{VCORE} = 4.7 µF	1.1	1.2	ms

(1) This is the latency from WFI instruction execution by CPU to LPM3.5 mode entry.
(2) This is the latency from WFI instruction execution by CPU to LPM4.5 mode entry.
(3) This is the latency from I/O wake-up event to start of user application code.

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5.25.3 Clock Specifications

Table 5-7 lists the input requirement for the low-frequency crystal oscillator, LFXT.

Table 5-7. Low-Frequency Crystal Oscillator, LFXT, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR	Crystal equivalent series resistance	f_{OSC} = 32.768 kHz	16	40	65	kΩ
C_{LFXT}	Capacitance from LFXT input to ground and from LFXT output to ground(1)		7.4	12	24	pF
C_{SHUNT}	Crystal shunt capacitance		0.6	0.8	1.6	pF
C_m	Crystal motional capacitance		1	2	10	fF

(1) Does not include board parasitics. Package and board add additional capacitance to C_{LFXT}.

Table 5-8 lists the characteristics of the low-frequency crystal oscillator, LFXT.

Table 5-8. Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC,LFXT}$	Current consumption(1)	f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF, Typical ESR and C_{SHUNT}	3.0 V		100		nA
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF, Typical ESR and C_{SHUNT}			120		
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {2}, $C_{L,eff}$ = 9 pF, Typical ESR and C_{SHUNT}			150		
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF, Typical ESR and C_{SHUNT}			170		
f_{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0(2)			32.768		kHz
DC_{LFXT}	LFXT oscillator duty cycle	f_{LFXT} = 32.768 kHz(2)		30%		70%	
$f_{LFXT,SW}$	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1(3) (4)		10	32.768	50	kHz
$DC_{LFXT,SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%		70%	
OA_{LFXT}	Oscillation allowance for LF crystals(5)	LFXTBYPASS = 0, LFXTDRIVE = {1}, f_{LFXT} = 32.768 kHz, $C_{L,eff}$ = 6 pF		200	240		kΩ
		LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32.768 kHz, $C_{L,eff}$ = 12 pF		300	340		

(1) Total current measured on both AVCC and DVCC supplies.
(2) Measured at ACLK pin.
(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT,SW}$.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF.
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF.
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF.
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF.

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Low-Frequency Crystal Oscillator, LFXT *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{LFXIN}	Integrated load capacitance at LFXIN terminal(6) (7)				2		pF
C_{LFXOUT}	Integrated load capacitance at LFXOUT terminal(6) (7)				2		pF
$t_{START,LFXT}$	Start-up time(8)	f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF, Typical ESR and C_{SHUNT}, FCNTLF_EN = 0(2)	3.0 V		1.1		s
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF, Typical ESR and C_{SHUNT}, FCNTLF_EN = 0(2)			1.3		
$f_{Fault,LFXT}$	Oscillator fault frequency(9) (10)			1		3	kHz

(6) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, CL,eff can be computed as CIN x COUT / (CIN + COUT), where CIN and COUT are the total capacitance at the LFXIN and LFXOUT terminals, respectively.
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF. Because the PCB adds additional capacitance, it must also be considered in the overall capacitance. TI recommends verifying that the recommended effective load capacitance of the selected crystal is met.
(8) Does not include programmable start-up counter.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition will set the fault flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-9 lists the input requirements for the high-frequency crystal oscillator, HFXT.

Table 5-9. High-Frequency Crystal Oscillator, HFXT, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR	Crystal equivalent series resistance	f_{OSC} = 1 MHz to ≤4 MHz		75	150	Ω
		f_{OSC} = >4 MHz to ≤8 MHz		75	150	
		f_{OSC} = >8 MHz to ≤16 MHz		40	80	
		f_{OSC} = >16 MHz to ≤24 MHz		30	60	
		f_{OSC} = >24 MHz to ≤32 MHz		20	40	
		f_{OSC} = >32 MHz to ≤48 MHz		15	30	
C_{HFXT}	Capacitance from HFXT input to ground and from HFXT output to ground	f_{OSC} = 1 MHz to 48 MHz	28	32	36	pF
C_{SHUNT}	Crystal shunt capacitance	f_{OSC} = 1 MHz to 48 MHz	1	3	7	pF
C_m	Crystal motional capacitance	f_{OSC} = 1 MHz to 48 MHz	3	7	30	fF

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Table 5-10 lists the characteristics of the high-frequency crystal oscillator, HFXT.

Table 5-10. High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC,HFXT}$	HFXT oscillator crystal current HF mode at typical ESR	f_{OSC} = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}	3.0 V		40		µA
		f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}			60		
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}			100		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}			180		
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}			260		
		f_{OSC} = 32 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}			320		
		f_{OSC} = 40 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}			480		
		f_{OSC} = 48 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}			550		
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 0 (1)		1		4	MHz
		HFXTBYPASS = 0, HFFREQ = 1 (1)		4.01		8	
		HFXTBYPASS = 0, HFFREQ = 2 (1)		8.01		16	
		HFXTBYPASS = 0, HFFREQ = 3 (1)		16.01		24	
		HFXTBYPASS = 0, HFFREQ = 4 (1)		24.01		32	
		HFXTBYPASS = 0, HFFREQ = 5 (1)		32.01		40	
		HFXTBYPASS = 0, HFFREQ = 6 (1)		40.01		48	
DC_{HFXT}	HFXT oscillator duty cycle	Measured at MCLK or HSMCLK, f_{HFXT} = 1 MHz to 48 MHz		40%	50%	60%	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1 (1)(2)		0.8		48	MHz
$DC_{HFXT, SW}$	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1, External clock used as a direct source to MCLK or HSMCLK with no divider (DIVM = 0 or DIVHS = 0).		45%		55%	
		HFXTBYPASS = 1, External clock used as a direct source to MCLK or HSMCLK with divider (DIVM > 0 or DIVHS > 0) or not used as a direct source to MCLK or HSMCLK.		40%		60%	

(1) Maximum frequency of operation of the entire device cannot be exceeded.
(2) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{HFXT, SW}$.

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High-Frequency Crystal Oscillator, HFXT *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
OA_{HFXT}	Oscillation allowance for HFXT crystals[3]	HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $f_{HFXT,HF}$ = 1 MHz, $C_{L,eff}$ = 16 pF		1225	5000		Ω
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $f_{HFXT,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF		640	1250		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $f_{HFXT,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF		360	750		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $f_{HFXT,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF		200	425		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $f_{HFXT,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF		135	275		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4, $f_{HFXT,HF}$ = 32 MHz, $C_{L,eff}$ = 16 pF		110	225		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5 $f_{HFXT,HF}$ = 40 MHz, $C_{L,eff}$ = 16 pF		105	160		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6, $f_{HFXT,HF}$ = 48 MHz, $C_{L,eff}$ = 16 pF		80	140		

(3) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

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High-Frequency Crystal Oscillator, HFXT *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{START,HFXT}$	Start-up time[4]	f_{OSC} = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0	3.0 V		4		ms
		f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0			1.8		
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0			0.7		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0			0.6		
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0			450		µs
		f_{OSC} = 32 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0			300		
		f_{OSC} = 40 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0			250		
		f_{OSC} = 48 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6, $C_{L,eff}$ = 16 pF, Typical ESR and C_{SHUNT}, FCNTHF_EN = 0			250		
C_{HFXIN}	Integrated load capacitance at HFXIN terminal[5] [6]				2		pF
C_{HFXOUT}	Integrated load capacitance at HFXOUT terminal[5] [6]				2		pF
$f_{Fault,HFXT}$	Oscillator fault frequency[7] [8]			400		700	kHz

(4) Does not include programable start-up counter.
(5) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, CL,eff can be computed as CIN x COUT / (CIN + COUT), where CIN and COUT is the total capacitance at the HFXIN and HFXOUT terminals, respectively.
(6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. Because the PCB adds additional capacitance, it must also be considered in the overall capacitance. TI recommends verifying that the recommended effective load capacitance of the selected crystal is met.
(7) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX might set the flag. A static condition or stuck at fault condition will set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-11 lists the characteristics of the DCO.

Table 5-11. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, T_A	MIN	TYP	MAX	UNIT
f_{RSEL0_CTR}	DCO center frequency accuracy for range 0 with calibrated factory settings	Internal resistor mode, DCORSEL = 0, DCOTUNE = 0		1.443	1.5	1.557	MHz
		External resistor mode, DCORSEL = 0, DCOTUNE = 0		1.482	1.5	1.518	
f_{RSEL1_CTR}	DCO center frequency accuracy for range 1 with calibrated factory settings	Internal resistor mode, DCORSEL = 1, DCOTUNE = 0		2.885	3	3.115	MHz
		External resistor mode, DCORSEL = 1, DCOTUNE = 0		2.964	3	3.036	
f_{RSEL2_CTR}	DCO center frequency accuracy for range 2 with calibrated factory settings	Internal resistor mode, DCORSEL = 2, DCOTUNE = 0		5.77	6	6.23	MHz
		External resistor mode, DCORSEL = 2, DCOTUNE = 0		5.928	6	6.072	
f_{RSEL3_CTR}	DCO center frequency accuracy for range 3 with calibrated factory settings	Internal resistor mode, DCORSEL = 3, DCOTUNE = 0		11.541	12	12.459	MHz
		External resistor mode, DCORSEL = 3, DCOTUNE = 0		11.856	12	12.144	
f_{RSEL4_CTR}	DCO center frequency accuracy for range 4 with calibrated factory settings	Internal resistor mode, DCORSEL = 4, DCOTUNE = 0		23.082	24	24.918	MHz
		External resistor mode, DCORSEL = 4, DCOTUNE = 0		23.712	24	24.288	
f_{RSEL5_CTR}	DCO center frequency accuracy for range 5 with calibrated factory settings	Internal resistor mode, DCORSEL = 5, DCOTUNE = 0		46.164	48	49.836	MHz
		External resistor mode, DCORSEL = 5, DCOTUNE = 0		47.424	48	48.576	
df_{DCO}/dT	DCO frequency drift with temperature(1)	Internal resistor mode, At fixed voltage	1.62 V to 3.7 V			250	ppm/°C
		External resistor mode(2) At fixed voltage	1.62 V to 3.7 V			40	
df_{DCO}/dV_{CC}	DCO frequency voltage drift with voltage(3)	At fixed temperature, applicable for both DCO Internal and External resistor modes	–40°C to 85 °C			0.1	%/V
f_{RSEL0}	DCO frequency range 0	DCORSEL = 0 DCO internal or external resistor mode	3.0 V, 25°C	0.98		2.26	MHz
f_{RSEL1}	DCO frequency range 1	DCORSEL = 1 DCO internal or external resistor mode	3.0 V, 25°C	1.96		4.51	MHz
f_{RSEL2}	DCO frequency range 2	DCORSEL = 2 DCO internal or external resistor mode	3.0 V, 25°C	3.92		9.02	MHz
f_{RSEL3}	DCO frequency range 3	DCORSEL = 3 DCO internal or external resistor mode	3.0 V, 25°C	7.84		18.04	MHz
f_{RSEL4}	DCO frequency range 4	DCORSEL = 4 DCO internal or external resistor mode	3.0 V, 25°C	15.68		36.07	MHz
f_{RSEL5}	DCO frequency range 5	DCORSEL = 5 DCO internal or external resistor mode	3.0 V, 25°C	31.36		52	MHz
f_{DCO_DC}	Duty cycle			47%	50%	53%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Does not include temperature coefficient of external resistor.
Recommended value of external resistor at DCOR pin: 91 kΩ, 0.1%, ±25 ppm/°C.
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

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DCO *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, T_A	MIN	TYP	MAX	UNIT
t_{DCO_JITTER}	DCO period jitter	DCORSEL = 5, DCOTUNE = 0			50	90	ps
		DCORSEL = 4, DCOTUNE = 0			80	120	
		DCORSEL = 3, DCOTUNE = 0			115	170	
		DCORSEL = 2, DCOTUNE = 0			160	240	
		DCORSEL = 1, DCOTUNE = 0			225	340	
		DCORSEL = 0, DCOTUNE = 0			450	550	
T_{DCO_STEP}	Step size	Step size of the DCO.			0.2%		
$t_{DCO_SETTLE_RANGE}$	DCO settling from worst case DCORSELn to DCORSELm	DCO settled to within 1.5% of steady state frequency				10	µs
$t_{DCO_SETTLE_TUNE}$	DCO settling worst case DCOTUNEn to DCOTUNEm within any DCORSEL setting	DCO settled to within 1.5% of steady state frequency				10	µs
t_{START}	DCO start-up time(4)	DCO settled to within 0.5% of steady state frequency			5		µs

(4) The maximum parasitic capacitance at the DCO external resistance pin (DCOR) should not exceed 5 pF to ensure the specified DCO start-up time.

Table 5-12 lists the overall tolerance of the DCO.

Table 5-12. DCO Overall Tolerance

over operating free-air temperature range (unless otherwise noted)

RESISTOR OPTION	TEMPERATURE CHANGE	TEMPERATURE DRIFT (%)	VOLTAGE CHANGE	VOLTAGE DRIFT (%)	OVERALL DRIFT (%)	OVERALL ACCURACY (%)
Internal resistor	–40°C to 85 °C	±3.125	1.62 V to 3.7 V	±0.2	±3.325	±3.825
	0°C	0	1.62 V to 3.7 V	±0.2	±0.2	±0.7
	–40°C to 85 °C	±3.125	0 V	0	±3.125	±3.625
External resistor with 25-ppm TCR	–40°C to 85 °C	±0.5	1.62 V to 3.7 V	±0.2	±0.7	±1.2
	0°C	0	1.62 V to 3.7 V	±0.2	±0.2	±0.7
	–40°C to 85 °C	±0.5	0 V	0	±0.5	±1

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Table 5-13 lists the characteristics of the internal very-low-power low-frequency oscillator (VLO).

Table 5-13. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VLO}	Current consumption(1)			50		nA
f_{VLO}	VLO frequency		6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift(2)			0.1		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(3)			0.2		%/V
DC_{VLO}	Duty cycle		40%	50%	60%	

(1) Current measured on DVCC supply
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-14 lists the characteristics of the internal-reference low-frequency oscillator (REFO) in 32.768-kHz mode.

Table 5-14. Internal-Reference Low-Frequency Oscillator (REFO) in 32.768-kHz Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO current consumption(2)				0.6		µA
f_{REFO}	REFO frequency calibrated				32.768		kHz
	REFO absolute tolerance calibrated	T_A = –40°C to 85°C				±3%	
		T_A = 25°C	3 V			±1.5%	
df_{REFO}/d_T	REFO frequency temperature drift(3)				0.012		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift(4)				0.2		%/V
DC_{REFO}	REFO duty cycle			40%	50%	60%	

(1) REFO is configured to 32.768-kHz mode with REFOFSEL = 0.
(2) Total current measured on both AVCC and DVCC supplies.
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-15 lists the characteristics of the internal-reference low-frequency oscillator (REFO) in 128-kHz mode.

Table 5-15. Internal-Reference Low-Frequency Oscillator (REFO) in 128-kHz Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
REFO	REFO current consumption(2)				1		µA
f_{REFO}	REFO frequency calibrated				128		kHz
	REFO absolute tolerance calibrated	T_A = –40°C to 85°C				±6%	
		T_A = 25°C	3 V			±1.5%	
df_{REFO}/d_T	REFO frequency temperature drift(3)				0.018		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift(4)				0.4		%/V
DC_{REFO}	REFO duty cycle			40%	50%	60%	

(1) REFO is configured to 128-kHz mode with REFOFSEL = 1.
(2) Total current measured on both AVCC and DVCC supplies.
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

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Table 5-16 lists the characteristics of the module oscillator (MODOSC).

Table 5-16. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption(1)				50		µA
f_{MODOSC}	MODOSC frequency			23	25	27	MHz
df_{MODOSC}/dT	MODOSC frequency temperature drift(2)				0.02		%/°C
df_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift(3)				0.3		%/V
DC_{MODOSC}	Duty cycle			40%	50%	60%	

(1) Total current measured on both AVCC and DVCC supplies.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-17 lists the characteristics of the system oscillator (SYSOSC).

Table 5-17. System Oscillator (SYSOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SYSOSC}	Current consumption(1)				30		µA
f_{SYSOSC}	SYSOSC frequency			4.25	5.0	5.75	MHz
df_{SYSOSC}/dT	SYSOSC frequency temperature drift(2)				0.03		%/°C
$df_{SYSOSC}/dVCC$	SYSOSC frequency supply voltage drift(3)				0.5		%/V
DC_{SYSOSC}	Duty cycle			40%	50%	60%	

(1) Current measured on AVCC supply.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

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5.25.4 Power Supply System

Table 5-18 lists the LDO V_{CORE} regulator characteristics.

Table 5-18. V_{CORE} Regulator (LDO) Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CORE0-HP}$	Static VCORE voltage Level 0 in active and LPM0 modes	Device power modes AM_LDO_VCORE0, LPM0_LDO_VCORE0	1.12	1.2	1.28	V
$V_{CORE1-HP}$	Static VCORE voltage Level 1 in active and LPM0 modes	Device power modes AM_LDO_VCORE1, LPM0_LDO_VCORE1	1.31	1.4	1.49	V
$V_{CORE0-LF}$	Static VCORE voltage Level 0 in low-frequency active and low frequency LPM0 modes	Device power modes AM_LF_VCORE0	1.12	1.2	1.28	V
$V_{CORE1-LF}$	Static VCORE voltage Level 1 in low-frequency active and low frequency LPM0 modes	Device power modes AM_LF_VCORE1	1.31	1.4	1.49	V
$V_{CORE0-LPM34}$	Static VCORE voltage Level 0 in LPM3 and LPM4 modes	Device power modes LPM3, LPM4	1.08	1.2	1.32	V
$V_{CORE1-LPM34}$	Static VCORE voltage Level 1 in LPM3 and LPM4 modes	Device power modes LPM3, LPM4	1.27	1.4	1.53	V
$V_{CORE0-LPM35}$	Static VCORE voltage Level 0 in LPM3.5 mode	Device power mode LPM3.5	1.08	1.2	1.32	V
$I_{INRUSH-ST}$	Inrush current at start-up	Device power-up			200	mA
$I_{PEAK-LDO}$	Peak current drawn by LDO from DV_{CC}				350	mA
$I_{SC-coreLDO}$	Short circuit current limit for core LDO	Measured when output is shorted to ground			300	mA

Table 5-19 lists the DC-DC V_{CORE} regulator characteristics.

Table 5-19. V_{CORE} Regulator (DC-DC) Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC-DCDC}$	Allowed DV_{CC} range for DC-DC operation	DCDC_FORCE = 1	1.8		3.7	V
V_{DCDC_SO} (1)	DC-DC to LDO switch over voltage	dDV_{CC}/dt = 1 V/ms, DCDC_FORCE = 0	1.8		2.0	V
$V_{CORE0-DCDC}$	Static VCORE voltage Level 0 in DC-DC high-performance modes	Device power modes AM_DCDC_VCORE0, LPM0_DCDC_VCORE0	1.12	1.2	1.28	V
$V_{CORE1-DCDC}$	Static VCORE voltage Level 1 in DC-DC high-performance modes	Device power modes AM_DCDC_VCORE1, LPM0_DCDC_VCORE1	1.31	1.4	1.49	V
$I_{PEAK-DCDC}$	Peak current drawn by DC-DC from DVCC				300	mA
$I_{SC-DCDC}$	Short circuit current limit for DC-DC	Measured when output is shorted to ground			500	mA

(1) When DV_{CC} falls below this voltage, internally the regulator switches over to LDO from DC-DC.

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Table 5-20 lists the VCCDET characteristics.

Table 5-20. PSS, VCCDET

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VCC_VCCDET-}$	VCCDET power-down level - trip point with falling V_{CC}	dDV_{CC}/d_t < 3 V/s (1)	0.64	1.12	1.55	V
$V_{VCC_VCCDET+}$	VCCDET power-up level - trip point with rising V_{CC}	dDV_{CC}/d_t < 3 V/s (1)	0.70	1.18	1.59	V
$V_{VCC_VCC_hys}$	VCCDET hysteresis		30	65	100	mV

(1) The VCCDET levels are measured with a slow-changing supply. Faster slopes can result in different levels.

Table 5-21 lists the SVSMH characteristics.

Table 5-21. PSS, SVSMH

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SVSMH}	$SVSM_H$ current consumption, low-power mode	SVSMHOFF = 0, SVSMHLP = 1		200	400	nA
	$SVSM_H$ current consumption, high-performance mode	SVSMHOFF = 0, SVSMHLP = 0		7	10	µA
$V_{SVSMH-,HP}$	$SVSM_H$ threshold level during high-performance mode (falling DV_{CC})	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s)	2.0	2.06	2.12	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s)	2.2	2.26	2.32	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s)	2.4	2.47	2.54	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s)	2.7	2.79	2.88	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s)	2.9	3.0	3.1	
$V_{SVSMH+,HP}$	$SVSM_H$ threshold level; High Performance Mode [rising DV_{CC}]	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s)	2.02	2.07	2.14	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s)	2.22	2.27	2.34	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s)	2.42	2.48	2.56	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s)	2.72	2.8	2.9	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s)	2.92	3.01	3.12	

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PSS, SVSMH *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SVSMH-,LP}$	$SVSM_H$ threshold level; Low Power Mode [falling DV_{CC}]	SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s)	1.55	1.62	1.71	V
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s)	1.55	1.62	1.71	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s)	1.55	1.62	1.71	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s)	2.0	2.09	2.18	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s)	2.2	2.3	2.4	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s)	2.4	2.51	2.62	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s)	2.7	2.83	2.94	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s)	2.87	3.0	3.13	
V_{SVSMH_hys}	$SVSM_H$ hysteresis			15	30	mV
$t_{PD,SVSMH}$	SVS_H propagation delay, high-performance mode	SVSMHOFF = 0, SVSMHLP = 0, very fast dV_{DVCC}/dt		3	10	µs
	SVS_H propagation delay, low-power mode	SVSMHOFF = 0, SVSMHLP = 1, very fast dV_{DVCC}/dt		25	100	
$t_{(SVSMH)}$	$SVSM_H$ on or off delay time	SVSMHOFF = 1 → 0, SVSMHLP = 0 (1)		17	40	µs

(1) If the SVSMH is kept disabled in active mode and is enabled before entering a low-power mode of the device (LPM3, LPM4, LPM3.5, or LPM4.5) care should be taken that sufficient time has elapsed since enabling of the module before entry into the device low-power mode to allow for successful wake up of the SVSMH module per the SVSMH on or off delay time specification. Otherwise, SVSMH may trip, causing the device to reset and wake up from the low-power mode.

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5.25.5 Digital I/Os

Table 5-22 lists the characteristics of the digital inputs.

Table 5-22. Digital Inputs (Applies to Both Normal and High-Drive I/Os)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2.2 V	0.99		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.21	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2.2 V	0.32		0.84	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	30	40	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins shared with analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg,ndio}$	Normal I/O high-impedance input leakage current	See (1)(2)	2.2 V, 3 V			±20	nA
$I_{lkg,hdio}$	High-drive I/O high-impedance input leakage current	See (1)(2)	2.2 V, 3 V			±20	nA
t_{int}	External interrupt timing (external trigger pulse duration to set interrupt flag)	Ports with interrupt capability and without glitch filter (3)	2.2 V, 3 V	20			ns
		Ports with interrupt capability and with glitch filter but glitch filter disabled (GLTFLT_EN = 0) (3)	2.2 V, 3 V	20			
		Ports with interrupt capability and with glitch filter, glitch filter enabled (GLTFTL_EN = 1) (4)	2.2 V, 3 V	0.25		1	µs
t_{RST}	External reset pulse duration on RSTn pin(5)		2.2 V, 3 V	1			µs

(1) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_{int} is met. It may be set by trigger signals shorter than t_{int}.
(4) A trigger pulse duration less than the MIN value is always filtered, and a trigger pulse duration more than the MAX value is always passed. The trigger pulse may or may not be filtered if the duration is between the MIN and MAX values.
(5) Not applicable if RSTn/NMI pin configured as NMI.

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Table 5-23 lists the characteristics of the normal-drive digital outputs. See Figure 5-19 through Figure 5-22 for the typical characteristics graphs.

Table 5-23. Digital Outputs, Normal I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(1)	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(1)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.60	
$f_{Px.y}$	Port output frequency (with RC load)(3)	VCORE = 1.4 V, C_L = 20 pF, R_L (4) (5)	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
$d_{Px.y}$	Port output duty cycle (with RC Load)	VCORE = 1.4 V, C_L = 20 pF, R_L (4) (5)	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
f_{Port_CLK}	Clock output frequency(3)	VCORE = 1.4 V, C_L = 20 pF(5)	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
d_{Port_CLK}	Clock output duty cycle	VCORE = 1.4 V, C_L = 20 pF(5)	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{rise,ana}$	Port output rise time, port pins with shared analog functions	C_L = 20 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,ana}$	Port output fall time, port pins with shared analog functions	C_L = 20 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit - it might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 3.2kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected to the output to V_{SS}.
(5) The output voltage reaches at least 20% and 80% V_{CC} at the specified toggle frequency.
(6) Measured between 20% of V_{CC} to 80% of V_{CC}.
(7) Measured between 80% of V_{CC} to 20% of V_{CC}.

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Table 5-24 lists the characteristics of the high-drive digital outputs. See Figure 5-23 through Figure 5-26 for the typical characteristics graphs.

Table 5-24. Digital Outputs, High-Drive I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –5 mA(1)	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –15 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –10 mA(1)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –20 mA(2)		V_{CC} – 0.50	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 5 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 10 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 20 mA(2)		V_{SS}	V_{SS} + 0.50	
$f_{Px.y}$	Port output frequency (with RC load)(3)	VCORE = 1.4 V, C_L = 80 pF, R_L (4) (5)	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
$d_{Px.y}$	Port output duty cycle (with RC Load)	VCORE = 1.4 V, C_L = 80 pF, R_L (4) (5)	1.62 V	45%	55%	
			2.2 V	45%	55%	
			3.0 V	45%	55%	
f_{Port_CLK}	Clock output frequency(3)	VCORE = 1.4 V, C_L = 80 pF(5)	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
d_{Port_CLK}	Clock output duty cycle	VCORE = 1.4 V, C_L = 80 pF(5)	1.62 V	45%	55%	
			2.2 V	45%	55%	
			3.0 V	45%	55%	
t_{rise}	Port output rise time	C_L = 80 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
t_{fall}	Port output fall time	C_L = 80 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit, and it might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 3.2 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 80 pF is connected to the output to V_{SS}.
(5) The output voltage reaches at least 20% and 80% V_{CC} at the specified toggle frequency.
(6) Measured between 20% of V_{CC} to 80% of V_{CC}.
(7) Measured between 80% of V_{CC} to 20% of V_{CC}.

Table 5-25 lists the frequencies of the pin-oscillator ports. See Figure 5-27 and Figure 5-28 for the typical characteristics graphs.

Table 5-25. Pin-Oscillator Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{Px.y}$	Pin-oscillator frequency	Px.y, C_L = 10 pF(1)	3.0 V		1900		kHz
		Px.y, C_L = 20 pF(1)	3.0 V		1150		kHz

(1) C_L is the external load capacitance connected from the output to VSS and includes all parasitic effects such as PCB traces.

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5.25.5.1 Typical Characteristics, Normal-Drive I/O Outputs at 3.0 V and 2.2 V

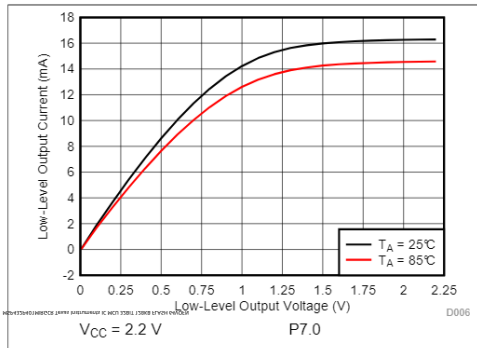


Figure 5-19. Low-Level Output Voltage vs Low-Level Output Current

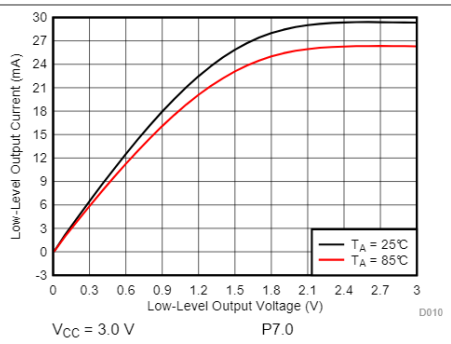


Figure 5-20. Low-Level Output Voltage vs Low-Level Output Current

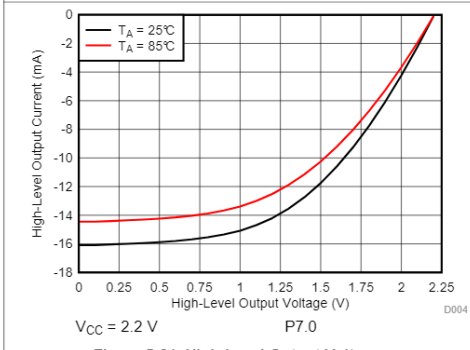


Figure 5-21. High-Level Output Voltage vs High-Level Output Current

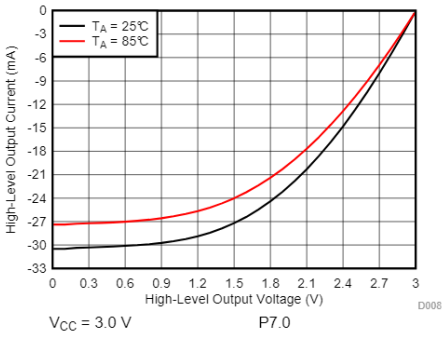
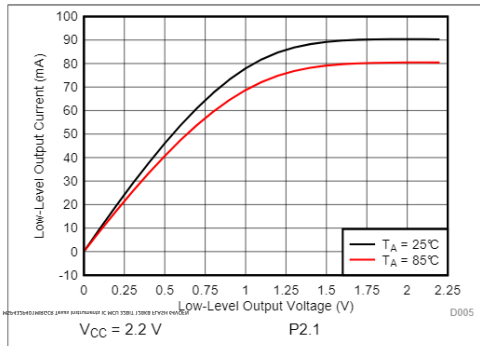


Figure 5-22. High-Level Output Voltage vs High-Level Output Current

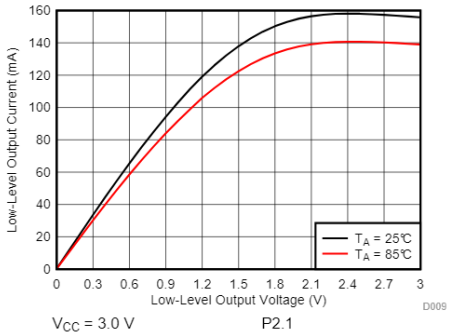
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5.25.5.2 Typical Characteristics, High-Drive I/O Outputs at 3.0 V and 2.2 V



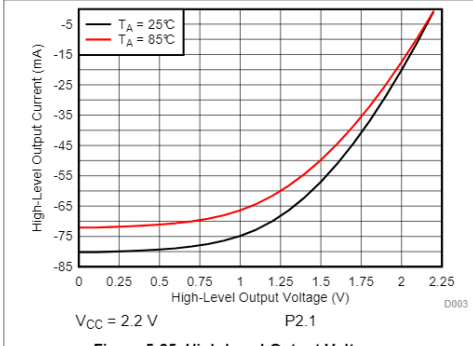
V_{CC} = 2.2 V P2.1

Figure 5-23. Low-Level Output Voltage vs Low-Level Output Current



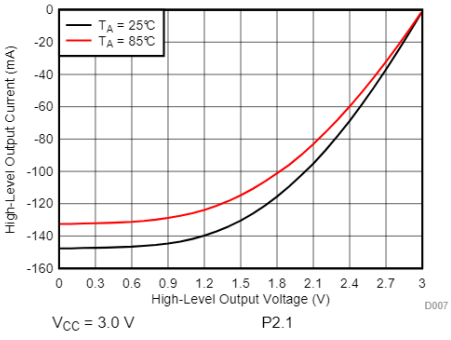
V_{CC} = 3.0 V P2.1

Figure 5-24. Low-Level Output Voltage vs Low-Level Output Current



V_{CC} = 2.2 V P2.1

Figure 5-25. High-Level Output Voltage vs High-Level Output Current



V_{CC} = 3.0 V P2.1

Figure 5-26. High-Level Output Voltage vs High-Level Output Current

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5.25.5.3 Typical Characteristics, Pin-Oscillator Frequency

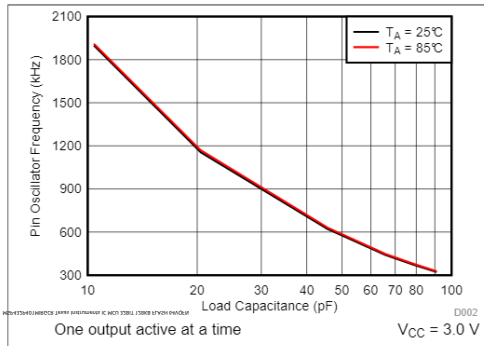


Figure 5-27. Load Capacitance vs Pin Oscillator Frequency

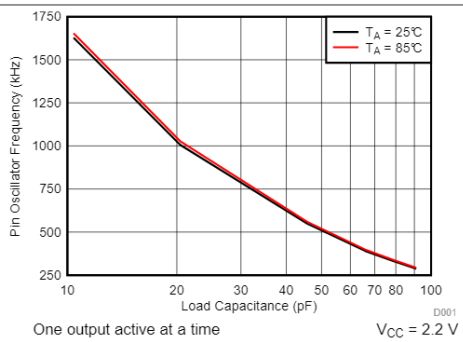


Figure 5-28. Load Capacitance vs Pin Oscillator Frequency

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5.25.6 14-Bit ADC

Table 5-26 lists the power supply and input range conditions for the ADC.

Table 5-26. 14-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 2		1.62		3.7	V
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 0		1.8		3.7	V
V(Ax)	Analog input voltage range[1]	All ADC analog input pins Ax		0		AVCC	V
V_{CM}	Input common-mode range	All ADC analog input pins Ax (ADC14DIF = 1)		0	VREF / 2	VREF	V
$I_{(ADC14)}$ single-ended mode	Operating supply current into AVCC and DVCC terminals[2]	$f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		490	640	µA
			2.2 V		450	580	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		215	270	
			2.2 V		210	260	
$I_{(ADC14)}$ differential mode	Operating supply current into AVCC and DVCC terminals[2]	$f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		690	875	µA
			2.2 V		620	785	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		275	335	
			2.2 V		260	320	
C_I	Input capacitance into a single terminal[3]				12	15	pF
R_I	Input MUX ON-resistance	0 V ≤ V(Ax) ≤ AVCC	1.8 V to 3.7 V		0.135	1	kΩ
			1.62 V to <1.8 V		0.15	1.5	

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference supply current is not included in current consumption parameter $I_{(ADC14)}$.
(3) Represents only the ADC switching capacitance. See the digital inputs electrical specification for internal parasitic pin capacitance.

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Table 5-27 lists the timing parameters of the ADC.

Table 5-27. 14-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC14CLK}$	ADC clock frequency (1)	ADC14PWRMD = 0	1.8 V to 3.7 V	0.128		25	MHz
		ADC14PWRMD = 2	1.62 V to 3.7 V	0.128		5.75	
$N_{CONVERT}$	Clock cycles for conversion	ADC14RES = 11			16		cycles
		ADC14RES = 10			14		
		ADC14RES = 01			11		
		ADC14RES = 00			9		
$t_{ADC14ON}$	Turnon settling time of ADC	See (2)				1.5	µs
t_{Sample}	Sampling time (3) (4)	R_S = 200 Ω, C_{pext} = 10 pF, R_I = 1 kΩ, C_I = 15 pF, C_{pint} = 5 pF		0.215			µs

(1) MODOSC can be used for 1 Msps and SYSOSC can be used for 200 ksps sampling rate operations of ADC.
(2) The condition is that the error in a conversion started after $t_{ADC14ON}$ is less than ±1 LSB. The reference and input signal are already settled.
(3) Sampling time should be at least 4 × (1 / $f_{ADC14CLK}$).
(4) $t_{sample} \geq (n + 1) \times \ln(2) \times [(R_S + R_I) \times C_I + R_S \times (C_{pext} + C_{pint})]$, where n = ADC resolution =14, R_S = external source resistance, C_{pext} = external parasitic capacitance.

Table 5-28 lists the linearity parameters of the ADC.

Table 5-28. 14-Bit ADC, Linearity Parameters (1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				14		bits
E_I	Integral linearity error (INL)				±2.3	LSB
E_D	Differential linearity error (DNL)		–0.99		1	LSB
E_O	Offset error	ADC14VRSEL = 0xE, 0xF		±0.2	±1	mV
		ADC14VRSEL = 0x1		±1.2	±2	
E_G	Gain error	ADC14VRSEL = 0xE		±2	±4	LSB
		ADC14VRSEL = 0xF		±20	±60	
		ADC14VRSEL = 0x1		±50	±180	
E_T	Total unadjusted error	ADC14VRSEL = 0xE		±4	±15	LSB
		ADC14VRSEL = 0xF		±22	±62	
		ADC14VRSEL = 0x1		±55	±185	

(1) Minimum reference voltage of 1.45 V is necessary to meet the specified accuracy. Lower reference voltage down to 1.2 V can be applied for 1 Msps sampling rate with reduced accuracy requirements.
(2) VeREF- pin should be connected to onboard ground for ADC14VRSEL = 0xE.

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Table 5-29 lists the dynamic parameters of the ADC.

Table 5-29. 14-Bit ADC, Dynamic Parameters(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD(2)	Signal-to-noise and distortion	1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, LDO based operation	71	73		dB
		1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, DC-DC based operation	62	70		
		1 Msps, ADC14DIF = 1, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine	79	81		
ENOB(2)	Effective number of bits	1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, LDO based operation	11.5	11.8		bit
		1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, DC-DC based operation	10	11.3		
		1 Msps, ADC14DIF = 1, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine	12.8	13.2		
CMRR_DC	Common-mode rejection ratio, DC	Common-mode input signal = 0 to VREF pp at DC, ADC14DIF = 1	70	85		dB
CMRR_AC	Common-mode rejection ratio, AC	Common-mode input signal = 0 to VREF pp at 1 MHz, ADC14DIF = 1	55	65		dB
PSRR_DC	Power supply rejection ratio, DC	$AV_{CC} = AV_{CC\ (min)}$ to $AV_{CC(max)}$, ADC14DIF = 0, ADC14VRSEL = 0xE		1	2.5	mV/V
		$AV_{CC} = AV_{CC\ (min)}$ to $AV_{CC(max)}$, ADC14DIF = 1, ADC14VRSEL = 0xE		50	150	µV/V
PSRR_AC	Power supply rejection ratio, AC	dAV_{CC} = 0.1 V at 1 kHz, ADC14DIF = 0, ADC14VRSEL = 0xE		1		mV/V
		dAV_{CC} = 0.1 V at 1 kHz, ADC14DIF = 1, ADC14VRSEL = 0xE		50		µV/V

(1) VeREF- pin should be connected to onboard ground for ADC14VRSEL = 0xE.
(2) ADC clock derived from HFXT oscillator.

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Table 5-30 lists the characteristics of the temperature sensor and built-in $V_{1/2}$.

Table 5-30. 14-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (1) (2)	ADC14ON = 1, ADC14TCMAP = 1, T_A = 0°C			685		mV
TC_{SENSOR}	See (2)	ADC14ON = 1, ADC14TCMAP = 1			1.9		mV/°C
t_{SENSOR} (sample)	Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected (3)	ADC14ON = 1, ADC14TCMAP = 1, Error of conversion result ≤ 1 LSB		5			µs
$V_{1/2}$	AVCC voltage divider for ADC14BATMAP = 1 on MAX input channel	ADC14ON = 1, ADC14BATMAP = 1		48%	50%	52%	
$t_{V\ 1/2}$ (sample)	Sample time required if ADC14BATMAP = 1 and channel MAX is selected (4)	ADC14ON = 1, ADC14BMAP = 1		1			µs

(1) The temperature sensor offset can be as much as ±35°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The TLV structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (Temperature,°C) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 250 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V\ 1/2\ (sample)}$. No additional on time is needed.

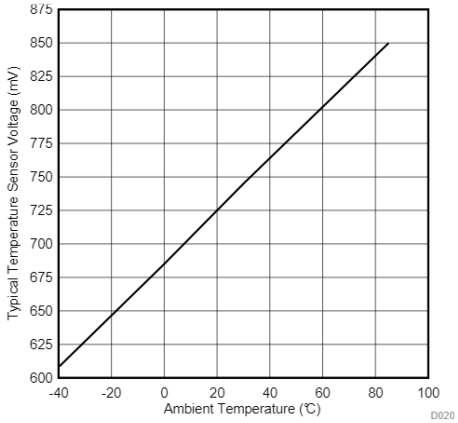


Figure 5-29. Typical Temperature Sensor Voltage

Table 5-31 lists the characteristics of the internal reference buffers of the ADC.

Table 5-31. 14-Bit ADC, Internal Reference Buffers

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REF+}	Operating supply current into AVCC terminal (1)	ADC ON, REFOUT = 0, ADC14PWRMD = 0, REFVSEL = {0, 1, 3}	3 V		600	800	µA
		ADC ON, REFOUT = 0, ADC14PWRMD = 2, REFVSEL = {0, 1, 3}			200	300	
		ADC ON, REFOUT = 1, ADC14PWRMD = 2, REFVSEL = {0, 1, 3}			650	850	
t_{on}	Turnon time		3 V			5	µs

(1) The internal reference current is supplied through terminal AVCC.

Table 5-32 lists the characteristics of the ADC external reference.

Table 5-32. 14-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

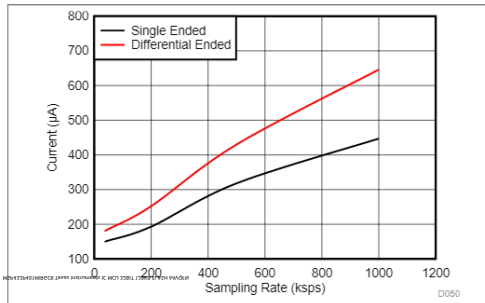
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input (1)		1.45		AV_{CC}	V
V_{eREF-}	Negative external reference voltage input				0	V
$(V_{eREF+} - V_{eREF-})$	Differential external reference voltage input (1)		1.45		AV_{CC}	V
I_{VeREF+} I_{VeREF-}	Static input current in single-ended input mode	1.45 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 25 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 0			±75	µA
		1.45 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 0			±15	
I_{VeREF+} I_{VeREF-}	Static input current in differential input mode	1.45 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 25 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 1			±150	µA
		1.45 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC14CLK}$ = 5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 1			±30	
C_{VeREF+}	Capacitance at VeREF+ terminal	See (2)	5			µF

(1) Lower reference voltage down to 1.2 V can be applied for 1 Msps sampling rate with reduced accuracy requirements of linearity parameters.
(2) Two decoupling capacitors, 5 µF and 50 nF, should be connected to VeREF+ terminal to decouple the dynamic current required for an external reference source if it is used for the ADC14. See also the *MSP432P4xx Family Technical Reference Manual*.

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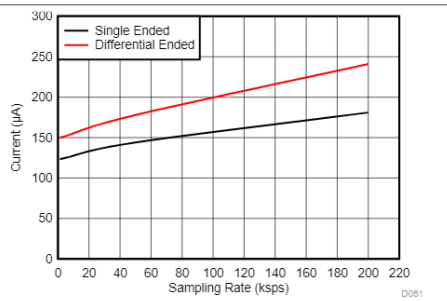
5.25.6.1 Typical Characteristics of ADC

typical characteristics at 3 V, 25°C, and 1-Msps sampling rate of ADC (unless otherwise specified)



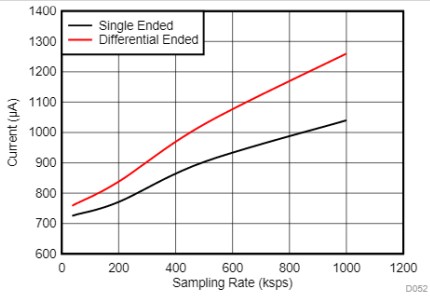
VRSEL = 14 VREF = 2.5 V
Resolution = 14 Bit ADC14PWRMD = 0

Figure 5-30. Current vs Sampling Rate



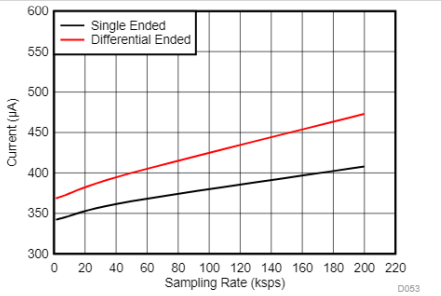
VRSEL = 14 VREF = 2.5 V
Resolution = 12 Bit ADC14PWRMD = 2

Figure 5-31. Current vs Sampling Rate



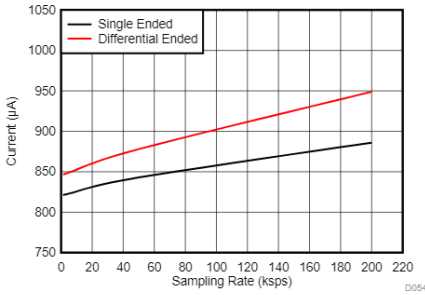
VRSEL = 1 VREF = 2.5 V
REFOUT = 0 ADC14PWRMD = 0
Resolution = 14 Bit

Figure 5-32. Current vs Sampling Rate



VRSEL = 1 VREF = 2.5 V
REFOUT = 0 ADC14PWRMD = 2
Resolution = 12 Bit

Figure 5-33. Current vs Sampling Rate



VRSEL = 1 VREF = 2.5 V
REFOUT = 1 ADC14PWRMD = 2
Resolution = 12 Bit

Figure 5-34. Current vs Sampling Rate

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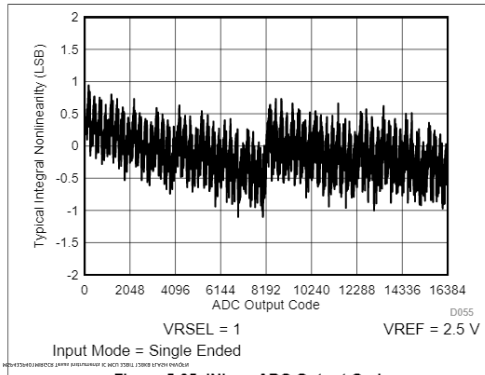


Figure 5-35. INL vs ADC Output Code

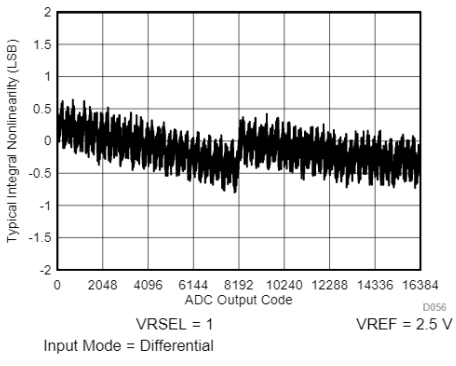


Figure 5-36. INL vs ADC Output Code

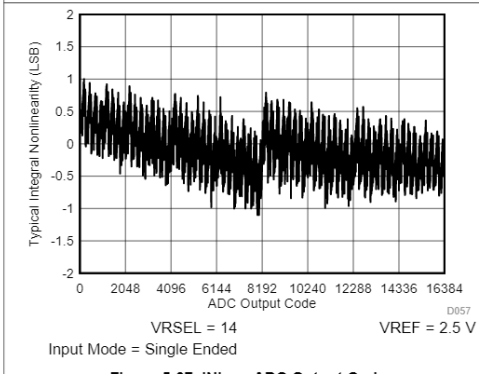


Figure 5-37. INL vs ADC Output Code

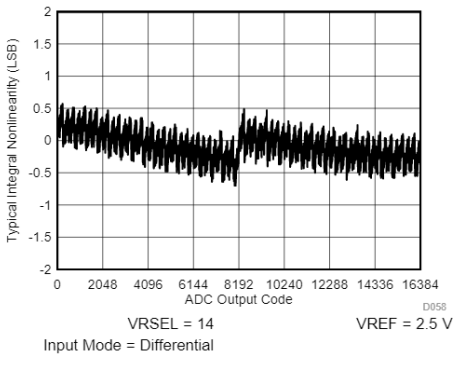


Figure 5-38. INL vs ADC Output Code

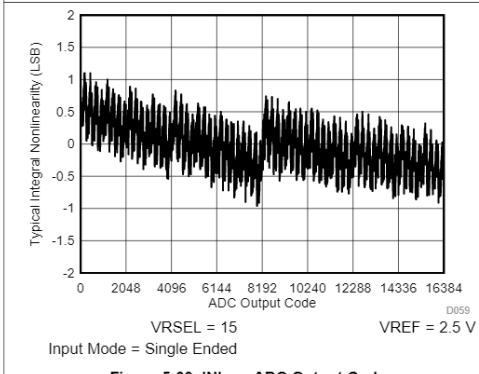


Figure 5-39. INL vs ADC Output Code

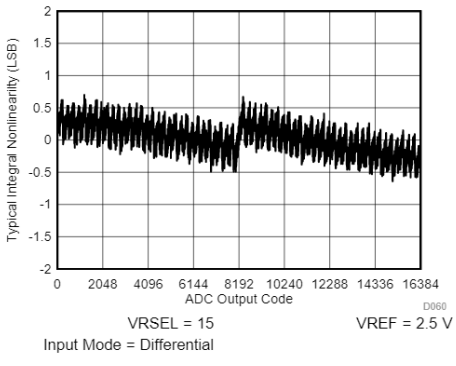


Figure 5-40. INL vs ADC Output Code

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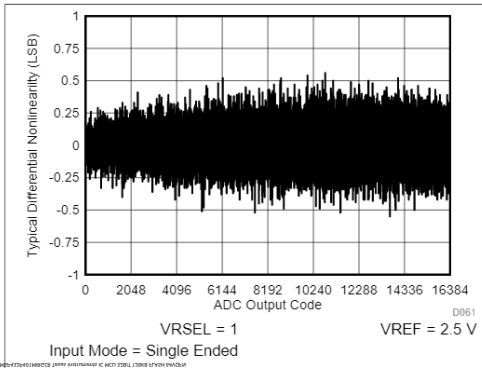


Figure 5-41. DNL vs ADC Output Code

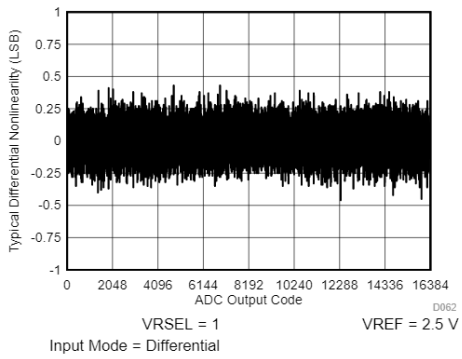


Figure 5-42. DNL vs ADC Output Code

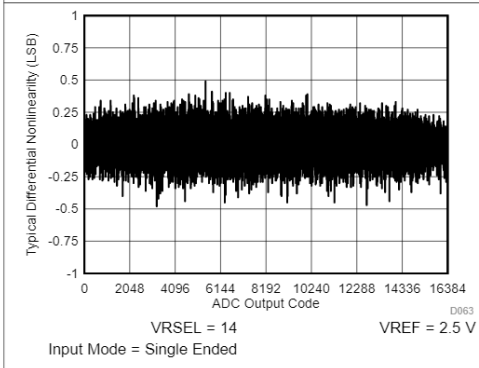


Figure 5-43. DNL vs ADC Output Code

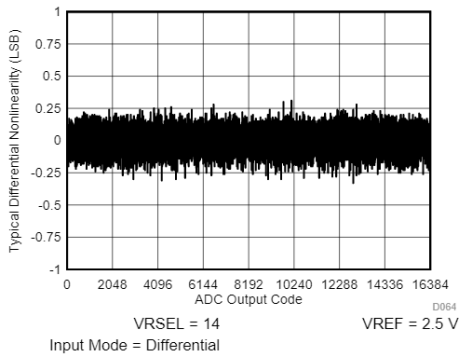


Figure 5-44. DNL vs ADC Output Code

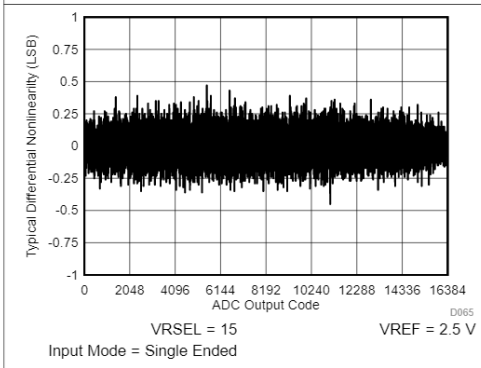


Figure 5-45. DNL vs ADC Output Code

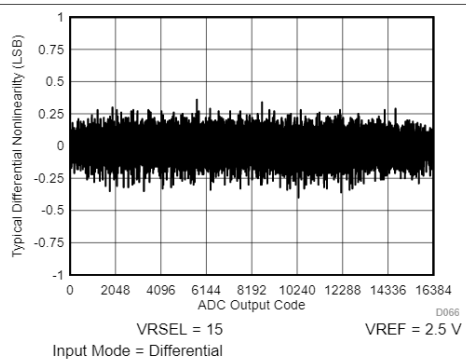
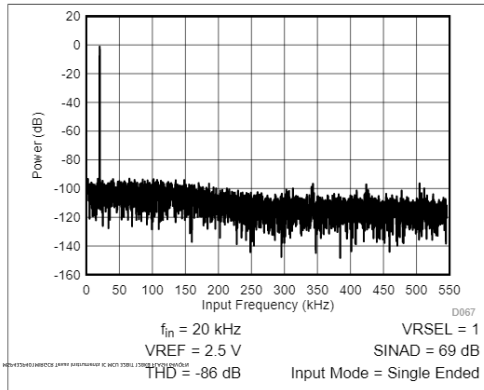


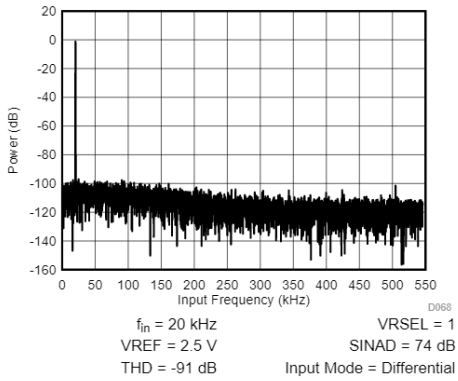
Figure 5-46. DNL vs ADC Output Code

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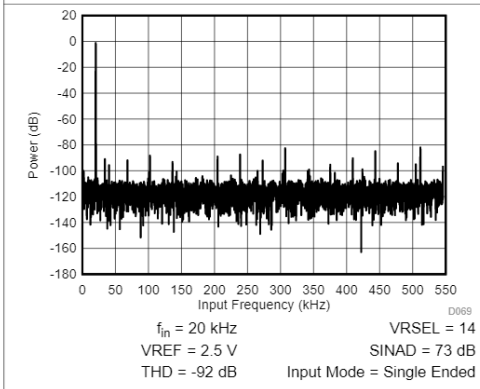
f_{in} = 20 kHz | VRSEL = 1
VREF = 2.5 V | SINAD = 69 dB
THD = -86 dB | Input Mode = Single Ended

Figure 5-47. Power vs Input Frequency



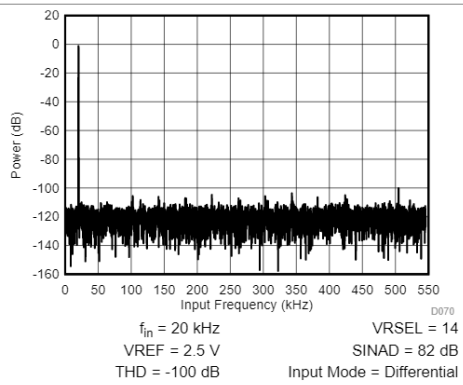
f_{in} = 20 kHz | VRSEL = 1
VREF = 2.5 V | SINAD = 74 dB
THD = -91 dB | Input Mode = Differential

Figure 5-48. Power vs Input Frequency



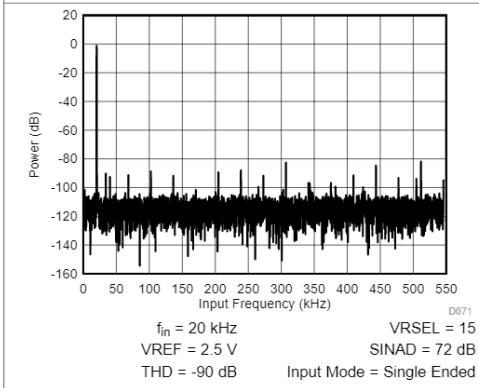
f_{in} = 20 kHz | VRSEL = 14
VREF = 2.5 V | SINAD = 73 dB
THD = -92 dB | Input Mode = Single Ended

Figure 5-49. Power vs Input Frequency



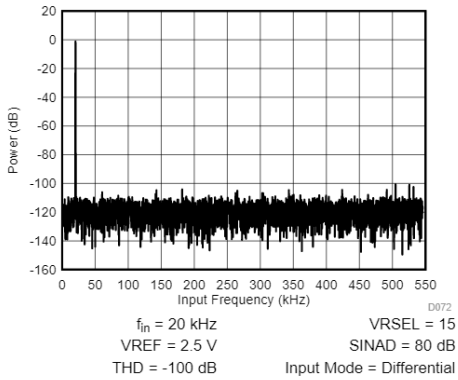
f_{in} = 20 kHz | VRSEL = 14
VREF = 2.5 V | SINAD = 82 dB
THD = -100 dB | Input Mode = Differential

Figure 5-50. Power vs Input Frequency



f_{in} = 20 kHz | VRSEL = 15
VREF = 2.5 V | SINAD = 72 dB
THD = -90 dB | Input Mode = Single Ended

Figure 5-51. Power vs Input Frequency



f_{in} = 20 kHz | VRSEL = 15
VREF = 2.5 V | SINAD = 80 dB
THD = -100 dB | Input Mode = Differential

Figure 5-52. Power vs Input Frequency

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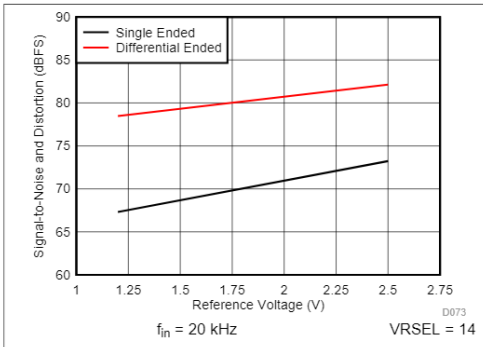


Figure 5-53. SINAD vs Reference Voltage

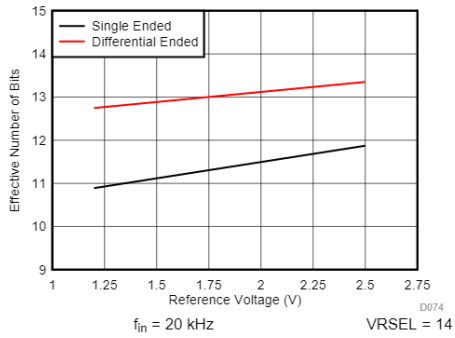


Figure 5-54. ENOB vs Reference Voltage

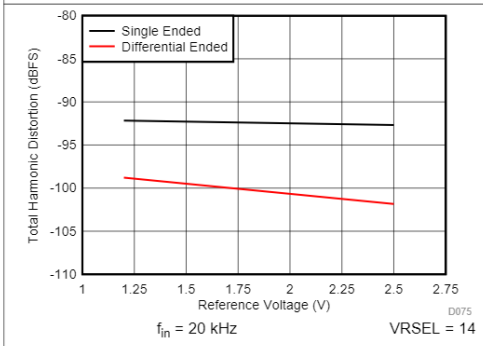


Figure 5-55. THD vs Reference Voltage

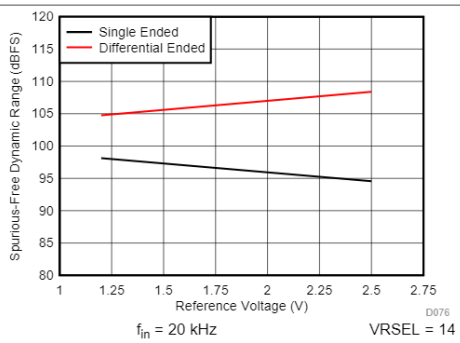


Figure 5-56. SFDR vs Reference Voltage

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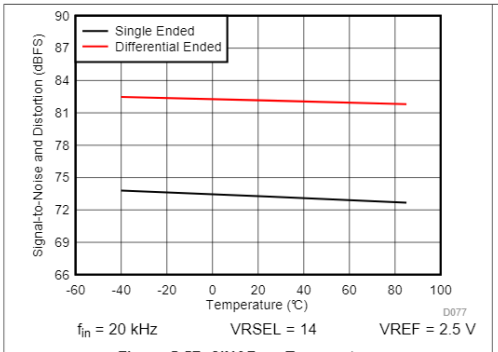


Figure 5-57. SINAD vs Temperature

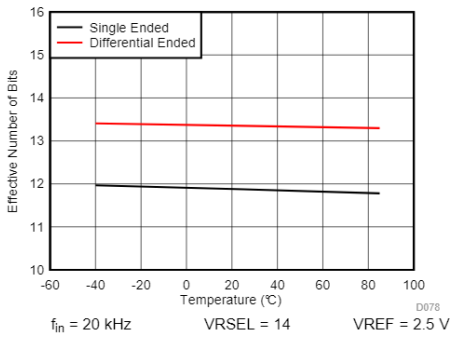


Figure 5-58. ENOB vs Temperature

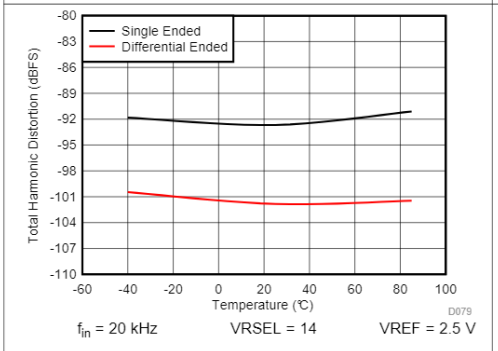


Figure 5-59. THD vs Temperature

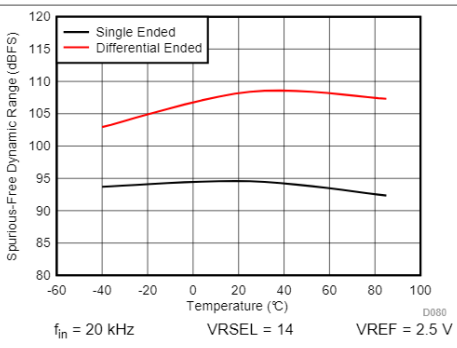


Figure 5-60. SFDR vs Temperature

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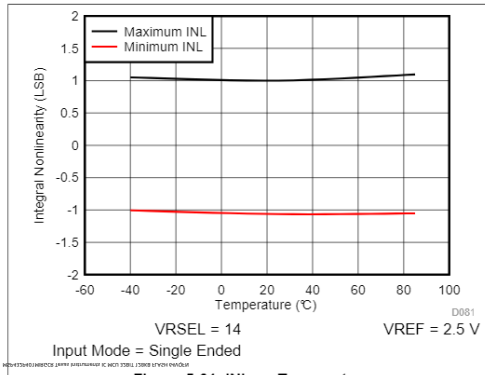


Figure 5-61. INL vs Temperature

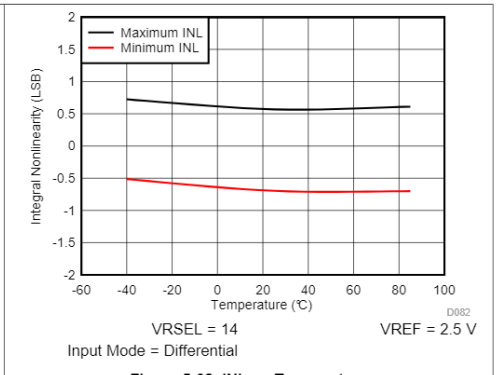


Figure 5-62. INL vs Temperature

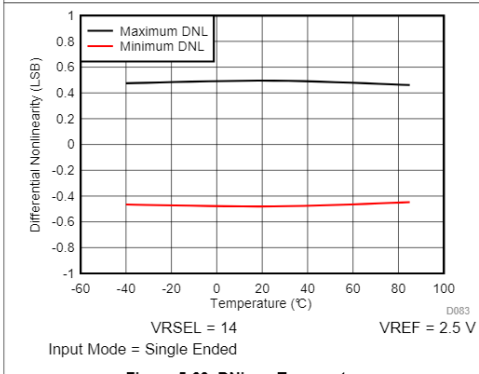


Figure 5-63. DNL vs Temperature

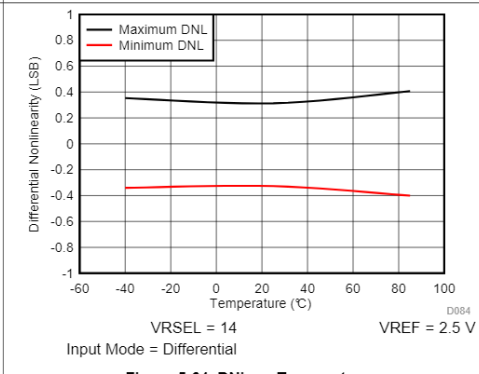
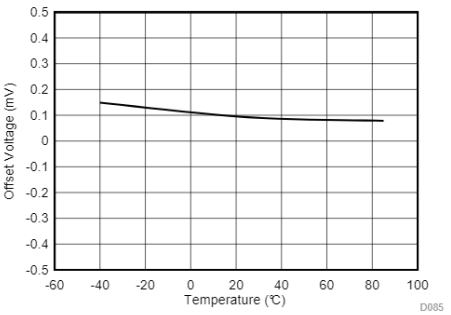
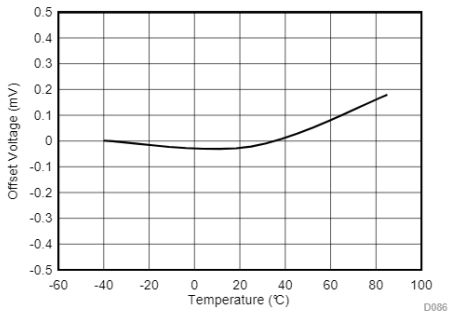


Figure 5-64. DNL vs Temperature



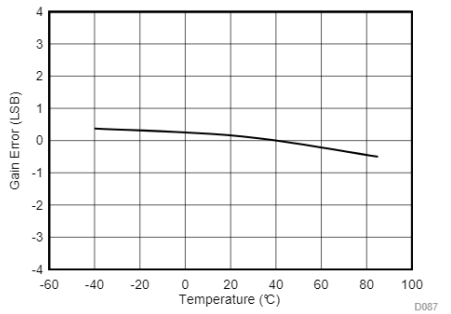
VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

Figure 5-65. Offset Voltage vs Temperature



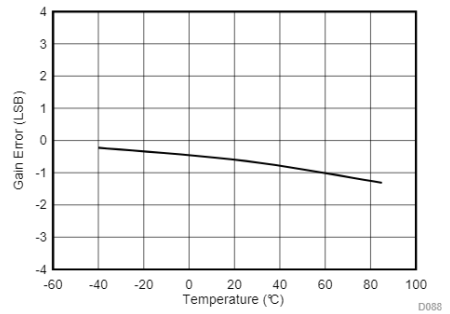
VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

Figure 5-66. Offset Voltage vs Temperature



VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

Figure 5-67. Gain Error vs Temperature



VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

Figure 5-68. Gain Error vs Temperature

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5.25.7 REF_A

Table 5-33 lists the characteristics of the REF_A built-in reference.

Table 5-33. REF_A, Built-In Reference *(LDO Operation)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {0} for 1.2 V, REFON = 1	1.62 V		1.2	±1%	V
		REFVSEL = {1} for 1.45 V, REFON = 1	1.75 V		1.45	±1%	
		REFVSEL = {3} for 2.5 V, REFON = 1	2.8 V		2.5	±1%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.62			V
		REFVSEL = {1} for 1.45 V		1.75			
		REFVSEL = {3} for 2.5 V		2.8			
I_{REF+}	Operating supply current into AVCC terminal(1)	REFON = 1	3 V		15	20	µA
$I_{O(VREF+)}$	VREF maximum load current, VREF+ terminal	REFVSEL = {0, 1, 3}, AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFON = REFOUT = 1		–1000		+10	µA
$I_{L(VREF+)}$	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 3}, I(VREF+) = +10 µA or –1000 µA, AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFON = REFOUT = 1				2500	µV/mA
$C_{VREF±}$	Capacitance at VREF+, VREF- terminals	REFON = REFOUT = 1		0		100	pF
$PSRR_DC_{REFOUT0}$	Power supply rejection ratio (DC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 0			50	350	µV/V
$PSRR_DC_{REFOUT1}$	Power supply rejection ratio (DC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 1			50	250	µV/V
$PSRR_AC_{REFOUT0}$	Power supply rejection ratio (AC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, dAVCC = 0.1 V at 1 kHz, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 0			2	10	mV/V
$PSRR_AC_{REFOUT1}$	Power supply rejection ratio (AC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, dAVCC = 0.1 V at 1 kHz, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 1			2	5	mV/V
TC_{REF+} (2)	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 3}, REFON = 1, T_A = –40°C to 85°C			10	25	ppm/°C
t_{SETTLE}	Settling time of reference voltage(3)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$ REFVSEL = {0, 1, 3}, REFON = 0 → 1			70	80	µs

(1) The internal reference current is supplied from terminal AVCC.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(3) The condition is that the error in a ADC conversion started after t_{SETTLE} is less than ±0.5 LSB.

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5.25.8 Comparator_E

Table 5-34 lists the characteristics of the comparator.

Table 5-34. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.62		3.7	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)	2.2 V, 3 V		10	15	µA
		CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)	2.2 V, 3 V		8	10	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 30°C	2.2 V, 3 V			0.5	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 85°C	2.2 V, 3 V			0.5	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Includes REF_A module current	CEREFACC = 0, CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0	2.2 V, 3 V		25	35	µA
		CEREFACC = 1, CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0	2.2 V, 3 V		10	15	
V_{REF}	Reference voltage level	CERSx = 11, CEREFLx = 01, CEREFACC = 0	1.62 V	1.17	1.2	1.23	V
		CERSx = 11, CEREFLx = 10, CEREFACC = 0	2.2 V	1.95	2.0	2.05	
		CERSx = 11, CEREFLx = 11, CEREFACC = 0	2.7 V	2.40	2.5	2.60	
		CERSx = 11, CEREFLx = 01, CEREFACC = 1	1.62 V	1.15	1.2	1.23	
		CERSx = 11, CEREFLx = 10, CEREFACC = 1	2.2 V	1.92	2.0	2.05	
		CERSx = 11, CEREFLx = 11, CEREFACC = 1	2.7 V	2.4	2.5	2.6	
V_{IC}	Common mode input range			0		VCC–1	V
V_{OFFSET}	Input offset voltage	CEPWRMD = 00		–10		+10	mV
		CEPWRMD = 01		–20		+20	
		CEPWRMD = 10		–20		+20	
C_{IN}	Input capacitance	CEPWRMD = 00 or CEPWRMD = 01			8		pF
		CEPWRMD = 10			8		
R_{SIN}	Series input resistance	On (switch closed)			2	4	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV			330	550	ns
		CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV			410	650	
		CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV				30	µs
$t_{PD,filter}$	Propagation delay with filter active	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00			0.6	0.9	µs
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01			1.1	1.6	
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10			2	3	
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11			4	6	

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Comparator_E *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{EN_CMP}	Comparator enable time	CEON = 0 to 1, CEPWRMD = 00, VIN+, VIN- from pins, Overdrive ≥ 20 mV			0.8	1	µs
		CEON = 0 to 1, CEPWRMD = 01, VIN+, VIN- from pins, Overdrive ≥ 20 mV			0.9	1.2	
		CEON = 0 to 1, CEPWRMD = 10, VIN+, VIN- from pins, Overdrive ≥ 20 mV			15	25	
$t_{EN_CMP_VREF}$	Comparator and reference ladder and reference voltage enable time	CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV			90	120	µs
		CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV			90	120	
		CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV			90	120	
		CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			90	180	
		CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			90	180	
		CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			90	180	
$t_{EN_CMP_RL}$	Comparator and reference ladder enable time	CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			1.5	2	µs
		CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			1.5	2	
		CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			15	25	
V_{CMP_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.9) / 32	VIN × (n + 1) / 32	VIN × (n + 1.1) / 32	V

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5.25.9 eUSCI

Table 5-35 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-35. eUSCI (UART Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	VCORE	VCC	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK External: UCLK Duty cycle = 50% ±10%	1.2 V			12	MHz
			1.4 V			24	
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)		1.2 V			5	MHz
			1.4 V			7	

Table 5-36 lists the characteristics of the eUSCI in UART mode.

Table 5-36. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0		5		20	ns
		UCGLITx = 1		20		60	
		UCGLITx = 2		30		100	
		UCGLITx = 3		50		150	

(1) Pulses on the UART receive input (UCxRX) that are shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-37 lists the supported clock frequencies of the eUSCI in SPI master mode.

Table 5-37. eUSCI (SPI Master Mode) Clock Frequency

PARAMETER		CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	SMCLK Duty cycle = 50% ±10%	VCORE = 1.2 V				12	MHz
			VCORE = 1.4 V				24	

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Table 5-38 lists the characteristics of the eUSCI in SPI master mode.

Table 5-38. eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10			1		UCxCLK cycles
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10			1		UCxCLK cycles
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10		1.62 V		30	ns
				3.7 V		20	ns
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10		1.62 V		20	ns
				3.7 V		15	ns
$t_{SU,MI}$	SOMI input data setup time		1.2 V	1.62 V	45		ns
			1.4 V	3.7 V	30		ns
$t_{HD,MI}$	SOMI input data hold time			1.62 V	0		ns
				3.7 V	0		ns
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF		1.62 V		14	ns
				3.7 V		7	ns
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF		1.62 V	0		ns
				3.7 V	0		ns

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} = max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-69 and Figure 5-70.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-69 and Figure 5-70.

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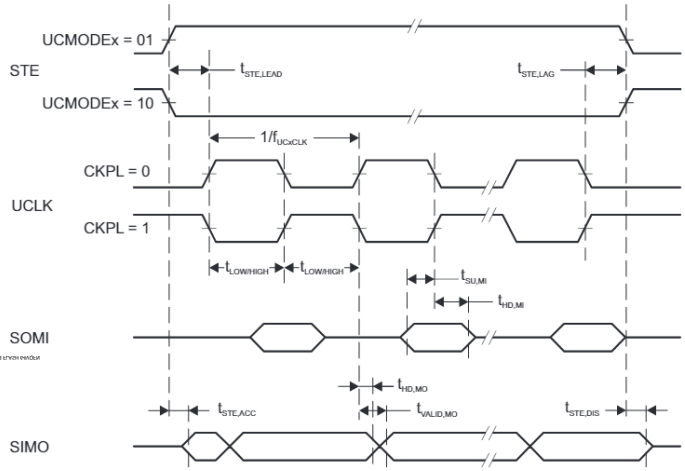


Figure 5-69. SPI Master Mode, CKPH = 0

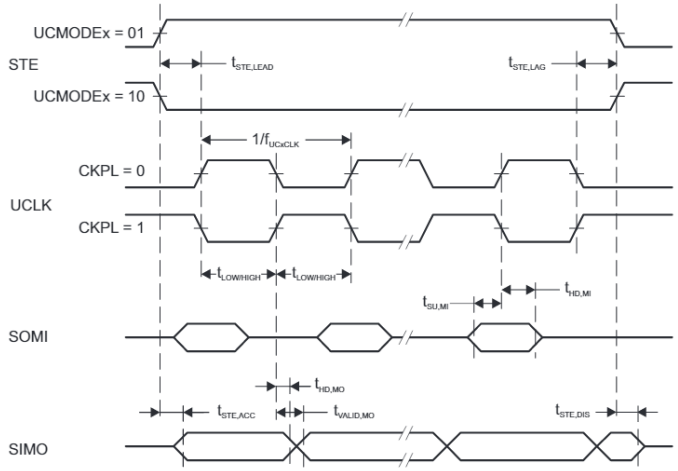


Figure 5-70. SPI Master Mode, CKPH = 1

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Table 5-39 lists the characteristics of the eUSCI in SPI slave mode.

Table 5-39. eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		1.62 V	45		ns
			3.7 V	20		
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		1.62 V	1		ns
			3.7 V	1		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		1.62 V		25	ns
			3.7 V		15	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		1.62 V		18	ns
			3.7 V		14	
$t_{SU,SI}$	SIMO input data setup time		1.62 V	3		ns
			3.7 V	2		
$t_{HD,SI}$	SIMO input data hold time		1.62 V	0		ns
			3.7 V	0		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	1.62 V		35	ns
			3.7 V		18	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF	1.62 V	10		ns
			3.7 V	6		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-71 and Figure 5-72.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-71 and Figure 5-72.

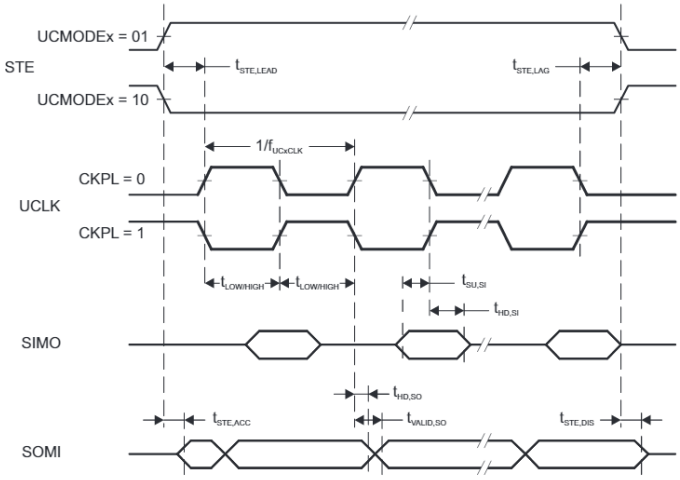


Figure 5-71. SPI Slave Mode, CKPH = 0

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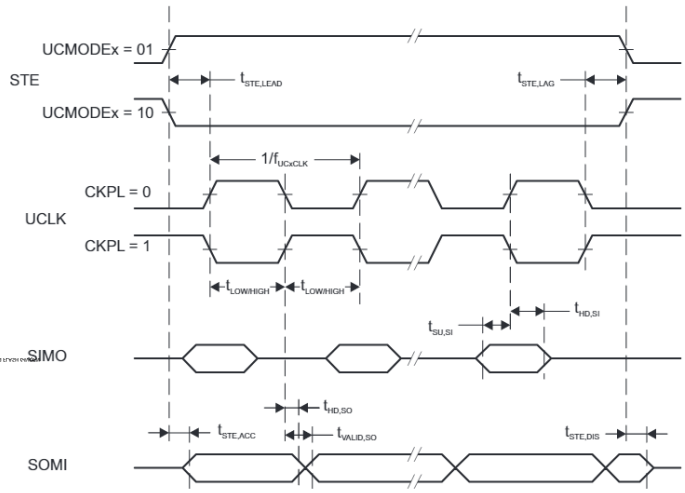


Figure 5-72. SPI Slave Mode, CKPH = 1

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Table 5-40 lists the supported clock frequencies of the eUSCI in I²C mode.

Table 5-40. eUSCI (I²C Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK External: UCLK Duty cycle = 50% ±10%	1.2 V			12	MHz
			1.4 V			24	
f_{SCL}	SCL clock frequency					1	MHz

Table 5-41 lists the characteristics of the eUSCI in I²C mode.

Table 5-41. eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-73)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	5.5			µs
		f_{SCL} = 400 kHz	1.5			
		f_{SCL} = 1 MHz	0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	5.5			µs
		f_{SCL} = 400 kHz	1.5			
		f_{SCL} = 1 MHz	0.6			
$t_{HD,DAT}$	Data hold time	f_{SCL} = 100 kHz	80			ns
		f_{SCL} = 400 kHz	80			
		f_{SCL} = 1 MHz	80			
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100 kHz	5.5			µs
		f_{SCL} = 400 kHz	1.5			
		f_{SCL} = 1 MHz	0.6			
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	5.5			µs
		f_{SCL} = 400 kHz	1.5			
		f_{SCL} = 1 MHz	0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	50		120	ns
		UCGLITx = 1	25		60	
		UCGLITx = 2	10		35	
		UCGLITx = 3	5		20	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1		27		ms
		UCCLTOx = 2		30		
		UCCLTOx = 3		33		

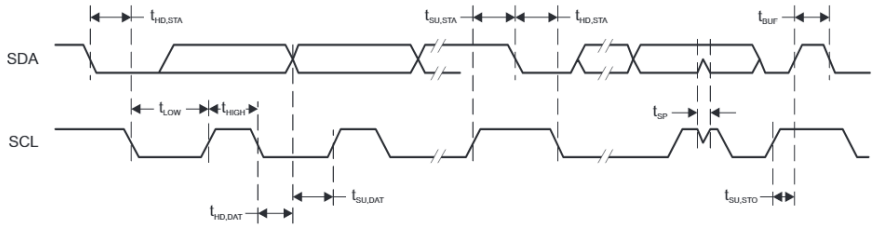


Figure 5-73. I²C Mode Timing

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5.25.10 Timers

Table 5-42 lists the characteristics of Timer_A.

Table 5-42. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK External: TACLK Duty cycle = 50% ±10%	1.2 V			12	MHz
			1.4 V			24	
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture			20		ns

Table 5-43 lists the characteristics of Timer32.

Table 5-43. Timer32

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
f_{T32}	Timer32 operating clock frequency(1)		1.2 V			24	MHz
			1.4 V			48	

(1) Timer32 operates on the same clock as the Cortex-M4 CPU.

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5.25.11 Memories

Table 5-44 lists the general characteristics of the flash memory.

Table 5-44. Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
$DVCC_{PGM/ERS}$	Supply voltage for program or erase	1.62	3.7	V
$I_{PGM/ERS, PEAK}$	Peak supply current from DVCC during program or erase		10	mA
$N_{Endurance}$	Program or erase endurance(1)	20000		cycles
$t_{Retention}$	Data retention duration	20		years

(1) Program or erase cycle for a bit is defined as the value of bit changing from 1 to 0 to 1.

Table 5-45 lists the characteristics of the flash operations using MSP432 peripheral driver libraries.

Table 5-45. Flash Operations Using MSP432 Peripheral Driver Libraries(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PGM_API, Word}$	Program time for 32-bit data using ROM_FlashCtl_programMemory() API	VCORE = 1.4 V, MCLK = 48 MHz		40	275	µs
$t_{PGM_API, Sector}$	Program time for 4KB of data (one sector) using ROM_FlashCtl_programMemory() API	VCORE = 1.4 V, MCLK = 48 MHz		4.5	71	ms
$t_{ERS_API, Sector}$	Sector erase time using ROM_FlashCtl_eraseSector() API	VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles <1k		9	309(2)	ms
		VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles >1k and <20k		9	3035(2)	ms
$t_{ERS_API, Mass-Erase}$	Mass erase time using ROM_FlashCtl_performMassErase() API	VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles <1k, MSP432P401R devices with 256KB of flash memory		12	19800(3)	ms
		VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles <1k, MSP432P401M devices with 128KB of flash memory		12	9900(3)	ms
I_{AVGPGM_API}	Average supply current from DVCC during program using ROM_FlashCtl_programMemory() API	VCORE = 1.2 V, MCLK = 3 MHz		5	7	mA
I_{AVGERS_API}	Average supply current from DVCC during erase using ROM_FlashCtl_eraseSector() API	VCORE = 1.2 V, MCLK = 3 MHz		2	3	mA

(1) MSP432 peripheral driver libraries executed from ROM.
(2) The maximum value is theoretically calculated by multiplying the typical value by N_{MAX_ERS} for the specific erase or program endurance.
(3) The maximum value is theoretically calculated by multiplying the typical value by N_{MAX_ERS} for the specific erase or program endurance and the total number of sectors in the flash main memory.

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Table 5-46 lists the characteristics of the flash stand-alone operations.

Table 5-46. Flash Stand-Alone Operations

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PGM, Immediate}$	Program time for one 32-bit data using immediate write mode	VER_PRE = 0, VER_PST = 1		40		µs
		VER_PRE = 1, VER_PST = 1		60		
$t_{PGM, Full-word}$	Program time for one 128-bit word using full word write mode	VER_PRE = 0, VER_PST = 1		40		µs
		VER_PRE = 1, VER_PST = 1		60		
$t_{PGM, Burst}$	Program time for 4×128-bit burst using burst write mode	AUTO_PRE = 0, AUTO_PST = 1		65		µs
		AUTO_PRE = 1, AUTO_PST = 1		85		
t_{ERS}	Time for sector erase or mass erase			9		ms
N_{MAX_PGM}	Maximum number of pulses to complete program operation				5	
N_{MAX_ERS}	Maximum number of pulses to complete erase operation	Number of erase or program cycles <1k			34	
		Number of erase or program cycles >1k and <20k			334	

Table 5-47 lists the characteristics of the SRAM.

Table 5-47. SRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SRAM_EN}	Current consumption of one SRAM bank when enabled	VCORE = 1.2 V		100	3500	nA
		VCORE = 1.4 V		300	5500	
I_{SRAM_RET}	Current consumption of one SRAM bank under retention	VCORE = 1.2 V		30	1250	nA
		VCORE = 1.4 V		35	1200	
$t_{SRAM_EN, one}$	Time taken to enable one SRAM bank			4	5	µs
$t_{SRAM_DIS, one}$	Time taken to disable one SRAM bank			4	5	µs
$t_{SRAM_EN, all}$	Time taken to enable all SRAM banks except Bank 0			7	8	µs
$t_{SRAM_DIS, all}$	Time taken to disable all SRAM banks except Bank 0			4	5	µs

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5.25.12 Emulation and Debug

Table 5-48 lists the characteristics of the JTAG interface.

Table 5-48. JTAG

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{TCK}	TCK clock frequency	0		10	MHz
t_{TCK}	TCK clock period	100			ns
t_{TCK_LOW}	TCK clock low time		$t_{TCK}/2$		ns
t_{TCK_HIGH}	TCK clock high time		$t_{TCK}/2$		ns
t_{TCK_RISE}	TCK rise time	0		10	ns
t_{TCK_FALL}	TCK fall time	0		10	ns
t_{TMS_SU}	TMS setup time to TCK rise	30			ns
t_{TMS_HLD}	TMS hold time from TCK rise	9			ns
t_{TDI_SU}	TDI setup time to TCK rise	20			ns
t_{TDI_HLD}	TDI hold time from TCK rise	7			ns
t_{TDO_ZDV}	TCK fall to data valid from high impedance		9	44	ns
t_{TDO_DV}	TCK fall to data valid from data valid		9	44	ns
t_{TDO_DVZ}	TCK fall to high impedance from data valid		8	38	ns

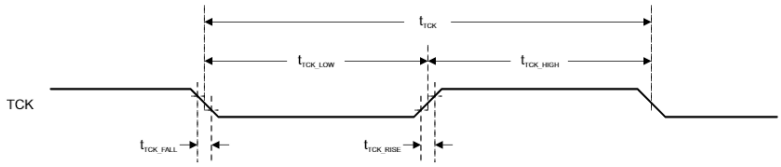


Figure 5-74. JTAG Test Clock Input Timing

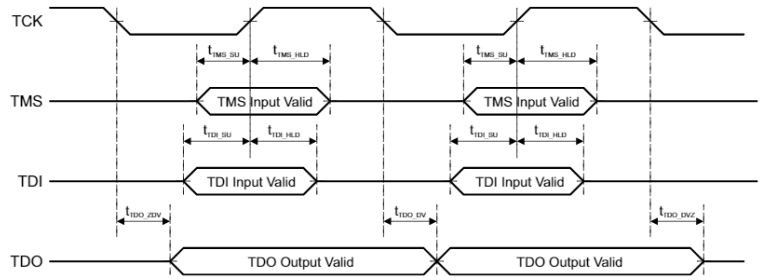


Figure 5-75. JTAG Test Access Port (TAP) Timing

6 Detailed Description

6.1 Overview

The MSP432P401x microcontroller is an ideal combination of the TI MSP430 low-power DNA, advance mixed-signal features, and the processing capabilities of the ARM 32-bit Cortex-M4 RISC engine. The microcontrollers ship with bundled driver libraries and are compatible with standard components of the ARM ecosystem.

6.2 Processor and Execution Features

The Cortex-M4 processor provides a high-performance low-cost platform that meets system requirements of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts. The Thumb®-2 mixed 16- and 32-bit instruction set of the processor delivers the high performance that is expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices (typically in the range of a few kilobytes of memory needed for microcontroller-class applications).

In the MSP432P401x MCUs, the Cortex-M4 processor can run up to 48 MHz, delivering high performance for the targeted class of applications, while at the same time maintaining ultra-low active power consumption.

6.2.1 Floating-Point Unit

The Cortex-M4 processor on the MSP432P401x MCUs includes a tightly coupled floating-point unit (FPU). The FPU is an IEEE 754 compliant single precision floating point module supporting add, subtract, multiply, divide, accumulate, and square-root operations. It also provides conversion between fixed-point and floating-point data formats and floating point constant instructions.

6.2.2 Memory Protection Unit

The Cortex-M4 processor on the MSP432P401x MCUs includes a tightly coupled memory protection unit (MPU) that supports up to eight protection regions. Applications can use the MPU to enforce memory privilege rules that isolate processes from each other or enforce memory access rules. These features are typically required for operating system handling purposes.

6.2.3 Nested Vectored Interrupt Controller (NVIC)

The NVIC supports up to 64 interrupts with eight levels of interrupt priority. The Cortex-M4 NVIC architecture allows for low latency, efficient interrupt and event handling, and seamless integration to device-level power-control strategies.

6.2.4 SysTick

The Cortex-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, and it is typically deployed either for operating system related purposes or as a general-purpose alarm mechanism.

6.2.5 Debug and Trace Features

The Cortex-M4 processor implements a complete hardware debug solution and provides high system visibility of the processor and memory through either a traditional 4-pin JTAG port or a 2-pin Serial Wire Debug (SWD) port, which is ideal for microcontrollers and other small-package devices. The SWJ-DP interface combines the SWD and JTAG debug ports into one module, which allows a seamless switch between the 2-pin and 4-pin modes of operation, depending on application needs.

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For system trace, the processor integrates an Instrumentation Trace Macrocell (ITM) alongside data watch points and a profiling unit. To enable simple and cost-effective profiling of the system trace events, a Serial Wire Viewer (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

NOTE

For detailed specifications and information on the programmer's model for the Cortex-M4 CPU and the associated peripherals mentioned throughout Section 6.2, see the appropriate reference manual at www.arm.com.

6.3 Memory Map

The device supports a 4GB address space that is divided into eight 512MB zones (see Figure 6-1).

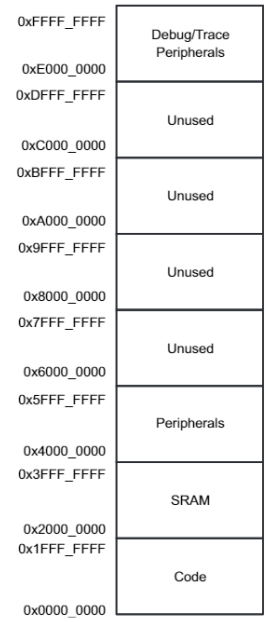


Figure 6-1. Device Memory Zones

6.3.1 Code Zone Memory Map

The region from 0x0000_0000 to 0x1FFF_FFFF is defined as the Code zone, and is accessible through the ICODE and DCODE buses of the Cortex-M4 processor and through the system DMA. This region maps the flash, the ROM, and the internal SRAM (permitting optimal single-cycle execution from the SRAM).

Figure 6-2 shows the MSP432P401x-specific memory map of the Code zone, as visible to the user code.

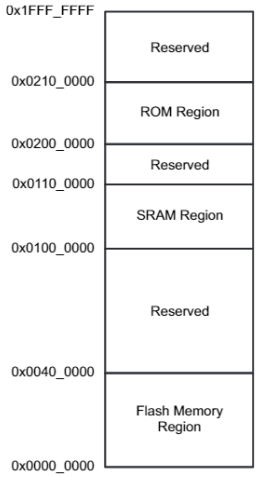


Figure 6-2. Code Zone Memory Map

6.3.1.1 Flash Memory Region

The 4MB region from 0x0000_0000 to 0x003F_FFFF is defined as the flash memory region. This region is further divided into different types of flash memory regions, which are explained in Section 6.4.1.

6.3.1.2 SRAM Region

The 1MB region from 0x0100_0000 to 0x010F_FFFF is defined as the SRAM region. This region is also aliased in the SRAM *zone* of the device, thereby allowing efficient access to the SRAM, both for instruction fetches and data reads. See Section 6.4.2 for more details.

6.3.1.3 ROM Region

The 1MB region from 0x0200_0000 to 0x020F_FFFF is defined as the ROM region. See Section 6.4.3 for details about the ROM.

6.3.2 SRAM Zone Memory Map

The SRAM zone of the device lies in the address range of 0x2000_0000 to 0x3FFF_FFFF. Figure 6-3 shows how this zone is divided.

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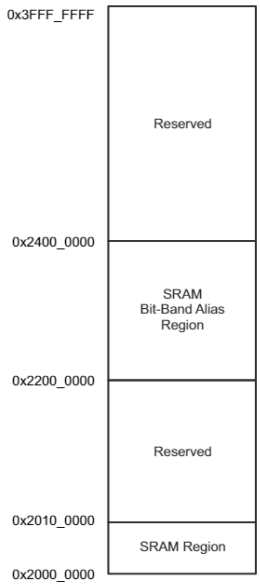


Figure 6-3. SRAM Zone Memory Map

6.3.2.1 SRAM Region

The 1MB region from 0x2000_0000 to 0x200F_FFFF is defined as the SRAM region. The SRAM accessible in this region is also aliased in the Code zone of the device, thereby allowing efficient access to the SRAM, both for instruction fetches and data reads. See Section 6.4.2 for details about the SRAM.

6.3.2.2 SRAM Bit-Band Alias Region

The 32MB region from 0x2200_0000 through 0x23FF_FFFF forms the bit-band alias region for the 1-MB SRAM region. Bit-banding is a feature of the Cortex-M4 processor and allows the application to set or clear individual bits throughout the SRAM space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

6.3.3 Peripheral Zone Memory Map

The Peripheral zone of the device lies in the address range of 0x4000_0000 to 0x5FFF_FFFF. Figure 6-4 shows how this range is further divided.

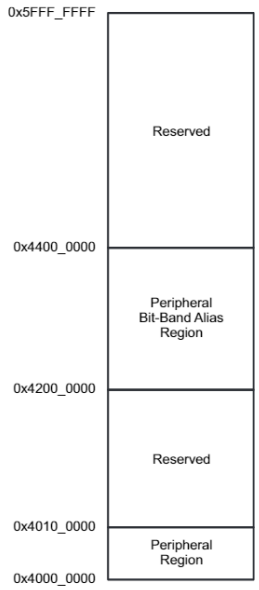


Figure 6-4. Peripheral Zone Memory Map

6.3.3.1 Peripheral Region

The 1MB region from 0x4000_0000 to 0x400F_FFFF is dedicated to the system and application control peripherals of the device. On the MSP432P401x MCUs, a total of 128KB of this region is dedicated for peripherals, while the rest is reserved. Table 6-1 lists the peripheral allocation within this 128-KB space. Note that all peripherals may not be available in all devices of the family (details in the REMARKS column). If a peripheral is listed as N/A for a particular device, treat the corresponding address space as reserved.

NOTE

Peripherals that are marked as 16-bit should be accessed through byte or half-word size read or write only. Any 32-bit access to these peripherals results in a bus error response.

Table 6-1. Peripheral Address Offsets

ADDRESS RANGE	PERIPHERAL	TABLE	REMARKS
0x4000_0000–0x4000_03FF	Timer_A0	Table 6-2	16-bit peripheral
0x4000_0400–0x4000_07FF	Timer_A1	Table 6-3	16-bit peripheral
0x4000_0800–0x4000_0BFF	Timer_A2	Table 6-4	16-bit peripheral
0x4000_0C00–0x4000_0FFF	Timer_A3	Table 6-5	16-bit peripheral
0x4000_1000–0x4000_13FF	eUSCI_A0	Table 6-6	16-bit peripheral
0x4000_1400–0x4000_17FF	eUSCI_A1	Table 6-7	16-bit peripheral
0x4000_1800–0x4000_1BFF	eUSCI_A2	Table 6-8	16-bit peripheral
0x4000_1C00–0x4000_1FFF	eUSCI_A3	Table 6-9	16-bit peripheral
0x4000_2000–0x4000_23FF	eUSCI_B0	Table 6-10	16-bit peripheral
0x4000_2400–0x4000_27FF	eUSCI_B1	Table 6-11	16-bit peripheral

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Table 6-1. Peripheral Address Offsets (continued)

ADDRESS RANGE	PERIPHERAL	TABLE	REMARKS
0x4000_2800–0x4000_2BFF	eUSCI_B2	Table 6-12	16-bit peripheral
0x4000_2C00–0x4000_2FFF	eUSCI_B3	Table 6-13	16-bit peripheral
0x4000_3000–0x4000_33FF	REF_A	Table 6-14	16-bit peripheral
0x4000_3400–0x4000_37FF	COMP_E0	Table 6-15	16-bit peripheral
0x4000_3800–0x4000_3BFF	COMP_E1	Table 6-16	16-bit peripheral
0x4000_3C00–0x4000_3FFF	AES256	Table 6-17	16-bit peripheral
0x4000_4000–0x4000_43FF	CRC32	Table 6-18	16-bit peripheral
0x4000_4400–0x4000_47FF	RTC_C	Table 6-19	16-bit peripheral
0x4000_4800–0x4000_4BFF	WDT_A	Table 6-20	16-bit peripheral
0x4000_4C00–0x4000_4FFF	Port Module	Table 6-21	16-bit peripheral
0x4000_5000–0x4000_53FF	Port Mapping Controller	Table 6-22	16-bit peripheral
0x4000_5400–0x4000_57FF	Capacitive Touch I/O 0	Table 6-23	16-bit peripheral
0x4000_5800–0x4000_5BFF	Capacitive Touch I/O 1	Table 6-24	16-bit peripheral
0x4000_5C00–0x4000_8FFF	Reserved		Read only, always reads 0h
0x4000_9000–0x4000_BFFF	Reserved		Read only, always reads 0h
0x4000_C000–0x4000_CFFF	Timer32	Table 6-25	
0x4000_D000–0x4000_DFFF	Reserved		Read only, always reads 0h
0x4000_E000–0x4000_FFFF	DMA	Table 6-26	
0x4001_0000–0x4001_03FF	PCM	Table 6-27	
0x4001_0400–0x4001_07FF	CS	Table 6-28	
0x4001_0800–0x4001_0FFF	PSS	Table 6-29	
0x4001_1000–0x4001_17FF	FLCTL	Table 6-30	
0x4001_1800–0x4001_1BFF	Reserved		Read only, always reads 0h
0x4001_1C00–0x4001_1FFF	Reserved		Read only, always reads 0h
0x4001_2000–0x4001_23FF	ADC14	Table 6-31	
0x4001_2400–0x4001_FFFF	Reserved		Read only, always reads 0h

Table 6-2. Timer_A0 Registers (Base Address: 0x4000_0000)

REGISTER NAME	ACRONYM	OFFSET
Timer_A0 Control	TA0CTL	00h
Timer_A0 Capture/Compare Control 0	TA0CCTL0	02h
Timer_A0 Capture/Compare Control 1	TA0CCTL1	04h
Timer_A0 Capture/Compare Control 2	TA0CCTL2	06h
Timer_A0 Capture/Compare Control 3	TA0CCTL3	08h
Timer_A0 Capture/Compare Control 4	TA0CCTL4	0Ah
Timer_A0 Counter	TA0R	10h
Timer_A0 Capture/Compare 0	TA0CCR0	12h
Timer_A0 Capture/Compare 1	TA0CCR1	14h
Timer_A0 Capture/Compare 2	TA0CCR2	16h
Timer_A0 Capture/Compare 3	TA0CCR3	18h
Timer_A0 Capture/Compare 4	TA0CCR4	1Ah
Timer_A0 Interrupt Vector	TA0IV	2Eh
Timer_A0 Expansion 0	TA0EX0	20h

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Table 6-3. Timer_A1 Registers (Base Address: 0x4000_0400)

REGISTER NAME	ACRONYM	OFFSET
Timer_A1 Control	TA1CTL	00h
Timer_A1 Capture/Compare Control 0	TA1CCTL0	02h
Timer_A1 Capture/Compare Control 1	TA1CCTL1	04h
Timer_A1 Capture/Compare Control 2	TA1CCTL2	06h
Timer_A1 Capture/Compare Control 3	TA1CCTL3	08h
Timer_A1 Capture/Compare Control 4	TA1CCTL4	0Ah
Timer_A1 Counter	TA1R	10h
Timer_A1 Capture/Compare 0	TA1CCR0	12h
Timer_A1 Capture/Compare 1	TA1CCR1	14h
Timer_A1 Capture/Compare 2	TA1CCR2	16h
Timer_A1 Capture/Compare 3	TA1CCR3	18h
Timer_A1 Capture/Compare 4	TA1CCR4	1Ah
Timer_A1 Interrupt Vector	TA1IV	2Eh
Timer_A1 Expansion 0	TA1EX0	20h

Table 6-4. Timer_A2 Registers (Base Address: 0x4000_0800)

REGISTER NAME	ACRONYM	OFFSET
Timer_A2 Control	TA2CTL	00h
Timer_A2 Capture/Compare Control 0	TA2CCTL0	02h
Timer_A2 Capture/Compare Control 1	TA2CCTL1	04h
Timer_A2 Capture/Compare Control 2	TA2CCTL2	06h
Timer_A2 Capture/Compare Control 3	TA2CCTL3	08h
Timer_A2 Capture/Compare Control 4	TA2CCTL4	0Ah
Timer_A2 Counter	TA2R	10h
Timer_A2 Capture/Compare 0	TA2CCR0	12h
Timer_A2 Capture/Compare 1	TA2CCR1	14h
Timer_A2 Capture/Compare 2	TA2CCR2	16h
Timer_A2 Capture/Compare 3	TA2CCR3	18h
Timer_A2 Capture/Compare 4	TA2CCR4	1Ah
Timer_A2 Interrupt Vector	TA2IV	2Eh
Timer_A2 Expansion 0	TA2EX0	20h

Table 6-5. Timer_A3 Registers (Base Address: 0x4000_0C00)

REGISTER NAME	ACRONYM	OFFSET
Timer_A3 Control	TA3CTL	00h
Timer_A3 Capture/Compare Control 0	TA3CCTL0	02h
Timer_A3 Capture/Compare Control 1	TA3CCTL1	04h
Timer_A3 Capture/Compare Control 2	TA3CCTL2	06h
Timer_A3 Capture/Compare Control 3	TA3CCTL3	08h
Timer_A3 Capture/Compare Control 4	TA3CCTL4	0Ah
Timer_A3 Counter	TA3R	10h
Timer_A3 Capture/Compare 0	TA3CCR0	12h
Timer_A3 Capture/Compare 1	TA3CCR1	14h
Timer_A3 Capture/Compare 2	TA3CCR2	16h
Timer_A3 Capture/Compare 3	TA3CCR3	18h
Timer_A3 Capture/Compare 4	TA3CCR4	1Ah
Timer_A3 Interrupt Vector	TA3IV	2Eh

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Table 6-5. Timer_A3 Registers (Base Address: 0x4000_0C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Timer_A3 Expansion 0	TA3EX0	20h

Table 6-6. eUSCI_A0 Registers (Base Address: 0x4000_1000)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A0 Control Word 0	UCA0CTLW0	00h
eUSCI_A0 Control Word 1	UCA0CTLW1	02h
eUSCI_A0 Baud Rate Control	UCA0BRW	06h
eUSCI_A0 Modulation Control	UCA0MCTLW	08h
eUSCI_A0 Status	UCA0STATW	0Ah
eUSCI_A0 Receive Buffer	UCA0RXBUF	0Ch
eUSCI_A0 Transmit Buffer	UCA0TXBUF	0Eh
eUSCI_A0 Auto Baud Rate Control	UCA0ABCTL	10h
eUSCI_A0 IrDA Control	UCA0IRCTL	12h
eUSCI_A0 Interrupt Enable	UCA0IE	1Ah
eUSCI_A0 Interrupt Flag	UCA0IFG	1Ch
eUSCI_A0 Interrupt Vector	UCA0IV	1Eh

Table 6-7. eUSCI_A1 Registers (Base Address: 0x4000_1400)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A1 Control Word 0	UCA1CTLW0	00h
eUSCI_A1 Control Word 1	UCA1CTLW1	02h
eUSCI_A1 Baud Rate Control	UCA1BRW	06h
eUSCI_A1 Modulation Control	UCA1MCTLW	08h
eUSCI_A1 Status	UCA1STATW	0Ah
eUSCI_A1 Receive Buffer	UCA1RXBUF	0Ch
eUSCI_A1 Transmit Buffer	UCA1TXBUF	0Eh
eUSCI_A1 Auto Baud Rate Control	UCA1ABCTL	10h
eUSCI_A1 IrDA Control	UCA1IRCTL	12h
eUSCI_A1 Interrupt Enable	UCA1IE	1Ah
eUSCI_A1 Interrupt Flag	UCA1IFG	1Ch
eUSCI_A1 Interrupt Vector	UCA1IV	1Eh

Table 6-8. eUSCI_A2 Registers (Base Address: 0x4000_1800)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A2 Control Word 0	UCA2CTLW0	00h
eUSCI_A2 Control Word 1	UCA2CTLW1	02h
eUSCI_A2 Baud Rate Control	UCA2BRW	06h
eUSCI_A2 Modulation Control	UCA2MCTLW	08h
eUSCI_A2 Status	UCA2STATW	0Ah
eUSCI_A2 Receive Buffer	UCA2RXBUF	0Ch
eUSCI_A2 Transmit Buffer	UCA2TXBUF	0Eh
eUSCI_A2 Auto Baud Rate Control	UCA2ABCTL	10h
eUSCI_A2 IrDA Control	UCA2IRCTL	12h
eUSCI_A2 Interrupt Enable	UCA2IE	1Ah
eUSCI_A2 Interrupt Flag	UCA2IFG	1Ch
eUSCI_A2 Interrupt Vector	UCA2IV	1Eh

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Table 6-9. eUSCI_A3 Registers (Base Address: 0x4000_1C00)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A3 Control Word 0	UCA3CTLW0	00h
eUSCI_A3 Control Word 1	UCA3CTLW1	02h
eUSCI_A3 Baud Rate Control	UCA3BRW	06h
eUSCI_A3 Modulation Control	UCA3MCTLW	08h
eUSCI_A3 Status	UCA3STATW	0Ah
eUSCI_A3 Receive Buffer	UCA3RXBUF	0Ch
eUSCI_A3 Transmit Buffer	UCA3TXBUF	0Eh
eUSCI_A3 Auto Baud Rate Control	UCA3ABCTL	10h
eUSCI_A3 IrDA Control	UCA3IRCTL	12h
eUSCI_A3 Interrupt Enable	UCA3IE	1Ah
eUSCI_A3 Interrupt Flag	UCA3IFG	1Ch
eUSCI_A3 Interrupt Vector	UCA3IV	1Eh

Table 6-10. eUSCI_B0 Registers (Base Address: 0x4000_2000)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B0 Control Word 0	UCB0CTLW0	00h
eUSCI_B0 Control Word 1	UCB0CTLW1	02h
eUSCI_B0 Bit Rate Control Word	UCB0BRW	06h
eUSCI_B0 Status Word	UCB0STATW	08h
eUSCI_B0 Byte Counter Threshold	UCB0TBCNT	0Ah
eUSCI_B0 Receive Buffer	UCB0RXBUF	0Ch
eUSCI_B0 Transmit Buffer	UCB0TXBUF	0Eh
eUSCI_B0 I2C Own Address 0	UCB0I2COA0	14h
eUSCI_B0 I2C Own Address 1	UCB0I2COA1	16h
eUSCI_B0 I2C Own Address 2	UCB0I2COA2	18h
eUSCI_B0 I2C Own Address 3	UCB0I2COA3	1Ah
eUSCI_B0 Received Address	UCB0ADDRX	1Ch
eUSCI_B0 Address Mask	UCB0ADDMASK	1Eh
eUSCI_B0 I2C Slave Address	UCB0I2CSA	20h
eUSCI_B0 Interrupt Enable	UCB0IE	2Ah
eUSCI_B0 Interrupt Flag	UCB0IFG	2Ch
eUSCI_B0 Interrupt Vector	UCB0IV	2Eh

Table 6-11. eUSCI_B1 Registers (Base Address: 0x4000_2400)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B1 Control Word 0	UCB1CTLW0	00h
eUSCI_B1 Control Word 1	UCB1CTLW1	02h
eUSCI_B1 Bit Rate Control Word	UCB1BRW	06h
eUSCI_B1 Status Word	UCB1STATW	08h
eUSCI_B1 Byte Counter Threshold	UCB1TBCNT	0Ah
eUSCI_B1 Receive Buffer	UCB1RXBUF	0Ch
eUSCI_B1 Transmit Buffer	UCB1TXBUF	0Eh
eUSCI_B1 I2C Own Address 0	UCB1I2COA0	14h
eUSCI_B1 I2C Own Address 1	UCB1I2COA1	16h
eUSCI_B1 I2C Own Address 2	UCB1I2COA2	18h
eUSCI_B1 I2C Own Address 3	UCB1I2COA3	1Ah
eUSCI_B1 Received Address	UCB1ADDRX	1Ch

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Table 6-11. eUSCI_B1 Registers (Base Address: 0x4000_2400) (continued)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B1 Address Mask	UCB1ADDMASK	1Eh
eUSCI_B1 I2C Slave Address	UCB1I2CSA	20h
eUSCI_B1 Interrupt Enable	UCB1IE	2Ah
eUSCI_B1 Interrupt Flag	UCB1IFG	2Ch
eUSCI_B1 Interrupt Vector	UCB1IV	2Eh

Table 6-12. eUSCI_B2 Registers (Base Address: 0x4000_2800)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B2 Control Word 0	UCB2CTLW0	00h
eUSCI_B2 Control Word 1	UCB2CTLW1	02h
eUSCI_B2 Bit Rate Control Word	UCB2BRW	06h
eUSCI_B2 Status Word	UCB2STATW	08h
eUSCI_B2 Byte Counter Threshold	UCB2TBCNT	0Ah
eUSCI_B2 Receive Buffer	UCB2RXBUF	0Ch
eUSCI_B2 Transmit Buffer	UCB2TXBUF	0Eh
eUSCI_B2 I2C Own Address 0	UCB2I2COA0	14h
eUSCI_B2 I2C Own Address 1	UCB2I2COA1	16h
eUSCI_B2 I2C Own Address 2	UCB2I2COA2	18h
eUSCI_B2 I2C Own Address 3	UCB2I2COA3	1Ah
eUSCI_B2 Received Address	UCB2ADDRX	1Ch
eUSCI_B2 Address Mask	UCB2ADDMASK	1Eh
eUSCI_B2 I2C Slave Address	UCB2I2CSA	20h
eUSCI_B2 Interrupt Enable	UCB2IE	2Ah
eUSCI_B2 Interrupt Flag	UCB2IFG	2Ch
eUSCI_B2 Interrupt Vector	UCB2IV	2Eh

Table 6-13. eUSCI_B3 Registers (Base Address: 0x4000_2C00)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B3 Control Word 0	UCB3CTLW0	00h
eUSCI_B3 Control Word 1	UCB3CTLW1	02h
eUSCI_B3 Bit Rate Control Word	UCB3BRW	06h
eUSCI_B3 Status Word	UCB3STATW	08h
eUSCI_B3 Byte Counter Threshold	UCB3TBCNT	0Ah
eUSCI_B3 Receive Buffer	UCB3RXBUF	0Ch
eUSCI_B3 Transmit Buffer	UCB3TXBUF	0Eh
eUSCI_B3 I2C Own Address 0	UCB3I2COA0	14h
eUSCI_B3 I2C Own Address 1	UCB3I2COA1	16h
eUSCI_B3 I2C Own Address 2	UCB3I2COA2	18h
eUSCI_B3 I2C Own Address 3	UCB3I2COA3	1Ah
eUSCI_B3 Received Address	UCB3ADDRX	1Ch
eUSCI_B3 Address Mask	UCB3ADDMASK	1Eh
eUSCI_B3 I2C Slave Address	UCB3I2CSA	20h
eUSCI_B3 Interrupt Enable	UCB3IE	2Ah
eUSCI_B3 Interrupt Flag	UCB3IFG	2Ch
eUSCI_B3 Interrupt Vector	UCB3IV	2Eh

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Table 6-14. REF_A Registers (Base Address: 0x4000_3000)

REGISTER NAME	ACRONYM	OFFSET
REF_A Control 0	REFCTL0	00h

Table 6-15. COMP_E0 Registers (Base Address: 0x4000_3400)

REGISTER NAME	ACRONYM	OFFSET
Comparator_E0 Control 0	CE0CTL0	00h
Comparator_E0 Control 1	CE0CTL1	02h
Comparator_E0 Control 2	CE0CTL2	04h
Comparator_E0 Control 3	CE0CTL3	06h
Comparator_E0 Interrupt	CE0INT	0Ch
Comparator_E0 Interrupt Vector Word	CE0IV	0Eh

Table 6-16. COMP_E1 Registers (Base Address: 0x4000_3800)

REGISTER NAME	ACRONYM	OFFSET
Comparator_E1 Control 0	CE1CTL0	00h
Comparator_E1 Control 1	CE1CTL1	02h
Comparator_E1 Control 2	CE1CTL2	04h
Comparator_E1 Control 3	CE1CTL3	06h
Comparator_E1 Interrupt	CE1INT	0Ch
Comparator_E1 Interrupt Vector Word	CE1IV	0Eh

Table 6-17. AES256 Registers (Base Address: 0x4000_3C00)

REGISTER NAME	ACRONYM	OFFSET
AES Accelerator Control 0	AESACTL0	00h
AES Accelerator Control 1	AESACTL1	02h
AES Accelerator Status	AESASTAT	04h
AES Accelerator Key	AESAKEY	06h
AES Accelerator Data In	AESADIN	08h
AES Accelerator Data Out	AESADOUT	0Ah
AES Accelerator XORed Data In	AESAXDIN	0Ch
AES Accelerator XORed Data In (no trigger)	AESAXIN	0Eh

Table 6-18. CRC32 Registers (Base Address: 0x4000_4000)

REGISTER NAME	ACRONYM	OFFSET
CRC32 Data Input Low	CRC32DI	000h
CRC32 Data In Reverse Low	CRC32DIRB	004h
CRC32 Initialization and Result Low	CRC32INIRES_LO	008h
CRC32 Initialization and Result High	CRC32INIRES_HI	00Ah
CRC32 Result Reverse Low	CRC32RESR_LO	00Ch
CRC32 Result Reverse High	CRC32RESR_HI	00Eh
CRC16 Data Input Low	CRC16DI	010h
CRC16 Data In Reverse Low	CRC16DIRB	014h
CRC16 Initialization and Result	CRC16INIRES	018h
CRC16 Result Reverse	CRC16RESR	01Eh

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Table 6-19. RTC_C Registers (Base Address: 0x4000_4400)

REGISTER NAME	ACRONYM	OFFSET
Real-Time Clock Control 0	RTCCTL0	00h
Real-Time Clock Control 1, 3	RTCCTL13	02h
Real-Time Clock Offset Calibration	RTCOCAL	04h
Real-Time Clock Temperature Compensation	RTCTCMP	06h
Real-Time Prescale Timer 0 Control	RTCPS0CTL	08h
Real-Time Prescale Timer 1 Control	RTCPS1CTL	0Ah
Real-Time Prescale Timer 0, 1 Counter	RTCPS	0Ch
Real Time Clock Interrupt Vector	RTCIV	0Eh
Real-Time Clock Seconds, Minutes	RTCTIM0	10h
Real-Time Clock Hour, Day of Week	RTCTIM1	12h
Real-Time Clock Date	RTCDATE	14h
Real-Time Clock Year	RTCYEAR	16h
Real-Time Clock Minutes, Hour Alarm	RTCAMINHR	18h
Real-Time Clock Day of Week, Day of Month Alarm	RTCADOWDAY	1Ah
Binary-to-BCD Conversion	RTCBIN2BCD	1Ch
BCD-to-Binary Conversion	RTCBCD2BIN	1Eh

Table 6-20. WDT_A Registers (Base Address: 0x4000_4800)

REGISTER NAME	ACRONYM	OFFSET
Watchdog Timer Control	WDTCTL	0Ch

Table 6-21. Port Registers (Base Address: 0x4000_4C00)

REGISTER NAME	ACRONYM	OFFSET
Port 1 Input	P1IN	000h
Port 2 Input	P2IN	001h
Port 1 Output	P1OUT	002h
Port 2 Output	P2OUT	003h
Port 1 Direction	P1DIR	004h
Port 2 Direction	P2DIR	005h
Port 1 Resistor Enable	P1REN	006h
Port 2 Resistor Enable	P2REN	007h
Port 2 Drive Strength	P2DS	009h
Port 1 Select 0	P1SEL0	00Ah
Port 2 Select 0	P2SEL0	00Bh
Port 1 Select 1	P1SEL1	00Ch
Port 2 Select 1	P2SEL1	00Dh
Port 1 Interrupt Vector	P1IV	00Eh
Port 1 Complement Selection	P1SELC	016h
Port 2 Complement Selection	P2SELC	017h
Port 1 Interrupt Edge Select	P1IES	018h
Port 2 Interrupt Edge Select	P2IES	019h
Port 1 Interrupt Enable	P1IE	01Ah
Port 2 Interrupt Enable	P2IE	01Bh
Port 1 Interrupt Flag	P1IFG	01Ch
Port 2 Interrupt Flag	P2IFG	01Dh
Port 2 Interrupt Vector	P2IV	01Eh
Port 3 Input	P3IN	020h

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Table 6-21. Port Registers (Base Address: 0x4000_4C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Port 4 Input	P4IN	021h
Port 3 Output	P3OUT	022h
Port 4 Output	P4OUT	023h
Port 3 Direction	P3DIR	024h
Port 4 Direction	P4DIR	025h
Port 3 Resistor Enable	P3REN	026h
Port 4 Resistor Enable	P4REN	027h
Port 3 Select 0	P3SEL0	02Ah
Port 4 Select 0	P4SEL0	02Bh
Port 3 Select 1	P3SEL1	02Ch
Port 4 Select 1	P4SEL1	02Dh
Port 3 Interrupt Vector	P3IV	02Eh
Port 3 Complement Selection	P3SELC	036h
Port 4 Complement Selection	P4SELC	037h
Port 3 Interrupt Edge Select	P3IES	038h
Port 4 Interrupt Edge Select	P4IES	039h
Port 3 Interrupt Enable	P3IE	03Ah
Port 4 Interrupt Enable	P4IE	03Bh
Port 3 Interrupt Flag	P3IFG	03Ch
Port 4 Interrupt Flag	P4IFG	03Dh
Port 4 Interrupt Vector	P4IV	03Eh
Port 5 Input	P5IN	040h
Port 6 Input	P6IN	041h
Port 5 Output	P5OUT	042h
Port 6 Output	P6OUT	043h
Port 5 Direction	P5DIR	044h
Port 6 Direction	P6DIR	045h
Port 5 Resistor Enable	P5REN	046h
Port 6 Resistor Enable	P6REN	047h
Port 5 Select 0	P5SEL0	04Ah
Port 6 Select 0	P6SEL0	04Bh
Port 5 Select 1	P5SEL1	04Ch
Port 6 Select 1	P6SEL1	04Dh
Port 5 Interrupt Vector	P5IV	04Eh
Port 5 Complement Selection	P5SELC	056h
Port 6 Complement Selection	P6SELC	057h
Port 5 Interrupt Edge Select	P5IES	058h
Port 6 Interrupt Edge Select	P6IES	059h
Port 5 Interrupt Enable	P5IE	05Ah
Port 6 Interrupt Enable	P6IE	05Bh
Port 5 Interrupt Flag	P5IFG	05Ch
Port 6 Interrupt Flag	P6IFG	05Dh
Port 6 Interrupt Vector	P6IV	05Eh
Port 7 Input	P7IN	060h
Port 8 Input	P8IN	061h
Port 7 Output	P7OUT	062h
Port 8 Output	P8OUT	063h

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Table 6-21. Port Registers (Base Address: 0x4000_4C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Port 7 Direction	P7DIR	064h
Port 8 Direction	P8DIR	065h
Port 7 Resistor Enable	P7REN	066h
Port 8 Resistor Enable	P8REN	067h
Port 7 Select 0	P7SEL0	06Ah
Port 8 Select 0	P8SEL0	06Bh
Port 7 Select 1	P7SEL1	06Ch
Port 8 Select 1	P8SEL1	06Dh
Port 7 Interrupt Vector	P7IV	06Eh
Port 7 Complement Selection	P7SELC	076h
Port 8 Complement Selection	P8SELC	077h
Port 7 Interrupt Edge Select	P7IES	078h
Port 8 Interrupt Edge Select	P8IES	079h
Port 7 Interrupt Enable	P7IE	07Ah
Port 8 Interrupt Enable	P8IE	07Bh
Port 7 Interrupt Flag	P7IFG	07Ch
Port 8 Interrupt Flag	P8IFG	07Dh
Port 8 Interrupt Vector	P8IV	07Eh
Port 9 Input	P9IN	080h
Port 10 Input	P10IN	081h
Port 9 Output	P9OUT	082h
Port 10 Output	P10OUT	083h
Port 9 Direction	P9DIR	084h
Port 10 Direction	P10DIR	085h
Port 9 Resistor Enable	P9REN	086h
Port 10 Resistor Enable	P10REN	087h
Port 9 Select 0	P9SEL0	08Ah
Port 10 Select 0	P10SEL0	08Bh
Port 9 Select 1	P9SEL1	08Ch
Port 10 Select 1	P10SEL1	08Dh
Port 9 Interrupt Vector	P9IV	08Eh
Port 9 Complement Selection	P9SELC	096h
Port 10 Complement Selection	P10SELC	097h
Port 9 Interrupt Edge Select	P9IES	098h
Port 10 Interrupt Edge Select	P10IES	099h
Port 9 Interrupt Enable	P9IE	09Ah
Port 10 Interrupt Enable	P10IE	09Bh
Port 9 Interrupt Flag	P9IFG	09Ch
Port 10 Interrupt Flag	P10IFG	09Dh
Port 10 Interrupt Vector	P10IV	09Eh
Port J Input	PJIN	120h
Port J Output	PJOUT	122h
Port J Direction	PJDIR	124h
Port J Resistor Enable	PJREN	126h
Port J Select 0	PJSEL0	12Ah
Port J Select 1	PJSEL1	12Ch
Port J Complement Select	PJSELC	136h

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Table 6-22. PMAP Registers (Base Address: 0x4000_5000)

REGISTER NAME	ACRONYM	OFFSET
Port Mapping Key	PMAPKEYID	00h
Port Mapping Control	PMAPCTL	02h
Port Mapping P2.0	P2MAP0	10h
Port Mapping P2.1	P2MAP1	11h
Port Mapping P2.2	P2MAP2	12h
Port Mapping P2.3	P2MAP3	13h
Port Mapping P2.4	P2MAP4	14h
Port Mapping P2.5	P2MAP5	15h
Port Mapping P2.6	P2MAP6	16h
Port Mapping P2.7	P2MAP7	17h
Port Mapping P3.0	P3MAP0	18h
Port Mapping P3.1	P3MAP1	19h
Port Mapping P3.2	P3MAP2	1Ah
Port Mapping P3.3	P3MAP3	1Bh
Port Mapping P3.4	P3MAP4	1Ch
Port Mapping P3.5	P3MAP5	1Dh
Port Mapping P3.6	P3MAP6	1Eh
Port Mapping P3.7	P3MAP7	1Fh
Port Mapping P7.0	P7MAP0	38h
Port Mapping P7.1	P7MAP1	39h
Port Mapping P7.2	P7MAP2	3Ah
Port Mapping P7.3	P7MAP3	3Bh
Port Mapping P7.4	P7MAP4	3Ch
Port Mapping P7.5	P7MAP5	3Dh
Port Mapping P7.6	P7MAP6	3Eh
Port Mapping P7.7	P7MAP7	3Fh

Table 6-23. Capacitive Touch I/O 0 Registers (Base Address: 0x4000_5400)

REGISTER NAME	ACRONYM	OFFSET
Capacitive Touch I/O 0 Control	CAPTIO0CTL	0Eh

Table 6-24. Capacitive Touch I/O 1 Registers (Base Address: 0x4000_5800)

REGISTER NAME	ACRONYM	OFFSET
Capacitive Touch I/O 1 Control	CAPTIO1CTL	0Eh

Table 6-25. Timer32 Registers (Base Address: 0x4000_C000)

REGISTER NAME	ACRONYM	OFFSET
Timer 1 Load	T32LOAD1	00h
Timer 1 Current Value	T32VALUE1	04h
Timer 1 Timer Control	T32CONTROL1	08h
Timer 1 Interrupt Clear	T32INTCLR1	0Ch
Timer 1 Raw Interrupt Status	T32RIS1	10h
Timer 1 Interrupt Status	T32MIS1	14h
Timer 1 Background Load	T32BGLOAD1	18h
Timer 2 Load	T32LOAD2	20h
Timer 2 Current Value	T32VALUE2	24h

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Table 6-25. Timer32 Registers (Base Address: 0x4000_C000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Timer 2 Timer Control	T32CONTROL2	28h
Timer 2 Interrupt Clear	T32INTCLR2	2Ch
Timer 2 Raw Interrupt Status	T32RIS2	30h
Timer 2 Interrupt Status	T32MIS2	34h
Timer 2 Background Load	T32BGLOAD2	38h

Table 6-26. DMA Registers (Base Address: 0x4000_E000)

REGISTER NAME	ACRONYM	OFFSET
Device Configuration Status	DMA_DEVICE_CFG	000h
Software Channel Trigger	DMA_SW_CHTRIG	004h
Channel 0 Source Configuration	DMA_CH0_SRCCFG	010h
Channel 1 Source Configuration	DMA_CH1_SRCCFG	014h
Channel 2 Source Configuration	DMA_CH2_SRCCFG	018h
Channel 3 Source Configuration	DMA_CH3_SRCCFG	01Ch
Channel 4 Source Configuration	DMA_CH4_SRCCFG	020h
Channel 5 Source Configuration	DMA_CH5_SRCCFG	024h
Channel 6 Source Configuration	DMA_CH6_SRCCFG	028h
Channel 7 Source Configuration	DMA_CH7_SRCCFG	02Ch
Interrupt 1 Source Channel Configuration	DMA_INT1_SRCCFG	100h
Interrupt 2 Source Channel Configuration	DMA_INT2_SRCCFG	104h
Interrupt 3 Source Channel Configuration	DMA_INT3_SRCCFG	108h
Interrupt 0 Source Channel Flag	DMA_INT0_SRCFLG	110h
Interrupt 0 Source Channel Clear Flag	DMA_INT0_CLRFLG	114h
Status	DMA_STAT	1000h
Configuration	DMA_CFG	1004h
Channel Control Data Base Pointer	DMA_CTLBASE	1008h
Channel Alternate Control Data Base Pointer	DMA_ALTBASE	100Ch
Channel Wait on Request Status	DMA_WAITSTAT	1010h
Channel Software Request	DMA_SWREQ	1014h
Channel Useburst Set	DMA_USEBURSTSET	1018h
Channel Useburst Clear	DMA_USEBURSTCLR	101Ch
Channel Request Mask Set	DMA_REQMASKSET	1020h
Channel Request Mask Clear	DMA_REQMASKCLR	1024h
Channel Enable Set	DMA_ENASET	1028h
Channel Enable Clear	DMA_ENACLR	102Ch
Channel Primary-Alternate Set	DMA_ALTSET	1030h
Channel Primary-Alternate Clear	DMA_ALTCLR	1034h
Channel Priority Set	DMA_PRIOSET	1038h
Channel Priority Clear	DMA_PRIOCLR	103Ch
Bus Error Clear	DMA_ERRCLR	104Ch

Table 6-27. PCM Registers (Base Address: 0x4001_0000)

REGISTER NAME	ACRONYM	OFFSET
Control 0	PCMCTL0	00h
Control 1	PCMCTL1	04h
Interrupt Enable	PCMIE	08h
Interrupt Flag	PCMIFG	0Ch

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Table 6-27. PCM Registers (Base Address: 0x4001_0000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Clear Interrupt Flag	PCMCLRIFG	10h

Table 6-28. CS Registers (Base Address: 0x4001_0400)

REGISTER NAME	ACRONYM	OFFSET
Key	CSKEY	00h
Control 0	CSCTL0	04h
Control 1	CSCTL1	08h
Control 2	CSCTL2	0Ch
Control 3	CSCTL3	10h
Clock Enable	CSCLKEN	30h
Status	CSSTAT	34h
Interrupt Enable	CSIE	40h
Interrupt Flag	CSIFG	48h
Clear Interrupt Flag	CSCLRIFG	50h
Set Interrupt Flag	CSSETIFG	58h
DCO External Resistor Calibration 0	CSDCOERCAL0	60h
DCO External Resistor Calibration 1	CSDCOERCAL1	64h

Table 6-29. PSS Registers (Base Address: 0x4001_0800)

REGISTER NAME	ACRONYM	OFFSET
Key	PSSKEY	00h
Control 0	PSSCTL0	04h
Interrupt Enable	PSSIE	34h
Interrupt Flag	PSSIFG	38h
Clear Interrupt Flag	PSSCLRIFG	3Ch

Table 6-30. FLCTL Registers (Base Address: 0x4001_1000)

REGISTER NAME	ACRONYM	OFFSET
Power Status	FLCTL_POWER_STAT	000h
Bank 0 Read Control	FLCTL_BANK0_RDCTL	010h
Bank 1 Read Control	FLCTL_BANK1_RDCTL	014h
Read Burst/Compare Control and Status	FLCTL_RDBRST_CTLSTAT	020h
Read Burst/Compare Start Address	FLCTL_RDBRST_STARTADDR	024h
Read Burst/Compare Length	FLCTL_RDBRST_LEN	028h
Read Burst/Compare Fail Address	FLCTL_RDBRST_FAILADDR	03Ch
Read Burst/Compare Fail Count	FLCTL_RDBRST_FAILCNT	040h
Program Control and Status	FLCTL_PRG_CTLSTAT	050h
Program Burst Control and Status	FLCTL_PRGBRST_CTLSTAT	054h
Program Burst Start Address	FLCTL_PRGBRST_STARTADDR	058h
Program Burst Data0 0	FLCTL_PRGBRST_DATA0_0	060h
Program Burst Data0 1	FLCTL_PRGBRST_DATA0_1	064h
Program Burst Data0 2	FLCTL_PRGBRST_DATA0_2	068h
Program Burst Data0 3	FLCTL_PRGBRST_DATA0_3	06Ch
Program Burst Data1 0	FLCTL_PRGBRST_DATA1_0	070h
Program Burst Data1 1	FLCTL_PRGBRST_DATA1_1	074h
Program Burst Data1 2	FLCTL_PRGBRST_DATA1_2	078h

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Table 6-30. FLCTL Registers (Base Address: 0x4001_1000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Program Burst Data1 3	FLCTL_PRGBRST_DATA1_3	07Ch
Program Burst Data2 0	FLCTL_PRGBRST_DATA2_0	080h
Program Burst Data2 1	FLCTL_PRGBRST_DATA2_1	084h
Program Burst Data2 2	FLCTL_PRGBRST_DATA2_2	088h
Program Burst Data2 3	FLCTL_PRGBRST_DATA2_3	08Ch
Program Burst Data3 0	FLCTL_PRGBRST_DATA3_0	090h
Program Burst Data3 1	FLCTL_PRGBRST_DATA3_1	094h
Program Burst Data3 2	FLCTL_PRGBRST_DATA3_2	098h
Program Burst Data3 3	FLCTL_PRGBRST_DATA3_3	09Ch
Erase Control and Status	FLCTL_ERASE_CTLSTAT	0A0h
Erase Sector Address	FLCTL_ERASE_SECTADDR	0A4h
Information Memory Bank 0 Write/Erase Protection	FLCTL_BANK0_INFO_WEPROT	0B0h
Main Memory Bank 0 Write/Erase Protection	FLCTL_BANK0_MAIN_WEPROT	0B4h
Information Memory Bank 1 Write/Erase Protection	FLCTL_BANK1_INFO_WEPROT	0C0h
Main Memory Bank 1 Write/Erase Protection	FLCTL_BANK1_MAIN_WEPROT	0C4h
Benchmark Control and Status	FLCTL_BMRK_CTLSTAT	0D0h
Benchmark Instruction Fetch Count	FLCTL_BMRK_IFETCH	0D4h
Benchmark Data Read Count	FLCTL_BMRK_DREAD	0D8h
Benchmark Count Compare	FLCTL_BMRK_CMP	0DCh
Interrupt Flag	FLCTL_IFG	0F0h
Interrupt Enable	FLCTL_IE	0F4h
Clear Interrupt Flag	FLCTL_CLRIFG	0F8h
Set Interrupt Flag	FLCTL_SETIFG	0FCh
Read Timing Control	FLCTL_READ_TIMCTL	100h
Read Margin Timing Control	FLCTL_READMARGIN_TIMCTL	104h
Program Verify Timing Control	FLCTL_PRGVER_TIMCTL	108h
Erase Verify Timing Control	FLCTL_ERSVER_TIMCTL	10Ch
Program Timing Control	FLCTL_PROGRAM_TIMCTL	114h
Erase Timing Control	FLCTL_ERASE_TIMCTL	118h
Mass Erase Timing Control	FLCTL_MASSERASE_TIMCTL	11Ch
Burst Program Timing Control	FLCTL_BURSTPRG_TIMCTL	120h

Table 6-31. ADC14 Registers (Base Address: 0x4001_2000)

REGISTER NAME	ACRONYM	OFFSET
Control 0	ADC14CTL0	00h
Control 1	ADC14CTL1	04h
Window Comparator Low Threshold 0	ADC14LO0	08h
Window Comparator High Threshold 0	ADC14HI0	0Ch
Window Comparator Low Threshold 1	ADC14LO1	10h
Window Comparator High Threshold 1	ADC14HI1	14h
Memory Control 0	ADC14MCTL0	18h
Memory Control 1	ADC14MCTL1	1Ch
Memory Control 2	ADC14MCTL2	20h
Memory Control 3	ADC14MCTL3	24h
Memory Control 4	ADC14MCTL4	28h
Memory Control 5	ADC14MCTL5	2Ch
Memory Control 6	ADC14MCTL6	30h

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Table 6-31. ADC14 Registers (Base Address: 0x4001_2000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Memory Control 7	ADC14MCTL7	34h
Memory Control 8	ADC14MCTL8	38h
Memory Control 9	ADC14MCTL9	3Ch
Memory Control 10	ADC14MCTL10	40h
Memory Control 11	ADC14MCTL11	44h
Memory Control 12	ADC14MCTL12	48h
Memory Control 13	ADC14MCTL13	4Ch
Memory Control 14	ADC14MCTL14	50h
Memory Control 15	ADC14MCTL15	54h
Memory Control 16	ADC14MCTL16	58h
Memory Control 17	ADC14MCTL17	5Ch
Memory Control 18	ADC14MCTL18	60h
Memory Control 19	ADC14MCTL19	64h
Memory Control 20	ADC14MCTL20	68h
Memory Control 21	ADC14MCTL21	6Ch
Memory Control 22	ADC14MCTL22	70h
Memory Control 23	ADC14MCTL23	74h
Memory Control 24	ADC14MCTL24	78h
Memory Control 25	ADC14MCTL25	7Ch
Memory Control 26	ADC14MCTL26	80h
Memory Control 27	ADC14MCTL27	84h
Memory Control 28	ADC14MCTL28	88h
Memory Control 29	ADC14MCTL29	8Ch
Memory Control 30	ADC14MCTL30	90h
Memory Control 31	ADC14MCTL31	94h
Memory 0	ADC14MEM0	98h
Memory 1	ADC14MEM1	9Ch
Memory 2	ADC14MEM2	A0h
Memory 3	ADC14MEM3	A4h
Memory 4	ADC14MEM4	A8h
Memory 5	ADC14MEM5	ACh
Memory 6	ADC14MEM6	B0h
Memory 7	ADC14MEM7	B4h
Memory 8	ADC14MEM8	B8h
Memory 9	ADC14MEM9	BCh
Memory 10	ADC14MEM10	C0h
Memory 11	ADC14MEM11	C4h
Memory 12	ADC14MEM12	C8h
Memory 13	ADC14MEM13	CCh
Memory 14	ADC14MEM14	D0h
Memory 15	ADC14MEM15	D4h
Memory 16	ADC14MEM16	D8h
Memory 17	ADC14MEM17	DCh
Memory 18	ADC14MEM18	E0h
Memory 19	ADC14MEM19	E4h
Memory 20	ADC14MEM20	E8h
Memory 21	ADC14MEM21	ECh

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Table 6-31. ADC14 Registers (Base Address: 0x4001_2000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Memory 22	ADC14MEM22	F0h
Memory 23	ADC14MEM23	F4h
Memory 24	ADC14MEM24	F8h
Memory 25	ADC14MEM25	FCh
Memory 26	ADC14MEM26	100
Memory 27	ADC14MEM27	104
Memory 28	ADC14MEM28	108
Memory 29	ADC14MEM29	10C
Memory 30	ADC14MEM30	110h
Memory 31	ADC14MEM31	114h
Interrupt Enable 0	ADC14IER0	13Ch
Interrupt Enable 1	ADC14IER1	140h
Interrupt Flag 0	ADC14IFGR0	144h
Interrupt Flag 1	ADC14IFGR1	148h
Clear Interrupt Flag 0	ADC14CLRIFGR0	14Ch
Clear Interrupt Flag 1	ADC14CLRIFGR1	150h
Interrupt Vector	ADC14IV	154h

6.3.3.2 Peripheral Bit Band Alias Region

The 32MB region from 0x4200_0000 through 0x43FF_FFFF forms the bit-band alias region for the 1MB peripheral region. Bit-banding is a feature of the Cortex-M4 processor and allows the application to set or clear individual bits throughout the peripheral memory space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

NOTE

The restriction of accessing 16-bit peripherals only through byte or half-word accesses also applies to the corresponding bit-band region of these peripherals. In other words, writes to the bit-band alias region for these peripherals must be in the form of byte or half-word accesses only.

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6.3.4 Debug and Trace Peripheral Zone

This zone maps the internal and external PPB regions of the Cortex-M4 (see Table 6-32). The following peripherals are mapped to this zone:

- Core and System debug control registers (internal PPB)
- NVIC and other registers in the System Control space of the Cortex-M4 (internal PPB)
- FPB, DWT, ITM (internal PPB)
- TPIU, Debug ROM table (external PPB)
- Reset Controller (external PPB)
- System Controller (external PPB)

Table 6-32. Debug Zone Memory Map

ADDRESS RANGE	MODULE OR PERIPHERAL	REMARKS
0xE000_0000–0xE000_0FFF	ITM	Internal PPB
0xE000_1000–0xE000_1FFF	DWT	Internal PPB
0xE000_2000–0xE000_2FFF	FPB	Internal PPB
0xE000_3000–0xE000_DFFF	Reserved	Internal PPB
0xE000_E000–0xE000_EFFF	Cortex-M4 System Control Space	Internal PPB
0xE000_F000–0xE003_FFFF	Reserved	Internal PPB
0xE004_0000–0xE004_0FFF	TPIU	External PPB
0xE004_1000–0xE004_1FFF	Reserved	External PPB
0xE004_2000–0xE004_23FF	Reset Controller (see Table 6-33)	External PPB
0xE004_2400–0xE004_2FFF	Reserved	External PPB
0xE004_3000–0xE004_33FF	System Controller (see Table 6-34)	External PPB
0xE004_3400–0xE004_3FFF	Reserved	External PPB
0xE004_4000–0xE004_43FF	System Controller	External PPB
0xE004_4400–0xE00F_EFFF	Reserved	External PPB
0xE00F_F000–0xE00F_FFFF	ROM Table (External PPB)	External PPB
0xE010_0000–0xFFFF_FFFF	Reserved	Vendor Space

NOTE

For the address maps of the ARM modules listed in Table 6-32, see the Cortex-M4 technical reference manual at www.arm.com.

Table 6-33. RSTCTL Registers

REGISTER NAME	ACRONYM	OFFSET
Reset Request	RSTCTL_RESET_REQ	000h
Hard Reset Status	RSTCTL_HARDRESET_STAT	004h
Hard Reset Status Clear	RSTCTL_HARDRESET_CLR	008h
Hard Reset Status Set	RSTCTL_HARDRESET_SET	00Ch
Soft Reset Status	RSTCTL_SOFTRESET_STAT	010h
Soft Reset Status Clear	RSTCTL_SOFTRESET_CLR	014h
Soft Reset Status Set	RSTCTL_SOFTRESET_SET	018h
PSS Reset Status	RSTCTL_PSSRESET_STAT	100h
PSS Reset Status Clear	RSTCTL_PSSRESET_CLR	104h
PCM Reset Status	RSTCTL_PCMRESET_STAT	108h
PCM Reset Status Clear	RSTCTL_PCMRESET_CLR	10Ch
Pin Reset Status	RSTCTL_PINRESET_STAT	110h

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Table 6-33. RSTCTL Registers (continued)

REGISTER NAME	ACRONYM	OFFSET
Pin Reset Status Clear	RSTCTL_PINRESET_CLR	114h
Reboot Reset Status	RSTCTL_REBOOTRESET_STAT	118h
Reboot Reset Status Clear	RSTCTL_REBOOTRESET_CLR	11Ch
CS Reset Status	RSTCTL_CSRESET_STAT	120h
CS Reset Status Clear	RSTCTL_CSRESET_CLR	124h

Table 6-34. SYSCTL Registers

REGISTER NAME	ACRONYM	OFFSET
Reboot Control	SYS_REBOOT_CTL	0000h
NMI Control and Status	SYS_NMI_CTLSTAT	0004h
Watchdog Reset Control	SYS_WDTRESET_CTL	0008h
Peripheral Halt Control	SYS_PERIHALT_CTL	000Ch
SRAM Size	SYS_SRAM_SIZE	0010h
SRAM Bank Enable	SYS_SRAM_BANKEN	0014h
SRAM Bank Retention Control	SYS_SRAM_BANKRET	0018h
Flash Size	SYS_FLASH_SIZE	0020h
Digital I/O Glitch Filter Control	SYS_DIO_GLTFLT_CTL	0030h
IP Protected Secure Zone Data Access Unlock	SYS_SECDATA_UNLOCK	0040h
Master Unlock	SYS_MASTER_UNLOCK	1000h
Boot Override Request 0	SYS_BOOTOVER_REQ0	1004h
Boot Override Request 1	SYS_BOOTOVER_REQ1	1008h
Boot Override Acknowledge	SYS_BOOTOVER_ACK	100Ch
Reset Request	SYS_RESET_REQ	1010h
Reset Status and Override	SYS_RESET_STATOVER	1014h
System Status	SYS_SYSTEM_STAT	1020h

6.4 Memories on the MSP432P401x

The MSP432P401x MCUs include flash memory and SRAM for general application purposes. In addition, the devices include a backup memory (a portion of total available SRAM) that is retained in low-power modes.

6.4.1 Flash Memory

The MSP432P401x MCUs include a high-endurance low-power flash memory that supports up to a minimum of 20000 write or erase cycles. The flash memory is 128 bits wide, thereby enabling high code execution performance by virtue of each fetch returning up to four 32-bit instructions (or up to eight 16-bit instructions). The flash is further divided into two types of subregions: main memory and information memory.

From a physical perspective, the flash memory comprises two banks, with the main and information memory regions divided equally between the two banks. This permits an application to carry out a simultaneous read or execute operation from one bank while the other bank may be undergoing a program or erase operation.

Figure 6-5 shows the memory map of the flash on MSP432P401x MCUs.

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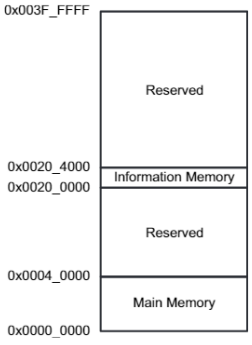


Figure 6-5. Flash Memory Map

6.4.1.1 Flash Main Memory (0x0000_0000 to 0x0003_FFFF)

The flash main memory on MSP432P401x MCUs can be up to 256KB. Flash main memory consists of up to 64 sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). The main memory can be viewed as two independent identical banks of up to 128KB each, allowing simultaneous read or execute from one bank while the other bank is undergoing a program or erase operation.

6.4.1.2 Flash Information Memory (0x0020_0000 to 0x0020_3FFF)

The flash information memory region is 16KB. Flash information memory consists of four sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). Table 6-35 describes different regions of flash information memory and the contents of each of the regions. The flash information memory region that contains the device descriptor (TLV) is factory configured for protection against write and erase operations.

Table 6-35. Flash Information Memory Regions

REGION	ADDRESS RANGE	CONTENTS	WRITE AND ERASE PROTECTED?
Bank 0, Sector 0	0x0020_0000–0x0020_0FFF	Flash Boot-override Mailbox	No
Bank 0, Sector 1	0x0020_1000–0x0020_1FFF	Device Descriptor (TLV)	Yes
Bank 1, Sector 0	0x0020_2000–0x0020_2FFF	TI BSL	No
Bank 1, Sector 1	0x0020_3000–0x0020_3FFF	TI BSL	No

6.4.1.3 Flash Operation

The flash memory provides multiple read and program modes of operation that the application can deploy. Up to 128 bits (memory word width) can be programmed (set from 1 to 0) in a single program operation. Although the CPU data buses are 32 bits wide, the flash can buffer 128-bit write data before initiating flash programming, thereby making it more seamless and power efficient for software to program large blocks of data at a time. In addition, the flash memory also supports a burst write mode that takes less time when compared to programming words individually. See Table 5-44 for information on timing parameters.

The flash main and information memory regions offer write/erase protection control at a sector granularity to enable software to optimize operations like mass erase while protecting certain regions of the flash. In low-power modes of operation, the flash memory is disabled and put in a power-down state to minimize leakage.

For details on the flash memory and its various modes of operation and configuration, see the *Flash Controller (FLCTL)* chapter in the *MSP432P4xx Family Technical Reference Manual*.

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NOTE

Depending on the CPU (MCLK) frequency and the active mode in use, the flash may need to be accessed with single/multiple wait states. Whenever there is a change required in the operating frequency, it is the responsibility of the application to ensure that the flash access wait states are configured correctly before the frequency change is effected. See the electrical specification for details on flash wait state requirements.

6.4.2 SRAM

The MSP432P401x MCUs support up to 64KB of SRAM, with the rest of the 1MB SRAM region reserved. The SRAM is aliased in both Code and SRAM zones. This enables fast single-cycle execution of code from the SRAM, as the Cortex-M4 processor pipelines instruction fetches to memory zones other than the Code space. As with the flash memory, the SRAM can be powered down or placed in a low-leakage retention state in low-power modes of operation.

Figure 6-6 shows the memory map of SRAM on MSP432P401x MCUs.

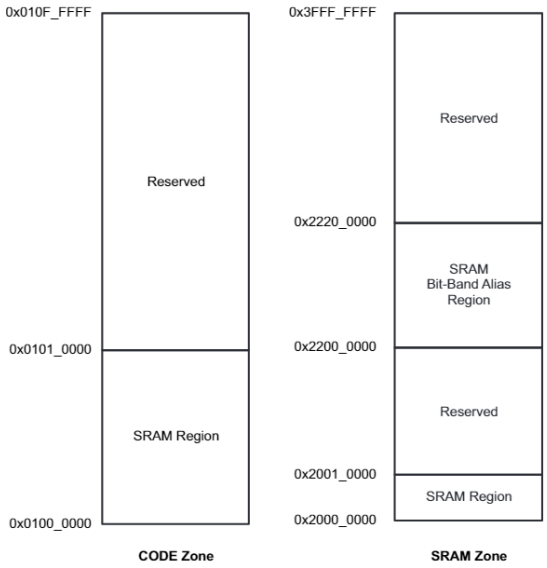


Figure 6-6. SRAM Map

6.4.2.1 SRAM Bank Enable Configuration

The application can optimize the power consumption of the SRAM. To enable this, the SRAM is divided into 8-KB banks that can be individually powered down. Banks that are powered down remain powered down in both active and low-power modes of operation, thereby limiting any unnecessary inrush current when the device transitions between active and retention-based low-power modes. The application can also disable one (or more) banks for a certain stage in the processing and enable it for another stage.

When a particular bank is disabled, reads to its address space return 0h, and writes are discarded. To prevent 'holes' in the memory map, if a particular bank is enabled, all the lower banks are also forced to enabled state. This ensures a contiguous memory map through the set of enabled banks instead of a allowing a disabled bank to appear between enabled banks. For example:

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- If there are eight banks in the device, values of 00111111 and 00000111 are acceptable.
- Values like 00010111 are not valid, and the resultant bank configuration is automatically set to 00011111.
- For example, for a 4-bank SRAM, the only allowed values are 0001, 0011, 0111, and 1111.

Bank 0 of SRAM is always enabled and cannot be disabled. For all other banks, any enable or disable change results in the SRAM_RDY bit of the SYS_SRAM_BANKEN register being set to 0 until the configuration change is effective. Any accesses to the SRAM is stalled during this time, and access resumes only after the SRAM banks are ready for read or write operations. This is handled transparently and does not require any code intervention. See the SRAM characteristics in the electrical specification for the SRAM bank enable or disable latency.

6.4.2.2 SRAM Bank Retention Configuration and Backup Memory

The application can optimize the leakage power consumption of the SRAM in LPM3 and LPM4 modes of operation. To enable this, each SRAM bank can be individually configured for retention. Banks that are enabled for retention retain their data through the LPM3 and LPM4 modes. The application can also retain a subset of the enabled banks.

For example, the application may need 32KB of SRAM for its processing needs (four banks are kept enabled). However, of these four banks, only one bank may contain critical data that must be retained in LPM3 or LPM4, while the rest are powered off completely to minimize power consumption.

Bank 0 of SRAM is always retained and cannot be powered down. Therefore, it also operates up as a possible backup memory in the LPM3, LPM4, and LPM3.5 modes of operation. In the case of LPM3 and LPM4 modes the full 8KB of SRAM bank 0 is retained but in the case of LPM3.5 mode only 6KB of SRAM bank 0 is retained. The 2KB of SRAM bank 0 over the address range 0x2000_0000 to 0x2000_007FF is not retained in LPM3.5 mode.

6.4.3 ROM

The MSP432P401x MCUs support 32KB of ROM, with the rest of the 1MB region reserved (for future upgrades). The lower 2KB of the ROM is reserved for TI internal purposes and accesses to this space returns an error response. The rest of the ROM is used for driver libraries.

NOTE

The entire ROM region returns an error response for write accesses. The lower 2KB of the ROM always returns an error response for any access.

6.5 DMA

The MSP432P401x MCUs implement an 8-channel ARM µDMA. This allows eight simultaneously active channels for data transfer between memory and peripherals without needing to use the bandwidth of the CPU (thereby reducing power by idling the CPU when there is no data processing required). In addition, the DMA remains active in multiple low-power modes of operation, allowing for a very low power state in which data can be transferred at low rates.

For maximum flexibility, up to eight DMA event sources can map to any of the eight channels. This is controlled through configuration registers in the DMA. In addition, the DMA can generate up to four interrupt requests (described in Section 6.5.2). For details regarding configuration of the DMA, see the DMA chapter in the *MSP432P4xx Family Technical Reference Manual*.

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6.5.1 DMA Source Mapping

Each channel of the eight available channels has a control register that can select any of the device-level DMA sources as the final source for that corresponding channel. Table 6-36 lists the sources available for mapping to each channel, based on the value of the Source Configuration (SRCCFG) register. The DMA transfers are initiated upon rising edge of the selected DMA source.

Table 6-36. DMA Sources

	SRCCFG = 0	SRCCFG = 1	SRCCFG = 2	SRCCFG = 3	SRCCFG = 4	SRCCFG = 5	SRCCFG = 6	SRCCFG = 7
Channel 0	Reserved	eUSCI_A0 TX	eUSCI_B0 TX0	eUSCI_B3 TX1	eUSCI_B2 TX2	eUSCI_B1 TX3	TA0CCR0	AES256_Trigger0
Channel 1	Reserved	eUSCI_A0 RX	eUSCI_B0 RX0	eUSCI_B3 RX1	eUSCI_B2 RX2	eUSCI_B1 RX3	TA0CCR2	AES256_Trigger1
Channel 2	Reserved	eUSCI_A1 TX	eUSCI_B1 TX0	eUSCI_B0 TX1	eUSCI_B3 TX2	eUSCI_B2 TX3	TA1CCR0	AES256_Trigger2
Channel 3	Reserved	eUSCI_A1 RX	eUSCI_B1 RX0	eUSCI_B0 RX1	eUSCI_B3 RX2	eUSCI_B2 RX3	TA1CCR2	Reserved
Channel 4	Reserved	eUSCI_A2 TX	eUSCI_B2 TX0	eUSCI_B1 TX1	eUSCI_B0 TX2	eUSCI_B3 TX3	TA2CCR0	Reserved
Channel 5	Reserved	eUSCI_A2 RX	eUSCI_B2 RX0	eUSCI_B1 RX1	eUSCI_B0 RX2	eUSCI_B3 RX3	TA2CCR2	Reserved
Channel 6	Reserved	eUSCI_A3 TX	eUSCI_B3 TX0	eUSCI_B2 TX1	eUSCI_B1 TX2	eUSCI_B0 TX3	TA3CCR0	DMAE0 (External Pin)
Channel 7	Reserved	eUSCI_A3 RX	eUSCI_B3 RX0	eUSCI_B2 RX1	eUSCI_B1 RX2	eUSCI_B0 RX3	TA3CCR2	ADC14

NOTE

Any source marked as Reserved is unused. It may be used for software-controlled DMA tasks, but typically it is reserved for enhancement purposes on future devices.

6.5.2 DMA Completion Interrupts

In the case of the ARM µDMA controller, it is usually the responsibility of software to maintain a list of channels that have completed their operation. To provide further flexibility, the MSP432P401x DMA supports four DMA completion interrupts, which are mapped in the following way:

- DMA_INT0: Logical OR of all completion events except those that are already mapped to DMA_INT1, DMA_INT2, or DMA_INT3.
- DMA_INT1, DMA_INT2, DMA_INT3: Can be mapped to the DMA completion event of any of the eight channels.

NOTE

Software must make sure that DMA_INT1, DMA_INT2, and DMA_INT3 are mapped to different channels, so that the same channel does not result in multiple interrupts at the NVIC.

6.5.3 DMA Access Privileges

The DMA has access to all of the memories and peripheral configuration interfaces of the device. If the device is configured for IP protection, DMA access to the flash is restricted to only the lower half (second bank) of the flash main and information memory regions. This prevents the DMA from being used as an unauthorized access source into the top half (first bank) of the flash, where secure data regions are housed.

6.6 Memory Map Access Details

The bus system on the MSP432P401x MCUs incorporates four masters, which can initiate various types of transactions:

- ICODE: Cortex-M4 instruction fetch bus. Accesses the Code zone only
- DCODE: Cortex-M4 data and literal load/store bus. Accesses the Code zone only. Debugger accesses to Code zone also appear on this bus.

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- SBUS: Cortex-M4 data read and write bus. Accesses to all zones except Code zones and PPB memory space only. Debugger accesses to this space also appear on this bus.
- DMA: Access to all zones except the PPB memory space

NOTE

The PPB space is dedicated only to the Cortex-M4 Private Peripheral Bus.

6.6.1 Master and Slave Access Priority Settings

Table 6-37 lists all of the available masters (rows) and their access permissions to slaves (columns). If multiple masters can access one slave, the table lists access priorities if arbitration is required. A lower number in the table indicates a higher arbitration priority (the priority is always fixed).

Table 6-37. Master and Slave Access Priority

	FLASH MEMORY	ROM	SRAM	PERIPHERALS
ICODE	3	2	4	N/A
DCODE	2 (1)	1	2	N/A
SBUS	N/A	N/A	3	2
DMA	1 (2)	N/A	1 (3)	1

(1) Access from the DCODE to flash memory may be restricted if the device is operating in a secure mode.
(2) Access from DMA to flash memory are restricted to Bank 1 if the device is operating in a secure mode with IP protection enabled. In such cases, access to Bank 0 returns an error response.
(3) Although the SRAM is mapped to both Code and System spaces, accesses from DMA to SRAM must use only the System space. DMA accesses to SRAM in Code space will result in bus error.

6.6.2 Memory Map Access Response

Table 6-38 summarizes the access responses to the entire memory map of the MSP432P401x MCUs.

Table 6-38. Memory Map Access Response

ADDRESS RANGE	DESCRIPTION	READ (1)	WRITE (1)	INSTRUCTION FETCH (1)
0x0000_0000–0x0003_FFFF	Flash Main Memory	OK	OK (2)(3)	OK
0x0004_0000–0x001F_FFFF	Reserved	Error	Error	Error
0x0020_0000–0x0020_3FFF	Flash Information Memory	OK	OK (3)	OK
0x0020_4000–0x00FF_FFFF	Reserved	Error	Error	Error
0x0100_0000–0x0100_FFFF	SRAM	OK	OK	OK
0x0101_0000–0x01FF_FFFF	Reserved	Error	Error	Error
0x0200_0000–0x0200_03FF	ROM (Reserved)	Error	Error	Error
0x0200_0400–0x0200_7FFF	ROM	OK	Error	OK
0x0200_8000–0x1FFF_FFFF	Reserved	Error	Error	Error
0x2000_0000–0x2000_FFFF	SRAM	OK	OK	OK
0x2001_0000–0x21FF_FFFF	Reserved	Error	Error	Error
0x2200_0000–0x23FF_FFFF	SRAM bit-band alias	OK (4)	OK	Error
0x2400_0000–0x3FFF_FFFF	Reserved	Error	Error	Error
0x4000_0000–0x4001_FFFF	Peripheral	OK	OK	Error
0x4002_0000–0x41FF_FFFF	Reserved	Error	Error	Error

(1) A reserved memory region returns 0h on reads and instruction fetches. Writes to this region are ignored.
(2) If the user memory address is part of a secure region, this access returns an error if it is initiated by an unauthorized source. For more details, see *Configuring Security and Bootloader (BSL) on MSP432P4xx*.
(3) Writes to this address are ignored if the sector has write protection enabled.
(4) Reads from the bit-band region return 00h if the bit is clear and 01h if the bit is set.

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Table 6-38. Memory Map Access Response (continued)

ADDRESS RANGE	DESCRIPTION	READ (1)	WRITE (1)	INSTRUCTION FETCH (1)
0x4200_0000–0x43FF_FFFF	Peripheral bit-band alias	OK (4)	OK	Error
0x4400_0000–0xDFFF_FFFF	Reserved	Error	Error	Error
0xE000_0000–0xE003_FFFF	Internal PPB (5)	OK	OK	Error
0xE004_0000–0xE004_0FFF	TPIU (External PPB)	OK	OK	Error
0xE004_1000–0xE004_1FFF	Reserved	Reserved	Reserved	Error
0xE004_2000–0xE004_23FF	Reset Controller (External PPB)	OK	OK	Error
0xE004_2400–0xE004_2FFF	Reserved	Reserved	Reserved	Error
0xE004_3000–0xE004_33FF	SYSCTL (External PPB)	OK	OK	Error
0xE004_3400–0xE004_3FFF	Reserved	Reserved	Reserved	Error
0xE004_4000–0xE004_43FF	SYSCTL (External PPB)	OK	OK	Error
0xE004_4400–0xE00F_EFFF	Reserved	Reserved	Reserved	Error
0xE00F_F000–0xE00F_FFFF	ROM Table (External PPB)	OK	OK	Error
0xE010_0000–0xFFFF_FFFF	Reserved	Error	Error	Error

(5) See the Cortex-M4 technical reference manual at www.arm.com for details of the memory map of the internal PPB.

6.7 Interrupts

The Cortex-M4 processor on MSP432P401x MCUs implements an NVIC with 64 external interrupt lines and 8 levels of priority. From an application perspective, the interrupt sources at the device level are divided into two classes, the NMI and the User Interrupts. Internally, the CPU exception model handles the various exceptions (internal and external events including CPU instruction, memory, and bus fault conditions) in a fixed and configurable order of priority. For details on the handling of various exception priorities (including CPU reset and fault models), see the ARM-V7M architecture reference manual at www.arm.com.

6.7.1 NMI

The NMI input of the NVIC has the following possible sources:

- External NMI pin (if configured in NMI mode)
- Oscillator fault condition
- Power Supply System (PSS) generated interrupts
- Power Control Manager (PCM) generated interrupts

6.7.2 Device-Level User Interrupts

Table 6-39 lists the various interrupt sources and their connection to the NVIC inputs

NOTE

Some sources may have multiple interrupt conditions, in which case the appropriate interrupt status/flag register of the source must be examined to differentiate between the generating conditions.

Table 6-39. NVIC Interrupts

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTISR[0]	PSS (1)	
INTISR[1]	CS (1)	
INTISR[2]	PCM (1)	

(1) This source can also be mapped to the system NMI. See the *MSP432P4xx Family Technical Reference Manual* for more details.

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Table 6-39. NVIC Interrupts (continued)

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTISR[3]	WDT_A	
INTISR[4]	FPU_INT (2)	Combined interrupt from flags in the FPSCR (part of Cortex-M4 FPU)
INTISR[5]	FLCTL	Flash Controller interrupt flags
INTISR[6]	COMP_E0	Comparator_E0 interrupt flags
INTISR[7]	COMP_E1	Comparator_E1 interrupt flags
INTISR[8]	Timer_A0	TA0CCTL0.CCIFG
INTISR[9]	Timer_A0	TA0CCTLx.CCIFG (x = 1 through 4), TA0CTL.TAIFG
INTISR[10]	Timer_A1	TA1CCTL0.CCIFG
INTISR[11]	Timer_A1	TA1CCTLx.CCIFG (x = 1 through 4), TA1CTL.TAIFG
INTISR[12]	Timer_A2	TA2CCTL0.CCIFG
INTISR[13]	Timer_A2	TA2CCTLx.CCIFG (x = 1 through 4), TA2CTL.TAIFG
INTISR[14]	Timer_A3	TA3CCTL0.CCIFG
INTISR[15]	Timer_A3	TA3CCTLx.CCIFG (x = 1 through 4), TA3CTL.TAIFG
INTISR[16]	eUSCI_A0	UART or SPI mode TX, RX, and Status Flags
INTISR[17]	eUSCI_A1	UART or SPI mode TX, RX, and Status Flags
INTISR[18]	eUSCI_A2	UART or SPI mode TX, RX, and Status Flags
INTISR[19]	eUSCI_A3	UART or SPI mode TX, RX, and Status Flags
INTISR[20]	eUSCI_B0	SPI or I^2C mode TX, RX, and Status Flags (I^2C in multiple-slave mode)
INTISR[21]	eUSCI_B1	SPI or I^2C mode TX, RX, and Status Flags (I^2C in multiple-slave mode)
INTISR[22]	eUSCI_B2	SPI or I^2C mode TX, RX, and Status Flags (I^2C in multiple-slave mode)
INTISR[23]	eUSCI_B3	SPI or I^2C mode TX, RX, and Status Flags (I^2C in multiple-slave mode)
INTISR[24]	ADC14	IFG[0-31], LO/IN/HI-IFG, RDYIFG, OVIFG, TOVIFG
INTISR[25]	Timer32_INT1	Timer32 Interrupt for Timer1
INTISR[26]	Timer32_INT2	Timer32 Interrupt for Timer2
INTISR[27]	Timer32_INTC	Timer32 Combined Interrupt
INTISR[28]	AES256	AESRDYIFG
INTISR[29]	RTC_C	OFIFG, RDYIFG, TEVIFG, AIFG, RT0PSIFG, RT1PSIFG
INTISR[30]	DMA_ERR	DMA error interrupt
INTISR[31]	DMA_INT3	DMA completion interrupt3
INTISR[32]	DMA_INT2	DMA completion interrupt2
INTISR[33]	DMA_INT1	DMA completion interrupt1
INTISR[34]	DMA_INT0 (3)	DMA completion interrupt0
INTISR[35]	I/O Port P1	P1IFG.x (x = 0 through 7)
INTISR[36]	I/O Port P2	P2IFG.x (x = 0 through 7)
INTISR[37]	I/O Port P3	P3IFG.x (x = 0 through 7)
INTISR[38]	I/O Port P4	P4IFG.x (x = 0 through 7)
INTISR[39]	I/O Port P5	P5IFG.x (x = 0 through 7)
INTISR[40]	I/O Port P6	P6IFG.x (x = 0 through 7)
INTISR[41]	Reserved	
INTISR[42]	Reserved	
INTISR[43]	Reserved	
INTISR[44]	Reserved	
INTISR[45]	Reserved	
INTISR[46]	Reserved	
INTISR[47]	Reserved	

(2) The FPU of the Cortex-M4 can generate interrupts due to multiple floating point exceptions. It is the responsibility of software to process and clear the interrupt flags in the FPSCR.
(3) DMA_INT0 has a different functionality from DMA_INT1, DMA_INT2, or DMA_INT3. See Section 6.5.2 for more details.

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Table 6-39. NVIC Interrupts (continued)

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTISR[48]	Reserved	
INTISR[49]	Reserved	
INTISR[50]	Reserved	
INTISR[51]	Reserved	
INTISR[52]	Reserved	
INTISR[53]	Reserved	
INTISR[54]	Reserved	
INTISR[55]	Reserved	
INTISR[56]	Reserved	
INTISR[57]	Reserved	
INTISR[58]	Reserved	
INTISR[59]	Reserved	
INTISR[60]	Reserved	
INTISR[61]	Reserved	
INTISR[62]	Reserved	
INTISR[63]	Reserved	

NOTE

The Interrupt Service Routine (ISR) must ensure that the relevant interrupt flag in the source peripheral is cleared before returning from the ISR. If this is not done, the same interrupt may be incorrectly triggered again as a new event, even though the event has already been processed by the ISR. As there may be a few cycles of delay between the execution of the write command and the actual write reflecting in the interrupt flag register of the peripheral, the recommendation is to carry out the write and wait for a few cycles before exiting the ISR. Alternatively, the application can do an explicit read to ensure that the flag is cleared before exiting the ISR.

6.8 System Control

System Control comprises the modules that govern the overall behavior of the device, including power management, operating modes, clocks, reset handling, and user configuration settings.

6.8.1 Device Resets

The MSP432P401x MCUs support multiple classes of reset. Each class results in a different level of initiation of device logic, thus allowing the application developer to initiate different resets based reset requirements during code development and debug. The following subsections cover the classes of reset in the device

6.8.1.1 Power On/Off Reset (POR)

The POR initiates a complete initialization of the application settings and device configuration information. This class of reset may be initiated either by the PSS, the PCM, the RSTn pin, the Clock System upon DCO external resistor short circuit fault, or the device emulation logic (through the debugger). From an application perspective, all sources of POR return the device to the same state of initialization.

NOTE

Depending on the source of the reset, the device may exhibit different wake-up latencies from the POR. This implementation enables optimization of the reset recovery time.

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6.8.1.2 Reboot Reset

The Reboot Reset is identical to the POR and allows the application to emulate a POR class reset without needing to power cycle the device or activate the RSTn pin. It can also be initiated through the debugger and, hence, does not affect the debug connection to the device. On the other hand, a POR results in a debug disconnect.

6.8.1.3 Hard Reset

The Hard Reset resets all modules that are set up or modified by the application. This includes all peripherals and the nondebug logic of the Cortex-M4. The MSP432P401x MCUs support up to 16 sources of Hard Reset. Table 6-40 lists the reset source allocation. The Reset Controller registers can be used to identify the source of reset in the device. For further details, see the *Reset Controller* chapter in the *MSP432P4xx Family Technical Reference Manual*.

Table 6-40. MSP432P401x Hard Reset Sources

RESET SOURCE NUMBER	SOURCE
0	SYSRESETREQ (System reset output of Cortex-M4)
1	WDT_A Time-out (1)
2	WDT_A Password Violation (1)
3	FLCTL (2)
4	Reserved (3)
5	Reserved (3)
6	Reserved (3)
7	Reserved (3)
8	Reserved (3)
9	Reserved (3)
10	Reserved (3)
11	Reserved (3)
12	Reserved (3)
13	Reserved (3)
14	CS (4)
15	PCM (5)

(1) The WDT_A generated resets can be mapped either as a Hard Reset or a Soft Reset.
(2) The FLCTL can generate a reset if a voltage anomaly is detected that can corrupt only flash reads and not the rest of the system.
(3) Reserved indicates that this source of Hard Reset is currently unused and left for future expansion.
(4) The CS is technically not a source of a Hard Reset, but if a Hard Reset occurs during clock source or frequency changes, the CS can extend the reset to allow the clocks to settle before releasing the system. This reduces the chance of nondeterministic behavior.
(5) The PCM is technically not a source of a Hard Reset, but if a Hard Reset causes power mode changes, the PCM can extend the reset to allow the system to settle before releasing the Reset. This reduces the chance of nondeterministic behavior.

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6.8.1.4 Soft Reset

The Soft Reset resets only the execution component of the system, which is the nondebug logic in the Cortex-M4 and the WDT_A. This reset remains nonintrusive to all other peripherals and system components. The MSP432P401x MCUs support up to 16 sources of Soft Reset. Table 6-41 lists the reset source allocation. The Reset Controller registers can be used to identify the source of reset in the design. For further details, see the *Reset Controller* chapter in the *MSP432P4xx Family Technical Reference Manual*.

Table 6-41. MSP432P401x Soft Reset Sources

RESET SOURCE NUMBER	SOURCE
0	CPU LOCKUP Condition (LOCKUP output of Cortex-M4)
1	WDT_A Time-out (1)
2	WDT_A Password Violation (1)
3	Reserved (2)
4	Reserved (2)
5	Reserved (2)
6	Reserved (2)
7	Reserved (2)
8	Reserved (2)
9	Reserved (2)
10	Reserved (2)
11	Reserved (2)
12	Reserved (2)
13	Reserved (2)
14	Reserved (2)
15	Reserved (2)

(1) The WDT_A generated resets can be mapped either as a Hard Reset or a Soft Reset.
(2) Reserved indicates that this source of Soft Reset is currently unused and left for future expansion.

NOTE

To support and enhance debug of reset conditions, the Reset Controller is located on the PPB of the device. This allows the Reset Controller to remain accessible even if the device is stuck in a Hard or Soft reset state. The Reset Controller permits overrides for Hard and Soft resets, thereby allowing an application to regain control of the device and isolate the cause of the stuck reset.

6.8.2 Power Supply System (PSS)

The PSS controls all the power supply related functionality of the device. It consists of the following components.

6.8.2.1 VCCDET

The VCCDET monitors the input voltage applied at the DVCC and AVCC pins of the device. When the V_{CC} is found to be below the operating range of the VCCDET trip points, it generates a brownout condition, thereby initiating a device reset (POR class reset).

6.8.2.2 Supply Supervisor and Monitor for High Side (SVSMH)

The SVSMH supervises and monitors the V_{CC}. SVSMH has a programmable threshold setting and can be used by the application to generate a reset or an interrupt if the V_{CC} dips below the desired threshold. In supervisor mode, the SVSMH generates a device reset (POR class reset). In monitor mode, the SVSMH generates an interrupt. The SVSMH can also be disabled if monitoring and supervision of the supply voltage are not required (offers further power savings).

6.8.2.3 Core Voltage Regulator

The MSP432P401x MCUs can be programmed to operate either with an LDO or with a DC-DC as the voltage regulator for the digital logic in the core domain of the device. The DC-DC offers significant boost in power efficiency for high-current high-performance applications. The LDO is a highly efficient regulator that offers power advantages at lower V_{CC} ranges and in the ultra-low-power modes of operation.

The core operating voltage (output of the LDO or DC-DC) is automatically set by the device depending on the selected operating mode of the device (see Table 6-42 for further details). The device offers seamless switching between LDO and DC-DC operating modes and also implements a seamless DC-DC fail-safe mechanism.

6.8.3 Power Control Manager (PCM)

The PCM controls the operating modes of the device and the switching between the modes. This is controlled by the application, which can choose modes to meet its power and performance requirements. Table 6-42 lists the operating modes of the device.

Table 6-42. MSP432P401x Operating Modes

OPERATING MODE	DESCRIPTION
AM_LDO_VCORE0	LDO based active mode, normal performance, core voltage level 0
LPM0_LDO_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_LDO_VCORE1	LDO based active mode, maximum performance, core voltage level 1
LPM0_LDO_VCORE1	Same as above, except that CPU is OFF (no code execution)
AM_DCDC_VCORE0	DC-DC based active mode, normal performance, core voltage level 0
LPM0_DCDC_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_DCDC_VCORE1	DC-DC based active mode, maximum performance, core voltage level 1
LPM0_DCDC_VCORE1	Same as above, except that CPU is OFF (no code execution)
AM_LF_VCORE0	LDO based low-frequency active mode, core voltage level 0
LPM0_LF_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_LF_VCORE1	LDO based low-frequency active mode, core voltage level 1
LPM0_LF_VCORE1	Same as above, except that CPU is OFF (no code execution)
LPM3_VCORE0	LDO based low-power mode with full state retention, core voltage level 0, RTC and WDT can be active
LPM3_VCORE1	LDO based low-power mode with full state retention, core voltage level 1, RTC and WDT can be active
LPM4_VCORE0	LDO based low-power mode with full state retention, core voltage level 0, all peripherals disabled.
LPM4_VCORE1	LDO based low-power mode with full state retention, core voltage level 1, all peripherals disabled
LPM3.5	LDO based low-power mode, core voltage level 0, no retention of peripheral registers, RTC and WDT can be active
LPM4.5	Core voltage turned off, wake-up only through pin reset or wake-up capable I/Os

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6.8.4 Clock System (CS)

The CS contains the sources of the various clocks in the device. It also controls the mapping between the sources and the different clocks in the device.

6.8.4.1 LFXT

The LFXT supports 32.768 kHz low-frequency crystals.

6.8.4.2 HFXT

The HFXT supports high-frequency crystals up to 48 MHz.

6.8.4.3 DCO

The DCO is a power-efficient tunable internal oscillator that generates up to 48 MHz. The DCO also supports a high-precision mode when using an external precision resistor.

6.8.4.4 Very Low-Power Low-Frequency Oscillator (VLO)

The VLO is an ultra-low-power internal oscillator that generates a low-accuracy clock at typical frequency of 9.4 kHz.

6.8.4.5 Low-Frequency Reference Oscillator (REFO)

The REFO can be used as an alternate low-power lower-accuracy source of a 32.768 kHz clock instead of the LFXT. The REFO can also be programmed to generate a 128 kHz clock.

6.8.4.6 Module Oscillator (MODOSC)

The MODOSC is an internal clock source that has a very low latency wake-up time. It is factory-calibrated to a frequency of 25 MHz. The MODOSC is typically used to supply a 'clock on request' to different modules. It can be used as a clock source for ADC operation at 1 Msps sampling rate.

6.8.4.7 System Oscillator (SYSOSC)

The SYSOSC is an internal clock source that is factory calibrated to a frequency of 5 MHz. It can be used as a clock source for ADC operation at 200 ksps sampling rate. In addition, the SYSOSC is also used for timing of various system-level control and management operations.

6.8.4.8 Fail-Safe Mechanisms

All clock sources that operate with external components have a built-in fail-safe mechanism that automatically switches to the relevant backup source, thereby ensuring that spurious or unstable clocks never impact the device operation. Table 6-43 shows the different types of clock source faults and the corresponding fail-safe clocks.

Table 6-43. Fail-Safe Clocks

Fault Type	Fail-Safe Clock
LFXT oscillator fault	REFO clock
HFXT oscillator fault	SYSOSC clock
DCO external resistor open circuit fault	DCO clock in internal resistor mode

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6.8.5 System Controller (SYSCTL)

The SYSCTL is a set of various miscellaneous features of the device, including SRAM bank configuration, RSTn/NMI function selection, and peripheral halt control. In addition, the SYSCTL enables device security features like JTAG and SWD lock and IP protection, which can be used to protect unauthorized accesses either to the entire device memory map or to certain selected regions of the flash. See the *System Controller* chapter in the *MSP432P4xx Family Technical Reference Manual* for more details.

NOTE

As is the case with the Cortex-M4 system control registers (in the internal PPB space), the System Controller module registers are mapped to the Cortex-M4 external PPB. This keeps the System Controller module accessible even when Hard or Soft resets are active.

6.9 Peripherals

6.9.1 Digital I/O

Up to 10 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt capability is available on ports P1 through P6.
- Wake-up capability from LPM3, LPM4, LPM3.5, and LPM4.5 modes on ports P1 through P6.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or in pairs (16-bit widths).
- Capacitive-touch functionality is supported on all pins of ports P1 through P10 and PJ.
- Four 20-mA high-drive I/Os on pins P2.0 to P2.3.
- Glitch filtering capability on selected digital I/Os.

6.9.1.1 Glitch Filtering on Digital I/Os

Some of the interrupt and wake-up capable digital I/Os can suppress glitches through the use of analog glitch filter to prevent unintentional interrupt or wake-up during device operation. The analog filter suppresses a minimum of 250-ns wide glitches. The glitch filter on these selected digital I/Os is enabled by default. If the glitch filtering capability is not required in the application, it can be bypassed using the SYS_DIO_GLTFLT_CTL register. When GLTFLT_EN bit in this register is cleared, the glitch filters on all the digital I/Os are bypassed. The glitch filter is automatically bypassed on a digital I/O when it is configured for peripheral or analog functionality by programming the respective PySEL0.x and PySEL1.x registers.

NOTE

The glitch filter is implemented on the following digital I/Os on MSP432P401x MCUs: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, and P6.7.

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6.9.2 Port Mapping Controller (PMAPCTL)

The port mapping controller allows flexible and reconfigurable mapping of digital functions.

6.9.2.1 Port Mapping Definitions

The port mapping controller on MSP432P401x MCUs allows reconfigurable mapping of digital functions on ports P2, P3, and P7. Table 6-44 lists the available mappings. Table 6-45 lists the default settings for all pins that support port mapping.

Table 6-44. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_UCA0CLK	eUSCI_A0 clock input/output (direction controlled by eUSCI)	
2	PM_UCA0RXD	eUSCI_A0 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA0SOMI	eUSCI_A0 SPI slave out master in (direction controlled by eUSCI)	
3	PM_UCA0TXD	eUSCI_A0 UART TXD (direction controlled by eUSCI – Output)	
	PM_UCA0SIMO	eUSCI_A0 SPI slave in master out (direction controlled by eUSCI)	
4	PM_UCB0CLK	eUSCI_B0 clock input/output (direction controlled by eUSCI)	
5	PM_UCB0SDA	eUSCI_B0 I^2C data (open drain and direction controlled by eUSCI)	
	PM_UCB0SIMO	eUSCI_B0 SPI slave in master out (direction controlled by eUSCI)	
6	PM_UCB0SCL	eUSCI_B0 I^2C clock (open drain and direction controlled by eUSCI)	
	PM_UCB0SOMI	eUSCI_B0 SPI slave out master in (direction controlled by eUSCI)	
7	PM_UCA1STE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
8	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
9	PM_UCA1RXD	eUSCI_A1 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA1SOMI	eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
10	PM_UCA1TXD	eUSCI_A1 UART TXD (direction controlled by eUSCI – Output)	
	PM_UCA1SIMO	eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
11	PM_UCA2STE	eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI)	
12	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
13	PM_UCA2RXD	eUSCI_A2 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA2SOMI	eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	
14	PM_UCA2TXD	eUSCI_A2 UART TXD (direction controlled by eUSCI – Output)	
	PM_ UCA2SIMO	eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
15	PM_UCB2STE	eUSCI_B2 SPI slave transmit enable (direction controlled by eUSCI)	
16	PM_UCB2CLK	eUSCI_B2 clock input/output (direction controlled by eUSCI)	
17	PM_UCB2SDA	eUSCI_B2 I^2C data (open drain and direction controlled by eUSCI)	
	PM_UCB2SIMO	eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)	
18	PM_UCB2SCL	eUSCI_B2 I^2C clock (open drain and direction controlled by eUSCI)	
	PM_UCB2SOMI	eUSCI_B2 SPI slave out master in (direction controlled by eUSCI)	
19	PM_TA0.0	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
20	PM_TA0.1	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
21	PM_TA0.2	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
22	PM_TA0.3	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
23	PM_TA0.4	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
24	PM_TA1.1	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1
25	PM_TA1.2	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
26	PM_TA1.3	TA1 CCR3 capture input CCI3A	TA1 CCR3 compare output Out3
27	PM_TA1.4	TA1 CCR4 capture input CCI4A	TA1 CCR4 compare output Out4

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Table 6-44. Port Mapping Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
28	PM_TA0CLK	Timer_A0 external clock input	None
	PM_C0OUT	None	Comparator-E0 output
29	PM_TA1CLK	Timer_A1 external clock input	None
	PM_C1OUT	None	Comparator-E1 output
30	PM_DMAE0	DMAE0 input	None
	PM_SMCLK	None	SMCLK
31 (0FFh)(1)	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is 31. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

Table 6-45. Default Mapping

PIN NAME	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P2.0/PM_UCA1STE	PM_UCA1STE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
P2.1/PM_UCA1CLK	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
P2.2/PM_UCA1RXD/ PM_UCA1SOMI	PM_UCA1RXD/ PM_UCA1SOMI	eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
P2.3/PM_UCA1TXD/ PM_UCA1SIMO	PM_UCA1TXD/ PM_UCA1SIMO	eUSCI_A1 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
P2.4/PM_TA0.1(1)	PM_TA0.1	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
P2.5/PM_TA0.2(1)	PM_TA0.2	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
P2.6/PM_TA0.3(1)	PM_TA0.3	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
P2.7/PM_TA0.4(1)	PM_TA0.4	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
P3.0/PM_UCA2STE	PM_UCA2STE	eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI)	
P3.1/PM_UCA2CLK	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
P3.2/PM_UCA2RXD/ PM_UCA2SOMI	PM_UCA2RXD/ PM_UCA2SOMI	eUSCI_A2 UART RXD (direction controlled by eUSCI – input)/ eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	
P3.3/PM_UCA2TXD/ PM_UCA2SIMO	PM_UCA2TXD/ PM_UCA2SIMO	eUSCI_A2 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
P3.4/PM_UCB2STE	PM_UCB2STE	eUSCI_B2 SPI slave transmit enable (direction controlled by eUSCI)	
P3.5/PM_UCB2CLK	PM_UCB2CLK	eUSCI_B2 clock input/output (direction controlled by eUSCI)	
P3.6/PM_UCB2SIMO/ PM_UCB2SDA	PM_UCB2SIMO/ PM_UCB2SDA	eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)/ eUSCI_B2 I^2C data (open drain and direction controlled by eUSCI)	
P3.7/PM_UCB2SOMI/ PM_UCB2SCL	PM_UCB2SOMI/ PM_UCB2SCL	eUSCI_B2 SPI slave out master in (direction controlled by eUSCI)/ eUSCI_B2 I^2C clock (open drain and direction controlled by eUSCI)	
P7.0/PM_SMCLK/ PM_DMAE0	PM_SMCLK/ PM_DMAE0	DMAE0 input	SMCLK
P7.1/PM_C0OUT/ PM_TA0CLK	PM_C0OUT/ PM_TA0CLK	Timer_A0 external clock input	Comparator-E0 output
P7.2/PM_C1OUT/ PM_TA1CLK	PM_C1OUT/ PM_TA1CLK	Timer_A1 external clock input	Comparator-E1 output
P7.3/PM_TA0.0	PM_TA0.0	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
P7.4/PM_TA1.4/C0.5(1)	PM_TA1.4	TA1 CCR4 capture input CCI4A	TA1 CCR4 compare output Out4
P7.5/PM_TA1.3/C0.4(1)	PM_TA1.3	TA1 CCR3 capture input CCI3A	TA1 CCR3 compare output Out3
P7.6/PM_TA1.2/C0.3(1)	PM_TA1.2	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
P7.7/PM_TA1.1/C0.2(1)	PM_TA1.1	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1

(1) Not available on the 64-pin RGC package.

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6.9.3 Timer_A

Timers TA0, TA1, TA2 and TA3 are 16-bit timers/counters (Timer_A type) with five capture/compare registers each. Each timer supports multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

6.9.3.1 Timer_A Signal Connection Tables

Table 6-46 through Table 6-49 list the interface signals of the Timer_A modules on the device and connections of the interface signals to the corresponding pins or internal signals. The following rules apply to the naming conventions used.

- The first column lists the device level pin or internal signal that sources the clocks and/or triggers into the Timer. The default assumption is that these are pins, unless specifically marked as (internal). Nomenclature used for internal signals is as follows:
  - CxOUT: output from Comparator x.
  - TAx_Cy: Output from Timer x, Capture/Compare module y.
- The second column lists the input signals of the Timer module.
- The third column lists the submodule of the Timer and also implies the functionality (Timer, Capture (Inputs or Triggers), or Compare (Outputs or PWM)).
- The fourth column lists the output signals of the Timer module.
- The fifth column lists the device-level pin or internal signal that is driven by the outputs of the Timer. The default assumption is that these are pins, unless specifically marked as (internal).

NOTE

The pin names listed in the tables are the complete names. It is the responsibility of the software to ensure that the pin is used in the intended mode for the targeted Timer functionality.

NOTE

Internal signals that are sourced by the Timer outputs may connect to other modules (for example, other timers or the ADC) in the device (as trigger sources).

Table 6-46. TA0 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P7.1/PM_C0OUT/PM_TA0CLK	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
C0OUT (internal)	INCLK			
P7.3/PM_TA0.0	CCI0A	CCR0	TA0	P7.3/PM_TA0.0 TA0_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.4/PM_TA0.1	CCI1A	CCR1	TA1	P2.4/PM_TA0.1 TA0_C1 (internal) ADC14 (internal) ADC14SHSx = {1}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.5/PM_TA0.2	CCI2A	CCR2	TA2	P2.5/PM_TA0.2 TA0_C2 (internal) ADC14 (internal) ADC14SHSx = {2}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.6/PM_TA0.3	CCI3A	CCR3	TA3	P2.6/PM_TA0.3 TA0_C3 (internal)
C1OUT (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.7/PM_TA0.4	CCI4A	CCR4	TA4	P2.7/PM_TA0.4 TA0_C4 (internal)
TA1_C4 (Internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

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Table 6-47. TA1 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P7.2/PM_C1OUT/PM_TA1CLK	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
C1OUT (internal)	INCLK			
P8.0/UCB3STE/TA1.0/C0.1	CCI0A	CCR0	TA0	P8.0/UCB3STE/TA1.0/C0.1 TA1_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.7/PM_TA1.1/C0.2	CCI1A	CCR1	TA1	P7.7/PM_TA1.1/C0.2 TA1_C1 (internal) ADC14 (internal) ADC14SHSx = {3}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.6/PM_TA1.2/C0.3	CCI2A	CCR2	TA2	P7.6/PM_TA1.2/C0.3 TA1_C2 (internal) ADC14 (internal) ADC14SHSx = {4}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.5/PM_TA1.3/C0.4	CCI3A	CCR3	TA3	P7.5/PM_TA1.3/C0.4 TA1_C3 (internal)
C1OUT (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.4/PM_TA1.4/C0.5	CCI4A	CCR4	TA4	P7.4/PM_TA1.4/C0.5 TA1_C4 (internal)
TA0_C4 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

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Table 6-48. TA2 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P4.2/ACLK/TA2CLK/A11	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 0 (internal)	INCLK			
P8.1/UCB3CLK/TA2.0/C0.0	CCI0A	CCR0	TA0	P8.1/UCB3CLK/TA2.0/C0.0 TA2_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P5.6/TA2.1/VREF+/VeREF+/C1.7	CCI1A	CCR1	TA1	P5.6/TA2.1/VREF+/VeREF+/C1.7 TA2_C1 (internal) ADC14 (internal) ADC14SHSx = {5}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P5.7/TA2.2/VREF-/VeREF-/C1.6	CCI2A	CCR2	TA2	P5.7/TA2.2/VREF-/VeREF-/C1.6 TA2_C2 (internal) ADC14 (internal) ADC14SHSx = {6}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1	CCI3A	CCR3	TA3	P6.6/TA2.3/UCB3SIMO/ UCB3SDA/C1.1 TA2_C3 (internal)
TA3_C3 (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0	CCI4A	CCR4	TA4	P6.7/TA2.4/UCB3SOMI/ UCB3SCL/C1.0 TA2_C4 (internal)
From Capacitive Touch I/O 0 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

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Table 6-49. TA3 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P8.3/TA3CLK/A22	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 1 (internal)	INCLK			
P10.4/TA3.0/C0.7	CCI0A	CCR0	TA0	P10.4/TA3.0/C0.7 TA3_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P10.5/TA3.1/C0.6	CCI1A	CCR1	TA1	P10.5/TA3.1/C0.6 TA3_C1 (internal) ADC14 (internal) ADC14SHSx = {7}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P8.2/TA3.2/A23	CCI2A	CCR2	TA2	P8.2/TA3.2/A23 TA3_C2 (internal)
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P9.2/TA3.3	CCI3A	CCR3	TA3	P9.2/TA3.3 TA3_C3 (internal)
TA2_C3 (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P9.3/TA3.4	CCI4A	CCR4	TA4	P9.3/TA3.4 TA3_C4 (internal)
From Capacitive Touch I/O 1 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

6.9.4 Timer32

Timer32 is an ARM dual 32-bit timer module. It contains two 32-bit timers, each of which can be configured as two independent 16-bit timers. The two timers can generate independent events or a combined event, which can be processed according to application requirements. Timer32 runs out of the same clock as the Cortex-M4 CPU.

6.9.5 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) and I^2C.

The MSP432P401x MCUs offer up to four eUSCI_A and four eUSCI_B modules.

6.9.6 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock. It integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, and temperature compensation. The RTC_C operation is available in LPM3 and LPM3.5 modes to minimize power consumption.

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6.9.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

CAUTION

The WDT must be set to interval mode before transitioning into the LPM3 or LPM3.5 modes of operation. This allows the WDT event to wake the device and return it to active modes of operation. Using the WDT in watchdog mode may result in nondeterministic behavior due to the generated reset.

The watchdog can generate a reset on either a time-out or a password violation. This reset can be configured to generate either a Hard Reset or a Soft Reset into the system. See the *MSP432P4xx Family Technical Reference Manual* for more details. The WDT should typically be configured to generate a Hard reset into the system. A Soft reset resets the CPU but leaves the rest of the system and peripherals unaffected. As a result, if the WDT is configured to generate a Soft reset, the application should assume responsibility for the fact that a Soft reset can corrupt an ongoing transaction from the CPU into the system.

Table 6-50 lists the clocks that can be selected as the source for the WDT_A module.

Table 6-50. WDT_A Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	BCLK

6.9.8 ADC14

The ADC14 module supports 14-bit analog-to-digital conversions up to 1 Msps sampling rate with differential and single-ended inputs. The module implements a 14-bit SAR core, sample and hold circuit, reference generator and a conversion result buffer. The window comparators with a lower and upper limit allow CPU independent result monitoring through different window comparator interrupt flags.

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The available ADC14 external trigger sources are summarized in Table 6-51.

Table 6-51. ADC14 Trigger Signal Connections

ADC14SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC14SC)
001	1	TA0_C1
010	2	TA0_C2
011	3	TA1_C1
100	4	TA1_C2
101	5	TA2_C1
110	6	TA2_C2
111	7	TA3_C1

Table 6-52, Table 6-53, and Table 6-54 list the available multiplexing between internal and external analog inputs of ADC14.

Table 6-52. ADC14 Channel Mapping on 100-Pin PZ Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 23	A23	Battery Monitor	ADC14BATMAP
Channel 22	A22	Temperature Sensor	ADC14TCMAP
Channel 21	A21	N/A (Reserved)	ADC14CH0MAP
Channel 20	A20	N/A (Reserved)	ADC14CH1MAP
Channel 19	A19	N/A (Reserved)	ADC14CH2MAP
Channel 18	A18	N/A (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as N/A or Reserved, it indicates that only the external source is available for that channel.
(2) See the ADC14 chapter in the *MSP432P4xx Family Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

Table 6-53. ADC14 Channel Mapping on 80-Pin ZXH Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 15	A15	Battery Monitor	ADC14BATMAP
Channel 14	A14	Temperature Sensor	ADC14TCMAP
Channel 13	A13	N/A (Reserved)	ADC14CH0MAP
Channel 12	A12	N/A (Reserved)	ADC14CH1MAP
Channel 11	A11	N/A (Reserved)	ADC14CH2MAP
Channel 10	A10	N/A (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as N/A or Reserved, it indicates that only the external source is available for that channel.
(2) See the ADC14 chapter in the *MSP432P4xx Family Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

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Table 6-54. ADC14 Channel Mapping on 64-Pin RGC Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 11	A11	Battery Monitor	ADC14BATMAP
Channel 10	A10	Temperature Sensor	ADC14TCMAP
Channel 9	A9	N/A (Reserved)	ADC14CH0MAP
Channel 8	A8	N/A (Reserved)	ADC14CH1MAP
Channel 7	A7	N/A (Reserved)	ADC14CH2MAP
Channel 6	A6	N/A (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as N/A or Reserved, it indicates that only the external source is available for that channel.
(2) See the ADC14 chapter in the *MSP432P4xx Family Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

6.9.9 Comparator_E (COMP_E)

The primary function of the COMP_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

There are two COMP_E modules available on the MSP432P401x MCUs.

6.9.10 Shared Reference (REF_A)

The REF_A generates of all the critical reference voltages that can be used by the various analog peripherals in the device. The reference voltage from REF_A can also be switched onto a device pin for external use.

6.9.11 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. It supports both a CRC32 and a CRC16 computation.

- The CRC16 computation signature is based on the CRC16-CCITT standard.
- The CRC32 computation signature is based on the CRC32-ISO3309 standard.

6.9.12 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-bit, 192-bit, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

6.9.13 True Random Seed

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

6.10 Code Development and Debug

The MSP432P401x MCUs support various methods through which the user can carry out code development and debug on the device.

6.10.1 JTAG and SWD Based Development, Debug, and Trace

The device supports both 4-pin JTAG and the 2-pin SWD modes of operation. The device is compatible with all standard Cortex-M4 debuggers available in the market today. The debug logic in the device has been designed to remain minimally intrusive to the application state. In low-power modes, the user can enable the debugger to override the state of the PSS, thereby gaining access to debug and trace features.

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In 2-pin SWD mode, the TDO pin can be used to export serial wire trace output (SWO) data. In addition, the TDI and TDO pins of the device can be reassigned as user I/Os. See Section 6.12.22 and Section 6.12.23 for more details.

NOTE

If the device has activated debug security, debugger accesses into the device is completely disabled. The debugger, however, is still be able to scan the run/halt state of the CPU. Further control of and visibility into the device is possible only after initiating a mass erase of the device flash contents.

6.10.2 Peripheral Halt Control

The Peripheral Halt Control register in the System Controller module allows the user independent control over the functionality of device peripherals during code development and debug. When the CPU is halted, the bits in this register can control whether the corresponding peripheral freezes its operation (such as incrementing, transmit, and receive) or continues its operation (debug remains nonintrusive). The registers of the peripheral remain accessible without regard to the values in the Peripheral Halt Control register.

6.10.3 Bootloader (BSL)

The BSL enables users to program flash or SRAM on the device using a UART or I^2C or SPI serial interface. Access to the device memory through the BSL is protected by a user-defined password. Table 6-55 lists the device pins that are required to use the BSL.

Table 6-55. BSL Pins and Functions

DEVICE PIN	BSL FUNCTION
P1.2	UART BSLRXD
P1.3	UART BSLTXD
P1.4	SPI BSLSTE
P1.5	SPI BSLCLK
P1.6	SPI BSLSIMO
P1.7	SPI BSLSOMI
P3.6	I^2C BSLSDA
P3.7	I^2C BSLSCL

The BSL is invoked under any of the following conditions.

- Flash main memory is erased
- Hardware invocation of BSL
- Software based API calls to BSL functions

The user can perform hardware invocation of BSL using any pin of ports P1, P2, or P3. The pin selected for this purpose should not be same as the ones used for BSL. The user can configure the device pin and its polarity through the flash boot-override mailbox. The BSL can then be invoked upon a power cycle or POR reset event with the configured pin.

For the complete description of the BSL features and its implementation, see the *MSP432P401R Bootloader (BSL) User's Guide*.

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6.10.4 Device Security

The MSP432P401xx MCUs offer the following two types of device security for the user application code programmed on to the device.

- JTAG and SWD Lock
- IP Protection

JTAG and SWD lock as the name indicates locks the JTAG and SWD interface of the device. IP protection is useful for protection of customer software IP, for example, in multiple-vendor development scenarios. Up to four IP-protected zones with configurable start address and size are supported. The security configurations of the device are done using the flash boot-override mailbox.

Also the SYSCTL module provides infrastructure for encrypted in-field updates to the application code on devices that are JTAG and SWD locked or have defined IP-protection zones. For complete details of the device security features, see the *System Controller (SYSCTL)* chapter in the *MSP432P4xx Family Technical Reference Manual*.

6.11 Performance Benchmarks

The MSP432P401xx MCUs achieve the following performance benchmarks under the given software configurations and profile configurations. These performance benchmarks were measured with system supply voltage of 2.97 V at an ambient temperature of 25°C.

6.11.1 ULPBench Performance: 192.3 ULPMark-CP

Table 6-56 shows the software configuration for this performance benchmark. Table 6-57 shows the profile configuration.

Table 6-56. Software Configuration

ITEMS	DETAILS
Compiler Name and Version	IAR EWARM v7.50.3
Compiler Flags	--endian=little --cpu=Cortex-M4F -e --fpu=VFPv4_sp -Ohs --no_size_constraints --mfc
ULPBench Profile and Version	v1.1.X
EnergyMonitor Software Version	1.1.3

Table 6-57. Profile Configuration

CONFIGURATION	DETAILS
Wakeup Timer Module	RTC
Wakeup Timer Clock Source	External Crystal
Wakeup Timer Frequency [Hz]	32768 Hz
Wakeup Timer Accuracy [ppm]	20 ppm
Active Power Mode Name	Active Mode
Active Mode Clock Configuration	CPU: 16 MHz, RTC: 32 KHz
Active Mode Voltage Integrity	1.62 V
Inactive Power Mode Name	LPM3
Inactive Clock Configuration	CPU: OFF, RTC: 32 kHz
Inactive Mode Voltage Integrity	1.62 V

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6.11.2 CoreMark/MHz Performance: 3.41

Table 6-58 shows the software configuration for this performance benchmark. Table 6-59 shows the profile configuration.

Table 6-58. Software Configuration

ITEMS	DETAILS
Compiler Name and Version	IAR EWARM v6.70.3
Compiler Flags	--no_size_constraints --debug --endian=little --cpu=Cortex-M4F -e --fpu=None -Ohs
CoreMark Profile and Version	v1.0

Table 6-59. Profile Configuration

CONFIGURATION	DETAILS
Active Power Mode Name	Active Mode
Active Mode Clock Configuration	CPU: 3 MHz
Active Mode Voltage Integrity	1.62 V

6.11.3 DMIPS/MHz (Dhrystone 2.1) Performance: 1.22

Table 6-60 shows the software configuration for this performance benchmark. Table 6-61 shows the profile configuration.

Table 6-60. Software Configuration

ITEMS	DETAILS
Compiler Name and Version	Keil uVision ARM Compiler v5.06 (build 20)
Compiler Flags	-c --cpu Cortex-M4.fp -g -O3 -Otime --apcs=interwork --asm --interleave --asm_dir –no_inline –no_multifile
Dhrystone Profile and Version	v2.1

Table 6-61. Profile Configuration

CONFIGURATION	DETAILS
Active Power Mode Name	Active Mode
Active Mode Clock Configuration	CPU: 3 MHz
Active Mode Voltage Integrity	1.62 V

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6.12 Input/Output Diagrams

6.12.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-62 summarizes the selection of the pin functions.

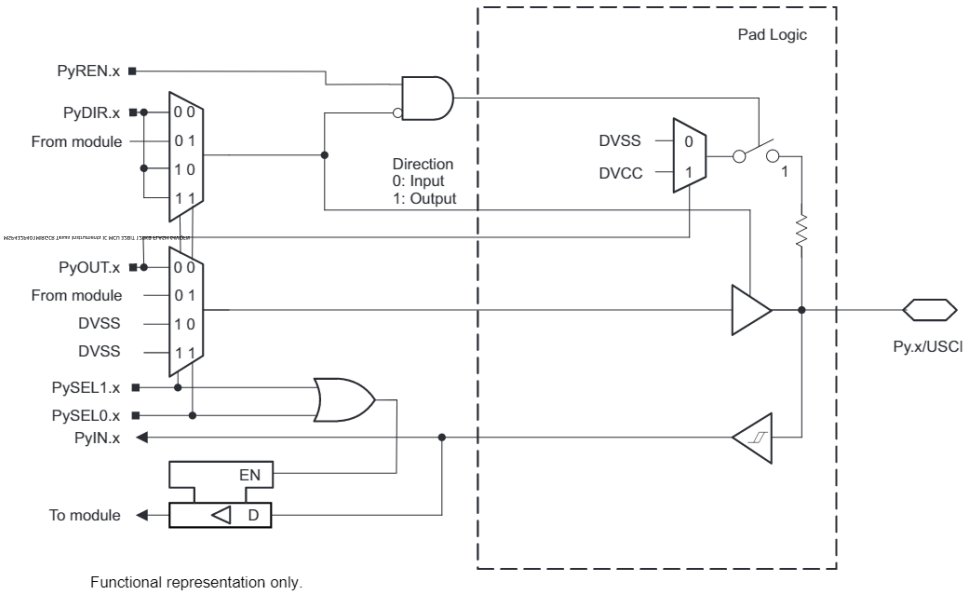


Figure 6-7. Py.x/USCI Pin Diagram

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Table 6-62. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/UCA0STE	0	P1.0 (I/O)	I: 0; O: 1	0	0
		UCA0STE	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.1/UCA0CLK	1	P1.1 (I/O)	I: 0; O: 1	0	0
		UCA0CLK	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.2/UCA0RXD/UCA0SOMI	2	P1.2 (I/O)	I: 0; O: 1	0	0
		UCA0RXD/UCA0SOMI	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.3/UCA0TXD/UCA0SIMO	3	P1.3 (I/O)	I: 0; O: 1	0	0
		UCA0TXD/UCA0SIMO	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.4/UCB0STE	4	P1.4 (I/O)	I: 0; O: 1	0	0
		UCB0STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.5/UCB0CLK	5	P1.5 (I/O)	I: 0; O: 1	0	0
		UCB0CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.6/UCB0SIMO/UCB0SDA	6	P1.6 (I/O)	I: 0; O: 1	0	0
		UCB0SIMO/UCB0SDA	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = don't care
(2) Direction controlled by eUSCI_A0 module.
(3) Direction controlled by eUSCI_B0 module.

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Table 6-62. Port P1 (P1.0 to P1.7) Pin Functions (continued)

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.7/UCB0SOMI/UCB0SCL	7	P1.7 (I/O)	I: 0; O: 1	0	0
		UCB0SOMI/UCB0SCL	X[3]	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

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6.12.2 Port P2 (P2.0 to P2.3) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-63 summarizes the selection of the pin functions.

Table 6-63. Port P2 (P2.0 to P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2MAPx
P2.0/PM_UCA1STE	0	P2.0 (I/O)	I: 0; O: 1	0	0	X
		UCA1STE	X[2]	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.1/PM_UCA1CLK	1	P2.1 (I/O)	I: 0; O: 1	0	0	X
		UCA1CLK	X[2]	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.2/PM_UCA1RXD/PM_UCA1SOMI	2	P2.2 (I/O)	I: 0; O: 1	0	0	X
		UCA1RXD/UCA1SOMI	X[2]	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.3/PM_UCA1TXD/PM_UCA1SIMO	3	P2.3 (I/O)	I: 0; O: 1	0	0	X
		UCA1TXD/UCA1SIMO	X[2]	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = don't care
(2) Direction controlled by eUSCI_A1 module.

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6.12.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-64 summarizes the selection of the pin functions.

Table 6-64. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.0/PM_UCA2STE	0	P3.0 (I/O)	I: 0; O: 1	0	0	X
		UCA2STE	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.1/PM_UCA2CLK	1	P3.1 (I/O)	I: 0; O: 1	0	0	X
		UCA2CLK	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.2/PM_UCA2RXD/PM_UCA2SOMI	2	P3.2 (I/O)	I: 0; O: 1	0	0	X
		UCA2RXD/UCA2SOMI	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.3/PM_UCA2TXD/PM_UCA2SIMO	3	P3.3 (I/O)	I: 0; O: 1	0	0	X
		UCA2TXD/UCA2SIMO	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.4/PM_UCB2STE	4	P3.4 (I/O)	I: 0; O: 1	0	0	X
		UCB2STE	X(3)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.5/PM_UCB2CLK	5	P3.5 (I/O)	I: 0; O: 1	0	0	X
		UCB2CLK	X(3)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = don't care
(2) Direction controlled by eUSCI_A2 module.
(3) Direction controlled by eUSCI_B2 module.

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Table 6-64. Port P3 (P3.0 to P3.7) Pin Functions (continued)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.6/PM_UCB2SIMO/PM_UCB2SDA	6	P3.6 (I/O)	I: 0; O: 1	0	0	X
		UCB2SIMO/UCB2SDA	X[3]	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.7/PM_UCB2SOMI/PM_UCB2SCL	7	P3.7 (I/O)	I: 0; O: 1	0	0	X
		UCB2SOMI/UCB2SCL	X[3]	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

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6.12.4 Port P9 (P9.4 to P9.7) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-65 summarizes the selection of the pin functions.

Table 6-65. Port P9 (P9.4 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.4/UCA3STE(2)	4	P9.4 (I/O)	I: 0; O: 1	0	0
		UCA3STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.5/UCA3CLK(2)	5	P9.5 (I/O)	I: 0; O: 1	0	0
		UCA3CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.6/UCA3RXD/UCA3SOMI(2)	6	P9.6 (I/O)	I: 0; O: 1	0	0
		UCA3RXD/UCA3SOMI	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.7/UCA3TXD/UCA3SIMO(2)	7	P9.7 (I/O)	I: 0; O: 1	0	0
		UCA3TXD/UCA3SIMO	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Direction controlled by eUSCI_A3 module.

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6.12.5 Port P10 (P10.0 to P10.3) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-66 summarizes the selection of the pin functions.

Table 6-66. Port P10 (P10.0 to P10.3) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10.0/UCB3STE(2)	0	P10.0 (I/O)	I: 0; O: 1	0	0
		UCB3STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P10.1/UCB3CLK(2)	1	P10.1 (I/O)	I: 0; O: 1	0	0
		UCB3CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P10.2/UCB3SIMO/UCB3SDA(2)	2	P10.2 (I/O)	I: 0; O: 1	0	0
		UCB3SIMO/UCB3SDA	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P10.3/UCB3SOMI/UCB3SCL(2)	3	P10.3 (I/O)	I: 0; O: 1	0	0
		UCB3SOMI/UCB3SCL	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Direction controlled by eUSCI_B3 module.

6.12.6 Port P2 (P2.4 to P2.7) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-67 summarizes the selection of the pin functions.

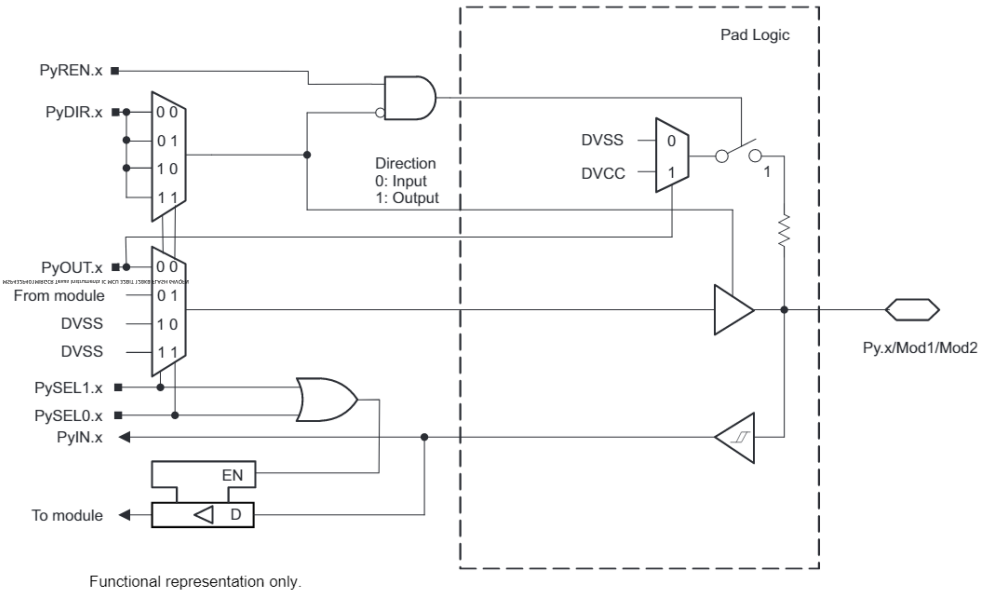


Figure 6-8. Py.x/Mod1/Mod2 Pin Diagram

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Table 6-67. Port P2 (P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2MAPx
P2.4/PM_TA0.1(2)	4	P2.4 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI1A	0	0	1	default
		TA0.1	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.5/PM_TA0.2(2)	5	P2.5 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI2A	0	0	1	default
		TA0.2	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.6/PM_TA0.3(2)	6	P2.6 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI3A	0	0	1	default
		TA0.3	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.7/PM_TA0.4(2)	7	P2.7 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI4A	0	0	1	default
		TA0.4	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = don't care
(2) Not available on the 64-pin RGC package.

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6.12.7 Port P7 (P7.0 to P7.3) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-68 summarizes the selection of the pin functions.

Table 6-68. Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.0/PM_SMCLK/ PM_DMAE0	0	P7.0 (I/O)	I: 0; O: 1	0	0	X
		DMAE0	0	0	1	default
		SMCLK	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P7.1/PM_C0OUT/ PM_TA0CLK	1	P7.1 (I/O)	I: 0; O: 1	0	0	X
		TA0CLK	0	0	1	default
		C0OUT	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P7.2/PM_C1OUT/ PM_TA1CLK	2	P7.2 (I/O)	I: 0; O: 1	0	0	X
		TA1CLK	0	0	1	default
		C1OUT	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P7.3/PM_TA0.0	3	P7.3 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI0A	0	0	1	default
		TA0.0	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = don't care

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6.12.8 Port P9 (P9.2 and P9.3) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-69 summarizes the selection of the pin functions.

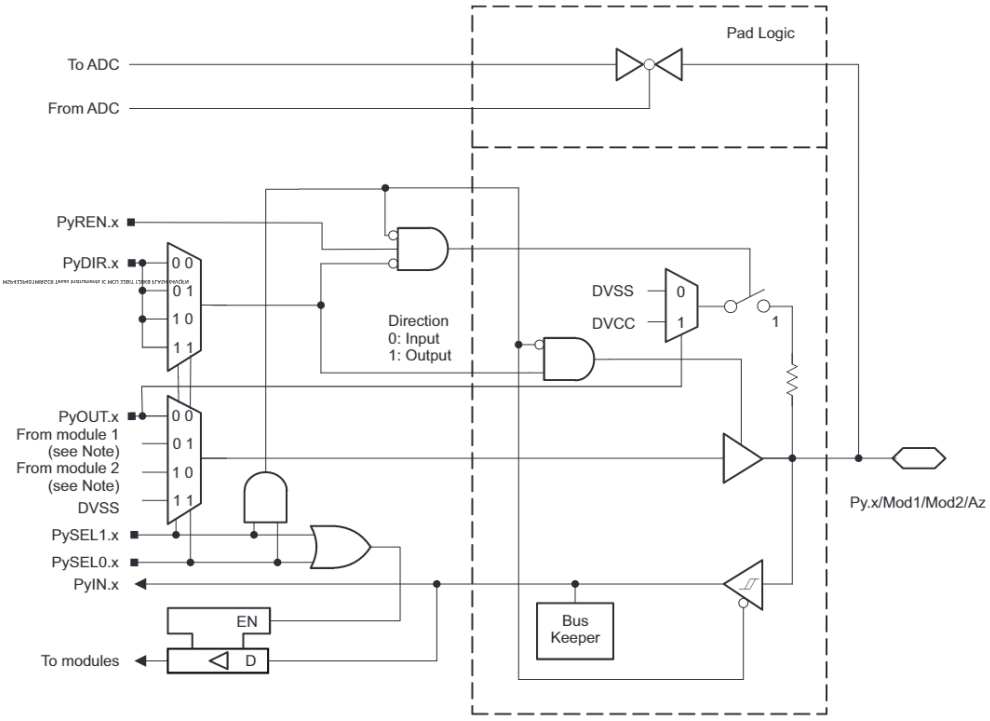
Table 6-69. Port P9 (P9.2 and P9.3) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.2/TA3.3(1)	2	P9.2 (I/O)	I: 0; O: 1	0	0
		TA3.CCI3A	0	0	1
		TA3.3	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.3/TA3.4(1)	3	P9.3 (I/O)	I: 0; O: 1	0	0
		TA3.CCI4A	0	0	1
		TA3.4	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) Not available on 80ZXH and 64RGC packages.

6.12.9 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-70 summarizes the selection of the pin functions.



Note: Output is DVSS if module 1 or module 2 function is not available. See the pin function tables.
Functional representation only.

Figure 6-9. Py.x/Mod1/Mod2/Az Pin Diagram

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Table 6-70. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.0/A13(2)	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A13(3)	X	1	1
P4.1/A12(2)	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A12(3)	X	1	1
P4.2/ACLK/TA2CLK/A11	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		ACLK	1		
		TA2CLK	0	1	0
		DVSS	1		
		A11(3)	X	1	1
P4.3/MCLK/RTCCLK/A10	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		MCLK	1		
		N/A	0	1	0
		RTCCLK	1		
		A10(3)	X	1	1
P4.4/HSMCLK/SVMHOUT/A9	4	P4.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		HSMCLK	1		
		N/A	0	1	0
		SVMHOUT	1		
		A9(3)	X	1	1
P4.5/A8	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A8(3)	X	1	1
P4.6/A7	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A7(3)	X	1	1

(1) X = don't care
(2) Not available on the 64-pin RGC package.
(3) Setting P4SEL1.x and P4SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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Table 6-70. Port P4 (P4.0 to P4.7) Pin Functions (continued)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.7/A6	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A6(3)	X	1	1

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6.12.10 Port P5 (P5.0 to P5.5) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-71 summarizes the selection of the pin functions.

Table 6-71. Port P5 (P5.0 to P5.5) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.0/A5	0	P5.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A5(2)	X	1	1
P5.1/A4	1	P5.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A4(2)	X	1	1
P5.2/A3	2	P5.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A3(2)	X	1	1
P5.3/A2	3	P5.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A2(2)	X	1	1
P5.4/A1	4	P5.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A1(2)	X	1	1
P5.5/A0	5	P5.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A0(2)	X	1	1

(1) X = don't care
(2) Setting P5SEL1.x and P5SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.12.11 Port P6 (P6.0 and P6.1) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-72 summarizes the selection of the pin functions.

Table 6-72. Port P6 (P6.0 and P6.1) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.0/A15(2)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A15(3)	X	1	1
P6.1/A14(2)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A14(3)	X	1	1

(1) X = don't care
(2) Not available on the 64-pin RGC package.
(3) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.12.12 Port P8 (P8.2 to P8.7) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-73 summarizes the selection of the pin functions.

Table 6-73. Port P8 (P8.2 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.2/TA3.2/A23(2)	2	P8.2 (I/O)	I: 0; O: 1	0	0
		TA3.CCI2A	0	0	1
		TA3.2	1		
		N/A	0	1	0
		DVSS	1		
		A23(3)	X	1	1
P8.3/TA3CLK/A22(2)	3	P8.3 (I/O)	I: 0; O: 1	0	0
		TA3CLK	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A22(3)	X	1	1
P8.4/A21(2)	4	P8.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A21(3)	X	1	1
P8.5/A20(2)	5	P8.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A20(3)	X	1	1
P8.6/A19(2)	6	P8.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A19(3)	X	1	1
P8.7/A18(2)	7	P8.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A18(3)	X	1	1

(1) X = don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.12.13 Port P9 (P9.0 and P9.1) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-74 summarizes the selection of the pin functions.

Table 6-74. Port P9 (P9.0 and P9.1) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.0/A17(2)	0	P9.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A17(3)	X	1	1
P9.1/A16(2)	1	P9.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A16(3)	X	1	1

(1) X = don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Setting P9SEL1.x and P9SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.12.14 Port P5 (P5.6 and P5.7) Input/Output With Schmitt Trigger

Figure 6-10 shows the port diagram. Table 6-75 summarizes the selection of the pin functions.

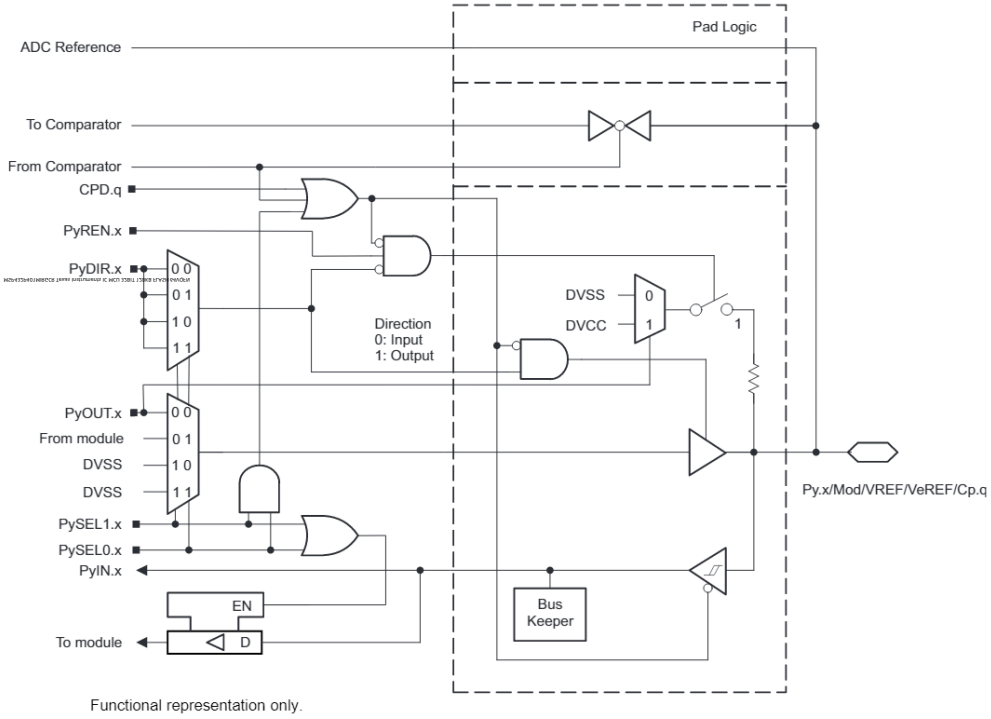


Figure 6-10. Py.x/Mod/VREF/VeREF/Cp.q Pin Diagram

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Table 6-75. Port P5 (P5.6 and P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.6/TA2.1/VREF+/VeREF+/C1.7	6	P5.6 (I/O)	I: 0; O: 1	0	0
		TA2.CCI1A	0	0	1
		TA2.1	1		
		N/A	0	1	0
		DVSS	1		
		VREF+, VeREF+, C1.7(2)(3)	X	1	1
P5.7/TA2.2/VREF-/VeREF-/C1.6	7	P5.7 (I/O)	I: 0; O: 1	0	0
		TA2.CCI2A	0	0	1
		TA2.2	1		
		N/A	0	1	0
		DVSS	1		
		VREF-, VeREF-, C1.6(2)(3)	X	1	1

(1) X = don't care
(2) Setting P5SEL1.x and P5SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.12.15 Port P6 (P6.2 to P6.5) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-76 summarizes the selection of the pin functions.

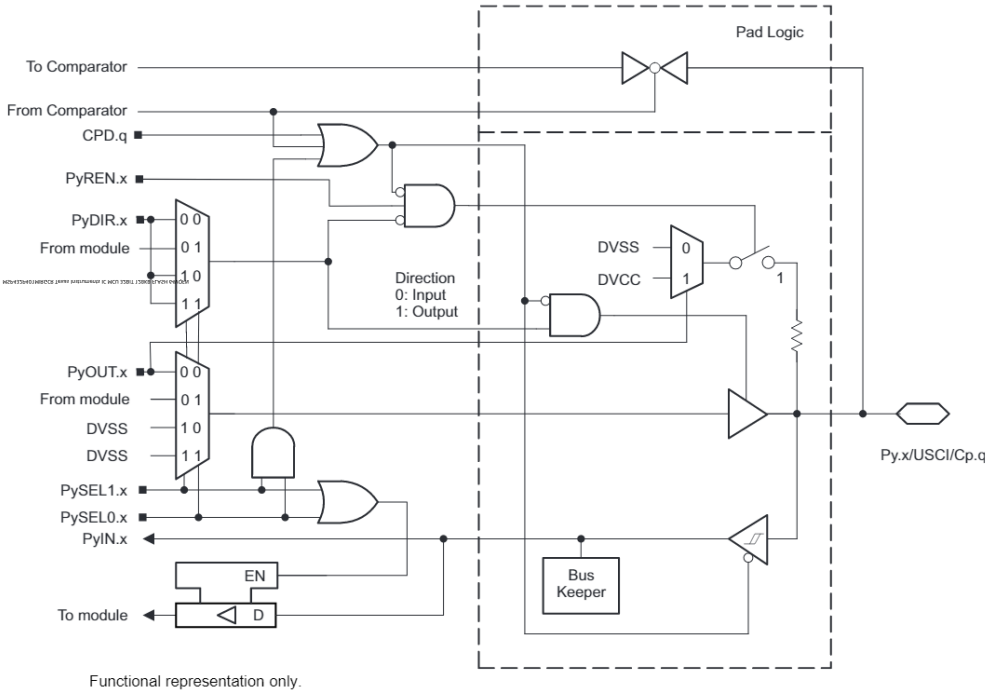


Figure 6-11. Py.x/USCI/Cp.q Pin Diagram

Table 6-76. Port P6 (P6.2 to P6.5) Pin Functions

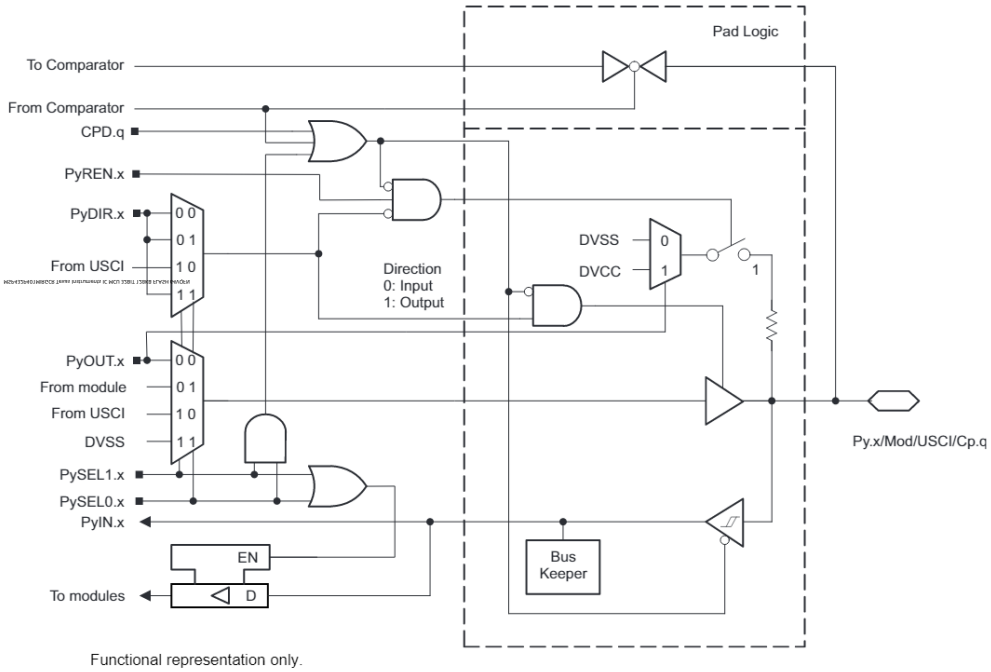
PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.2/UCB1STE/C1.5(2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		UCB1STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.5(4)(5)	X	1	1
P6.3/UCB1CLK/C1.4(2)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		UCB1CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.4(4)(5)	X	1	1
P6.4/UCB1SIMO/UCB1SDA/C1.3(2)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		UCB1SIMO/UCB1SDA	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.3(4)(5)	X	1	1
P6.5/UCB1SOMI/UCB1SCL/C1.2(2)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		UCB1SOMI/UCB1SCL	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.2(4)(5)	X	1	1

(1) X = don't care
(2) Not available on the 64-pin RGC package.
(3) Direction controlled by eUSCI_B1 module.
(4) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.12.16 Port P6 (P6.6 and P6.7) Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 6-77 summarizes the selection of the pin functions.



Functional representation only.

Figure 6-12. Py.x/Mod/USCI/Cp.q Pin Diagram

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Table 6-77. Port P6 (P6.6 and P6.7) Pin Functions

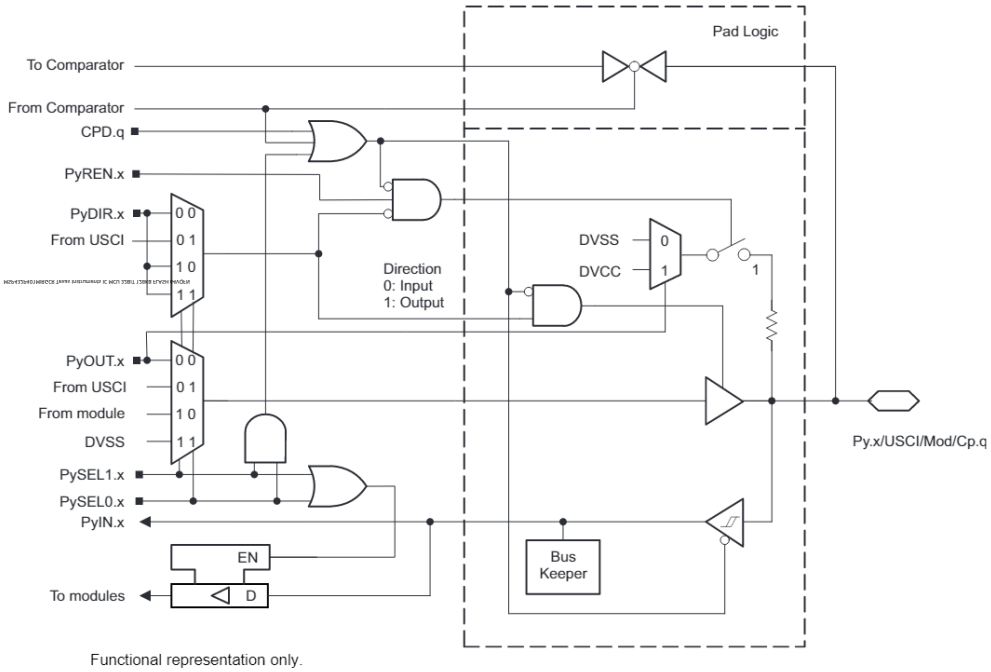
PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1	6	P6.6 (I/O)	I: 0; O: 1	0	0
		TA2.CCI3A	0	0	1
		TA2.3	1		
		UCB3SIMO/UCB3SDA	X(2)	1	0
		C1.1(3)(4)	X	1	1
P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0	7	P6.7 (I/O)	I: 0; O: 1	0	0
		TA2.CCI4A	0	0	1
		TA2.4	1		
		UCB3SOMI/UCB3SCL	X(2)	1	0
		C1.0(3)(4)	X	1	1

(1) X = don't care
(2) Direction controlled by eUSCI_B3 module.
(3) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.12.17 Port P8 (P8.0 and P8.1) Input/Output With Schmitt Trigger

Figure 6-13 shows the port diagram. Table 6-78 summarizes the selection of the pin functions.



Functional representation only.

Figure 6-13. Py.x/USCI/Mod/Cp.q Pin Diagram

Table 6-78. Port P8 (P8.0 and P8.1) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.0/UCB3STE/TA1.0/C0.1	0	P8.0 (I/O)	I: 0; O: 1	0	0
		UCB3STE	X(2)	0	1
		TA1.CCI0A	0	1	0
		TA1.0	1		
		C0.1(3)(4)	X	1	1
P8.1/UCB3CLK/TA2.0/C0.0	1	P8.1 (I/O)	I: 0; O: 1	0	0
		UCB3CLK	X(2)	0	1
		TA2.CCI0A	0	1	0
		TA2.0	1		
		C0.0(3)(4)	X	1	1

(1) X = don't care
(2) Direction controlled by eUSCI_B3 module.
(3) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.12.18 Port P10 (P10.4 and P10.5) Input/Output With Schmitt Trigger

Figure 6-14 shows the port diagram. Table 6-79 summarizes the selection of the pin functions.

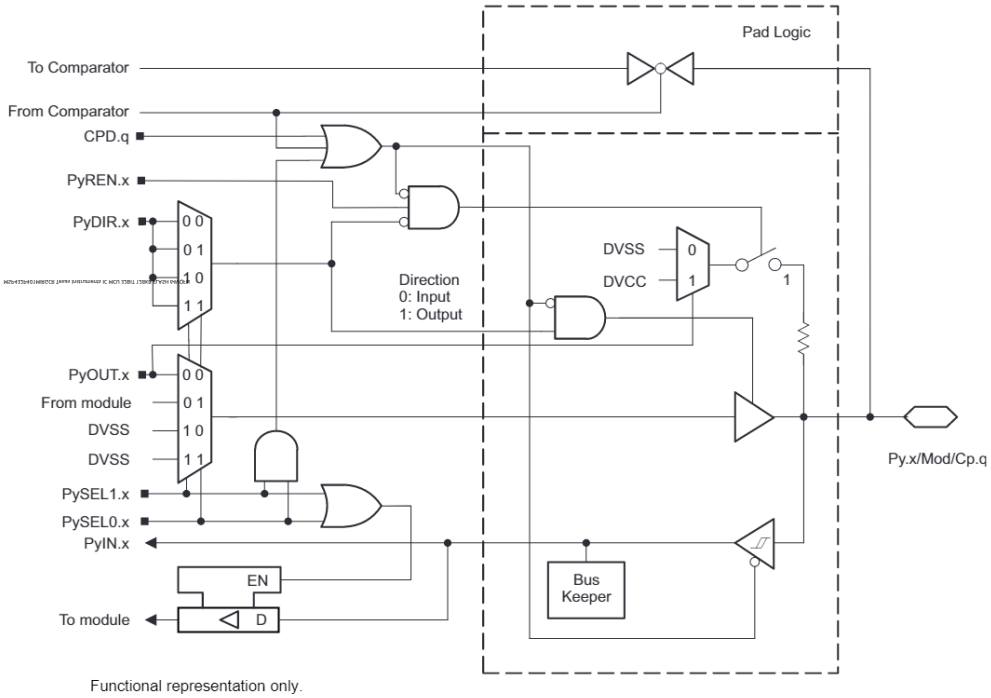


Figure 6-14. Py.x/Mod/Cp.q Pin Diagram

Table 6-79. Port P10 (P10.4 and P10.5) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10.4/TA3.0/C0.7(2)	4	P10.4 (I/O)	I: 0; O: 1	0	0
		TA3.CCI0A	0	0	1
		TA3.0	1		
		N/A	0	1	0
		DVSS	1		
		C0.7(3)(4)	X	1	1
P10.5/TA3.1/C0.6(2)	5	P10.5 (I/O)	I: 0; O: 1	0	0
		TA3.CCI1A	0	0	1
		TA3.1	1		
		N/A	0	1	0
		DVSS	1		
		C0.6(3)(4)	X	1	1

(1) X = don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Setting P10SEL1.x and P10SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.12.19 Port P7 (P7.4 to P7.7) Input/Output With Schmitt Trigger

Figure 6-15 shows the port diagram. Table 6-80 summarizes the selection of the pin functions.

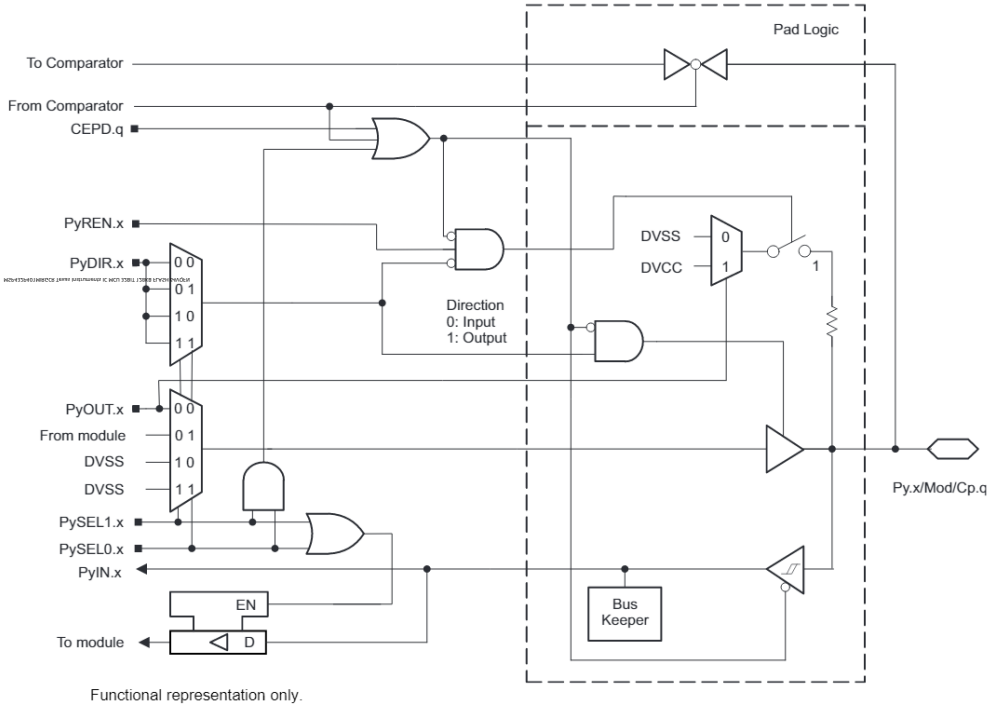


Figure 6-15. Py.x/Mod/Cp.q Pin Diagram

Table 6-80. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.4/PM_TA1.4/C0.5[2]	4	P7.4 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI4A	0	0	1	default
		TA1.4	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.5[3][4]	X	1	1	X
P7.5/PM_TA1.3/C0.4[2]	5	P7.5 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI3A	0	0	1	default
		TA1.3	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.4[3][4]	X	1	1	X
P7.6/PM_TA1.2/C0.3[2]	6	P7.6 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI2A	0	0	1	default
		TA1.2	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.3[3][4]	X	1	1	X
P7.7/PM_TA1.1/C0.2[2]	7	P7.7 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI1A	0	0	1	default
		TA1.1	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.2[3][4]	X	1	1	X

(1) X = don't care
(2) Not available on the 64-pin RGC package.
(3) Setting P7SEL1.x and P7SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.12.20 Port PJ (PJ.0 and PJ.1) Input/Output With Schmitt Trigger

Figure 6-16 and Figure 6-17 show the port diagram. Table 6-81 summarizes the selection of the pin functions.

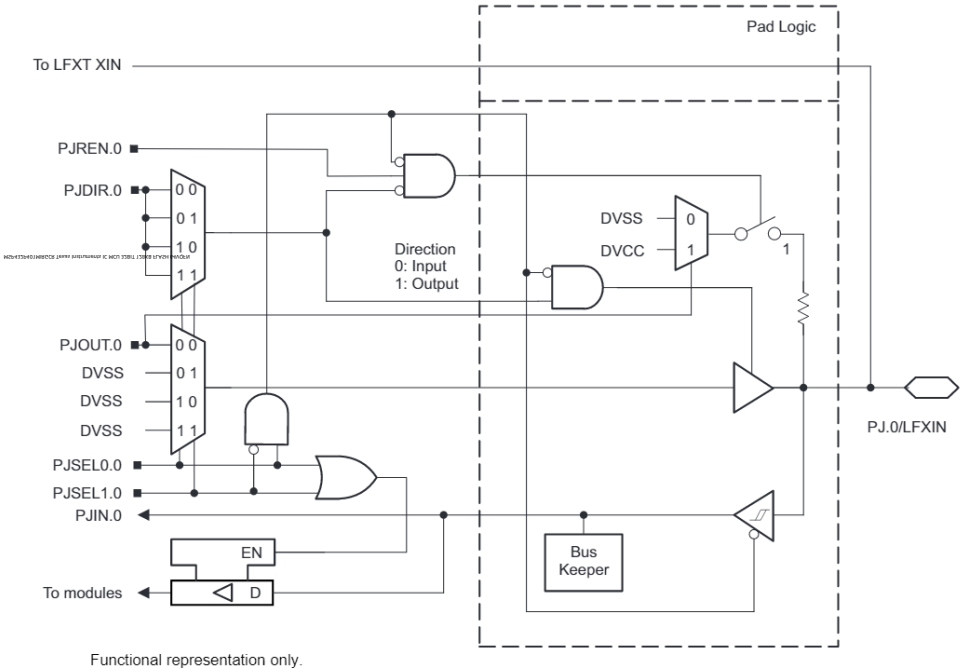
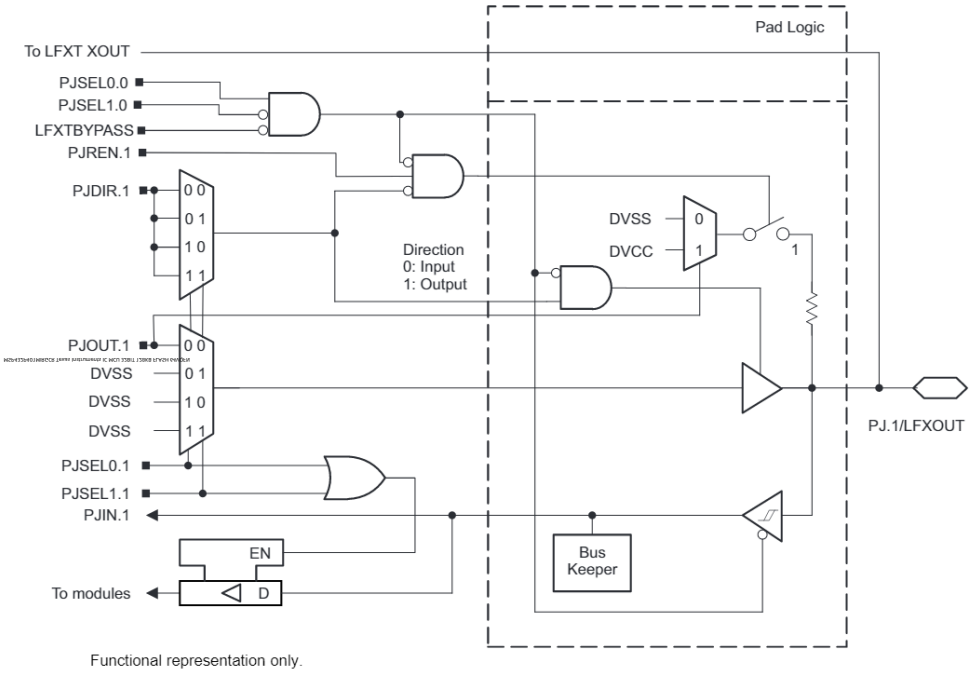


Figure 6-16. Port PJ (PJ.0) Diagram



Functional representation only.

Figure 6-17. Port PJ (PJ.1) Diagram

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Table 6-81. Port PJ (PJ.0 and PJ.1) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)					
			PJDIR.x	PJSEL1.1	PJSEL0.1	PJSEL1.0	PJSEL0.0	LFXT BYPASS
PJ.0/LFXIN	0	PJ.0 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		DVSS	1					
		LFXIN crystal mode (2)	X	X	X	0	1	0
		LFXIN bypass mode (2)	X	X	X	0	1	1
PJ.1/LFXOUT	1	PJ.1 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		LFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = don't care
(2) Setting PJSEL1.0 = 0 and PJSEL0.0 = 1 causes the general-purpose I/O to be disabled. When LFXTBYPASS = 0, PJ.0 and PJ.1 are configured for crystal operation and PJSEL1.1 and PJSEL0.1 are do not care. When LFXTBYPASS = 1, PJ.0 is configured for bypass operation and PJ.1 is configured as general-purpose I/O.
(3) When PJ.0 is configured in bypass mode, PJ.1 is configured as general-purpose I/O.
(4) With PJSEL0.1 = 1 or PJSEL1.1 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

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6.12.21 Port PJ (PJ.2 and PJ.3) Input/Output With Schmitt Trigger

Figure 6-18 and Figure 6-19 show the port diagrams. Table 6-82 summarizes the selection of the pin functions.

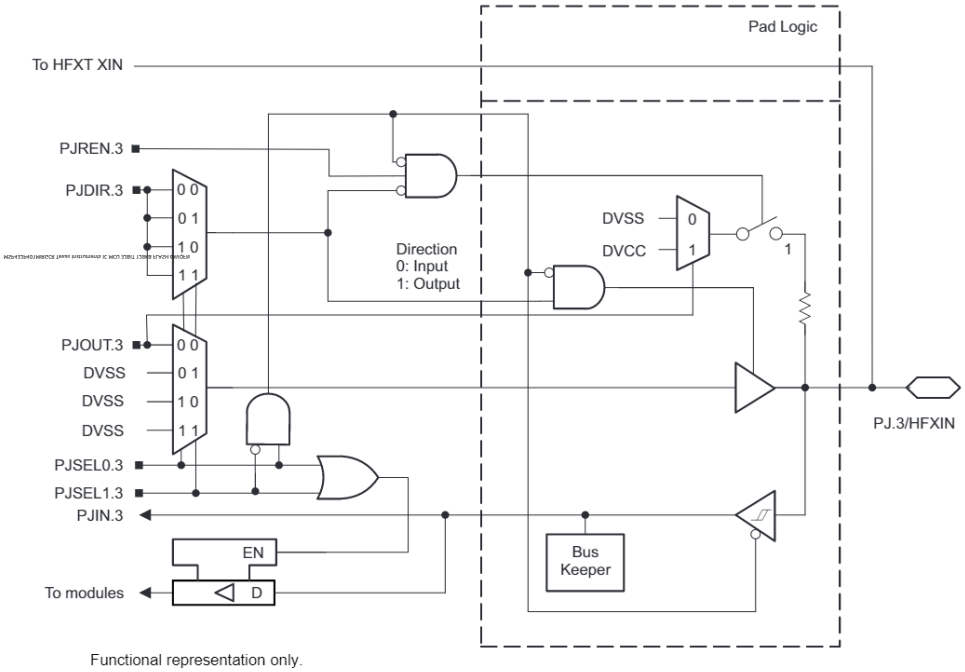


Figure 6-18. Port PJ (PJ.2) Diagram

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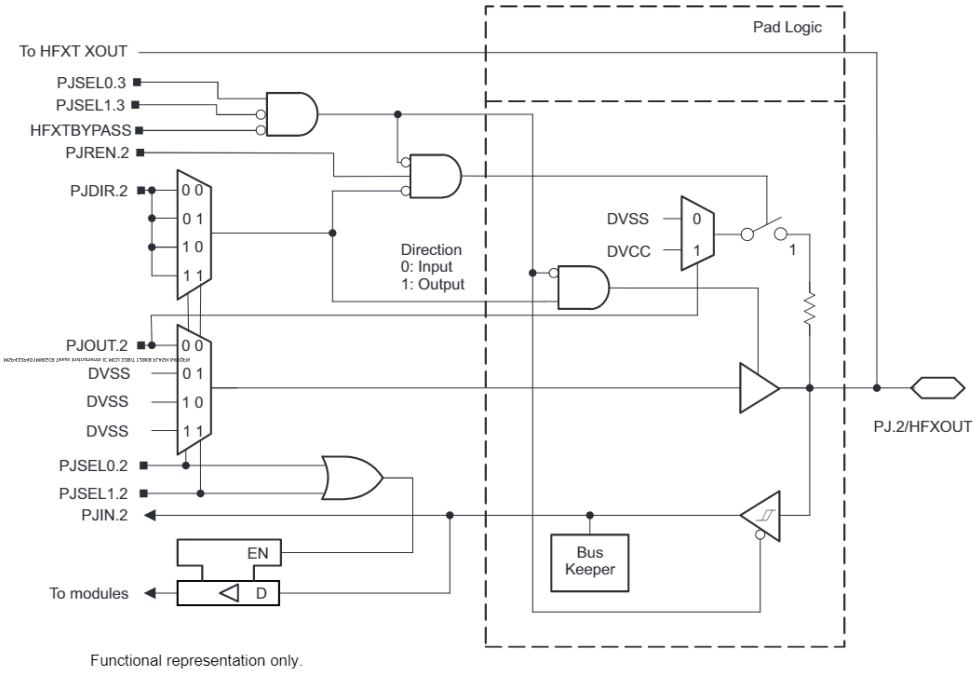


Figure 6-19. Port PJ (PJ.3) Diagram

Table 6-82. Port PJ (PJ.2 and PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)					
			PJDIR.x	PJSEL1.2	PJSEL0.2	PJSEL1.3	PJSEL0.3	HFXT BYPASS
PJ.3/HFXIN	3	PJ.3 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		DVSS	1					
		HFXIN crystal mode (2)	X	X	X	0	1	0
		HFXIN bypass mode (2)	X	X	X	0	1	1
PJ.2/HFXOUT	2	PJ.2 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		HFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = don't care
(2) Setting PJSEL1.3 = 0 and PJSEL0.3 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.2 and PJ.3 are configured for crystal operation and PJSEL1.2 and PJSEL0.2 are do not care. When HFXTBYPASS = 1, PJ.3 is configured for bypass operation and PJ.2 is configured as general-purpose I/O.
(3) When PJ.3 is configured in bypass mode, PJ.2 is configured as general-purpose I/O.
(4) With PJSEL0.2 = 1 or PJSEL1.2 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

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6.12.22 Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

Table 6-83 summarizes the selection of the pin functions.

Table 6-83. Port PJ (PJ.4 to PJ.5) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			SWJ MODE OF OPERATION (1)
			PJDIR.x	PJSEL1.x	PJSEL0.x	
PJ.4/TDI (2)	4	PJ.4 (I/O)	I: 0; O: 1	0	0	X
		TDI	X	0	1	JTAG (4 wire)
		DVcc				SWD (2 wire)
		DVcc	X	1	X	X
PJ.5/TDO/SWO (3)	5	PJ.5 (I/O)	I: 0; O: 1	0	0	X
		TDO	X	0	1	JTAG (4 wire)
		SWO				SWD (2 wire)
		Hi-Z	X	1	X	X

(1) X indicates that the value of the control signal or mode of operation has no effect on the functionality.
(2) This pin is internally pulled up if PJSEL0.x is 1.
(3) When used in debug configuration, this pin must be pulled to ground through an external pulldown resistor.

6.12.23 Ports SWCLKTCK and SWDIOTMS With Schmitt Trigger

Table 6-84 summarizes the selection of the pin functions.

Table 6-84. Ports SWCLKTCK and SWDIOTMS Pin Functions

PIN NAME	FUNCTION	SWJ MODE OF OPERATION
SWCLKTCK (1)	TCK (input)	JTAG (4 wire)
	SWCLK (input)	SWD (2 wire)
SWDIOTMS (2)	TMS (input)	JTAG (4 wire)
	SWDIO (I/O)	SWD (2 wire)

(1) This pin is internally pulled to DV_{SS}.
(2) This pin is internal pulled to DV_{CC}.

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6.13 Device Descriptors (TLV)

Table 6-85 summarizes the Device IDs of the MSP432P401xx MCUs. Table 6-86 lists the contents of the device descriptor tag-length-value (TLV) structure for the MSP432P401xx MCUs.

Table 6-85. Device IDs

DEVICE	DEVICE ID
MSP432P401RIPZ	0000A000h
MSP432P401MIPZ	0000A001h
MSP432P401RIZXH	0000A002h
MSP432P401MIZXH	0000A003h
MSP432P401RIRGC	0000A004h
MSP432P401MIRGC	0000A005h

Table 6-86. Device Descriptor Table(1)

	DESCRIPTION	ADDRESS	VALUE
	TLV checksum	00201000h	per unit
Info Block	Device Info Tag	00201004h	0000000Bh
	Device Info Length	00201008h	00000004h
	Device ID	0020100Ch	See Table 6-85
	Hardware Revision	00201010h	per unit
	Boot-Code Revision	00201014h	per unit
	ROM Driver Library Revision	00201018h	per unit
Die Record	Die Record Tag	0020101Ch	0000000Ch
	Die Record Length	00201020h	00000008h
	Die X Position	00201024h	per unit
	Die Y Position	00201028h	per unit
	Wafer ID	0020102Ch	per unit
	Lot ID	00201030h	per unit
	Reserved	00201034h	per unit
	Reserved	00201038h	per unit
	Reserved	0020103Ch	per unit
	Test Results	00201040h	per unit
Clock System Calibration	Clock System Calibration Tag	00201044h	00000003h
	Clock System Calibration Length	00201048h	00000010h
	DCO IR mode: Frequency calibration for DCORSEL 0 to 4	0020104Ch	per unit
	DCO IR mode: Frequency calibration for DCORSEL 5	00201050h	per unit
	Reserved	00201054h	not defined
	Reserved	00201058h	not defined
	Reserved	0020105Ch	not defined
	Reserved	00201060h	not defined
	DCO IR Mode: DCO Constant (K) for DCORSEL 0 to 4	00201064h	per unit
	DCO IR Mode: DCO Constant (K) for DCORSEL 5	00201068h	per unit
	DCO ER Mode: Frequency calibration for DCORSEL 0 to 4	0020106Ch	per unit
	DCO ER Mode: Frequency calibration for DCORSEL 5	00201070h	per unit
	Reserved	00201074h	not defined
	Reserved	00201078h	not defined
	Reserved	0020107Ch	not defined
	Reserved	00201080h	not defined
	DCO ER Mode: DCO Constant (K) for DCORSEL 0 to 4	00201084h	per unit
	DCO ER Mode: DCO Constant (K) for DCORSEL 5	00201088h	per unit

(1) per unit = content can differ from device to device

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Table 6-86. Device Descriptor Table[1] (continued)

	DESCRIPTION	ADDRESS	VALUE
ADC14 Calibration	ADC14 Calibration Tag	0020108Ch	00000005h
	ADC14 Calibration Length	00201090h	00000018h
	Reserved	00201094h	not defined
	Reserved	00201098h	FFFFFFFFh
	Reserved	0020109Ch	FFFFFFFFh
	Reserved	002010A0h	FFFFFFFFh
	Reserved	002010A4h	FFFFFFFFh
	Reserved	002010A8h	FFFFFFFFh
	Reserved	002010ACh	FFFFFFFFh
	Reserved	002010B0h	FFFFFFFFh
	Reserved	002010B4h	FFFFFFFFh
	Reserved	002010B8h	FFFFFFFFh
	Reserved	002010BCh	FFFFFFFFh
	Reserved	002010C0h	FFFFFFFFh
	Reserved	002010C4h	FFFFFFFFh
	Reserved	002010C8h	FFFFFFFFh
	Reserved	002010CCh	FFFFFFFFh
	Reserved	002010D0h	FFFFFFFFh
	Reserved	002010D4h	FFFFFFFFh
	Reserved	002010D8h	not defined
	ADC 1.2-V Reference Temperature Sensor 30°C	002010DCh	per unit
	ADC 1.2-V Reference Temperature Sensor 85°C	002010E0h	per unit
	ADC 1.45-V Reference Temperature Sensor 30°C	002010E4h	per unit
	ADC 1.45-V Reference Temperature Sensor 85°C	002010E8h	per unit
	ADC 2.5-V Reference Temperature Sensor 30°C	002010ECh	per unit
	ADC 2.5-V Reference Temperature Sensor 85°C	002010F0h	per unit
REF Calibration	REF Calibration Tag	002010F4h	00000008h
	REF Calibration Length	002010F8h	00000003h
	Reserved	002010FCh	not defined
	Reserved	00201100h	not defined
	Reserved	00201104h	not defined
Flash Info	Flash Info Tag	00201108h	00000004h
	Flash Info Length	0020110Ch	00000002h
	Flash Maximum Programming Pulses	00201110h	00000005h
	Flash Maximum Erase Pulses	00201114h	0000014Eh
Random Number	128-Bit Random Number Tag	00201118h	0000000Dh
	Random Number Length	0020111Ch	00000004h
	128-Bit Random Number[2]	00201120h	per unit
		00201124h	per unit
		00201128h	per unit
		0020112Ch	per unit
BSL Configuration	BSL Configuration Tag	00201130h	0000000Fh
	BSL Configuration Length	00201134h	00000004h
	BSL Peripheral Interface Selection	00201138h	FFC2D0C0h
	BSL Port Interface Configuration for UART	0020113Ch	FCFFFDA0h
	BSL Port Interface Configuration for SPI	00201140h	F0FF9770h
	BSL Port Interface Configuration for I2C	00201144h	FCFFFF72h
TLV End	TLV End Word	00201148h	0BD0E11Dh
	Reserved	0020114Ch-00201FFFh	FFFFFFFFh

(2) 128-Bit Random Number: The random number is generated during production test using the CryptGenRandom() function from Microsoft®.

6.14 Identification

6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see Section 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entry in the Device Descriptor structure (see Section 6.13).

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see Section 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entry in the Device Descriptor structure (see Section 6.13).

6.14.3 ARM Cortex-M4F ROM Table Based Part Number

The MSP432P4xx family of MCUs incorporates a part number for the device for the IDEs to recognize the device, in addition to the device IDs specified in the device descriptors (TLV). This section describes how this information is organized on the device.

IEEE 1149.1 defines the use of a IDCODE register in the JTAG chain to provide the fields in Table 6-87

Table 6-87. Structure of Device Identification Code

Bit Position	Field Description
31-28	Version
27-12	Part Number of the device
11-1	Manufacturer Identity
0	Reserved (Always tied to 1)

On MSP432P4xx MCUs, all these fields are implemented on the ARM Cortex-M4 ROM table. The part number can be read by the IDE tools (TI internal or third party) to determine the device. Figure 6-20 shows the Peripheral ID register bit descriptions from the ARM Cortex-M4 specifications. See the *ARM Debug interface V5 Architecture Specification* for bit-level details on the ARM Cortex-M4 Peripheral ID registers.

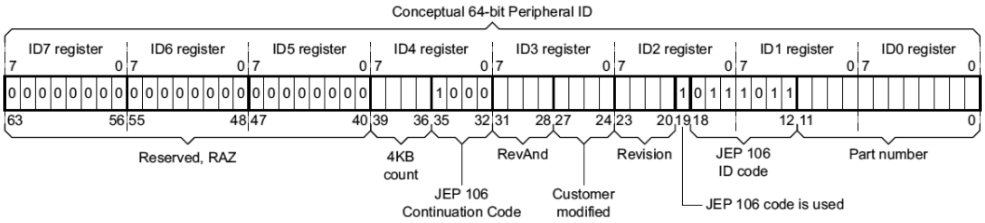


Figure 6-20. ARM Cortex-M4 Peripheral ID Register Description

Figure 6-20 shows that a one-to-one mapping is not possible for the following fields from Table 6-87

1. Version: IEEE 1149.1 defines a 4 bit field where as the Coresight compliant PID registers have 4 bits each for Revision (major revision) and RevAnd (minor revision)

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2. Part Number: IEEE 1149.1 defines a 16 bit entity. However, the PID registers in the ROM table have only 12 bits reserved for this purpose (Part number – PID1 and PID0 registers).

For the MSP432P4xx MCUs, the Revision and RevAnd fields are used for tracking the major and minor revisions. Also the Customer modified (4 bit) field is used for extending the Part number to 16 bits, to accommodate all of the fields needed by IEEE 1149.1 in the ROM table.

As an example, the ROM table with IEEE 1149.1-complaint device IDCODE for the MSP432P401xx MCU is 0000-1011-1001-1010-1111-0000-0010-1111 (see Figure 6-21).

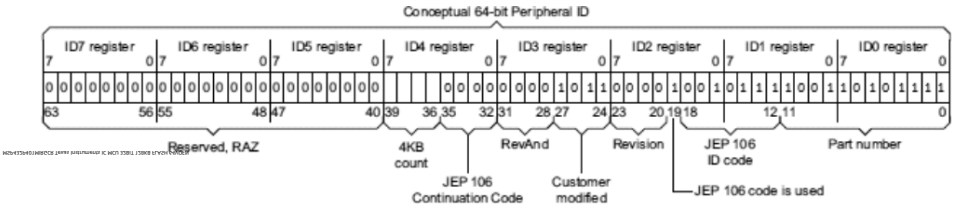


Figure 6-21. Example of ROM PID Entries for MSP432P401xx MCU

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP432 microcontrollers. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 4.7-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin (see Figure 7-1). Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital-to-analog circuits on the board and for high analog accuracy.

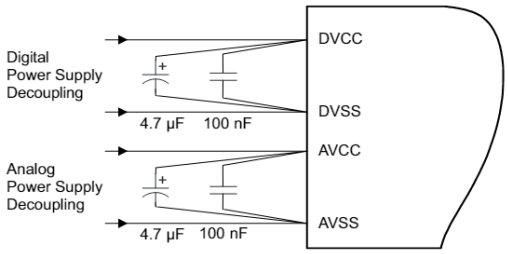


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

The device supports a low-frequency crystal (32.768 kHz) on the LFXT pins and a high-frequency crystal on the HFXT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes.

Figure 7-2 shows a typical connection diagram.

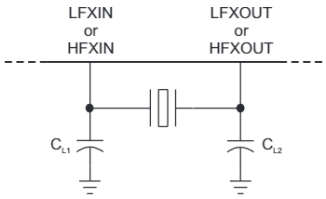


Figure 7-2. Typical Crystal Connection

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See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP432 devices.

7.1.3 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- See *Circuit Board Layout Techniques* for a detailed discussion of printed-circuit-board (PCB) layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.4 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device.

7.2 Peripheral and Interface-Specific Design Information

7.2.1 ADC14 Peripheral

7.2.1.1 Partial Schematic

Figure 7-3 shows a partial schematic of the ADC14 external connections.

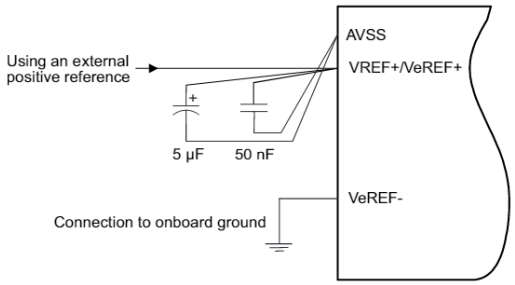


Figure 7-3. ADC14 Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 7.1.1 combined with the connections shown in Section 7.2.1.1 prevent this.

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In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommend to achieve high accuracy.

Figure 7-3 shows the recommended decoupling circuit when an external voltage reference is used.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 5-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 50-nF bypass capacitor is used to filter out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 7-3) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC14, the analog differential input signals must be routed close together to minimize the effect of noise on the resulting signal.

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8 Device and Documentation Support

8.1 Getting Started and Next Steps

For more information on the MSP432 family of microcontrollers and the tools and libraries that are available to help with your development, visit Getting Started with MSP432P4x.

8.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP432 MCU devices and support tools. Each MSP432 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP432P401R). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

PMS – Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed Texas Instruments internal qualification testing.

MSP – Fully-qualified development-support product

XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

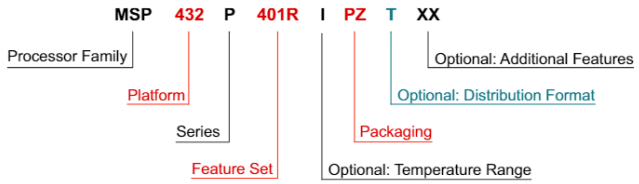
"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). Figure 8-1 provides a legend for reading the complete device name for any family member.

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Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon			
Platform	432 = TI's 32-Bit Low-Power Microcontroller Platform			
Series	P = Performance and Low-Power Series			
Feature Set	**First Digit** 4 = Flash-based devices up to 48 MHz	**Second Digit** 0 = General purpose	**Third Digit** 1 = ADC14	**Fourth Digit** R = 256KB of flash 64KB of SRAM M = 128KB of flash 32KB of SRAM
Optional: Temperature Range	S = 0°C to 50°C I = –40°C to 85°C T = –40°C to 105°C			
Packaging	http://www.ti.com/packaging			
Optional: Distribution Format	T = Small reel R = Large reel No markings = Tube or tray			
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified			

Figure 8-1. Device Nomenclature

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8.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at TI 32-bit MSP432 microcontrollers.

Table 8-1 lists the supported debug features. See the *Code Composer Studio 6.1 for MSP432 User's Guide* for details on the available hardware features. See *Advanced Debugging Using the Enhanced Emulation Module (EEM) With Code Composer Studio Version 6* and *MSP430™ Advanced Power Optimizations: ULP Advisor™ and EnergyTrace™ Technology* for further usage information.

Table 8-1. Hardware Debug Features

FAMILY	JTAG	SWD	NUMBER OF BREAKPOINTS	ITM	DWT	FPB
MSP432P4xx	Yes	Yes	6	Yes	Yes	Yes

EnergyTrace technology is supported with Code Composer Studio version 6.0 and newer. It requires specialized debugger circuitry, which is supported with the second-generation onboard eZ-FET flash emulation tool and second-generation stand-alone MSP-FET JTAG emulator. See *MSP430 Advanced Power Optimizations: ULP Advisor™ and EnergyTrace™ Technology*, the *Code Composer Studio 6.1 for MSP432 User's Guide*, and the *MSP432 Hardware Tools User's Guide* for more detailed information.

Design Kits and Evaluation Modules

100-Pin Target Development Board for MSP432P4x MCUs The MSP-TS432PZ100 is a stand-alone ZIF socket target board used to program and debug the MSP432 in-system through the JTAG interface or the Serial Wire Debug (SWD 2-wire JTAG) protocol. The development board supports all MSP432P401x flash parts in a 100-pin LQFP package (TI package code: PZ).

MSP432P401R LaunchPad™ Development Kit The MSP432P401R LaunchPad development kit enables you to develop high-performance applications that benefit from low-power operation. The kit features the MSP432P401R MCU, which includes a 48-MHz ARM Cortex M4F, 95-µA/MHz active power, and 850-nA RTC operation, a 14-bit 1-MSPS differential SAR ADC, and an AES256 accelerator.

Software

MSP432P401x Code Examples C Code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

MSP432 Capacitive Touch Software Library Free libraries for enabling capacitive touch capabilities on MSP432 MCUs.

MSP EnergyTrace™ Technology EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor ULP (Ultra-Low Power) Advisor is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application.

RTOS for MSP432 MSP432 MCUs offer compatibility with several TI and third party Real-Time Operating Systems (RTOS). Visit this link to learn about the key features of each to suit your design needs.

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TI-RTOS: Real-Time Operating System (RTOS) TI-RTOS accelerates development schedules by eliminating the need to create basic system software functions from scratch. TI-RTOS scales from a minimal footprint real-time multitasking kernel - TI-RTOS Kernel (formerly known as SYS/BIOS) - to a complete RTOS solution including protocol stacks, multicore communications, device drivers and power management. By providing essential system software components pretested and preintegrated, TI-RTOS enables developers to focus on differentiating their application.

MSP Driver Library Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 and MSP432 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP Graphics Library The MSP Graphics Library is a royalty-free set of graphics primitives for creating graphical user interfaces on MSP430 and MSP432 microcontroller-based boards that have a graphical display. The graphical library consists of two building layers of functionality: the display driver layer, specific to the display in use, and the graphics primitives layer, which draws points, lines, rectangles, circles, text, and bitmap images.

Digital Signal Processing Library The Texas Instruments™ Digital Signal Processing library is a set of highly optimized functions to perform many common signal processing operations on fixed-point numbers for MSP430™ and MSP432™ microcontrollers. This function set is typically utilized for applications where processing-intensive transforms are done in real-time for minimal energy and with very high accuracy. This library's optimal utilization of the MSP families' intrinsic hardware for fixed-point math allows for significant performance gains.

Development Tools

Code Composer Studio Integrated Development Environment for MSP Microcontrollers Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. For more information, see the *Code Composer Studio 6.1 for MSP432 User's Guide*.

ARM® Keil® MDK – Free 32KB IDE The ARM Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications. Keil MDK supports the low-power and high-performance MSP432 MCU family, and includes a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint. For more information, see the *ARM Keil MDK Version 5 for MSP432 User's Guide*.

IAR Embedded Workbench Kickstart IAR Embedded Workbench Kickstart for MSP is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications based on MSP430 and MSP432 microcontrollers. The code size limitation of C/C++ compiler is set to 8 KB for MSP430 devices and 32KB for MSP432 devices. For more information, see the *IAR Embedded Workbench for ARM 7.x for MSP432 User's Guide*.

Debuggers for MSP432 MSP432 MCUs are designed to work with a variety of debuggers from Texas Instruments and third-party vendors.

MSP MCU Programmer and Debugger The MSP-FET is a powerful emulation development tool – often called a debug probe – that allows users to quickly begin application development on MSP low-power microcontrollers.

MSP-GANG Production Programmer The MSP Gang Programmer is an MSP430 and MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process.

Pin Mux Tool The Pin MUX Utility is a software tool that provides a graphical user interface for configuring pin multiplexing settings, resolving conflicts, and specifying I/O cell characteristics for TI MPUs. Results are output as C header and code files that can be imported into software development kits or used to configure customer's custom software. Version 3 of the Pin Mux utility can automatically selecting a mux configuration that satisfies the requirements entered by the user.

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8.4 Documentation Support

The following documents describe the MSP430P401x MCUs. Copies of these documents are available on the TI website.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (see Section 8.5 for links to product folders). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP432P401R Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

MSP432P401M Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

User's Guides

MSP432P4xx Family Technical Reference Manual Detailed description of all modules and peripherals available in this device family.

Code Composer Studio 6.1 for MSP432 User's Guide This manual describes the use of the TI Code Composer Studio IDE (CCS) version 6.1 with the MSP432 low-power microcontrollers.

IAR Embedded Workbench for ARM 7.x for MSP432 User's Guide This manual describes the use of IAR Embedded Workbench for ARM (EWARM) version 7.x with the MSP432 low-power microcontrollers.

ARM Keil MDK Version 5 for MSP432 User's Guide This user's guide describes the use of the ARM Keil MDK version 5 with the MSP432 low-power microcontrollers.

GCC ARM Embedded Toolchain for MSP432 User's Guide This manual describes the setup and basic operation of the MSP432 programming and debug using GCC ARM compiler and the GDB debugger.

MSP432P401R Bootloader (BSL) User's Guide The MSP432 BSL enables users to communicate with embedded memory in the MSP432 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required.

MSP432 Capacitive Touch Software Library Programmer's Guide MSP432 microcontrollers are equipped with the peripherals needed to perform a capacitance measurement. The purpose of the capacitive touch software library is to create a single interface that can be integrated with the peripheral set found in MSP432 devices. This document explains the capacitive touch library configuration and use with MSP432 devices.

Application Reports

MSP432 Platform Porting The goals for this porting guide is to help developers accurately assess the effort to port an existing application from one MSP platform to another, ultimately to derive a porting strategy with complete hardware and software coverage that properly ports the existing application without introducing bugs due to platform differences yet taking advantages of the unique features or performance improvements introduced in the new platform.

Designing an Ultra-Low-Power (ULP) Application With MSP432™ Microcontrollers With the growing system complexity in ultra-low-power microcontroller applications, minimizing the overall energy consumption is one of the most difficult problems to solve. Multiple aspects including silicon, other onboard hardware components, and application software must be considered. There are some obvious generic techniques that can be used to reduce energy consumption such as reducing operating voltage or frequency. Many of these generic techniques may not greatly reduce energy consumption independently, but taken as a whole, the results can be significant, as there are many interdependencies across these components.

Maximizing MSP432P4xx Voltage Regulator Efficiency This application report describes the relationship of the MSP432P4xx DC-DC and LDO, provides guidelines on choosing which is most efficient for your application, and gives board layout considerations for the DC-DC.

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Leveraging Low-Frequency Power Modes on MSP432P4xx Microcontrollers Low power consumption is very important in all battery powered embedded applications. But the operating frequency of these embedded applications can be diverse based the needs of the application. Some applications might require operating at higher frequencies, in the order of several megahertz, while some other applications might require operating at lower frequencies, in the order of a few tens or a few hundreds of kilohertz. There are several microcontrollers in the market that offer good active mode power consumption when the operating frequency is in the order of several megahertz. But it is a challenge to get the power consumption low when the operating frequency is in the order of kilohertz. The low-frequency power modes available on the MSP432P4xx microcontrollers offer very low power consumption when low frequency of operation is used by the target application.

Software IP Protection on MSP432P4xx Microcontrollers Differentiations in embedded software applications enable differentiated products. Companies invest significant money in building differentiated software application. Hence, protecting this investment (application or portions of the application) is extremely important. This application note describes how to protect software intellectual property (IP) running on the Texas Instruments MSP432P401x family of microcontrollers.

Code Conversion Application for MSP432P401R This application note describes the use of the code conversion application delivered with version 2.0.0 (and above) of the MSP432P401R device header files. In these revisions of the MSP432P401R device header files, the coding style has been adapted to CMSIS. This may lead to compilation errors in user code if the code is not converted. MSP430 style register definitions have also been removed with exception of legacy 16-bit IPs (see msp432p401r_classic.h).

8.5 Related Links

Table 8-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP432P401R	Click here	Click here	Click here	Click here	Click here
MSP432P401M	Click here	Click here	Click here	Click here	Click here

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 Trademarks

MSP432, MSP430, ULP Advisor, EnergyTrace, LaunchPad, Texas Instruments, E2E are trademarks of Texas Instruments.
ARM, Cortex, Thumb, Keil are registered trademarks of ARM Ltd.
ULPBench, ULPMark are trademarks of EEMBC.
All other trademarks are the property of their respective owners.

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8.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

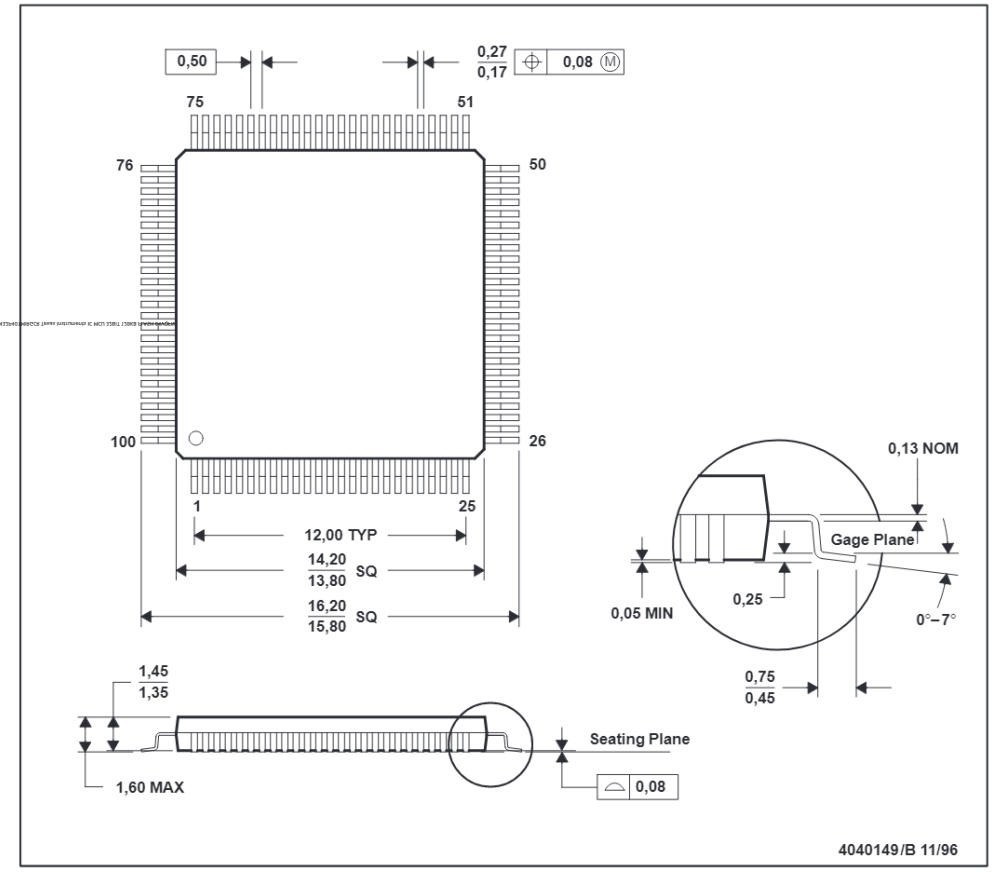
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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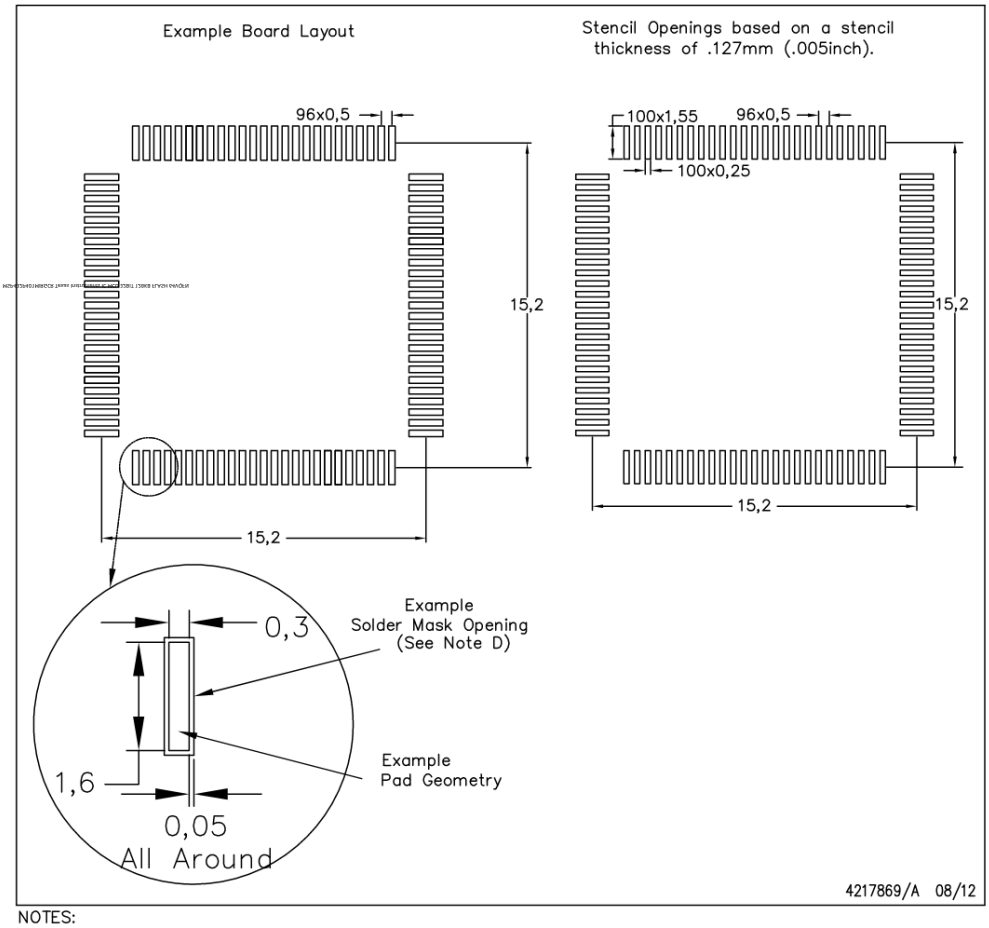
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

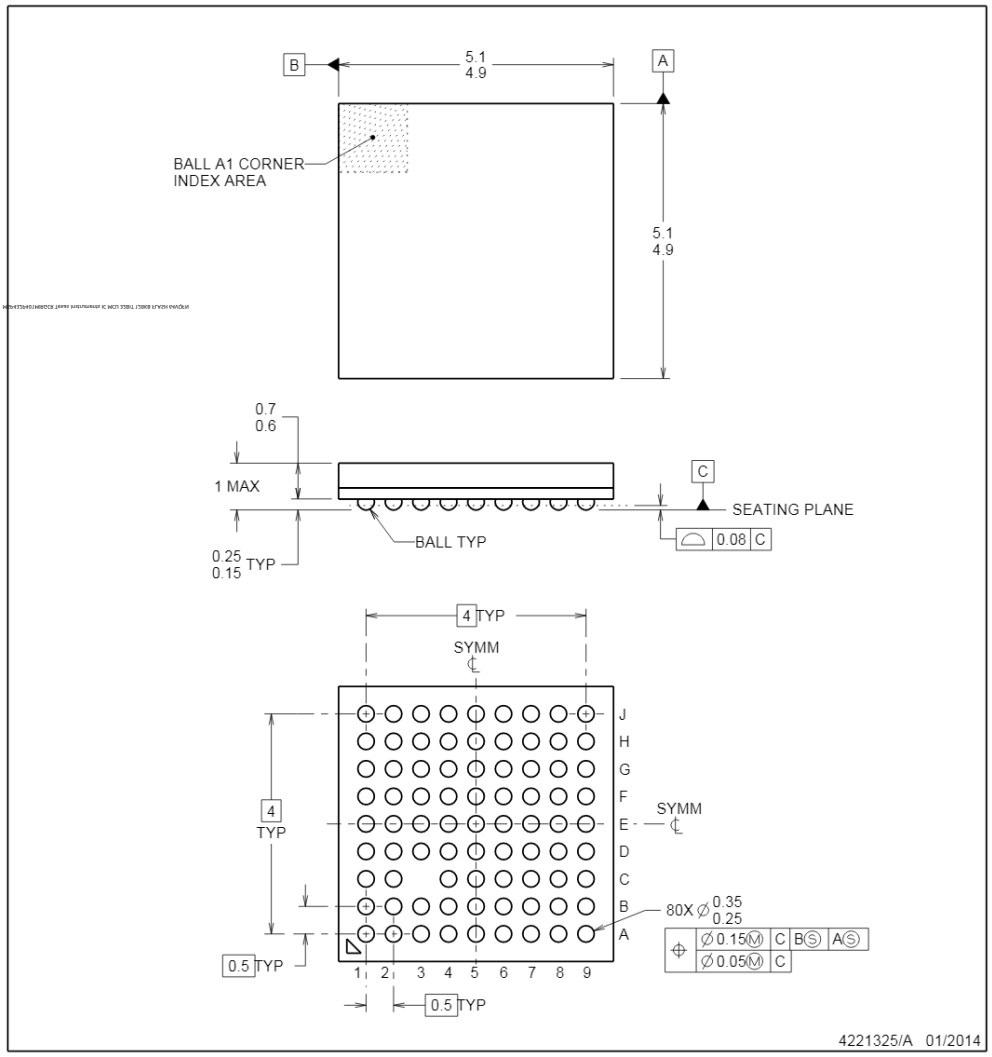
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

ZXH0080A

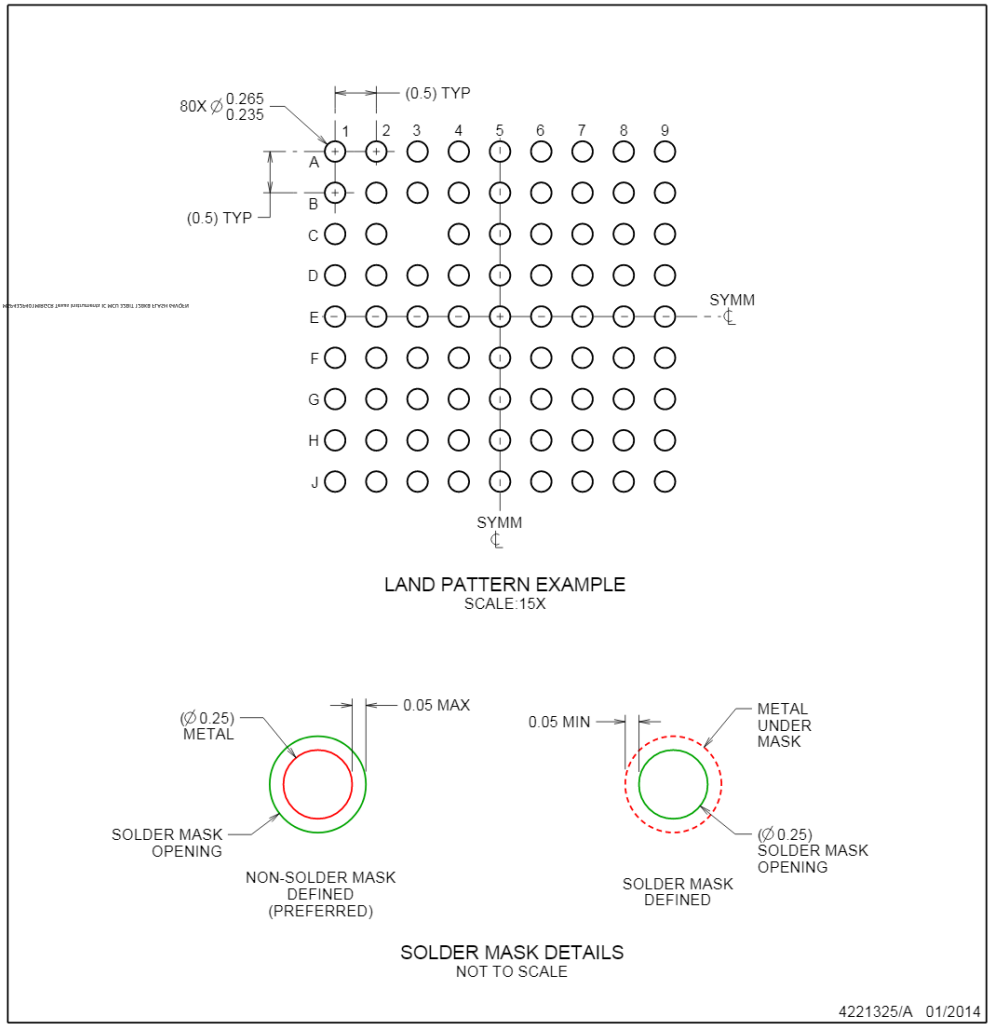
NFBGA - 1 mm max height

BALL GRID ARRAY



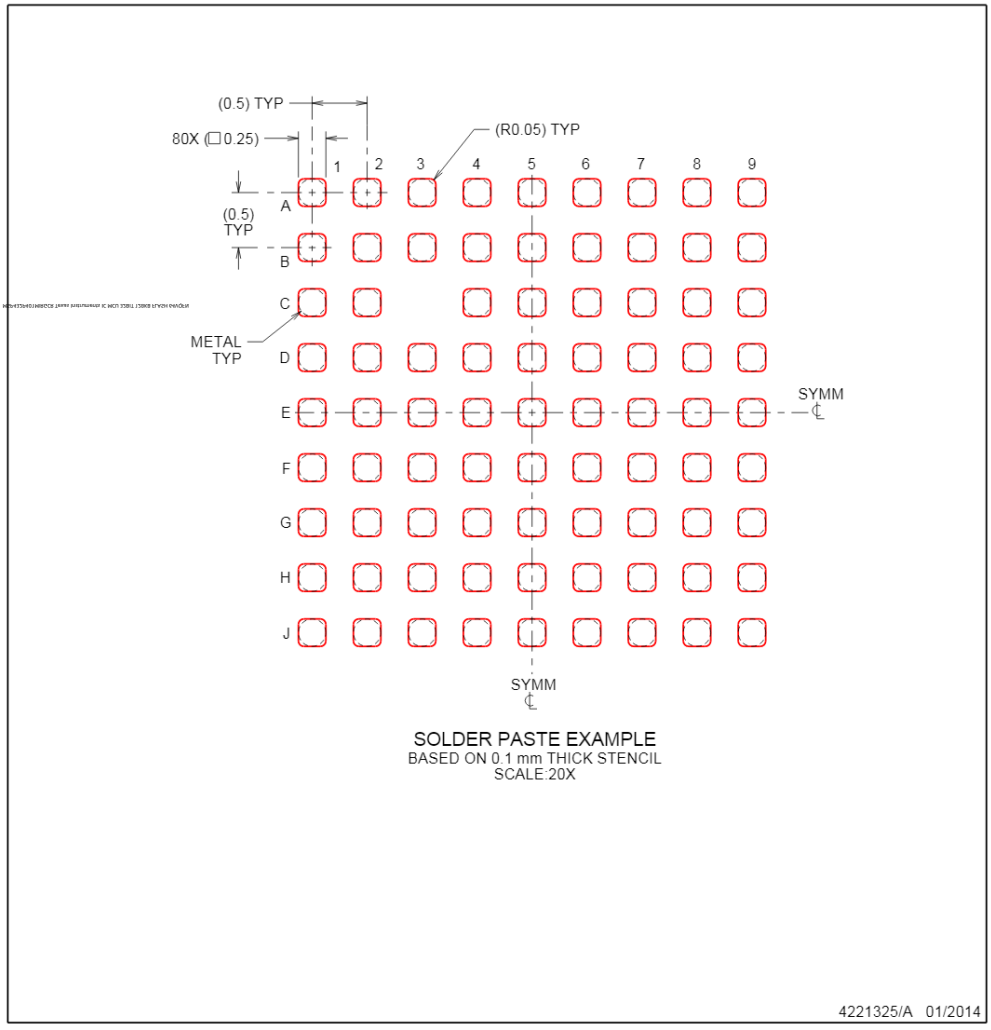
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).



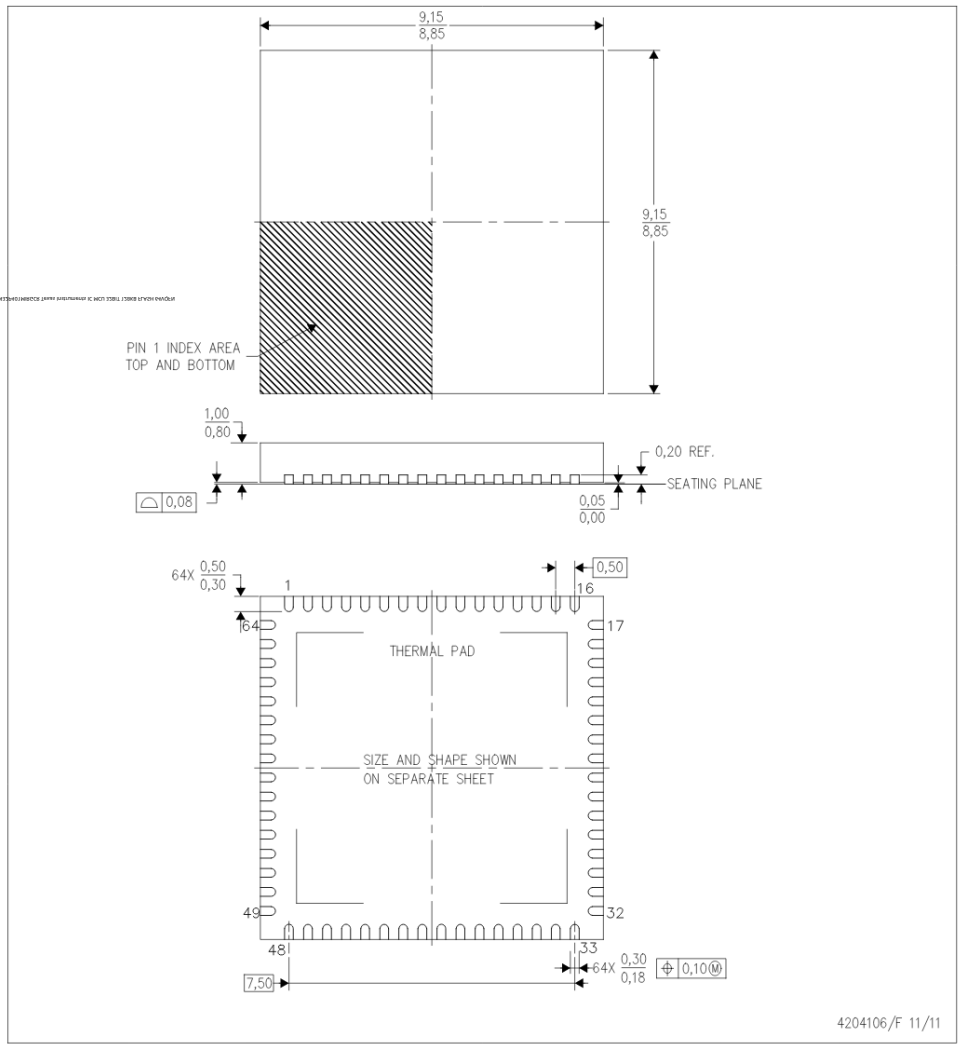
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221325/A 01/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

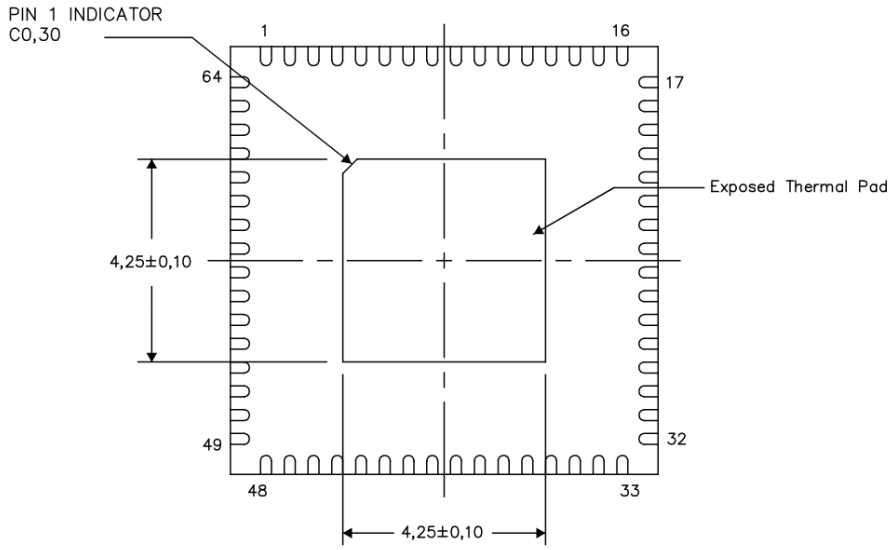
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206192–3/AE 03/15

NOTE: A. All linear dimensions are in millimeters

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP432P401MIPZ	PREVIEW	LQFP	PZ	100	90	TBD	Call TI	Call TI	-40 to 85		
MSP432P401MIPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	MSP432P401M	Samples
MSP432P401MIRGC	PREVIEW	VQFN	RGC	64	100	TBD	Call TI	Call TI	-40 to 85		
MSP432P401MIRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI	-40 to 85		
MSP432P401MIRGCT	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI	-40 to 85		
MSP432P401MIZXH	PREVIEW	NFBGA	ZXH	80	360	TBD	Call TI	Call TI	-40 to 85		
MSP432P401MIZXHR	PREVIEW	NFBGA	ZXH	80	2500	TBD	Call TI	Call TI	-40 to 85		
MSP432P401MIZXHT	PREVIEW	NFBGA	ZXH	80	250	TBD	Call TI	Call TI	-40 to 85		
MSP432P401RIPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	MSP432P401R	Samples
MSP432P401RIRGC	PREVIEW	VQFN	RGC	64	100	TBD	Call TI	Call TI	-40 to 85		
MSP432P401RIRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI	-40 to 85		
MSP432P401RIRGCT	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI	-40 to 85		
MSP432P401RIZXH	PREVIEW	NFBGA	ZXH	80	360	TBD	Call TI	Call TI	-40 to 85		
MSP432P401RIZXHR	PREVIEW	NFBGA	ZXH	80	2500	TBD	Call TI	Call TI	-40 to 85		
MSP432P401RIZXHT	PREVIEW	NFBGA	ZXH	80	250	TBD	Call TI	Call TI	-40 to 85		
XMS432P401MIPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI	-40 to 85		
XMS432P401RIPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI	-40 to 85		
XMS432P401RIRGCT	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI	-40 to 85		
XMS432P401RIZXHR	PREVIEW	NFBGA	ZXH	80	1000	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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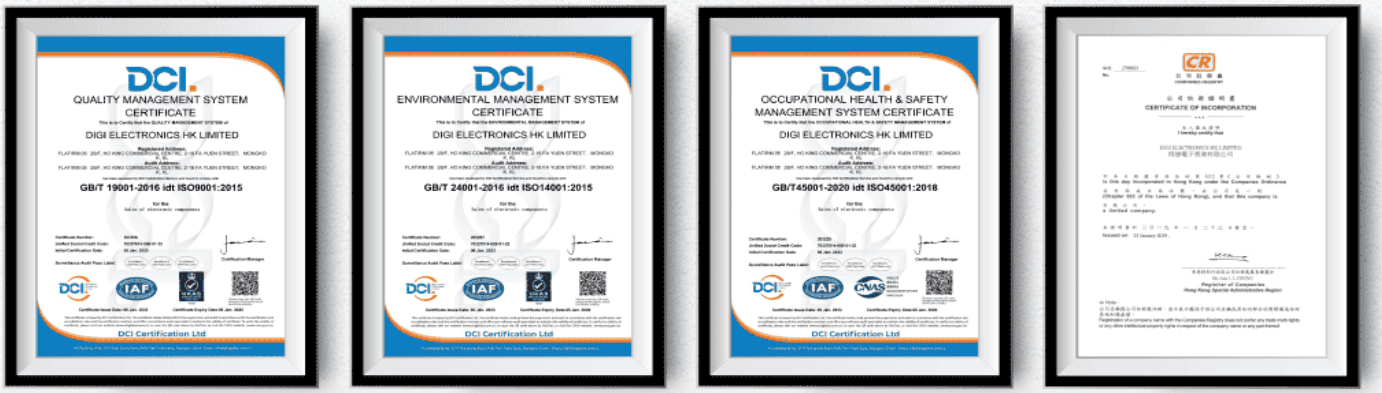
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