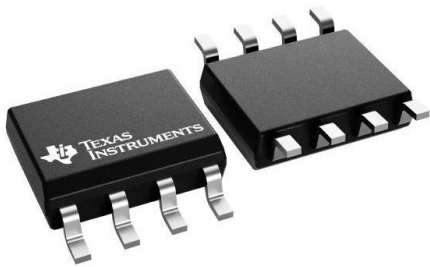


OPA1633DGNR Datasheet

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<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	OPA1633DGNR-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	OPA1633DGNR
Description	IC
Detailed Description	Standard Amplifier 1 Circuit Differential 8-HVSSOP



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

OPA1633DGNR

Series:

-

Amplifier Type:

Standard

Output Type:

Differential

Gain Bandwidth Product:

200 MHz

Current - Input Bias:

6.8 μ A

Current - Supply:

11mA

Voltage - Supply Span (Min):

4 V

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

8-PowerTSSOP, 8-MSOP (0.118", 3.00mm Width)

Manufacturer:

Texas Instruments

Product Status:

Active

Number of Circuits:

1

Slew Rate:

80V/ μ s

-3db Bandwidth:

200 MHz

Voltage - Input Offset:

200 μ V

Current - Output / Channel:

85 mA

Voltage - Supply Span (Max):

35 V

Mounting Type:

Surface Mount

Supplier Device Package:

8-HVSSOP

OPA1633 High-Performance, Fully Differential Audio Operational Amplifier



1 Features

- Excellent sound quality
- Ultra low distortion: 132 dB
- Low noise: 1.1 nV/√Hz
- High speed:
 - Slew rate: 80 V/μs
 - Gain bandwidth product: 200 MHz
- Fully differential architecture:
 - Balanced input and output converts single-ended input to balanced differential output
- Wide supply range: ±2.5 V to ±17.5 V
- Shutdown current: 0.77 mA ($V_S = \pm 5$ V)
- Temperature range: –40°C to +85°C
- Packages: HVSSOP-8, SOIC-8

2 Applications

- Professional audio mixer or control surface
- Professional microphones and wireless systems
- Professional speaker systems
- Professional audio amplifier
- Soundbar
- Turntable
- Professional video camera
- Guitar and other instrument amplifier
- Data acquisition (DAQ)
- Pin-compatible upgrade to the [OPA1632](#)

3 Description

The OPA1633 is a fully differential amplifier (FDA) designed to drive high-performance audio analog-to-digital converters (ADCs) or as a predriver for class-D amplifiers.

The OPA1633 delivers excellent audio quality, very low noise, a large output voltage swing, and a high current drive. The OPA1633 has an excellent gain bandwidth of 200 MHz and a very fast slew rate of 80 V/μs that helps produce exceptionally low distortion. A very low input voltage noise of 1.1 nV/√Hz further provides maximum signal-to-noise ratio and dynamic range.

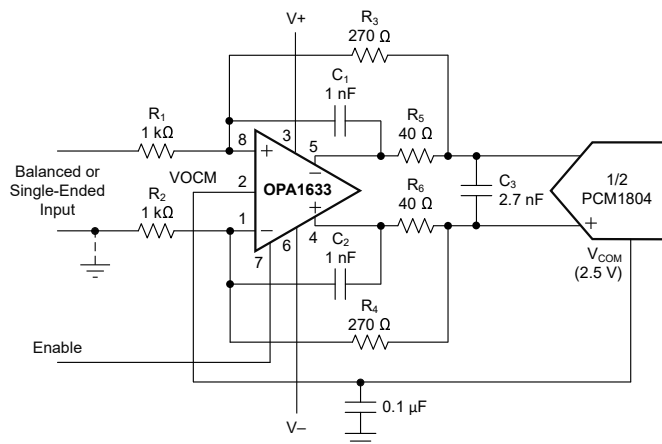
The flexibility of the fully differential architecture allows for easy implementation of a single-ended to fully differential output conversion. Differential output reduces even-order harmonics and minimizes common-mode noise interference. The OPA1633 provides excellent performance when used to drive high-performance audio ADCs such as the [PCM1804](#). A shutdown feature is included to save power when the device is not in use.

The OPA1633 is characterized to operate from –40°C to +85°C and available in an SO-8 package and a thermally enhanced, HVSSOP PowerPAD™ integrated circuit package.

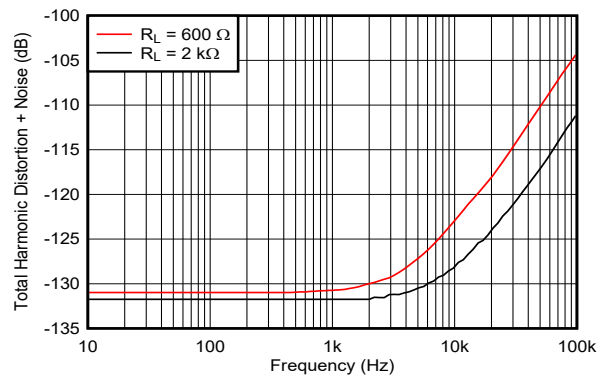
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
OPA1633	D (SOIC, 8)	4.9 mm × 6 mm
	DGN (HVSSOP, 8)	3 mm × 4.9 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Diagram



THD + Noise vs Frequency



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2 Applications	1	8 Application and Implementation	13
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2023) to Revision A (June 2023)	Page
• Changed data sheet status from advanced information (preview) to production data (active).....	1

5 Pin Configuration and Functions

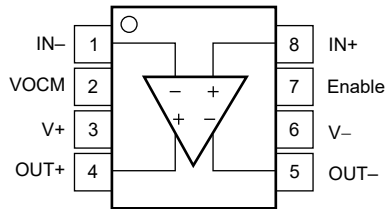


Figure 5-1. D Package, 8-Pin SOIC or DGN⁽¹⁾ Package, 8-Pin HVSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽²⁾	DESCRIPTION
NAME	NO.		
Enable	7	I	Active-high enable pin
V+	3	I/O	Positive supply voltage pin
V-	6	I/O	Negative supply voltage pin
IN+	8	I	Positive input voltage pin
IN-	1	I	Negative input voltage pin
VOCM	2	I	Output common-mode control voltage pin
OUT+	4	O	Positive output voltage pin
OUT-	5	O	Negative output voltage pin

- (1) Solder the exposed DGN package thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.
- (2) I = input, O = output.

OPA1633

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT
V _S	Supply voltage		±18.5	V
	Supply turn on and turn off dV/dT ⁽³⁾		1.7	V/μs
V _I	Input voltage		±V _S	V
I _O	Output current		150	mA
I _{IN}	Continuous input current		10	mA
V _{ID}	Differential input voltage		±1.5	V
T _J	Junction temperature		150	°C
T _A	Ambient temperature	–40	85	°C
T _{stg}	Storage temperature	–65	150	°C

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- The OPA1633 HVSSOP PowerPAD integrated circuit package incorporates a thermal pad on the underside of the chip. This thermal pad acts as a heat sink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief [SLMA002](#) for more information about using the thermally-enhanced PowerPAD integrated circuit package.
- Stay below this specification to make sure that the edge-triggered ESD absorption devices across the supply pins remain off.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _S	Supply voltage	Dual	±2	±17.5	V
		Single	4	35	
T _A	Ambient temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA1633		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	126.3	57.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	67.3	76.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	69.8	30.0	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	19.5	4.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	69.0	29.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	14.3	°C/W

- For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $V_S = \pm 15\text{ V}$, $R_F = 390\ \Omega$, $R_L = 800\ \Omega$, and $G = +1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.2	2	mV
dV_{OS}/dT	Offset voltage drift				± 0.6		$\mu\text{V}/^\circ\text{C}$
PSRR	Power supply rejection ratio				13	100	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT							
I_B	Input bias current				6.8	11.5	μA
I_{OS}	Input offset current				± 20	± 400	nA
NOISE							
e_N	Input voltage noise density		$f = 10\text{ kHz}$		1.1		$\text{nV}/\sqrt{\text{Hz}}$
i_N	Input current noise density		$f = 10\text{ kHz}$		1.3		$\text{pA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			$(V^-) + 1.5$		$(V^+) - 1$	
CMRR	Common-mode rejection ratio			80	100		dB
INPUT IMPEDANCE							
	Input impedance	Common-mode	Measured into each input pin		$320 \parallel 1.3$		$\text{M}\Omega \parallel \text{pF}$
		Differential	Measured into each input pin		$12 \parallel 2.3$		$\text{k}\Omega \parallel \text{pF}$
OPEN-LOOP GAIN							
A_{OL}	Open-loop gain			91	97		dB
FREQUENCY RESPONSE							
SSBW	Small signal bandwidth	$(V_O = 100\text{ mV}_{PP}, \text{ peaking} < 0.5\text{ dB})$	$G = +1, R_F = 348\ \Omega$		200		MHz
			$G = +2, R_F = 602\ \Omega$		117		
			$G = +5, R_F = 1.5\text{ k}\Omega$		53		
			$G = +10, R_F = 3.01\text{ k}\Omega$		26		
	Bandwidth for 0.1-dB flatness		$G = +1, V_O = 100\text{ mV}_{PP}$		40		MHz
	Peaking at a gain of 1		$V_O = 100\text{ mV}_{PP}$		0.25		dB
LSBW	Large-signal bandwidth		$G = +2, V_O = 20\text{ V}_{PP}$		3		MHz
SR	Slew rate (25% to 75%)		$G = +1$		80		$\text{V}/\mu\text{s}$
			Rise and fall time	$G = +1, V_O = 5\text{-V step}$	62		ns
t_s	Settling time	To 0.1%	$G = +1, V_O = 2\text{-V step}$		30		ns
		To 0.01%	$G = +1, V_O = 2\text{-V step}$		40		
THD+N	Total harmonic distortion + noise	Differential input/output	$G = +1, f = 1\text{ kHz}, V_O = 3\text{ V}_{RMS}$	$R_L = 600\ \Omega$	131		dB
				$R_L = 2\text{ k}\Omega$	132		
		Single-ended in/differential out	$G = +1, f = 1\text{ kHz}, V_O = 3\text{ V}_{RMS}$	$R_L = 600\ \Omega$	131		
				$R_L = 2\text{ k}\Omega$	132		
IMD	Intermodulation distortion	Differential input/output	$G = +1, \text{ SMPTE/DIN}, V_O = 2\text{ V}_{PP}$	$R_L = 600\ \Omega$	125		dB
				$R_L = 2\text{ k}\Omega$	125		
		Single-ended in/differential out	$G = +1, \text{ SMPTE/DIN}, V_O = 2\text{ V}_{PP}$	$R_L = 600\ \Omega$	125		
				$R_L = 2\text{ k}\Omega$	125		
	Headroom		$\text{THD} < 0.01\%, R_L = 2\text{ k}\Omega$		40		V_{PP}

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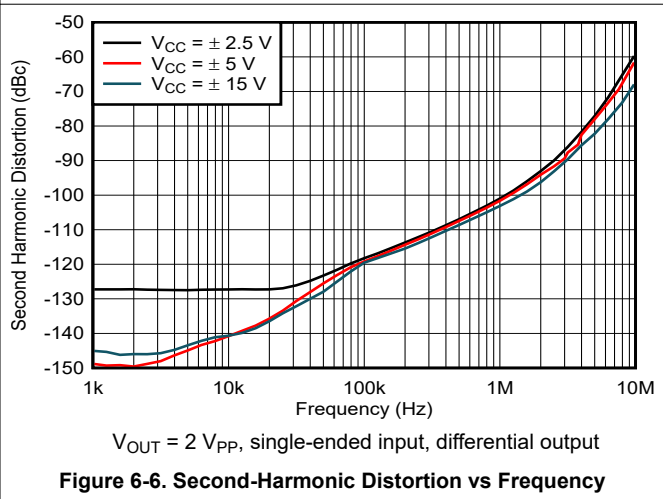
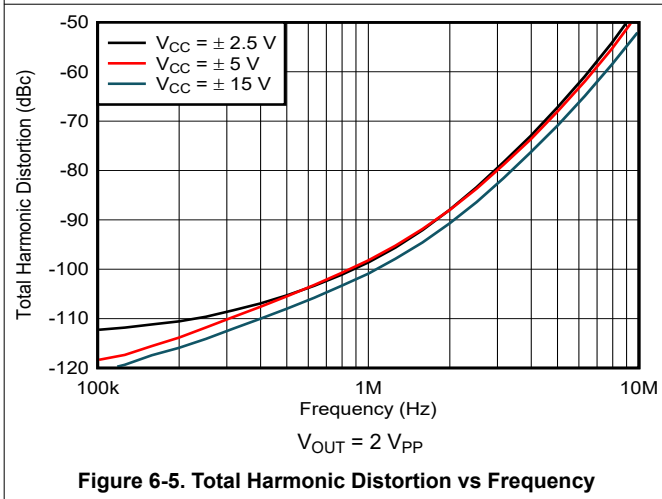
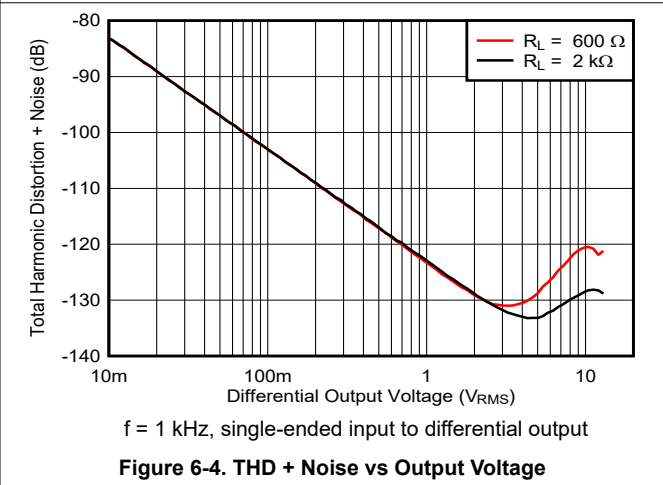
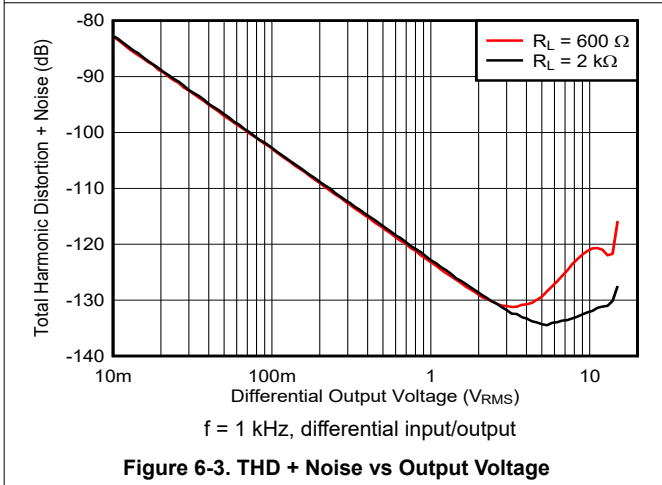
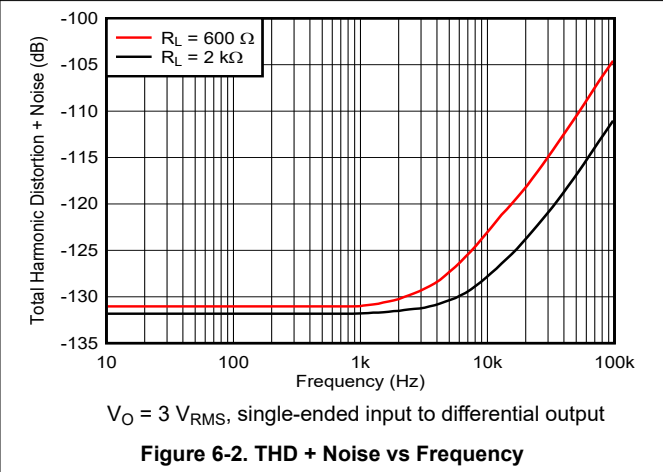
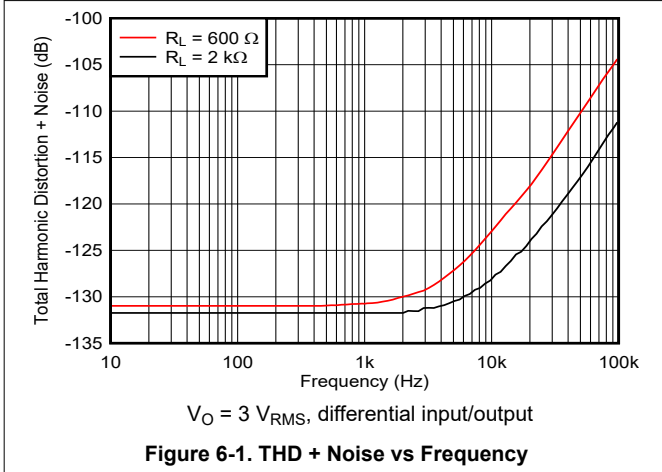
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6.5 Electrical Characteristics (continued)at $V_S = \pm 15\text{ V}$, $R_F = 390\ \Omega$, $R_L = 800\ \Omega$, and $G = +1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing	$R_L = 1\text{ k}\Omega$	$(V^+) - 1.9$		$(V^-) + 1.9$	V
I_O	Output current		65	85		mA
	Closed-loop output impedance	$G = +1$, $f = 100\text{ kHz}$		0.1		Ω
POWER DOWN						
	Enable voltage threshold			$(V^-) + 1.45$	$(V^-) + 1.5$	V
	Disable voltage threshold		$(V^-) + 0.8$	$(V^-) + 1.4$		V
I_{SD}	Shutdown current	$V_S = \pm 5\text{ V}$, $V_{Enable} = -5\text{ V}$		0.77		mA
		$V_S = \pm 15\text{ V}$, $V_{Enable} = -15\text{ V}$		1.4		
	Turn-on delay	Time for I_Q to reach 50%		0.12		μs
	Turn-off delay	Time for I_Q to reach 50%		0.03		μs
POWER SUPPLY						
I_Q	Quiescent current			11	13.2	mA

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_F = 348\ \Omega$, $G = +1$, and $R_L = 2\ \text{k}\Omega$ (unless otherwise noted)



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6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_F = 348\ \Omega$, $G = +1$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

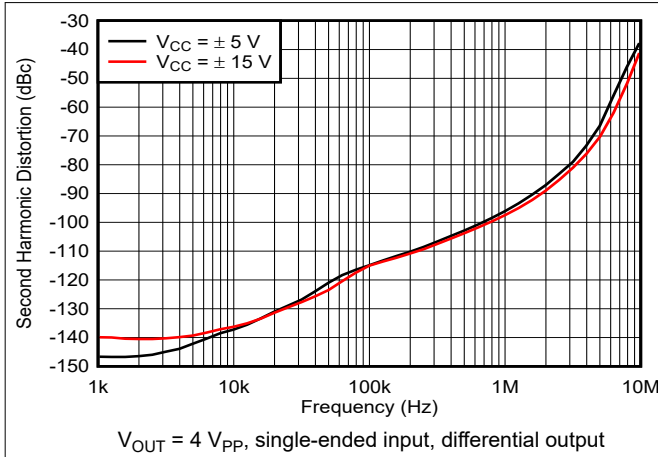


Figure 6-7. Second-Harmonic Distortion vs Frequency

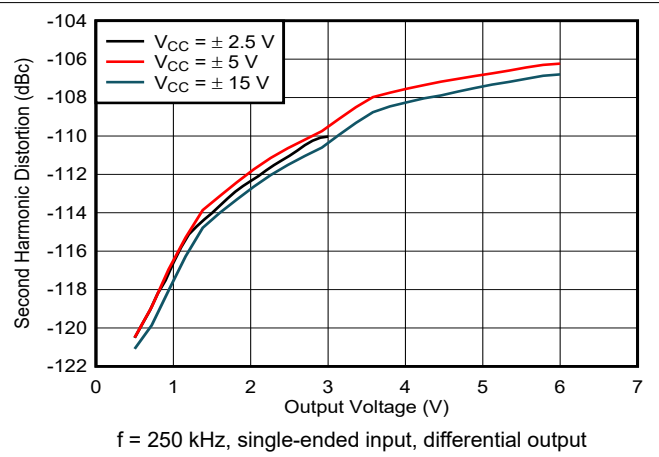


Figure 6-8. Second-Harmonic Distortion vs Output Voltage

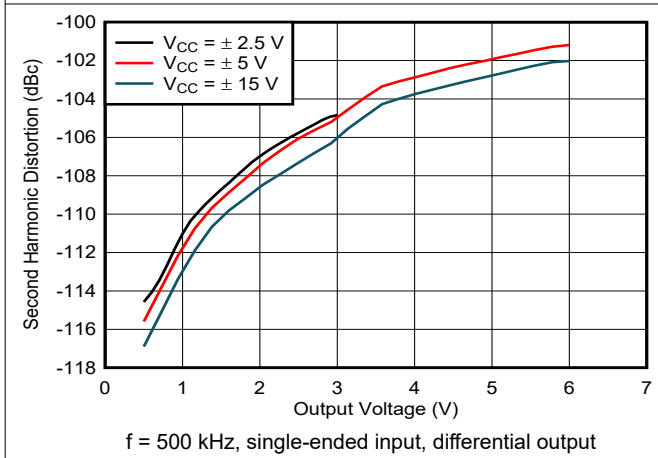


Figure 6-9. Second-Harmonic Distortion vs Output Voltage

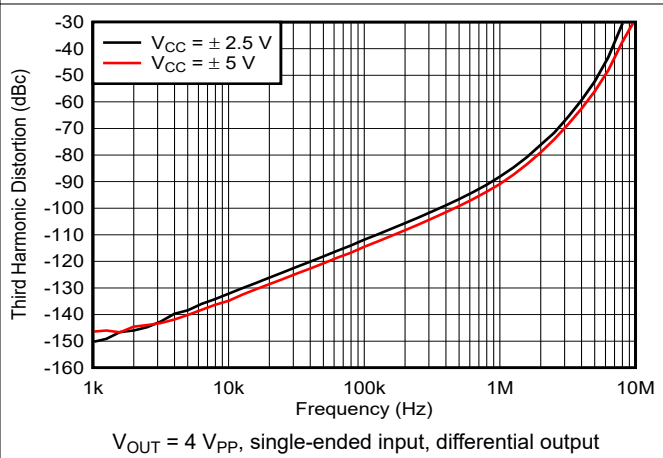


Figure 6-10. Third-Harmonic Distortion vs Frequency

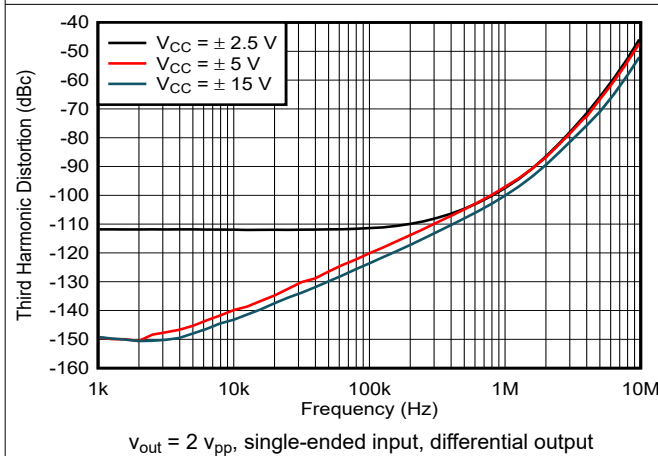


Figure 6-11. Third-Harmonic Distortion vs Frequency

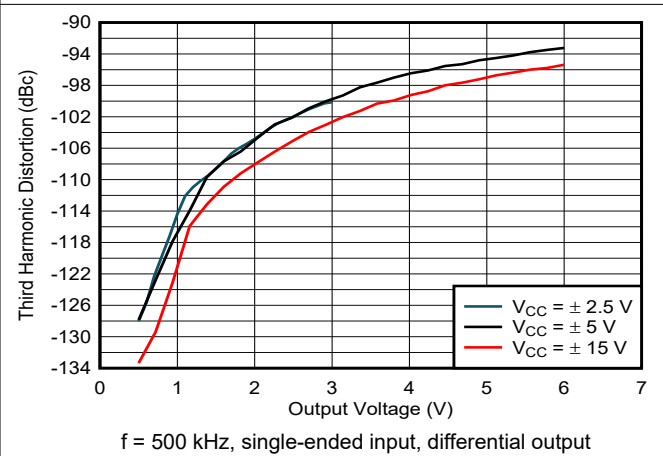


Figure 6-12. Third-Harmonic Distortion vs Output Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_F = 348\ \Omega$, $G = +1$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

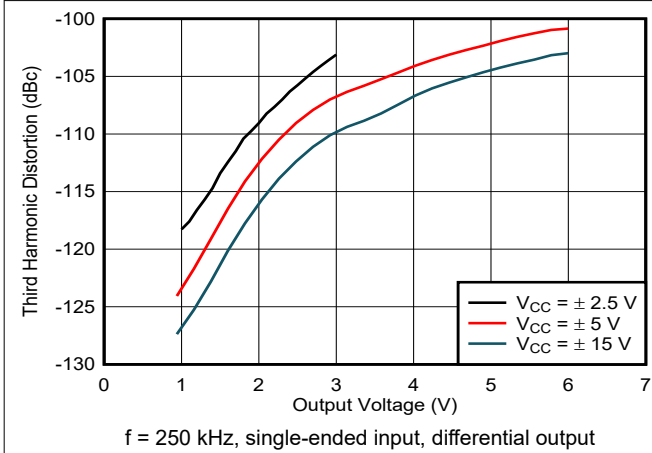


Figure 6-13. Third-Harmonic Distortion vs Output Voltage

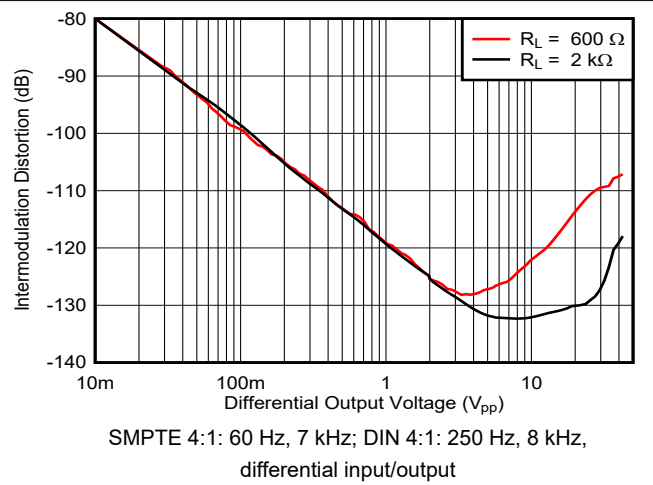


Figure 6-14. Intermodulation Distortion vs Output Voltage

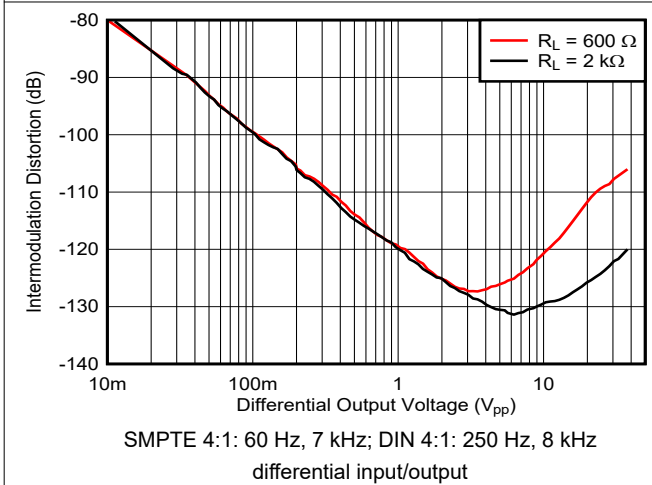


Figure 6-15. Intermodulation Distortion vs Output Voltage

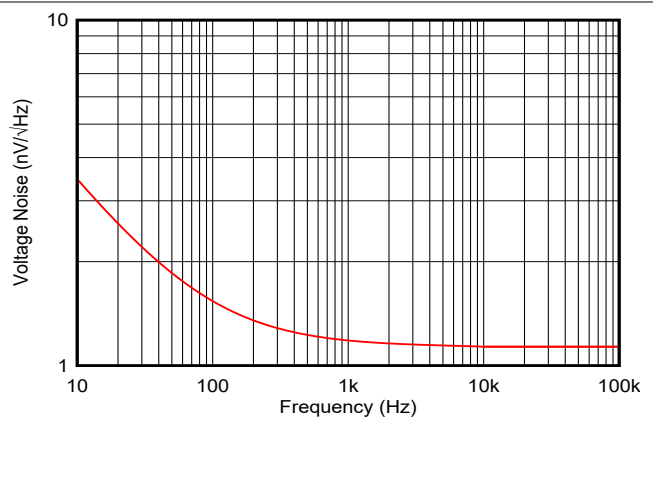


Figure 6-16. Voltage Noise vs Frequency

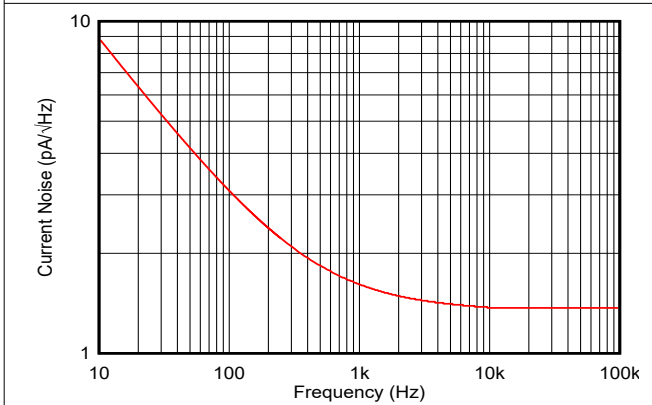


Figure 6-17. Current Noise vs Frequency

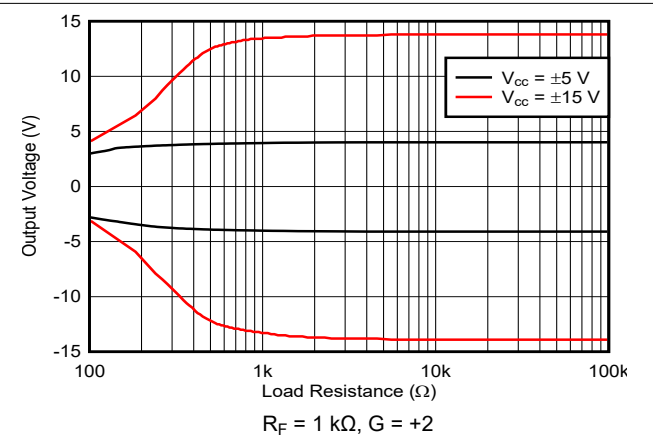


Figure 6-18. Output Voltage vs Differential Load Resistance

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6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_F = 348\ \Omega$, $G = +1$, and $R_L = 2\ \text{k}\Omega$ (unless otherwise noted)

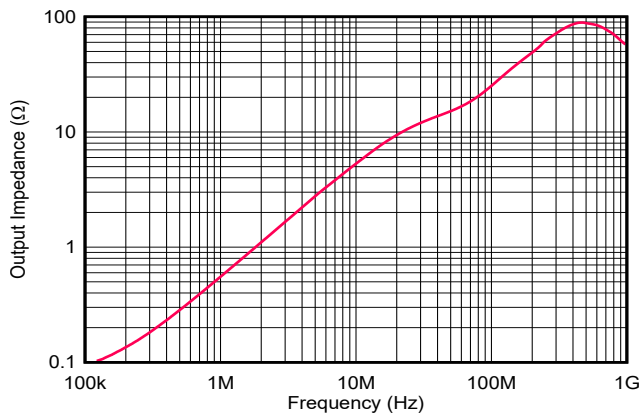


Figure 6-19. Output Impedance vs Frequency

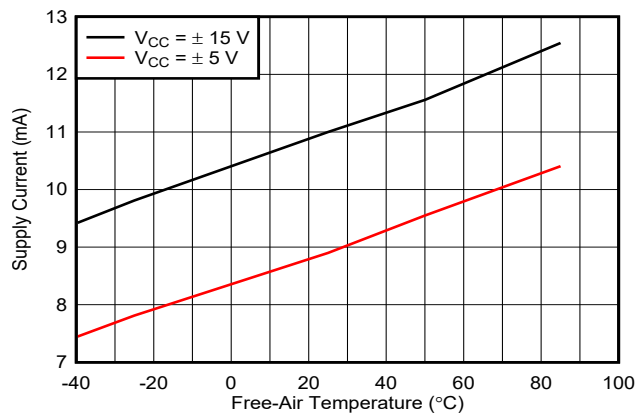


Figure 6-20. Supply Current vs Free-Air Temperature

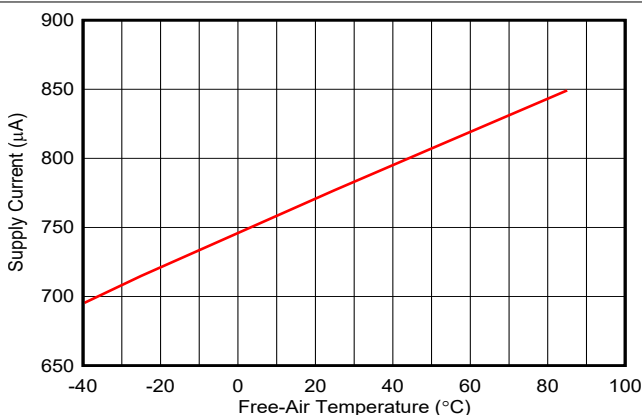


Figure 6-21. Supply Current vs Free-Air Temperature (Shutdown State)

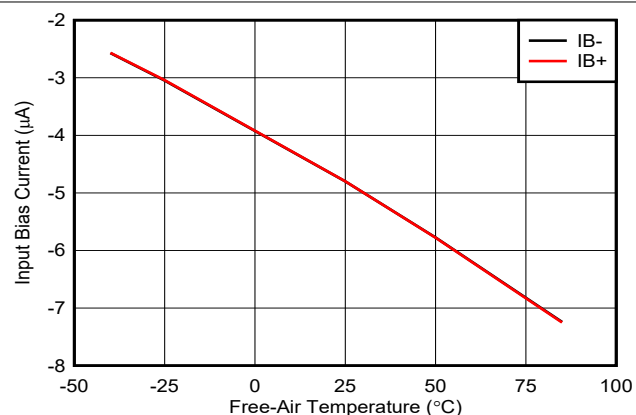


Figure 6-22. Input Bias Current vs Free-Air Temperature

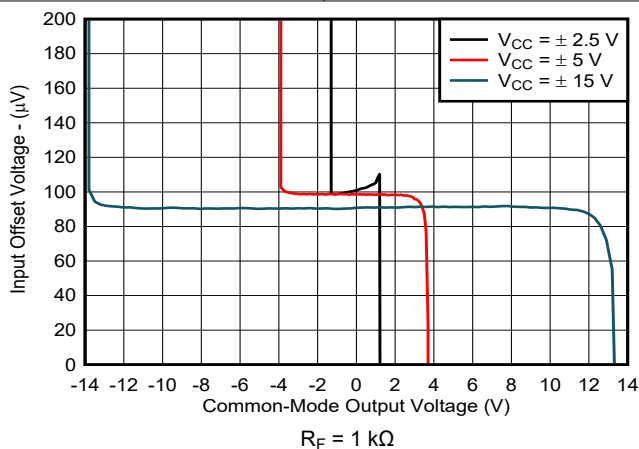


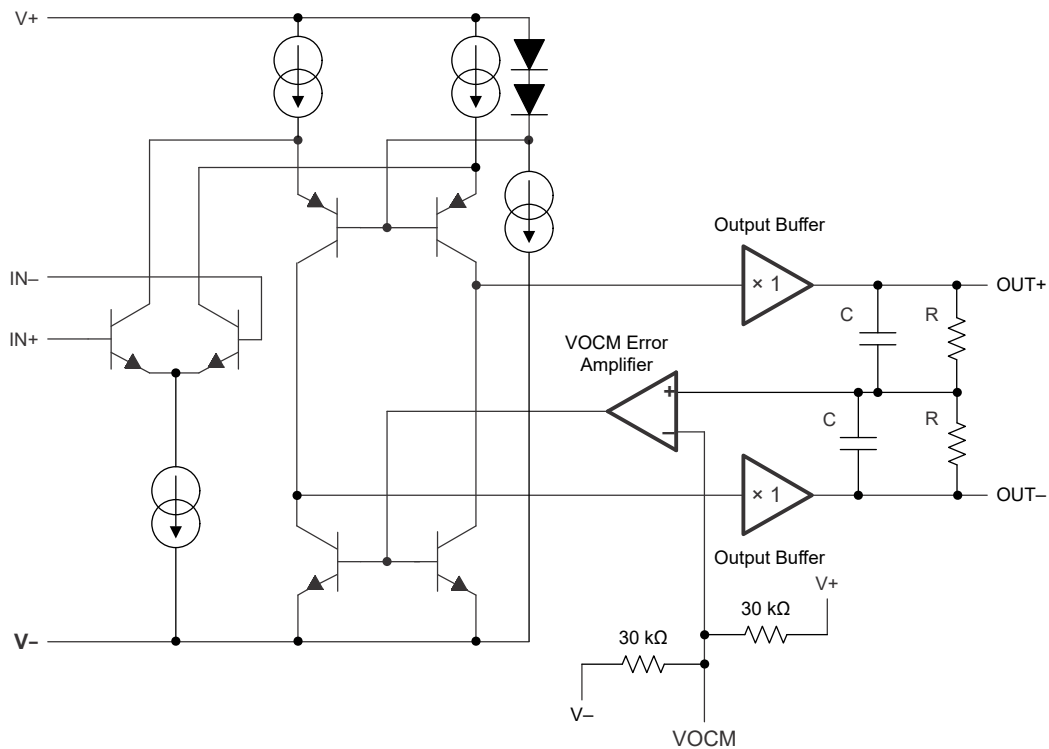
Figure 6-23. Input Offset Voltage vs Common-Mode Output Voltage

7 Detailed Description

7.1 Overview

The OPA1633 is a fully differential amplifier (FDA). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, refer to the [Fully Differential Amplifiers application note](#).

7.2 Functional Block Diagram



OPA1633

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7.3 Feature Description

Figure 7-1 and Figure 7-2 depict the differences between the operation of the OPA1633 in two different modes. FDAs can work with a differential input or be implemented as a single-ended input and differential output.

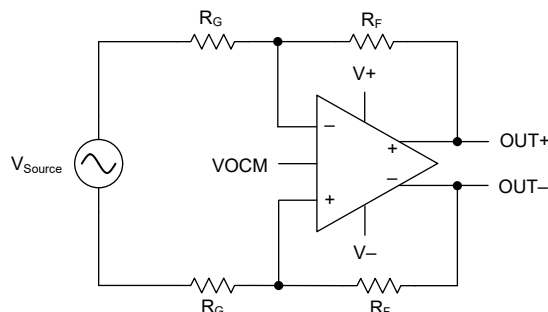


Figure 7-1. Amplifying Differential Input Signals

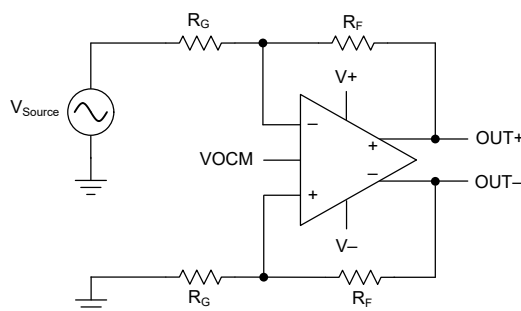


Figure 7-2. Amplifying Single-Ended Input Signals

7.4 Device Functional Modes

7.4.1 Shutdown Function

The shutdown (enable) function of the OPA1633 is referenced to the negative supply of the operational amplifier. A valid logic low (< 0.8 V above negative supply) applied to the Enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than 2 V above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pullup resistor enables the device. Turn-on and turn-off times are approximately 2 μ s each.

Quiescent current is reduced to approximately 0.77 mA when the amplifier is disabled. When disabled, the output stage is *not* in a high-impedance state. Thus, the shutdown function cannot be used to create a multiplexed switching function in series with multiple amplifiers.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the OPA1633. A voltage applied to the VO_{CM} pin from a low-impedance source can be used to directly set the output common-mode voltage. If left floating, the VO_{CM} pin defaults to the mid-rail voltage, defined as:

$$\frac{(V+) + (V-)}{2} \quad (1)$$

To minimize common-mode noise, connect a 0.1- μ F bypass capacitor to the VO_{CM} pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. This current is supplied by the output stage of the amplifier; therefore, additional power dissipation is created. For commonly used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current can be significant in some applications and can dictate use of the HVSSOP (DGN) PowerPAD integrated circuit package to effectively control self-heating.

8.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$\text{Output Balance Error} = \frac{\left(\frac{(V_{\text{OUT}+}) - (V_{\text{OUT}-})}{2} \right)}{(V_{\text{OUT}+}) - (V_{\text{OUT}-})} \quad (2)$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, use 1% tolerance resistors or better to optimize performance. [Table 8-1](#) provides the recommended resistor values to use for a particular gain.

Table 8-1. Recommended Resistor Values

GAIN (V/V)	R _G (Ω)	R _F (Ω)
1	390	390
2	374	750
5	402	2010
10	402	4020

OPA1633

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8.2 Typical Application

Figure 8-1 shows the OPA1633 used as a differential-output driver for the PCM1804 high-performance audio ADC.

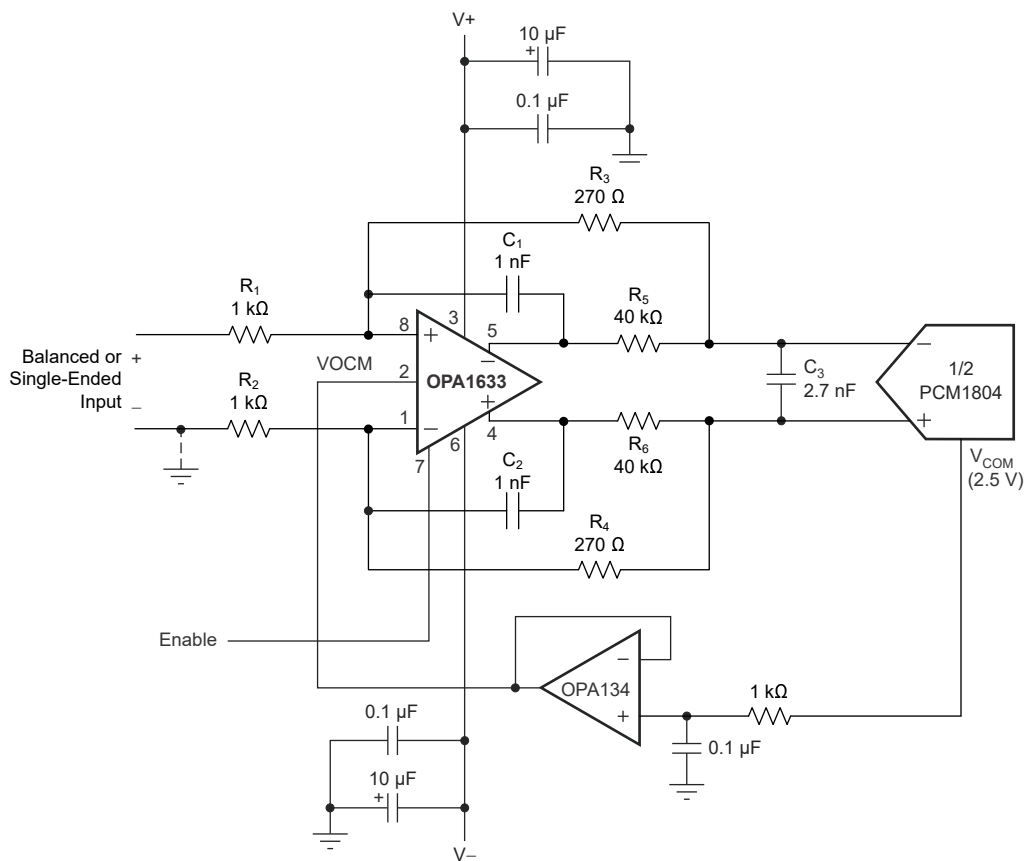


Figure 8-1. ADC Driver for Professional Audio

8.2.1 Design Requirements

Table 8-2 provides example design parameters and values for the typical application design example shown in Figure 7-1.

Table 8-2. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±17.5 V
Amplifier topology	Voltage feedback
Output control	DC-coupled with output common-mode control capability
Filter requirement	500-kHz, multiple-feedback low-pass filter

8.2.2 Detailed Design Procedure

Supply voltages of ± 15 V are commonly used for the OPA1633. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as ± 8 V can be used in this application with excellent performance. This lower-voltage operation reduces power dissipation and heat rise. Bypass power supplies with 10- μ F tantalum capacitors in parallel with 0.1- μ F ceramic capacitors to avoid possible oscillations and instability.

The V_{COM} reference voltage output on the **PCM1804** ADC provides the proper input common-mode reference voltage (2.5 V). This V_{COM} voltage is buffered with op amp by the **OPA134** and drives the output common-mode voltage pin of the OPA1633. This biases the average output voltage of the OPA1633 to 2.5 V.

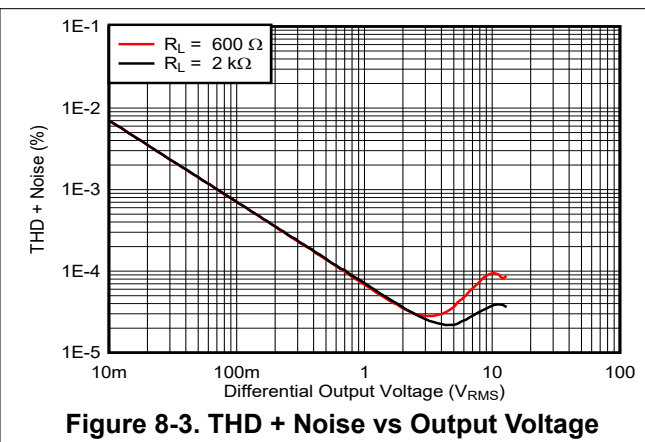
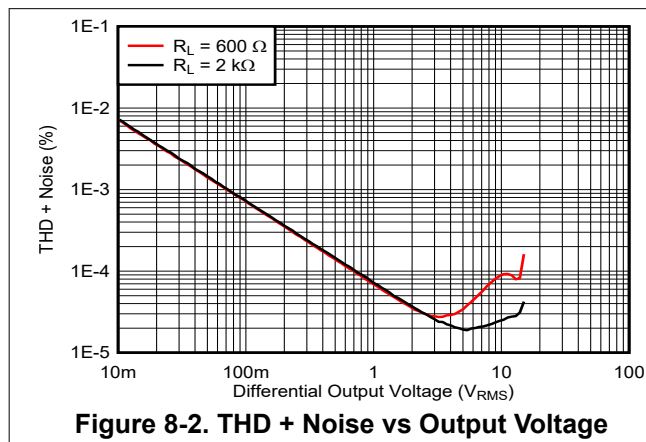
The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly used audio line levels. Gain can be adjusted, if necessary, by changing the values of R_1 and R_2 . Keep the feedback resistor values (R_3 and R_4) relatively low, as indicated, for best noise performance.

Resistors R_5 , R_6 , and C_3 provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values can help optimize performance with different ADCs.

Make sure to maintain accurate resistor matching on R_1/R_2 and R_3/R_4 to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, see **Figure 8-1**), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Choose capacitors C_1 , C_2 , and C_3 carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

8.2.3 Application Curves



8.3 Power Supply Recommendations

The OPA1633 device is designed to operate on power supplies ranging from ± 2.5 V to ± 17.5 V. Single power supplies ranging from 5 V to 35 V can also be used. Use a power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, make sure to provide isolation between digital signal noise and the analog input pins. The OPA1633 is connected to power supplies through pin 3 (V+) and pin 6 (V-). Decouple each supply pin to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane, configure the vias for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, do not power on the OPA1633 device with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

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8.4 Layout**8.4.1 Layout Guidelines**

1. The thermal pad is electrically isolated from the silicon and all leads. Connecting the thermal pad to any potential voltage between the power-supply voltages is acceptable; however, best practice is to tie to ground because ground is generally the largest conductive plane.
2. Prepare the printed circuit board (PCB) with a top-side etch pattern, as shown in [Figure 8-4](#). Use etch for the leads as well as etch for the thermal pad.
3. Place five holes in the area of the thermal pad. Keep these holes 13 mils (0,03302 cm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA1633 device, and can be larger than the 13-mil diameter vias directly under the thermal pad. The vias can be larger because the vias are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane.
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This slow heat transfer makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, make sure the holes under the OPA1633 PowerPAD package connect to the internal plane with a complete connection around the entire circumference of the plated through-hole.
7. The top-side solder mask must leave the package pins and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area. This configuration prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the device pins.

With these preparatory steps in place, the device is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This process results in a part that is properly installed.

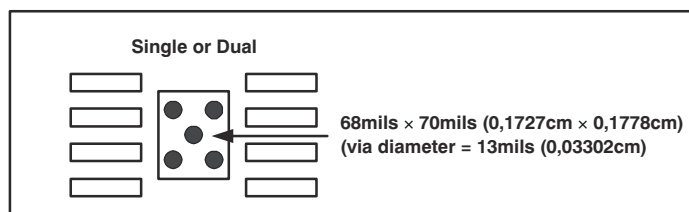


Figure 8-4. PowerPAD Integrated Circuit Package PCB Etch and Via Pattern

8.4.1.1 PowerPAD™ Integrated Circuit Package Design Considerations

The OPA1633 is available in a thermally-enhanced PowerPAD integrated circuit package. This package is constructed using a downset leadframe upon which the die is mounted (see [Figure 8-5\(a\)](#) and [Figure 8-5\(b\)](#)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see [Figure 8-5\(c\)](#)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

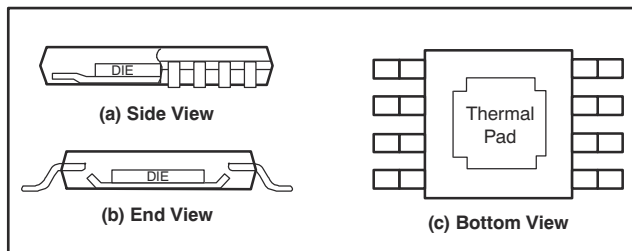


Figure 8-5. Views of the Thermally-Enhanced Package

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the thermal pad to the PCB is always required, even with applications that have low power dissipation. The PowerPAD integrated circuit package provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

8.4.1.2 Power Dissipation and Thermal Considerations

The OPA1633 does not have thermal shutdown protection. Make sure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, make sure that the junction temperature does not exceed 125°C.

The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}} \quad (3)$$

where:

- P_{DMax} is the maximum power dissipation in the amplifier (W)
- T_{Max} is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W)
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the OPA1633 is offered in an HVSSOP-8 with PowerPAD integrated circuit package. The thermal coefficient for the HVSSOP (DGN) package is substantially improved over the traditional SO package.

OPA1633

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8.4.2 Layout Example

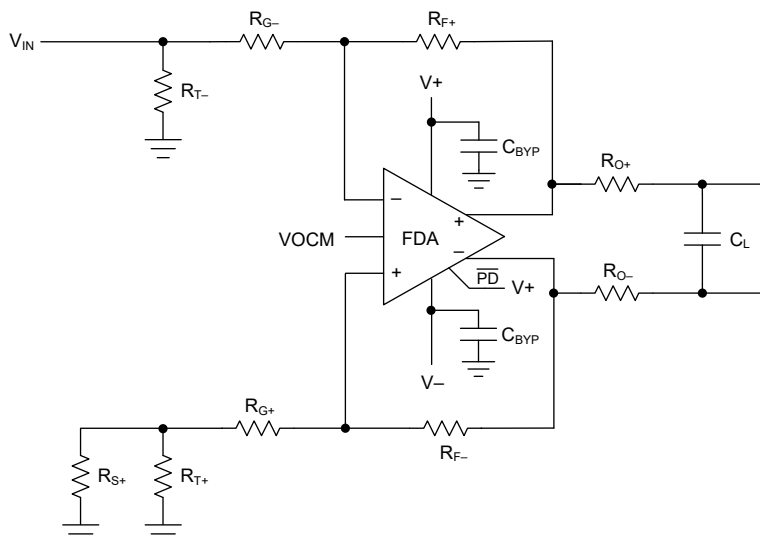


Figure 8-6. Representative Schematic for Example Layout

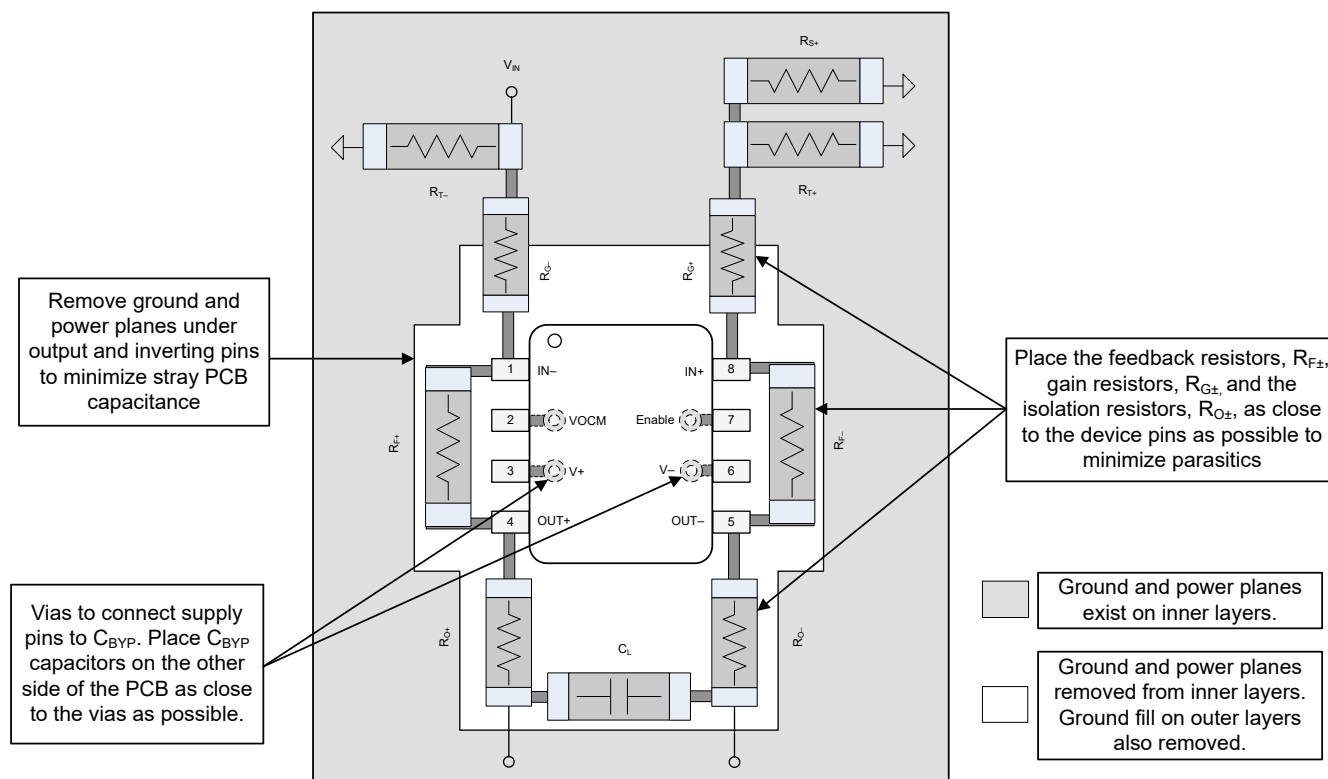


Figure 8-7. Example Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Fully Differential Amplifiers application note](#)
- Texas Instruments, [TI Precision Labs - Fully Differential Amplifiers video series](#)
- Texas Instruments, [Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers application note](#)
- Texas Instruments, [Analog Audio Amplifier Front-End Reference Design With Improved Noise and Distortion](#)
- Texas Instruments, [Public Announcement Audio Reference Design utilizing Best in Class Boost Controller](#)
- Texas Instruments, [Motherboard/controller for the AMC1210 Reference Design](#)
- Texas Instruments, [TPA6120A2 Stereo, 9.0 to 33.0-V, Analog Input Headphone Amplifier With 128-dB Dynamic Range](#)
- Texas Instruments, [OPA2863 Dual, Low-Power, 110-MHz, 12-V, RRIO Voltage Feedback Amplifier](#)
- Texas Instruments, [OPA2834 Ultra-Low Power, 50-MHz Rail-to-Rail Out, Negative Rail In, Voltage-feedback Op Amp](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1633DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2USJ	Samples
OPA1633DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	O1633	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

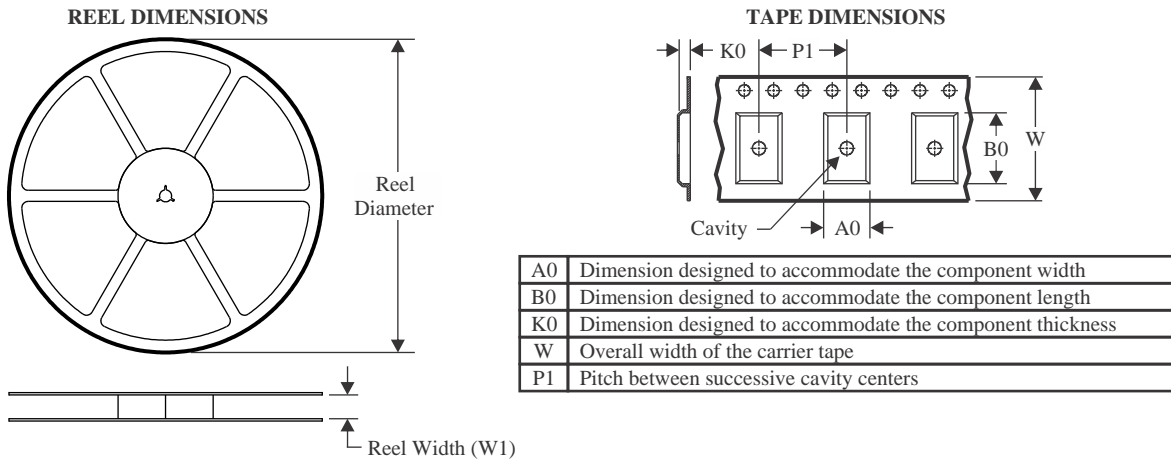
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

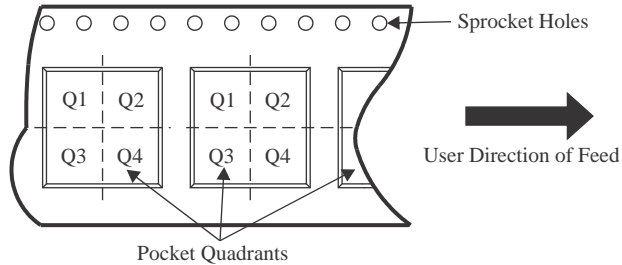
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TAPE AND REEL INFORMATION



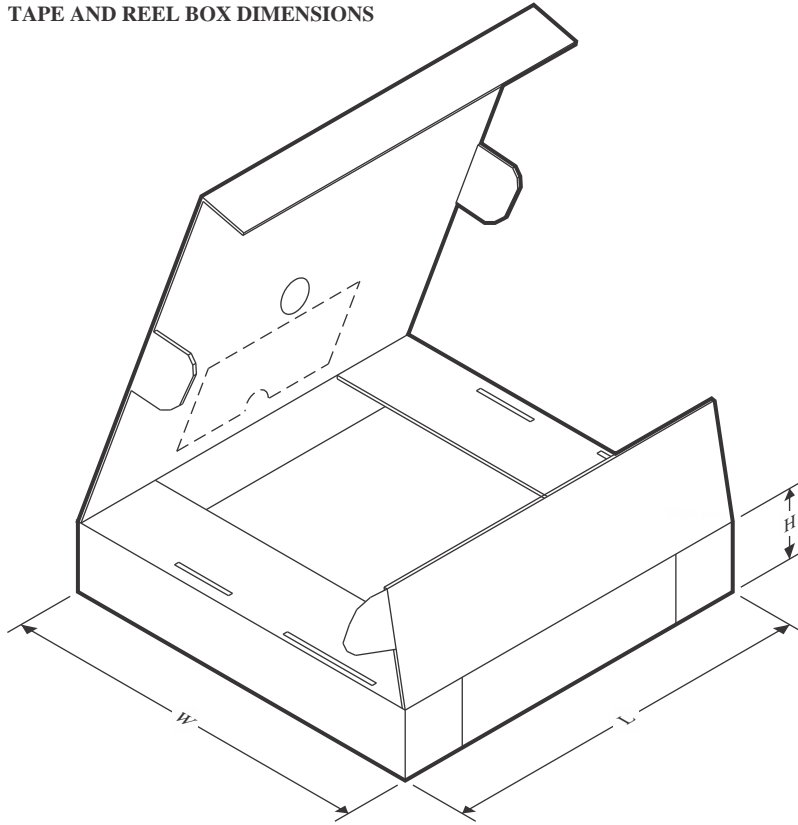
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

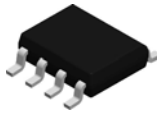
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1633DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1633DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

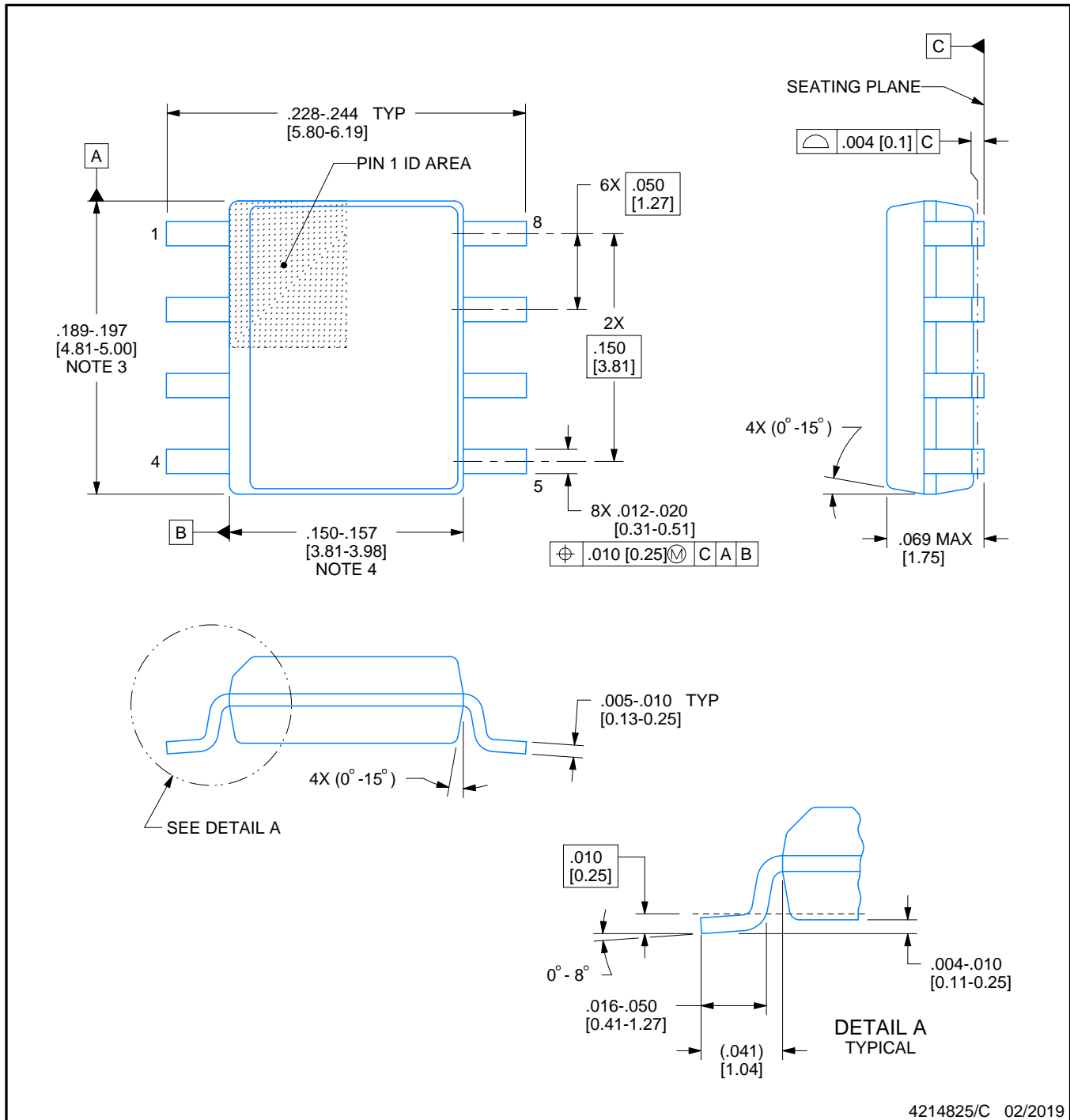


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1633DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
OPA1633DR	SOIC	D	8	2500	356.0	356.0	35.0

**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

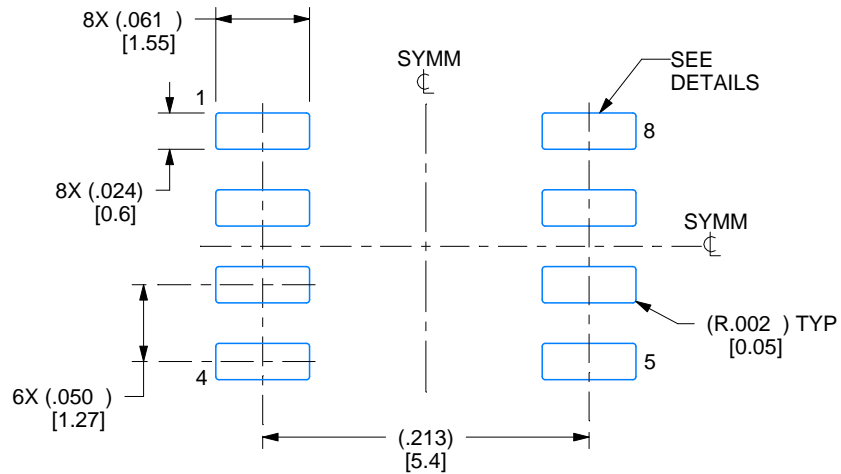
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

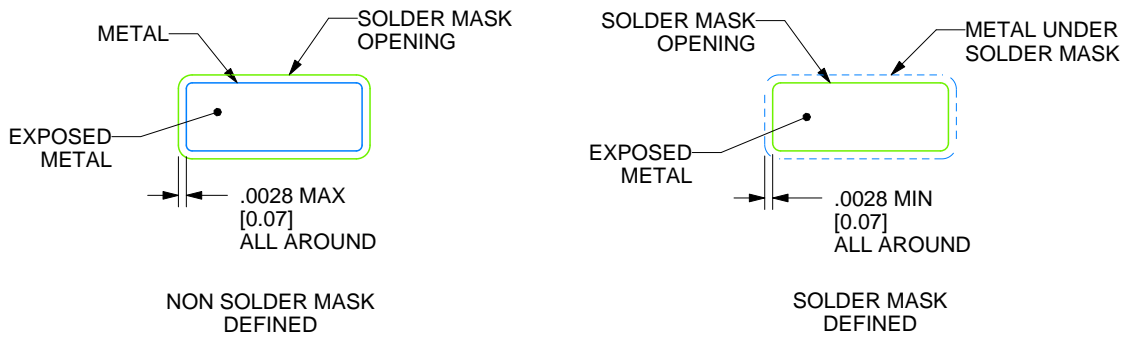
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

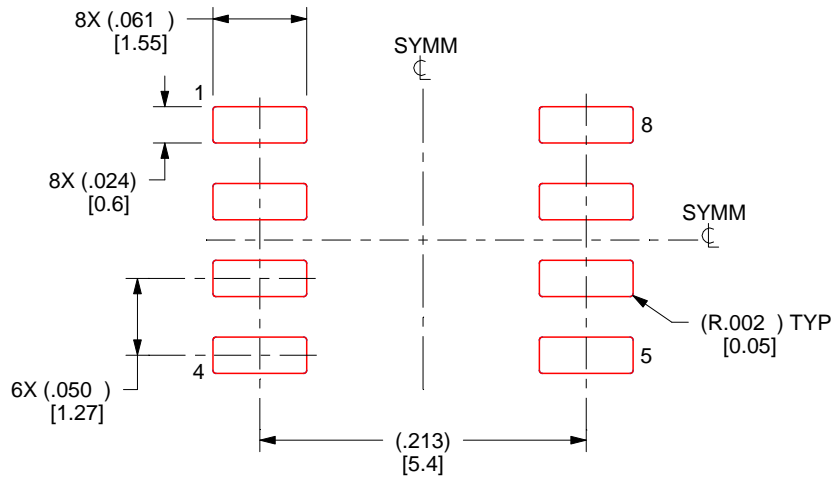
4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN**D0008A****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
 BASED ON .005 INCH [0.125 MM] THICK STENCIL
 SCALE:8X

4214825/C 02/2019

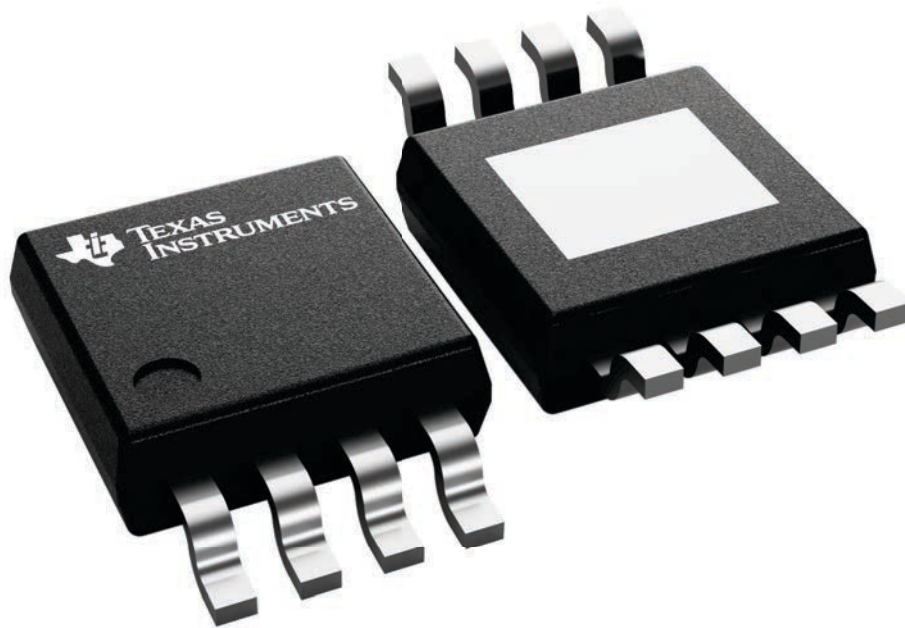
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW**DGN 8****PowerPAD™ HVSSOP - 1.1 mm max height****3 x 3, 0.65 mm pitch**

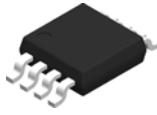
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



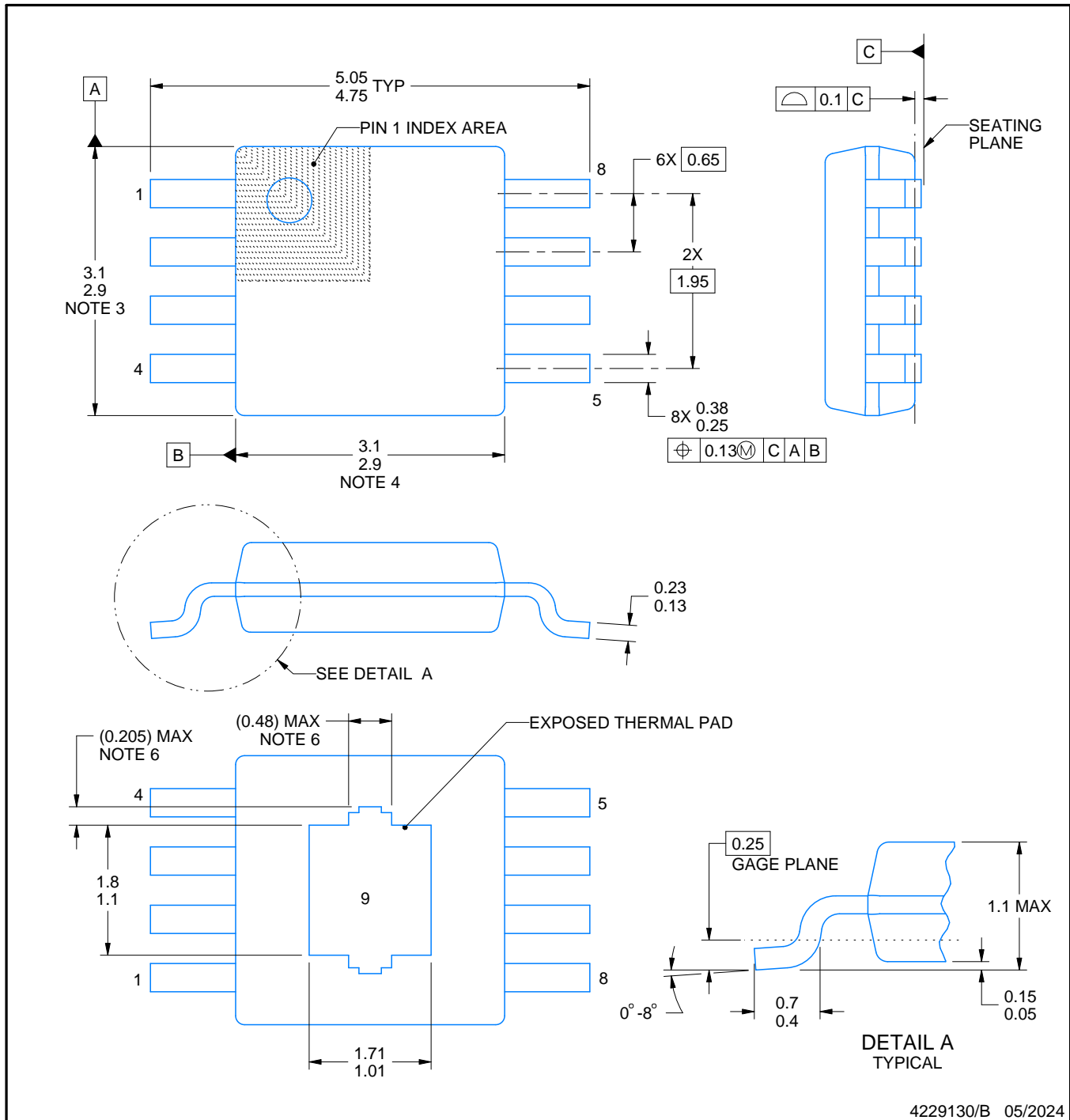
PACKAGE OUTLINE

DGN0008H



PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

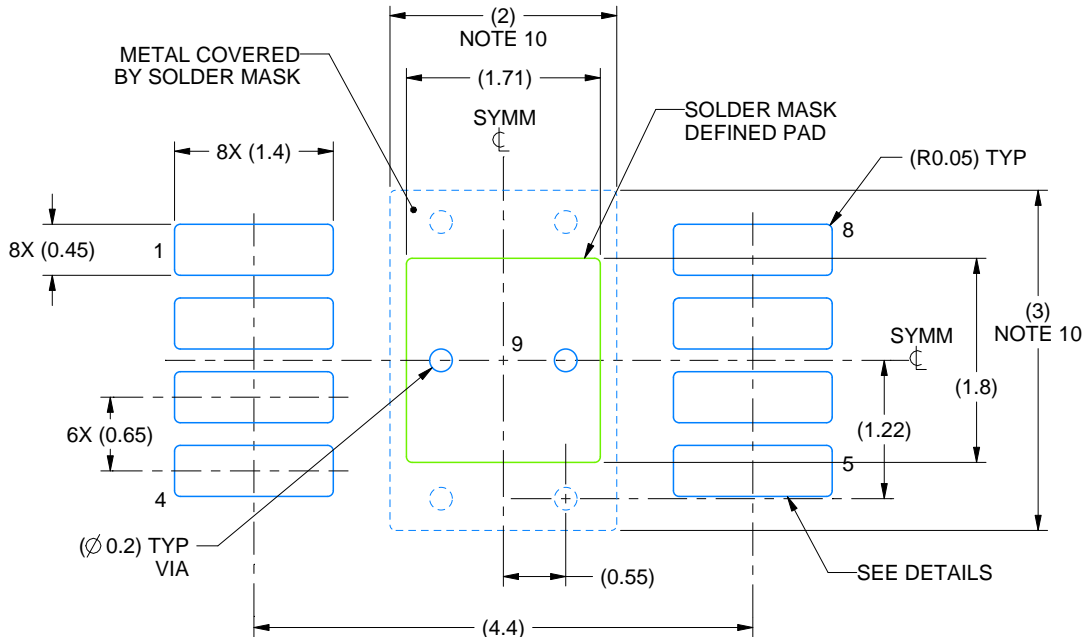
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-187.
- Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

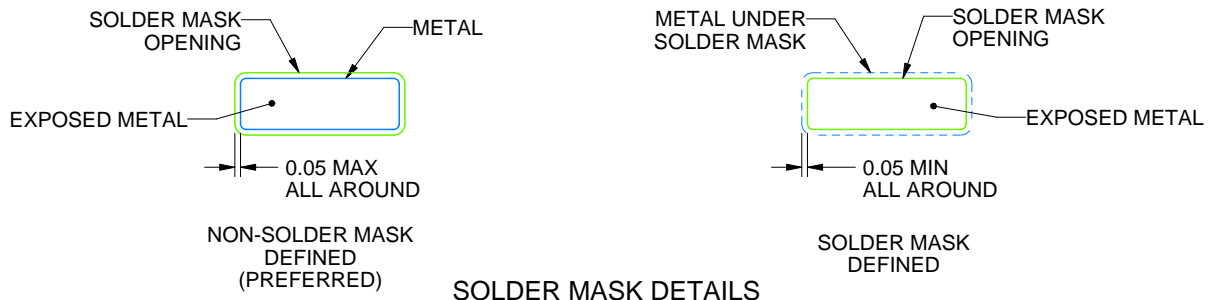
DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

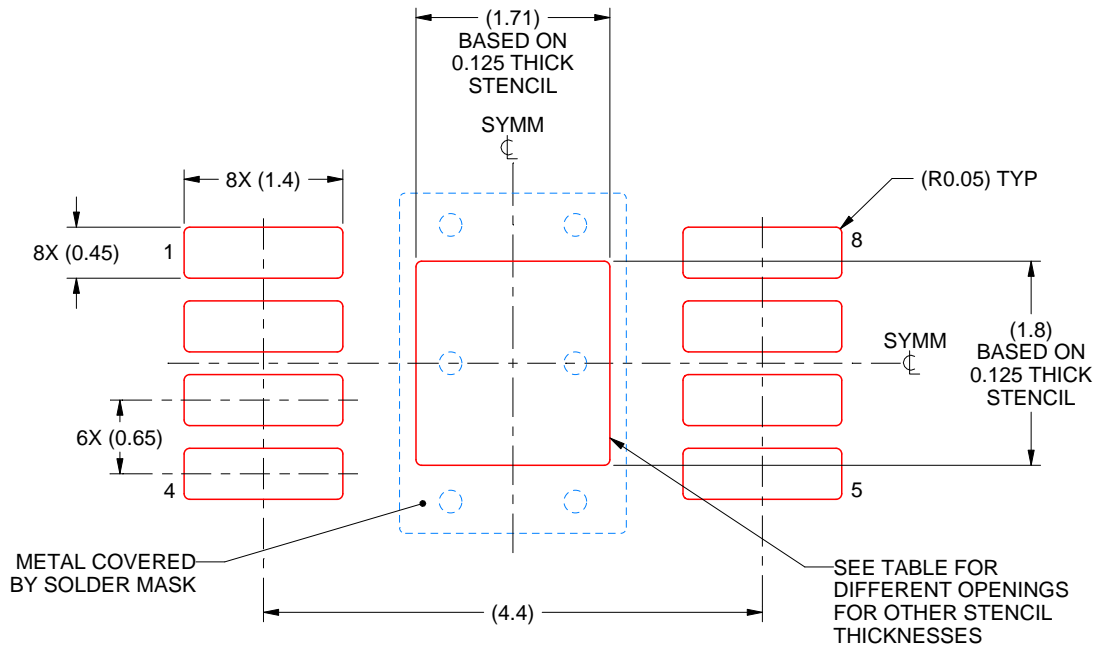
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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