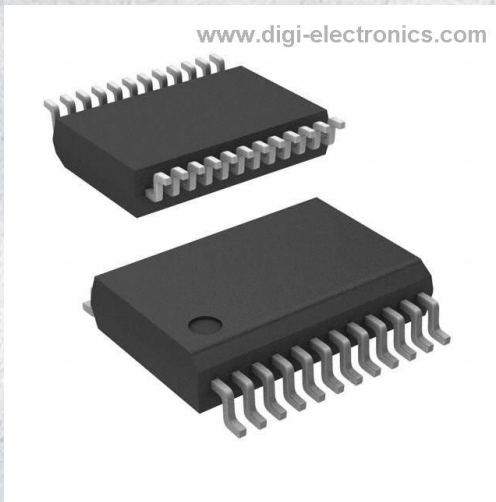


# SN74ABT543ADBRG4 Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	SN74ABT543ADBRG4-DG
Manufacturer	<a href="#">Texas Instruments</a>
Manufacturer Product Number	SN74ABT543ADBRG4
Description	IC TXRX NON-INVERT 5.5V 24SSOP
Detailed Description	Transceiver, Non-Inverting 1 Element 8 Bit per Element 3-State Output 24-SSOP



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RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

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## Purchase and inquiry

Manufacturer Product Number:

SN74ABT543ADBRG4

Series:

74ABT

Logic Type:

Transceiver, Non-Inverting

Number of Bits per Element:

8

Output Type:

3-State

Voltage - Supply:

4.5V ~ 5.5V

Mounting Type:

Surface Mount

Supplier Device Package:

24-SSOP

Manufacturer:

Texas Instruments

Product Status:

Discontinued at Digi-Key

Number of Elements:

1

Input Type:

-

Current - Output High, Low:

32mA, 64mA

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

24-SSOP (0.209", 5.30mm Width)

Base Product Number:

74ABT543

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



# SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

## description

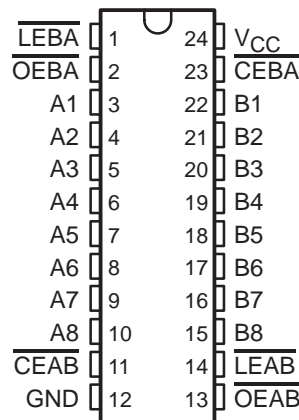
The 'ABT543A octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ( $\overline{\text{LEAB}}$  or  $\overline{\text{LEBA}}$ ) and output-enable ( $\overline{\text{OEAB}}$  or  $\overline{\text{OEBA}}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{\text{CEAB}}$ ) input must be low to enter data from A or to output data from B. If  $\overline{\text{CEAB}}$  is low and  $\overline{\text{LEAB}}$  is low, the A-to-B latches are transparent; a subsequent low-to-high transition of  $\overline{\text{LEAB}}$  puts the A latches in the storage mode. With  $\overline{\text{CEAB}}$  and  $\overline{\text{OEAB}}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$  inputs.

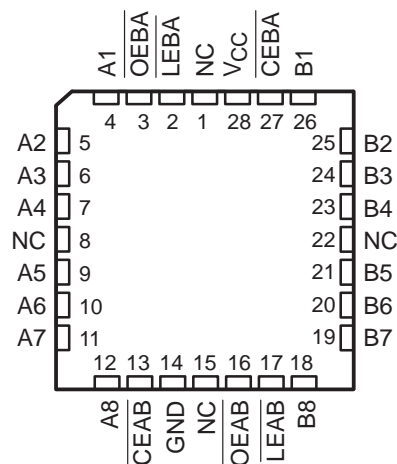
To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT543A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT543A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT543A . . . JT OR W PACKAGE  
SN74ABT543A . . . DB, DW, NT, OR PW PACKAGE  
(TOP VIEW)



SN54ABT543A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN54ABT543A, SN74ABT543A

## OCTAL REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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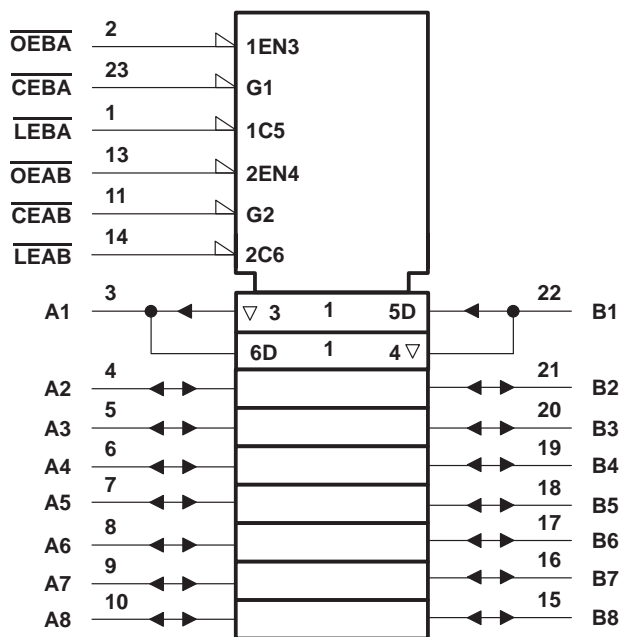
FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^\ddagger$
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$ .

‡ Output level before the indicated steady-state input conditions were established

### logic symbols§

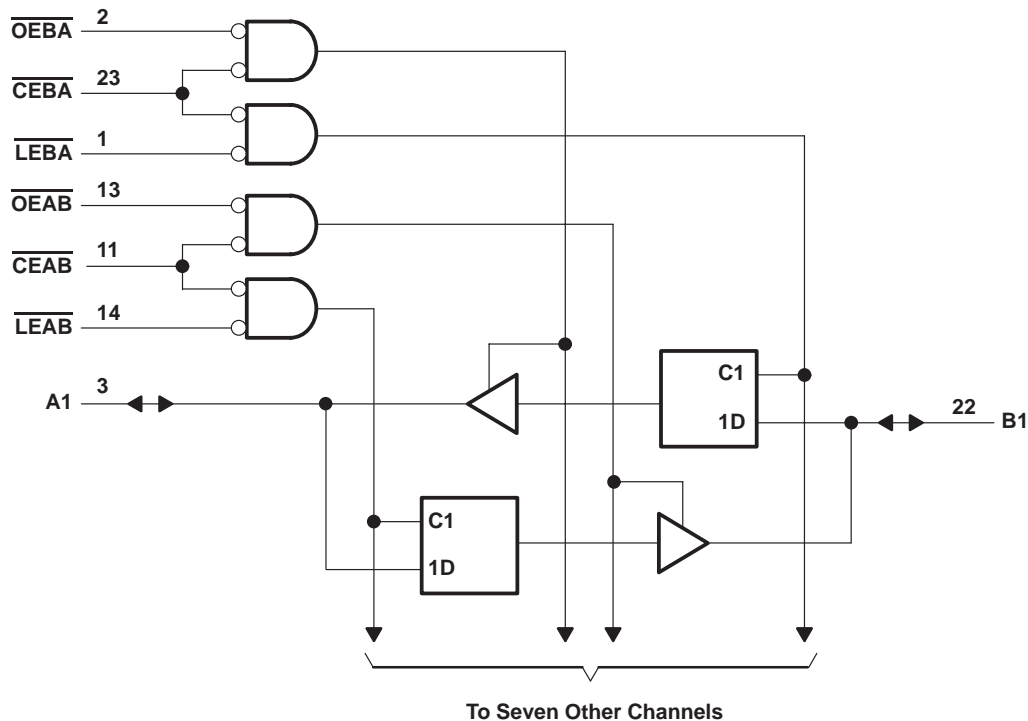


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

# SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT543A .....	96 mA
SN74ABT543A .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	104°C/W
DW package .....	81°C/W
NT package .....	67°C/W
PW package .....	120°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

# SN54ABT543A, SN74ABT543A

## OCTAL REGISTERED TRANSCIEVERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

		SN54ABT543A		SN74ABT543A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT543A		SN74ABT543A		UNIT		
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V		
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$		2.5		2.5		2.5		V		
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$		3		3		3				
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$		2		2					
								2			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$			0.55		0.55		V		
		$I_{OL} = 64\text{ mA}$			0.55*		0.55				
$V_{hys}$			100						mV		
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$		$\pm 1$		$\pm 1$	$\mu\text{A}$	
	A or B ports				$\pm 100$		$\pm 100$		$\pm 100$		
$I_{OZH}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			$10^\S$		$10^\S$		$10^\S$	$\mu\text{A}$		
$I_{OZL}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$			$-10^\S$		$-10^\S$		$-10^\S$	$\mu\text{A}$		
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O \leq 4.5\text{ V}$			$\pm 100$				$\pm 100$	$\mu\text{A}$		
$I_{CEX}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$	Outputs high		50		50		50	$\mu\text{A}$		
$I_{O}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$		-50*	-100	-180*	-50	-200	-50	-180	mA	
$I_{CC}$	A or B ports	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high		1	250*		350		250	$\mu\text{A}$
			Outputs low		24	30*		34		30	mA
			Outputs disabled		0.5	250*		350		250	$\mu\text{A}$
$\Delta I_{CC}^\#$	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND			1.5		1.5		1.5	mA		
$C_i$	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$		4					pF		
$C_{io}$	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$		7					pF		

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

# SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT543A		UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		
			MIN	MAX	
t <sub>w</sub>	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low		3.5	3.5	ns
t <sub>su</sub>	Data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	High	2.5	2.5	ns
		Low	3	3	
	Data before $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	High	2.5	2.5	
		Low	3	3	
t <sub>h</sub>	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$		1	1	ns
	Data after $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$		1	1	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT543A		UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		
			MIN	MAX	
t <sub>w</sub>	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low		3.5	3.5	ns
t <sub>su</sub>	Data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	High	3.5	3.5	ns
		Low	3	3	
	Data before $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	High	3.5	3.5	
		Low	3	3	
t <sub>h</sub>	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$		0.5	0.5	ns
	Data after $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$		0.5	0.5	

# SN54ABT543A, SN74ABT543A

## OCTAL REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT543A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	1.6†	4.4	4.4	1.6†	5.5	ns
$t_{PHL}$			1.6	4.4	5.1	1.6	6.2	
$t_{PLH}$	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.6†	4.1	5.1	1.6†	6.6	ns
$t_{PHL}$			1.6	4.6	5.4	1.6	6.4	
$t_{PZH}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	4.1	1.4	5.1	ns
$t_{PZL}$			2	5	4.9	2	5.8	
$t_{PHZ}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5†	5.9	5.8	2.5†	6.9	ns
$t_{PLZ}$			2.5†	5.5	6.1	2.5†	7.6	
$t_{PZH}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	4.7	1.4	5.6	ns
$t_{PZL}$			2	5	5.7	2	6.2	
$t_{PHZ}$	CEBA or CEAB	A or B	3.2†	5.9	6.5	3.2†	7.3	ns
$t_{PLZ}$			2.5†	5.5	6.7	2.5†	7.8	

† This data sheet limit may vary among suppliers.

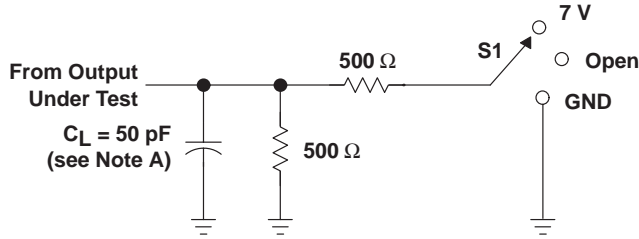
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT543A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	1.8†	4.4	5.9	1.8†	6.9	ns
$t_{PHL}$			1.9	4.4	5.9	1.9	6.9	
$t_{PLH}$	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.5†	4.1	5.6	1.5†	6.6	ns
$t_{PHL}$			2.1	4.6	6.1	2.1	7.1	
$t_{PZH}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
$t_{PZL}$			2.5	5	6.5	2.5	7.5	
$t_{PHZ}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5†	5.9	7.4	2.5†	8.4	ns
$t_{PLZ}$			2.5†	5.5	7	2.5†	8	
$t_{PZH}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
$t_{PZL}$			2.5	5	6.5	2.5	7.5	
$t_{PHZ}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2.9†	5.9	7.4	2.9†	8.4	ns
$t_{PLZ}$			2.4†	5.5	7	2.4†	8	

† This data sheet limit may vary among suppliers.

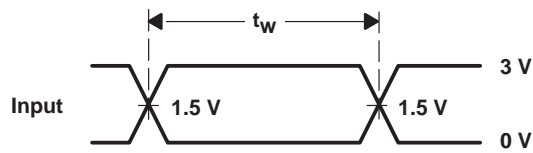


**PARAMETER MEASUREMENT INFORMATION**

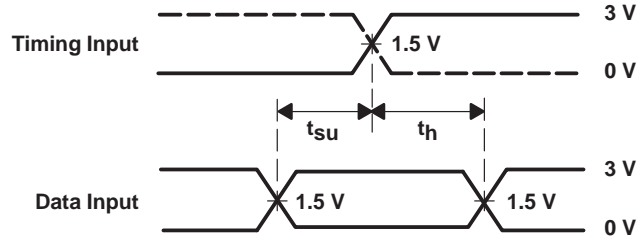


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

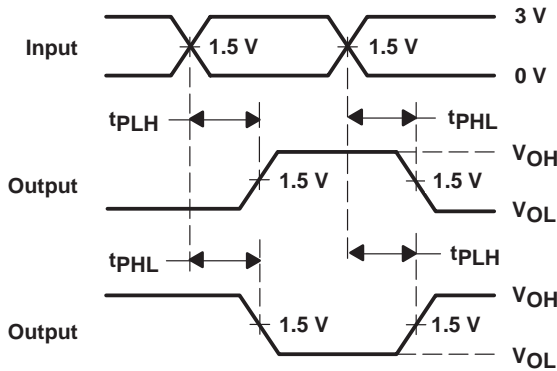
**LOAD CIRCUIT**



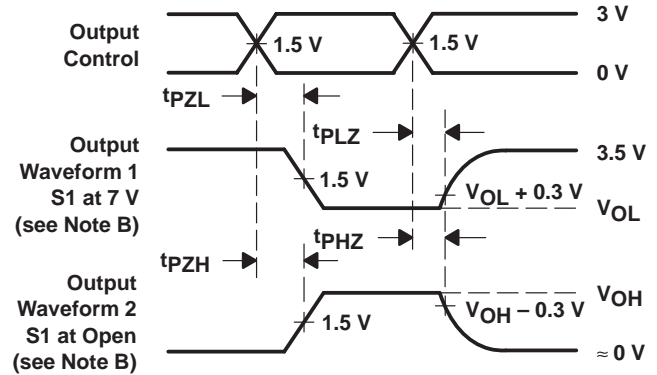
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9231402Q3A	ACTIVE	LCCC	FK	28	42	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9231402Q3A SNJ54 ABT543AFK	<a href="#">Samples</a>
SN74ABT543ADBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A	<a href="#">Samples</a>
SN74ABT543ADBRG4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A	<a href="#">Samples</a>
SN74ABT543ADW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT543A	<a href="#">Samples</a>
SN74ABT543ADWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT543A	<a href="#">Samples</a>
SN74ABT543APW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A	<a href="#">Samples</a>
SN74ABT543APWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A	<a href="#">Samples</a>
SNJ54ABT543AFK	ACTIVE	LCCC	FK	28	42	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9231402Q3A SNJ54 ABT543AFK	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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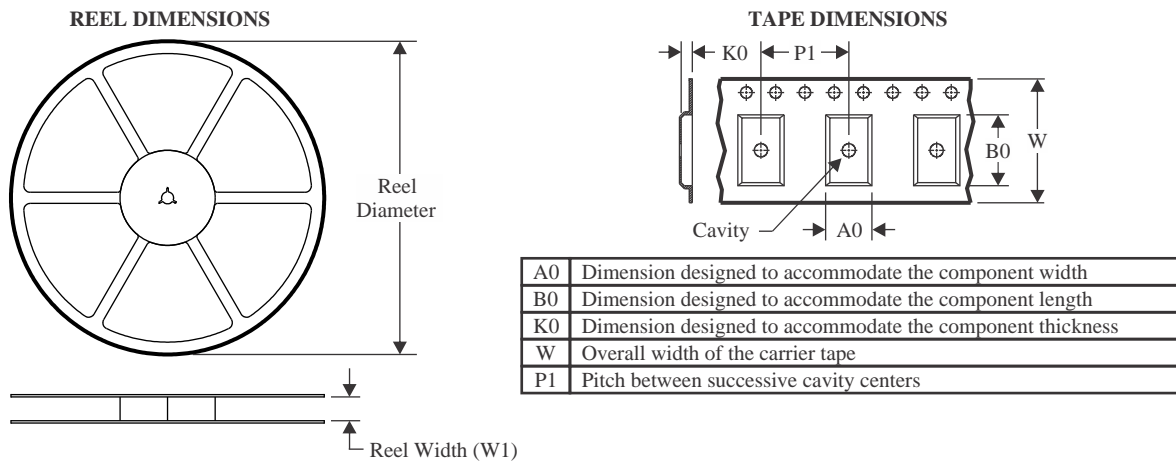
**OTHER QUALIFIED VERSIONS OF SN54ABT543A, SN74ABT543A :**

- Catalog : [SN74ABT543A](#)
- Military : [SN54ABT543A](#)

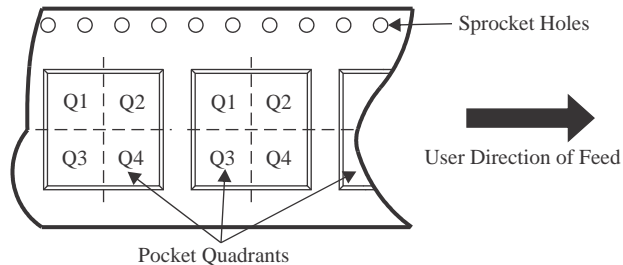
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



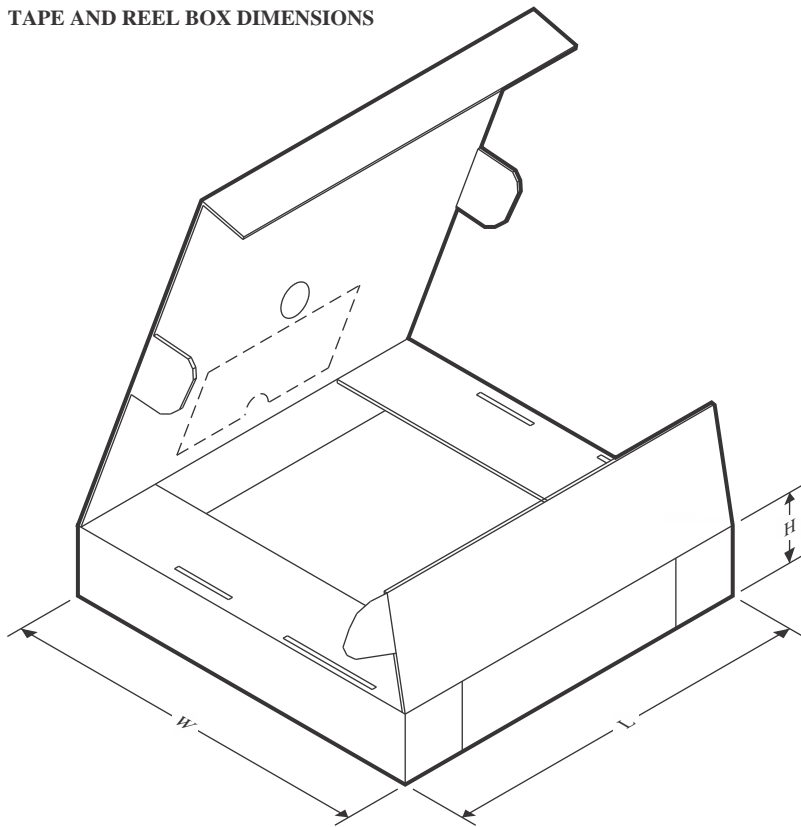
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT543ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT543ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT543APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

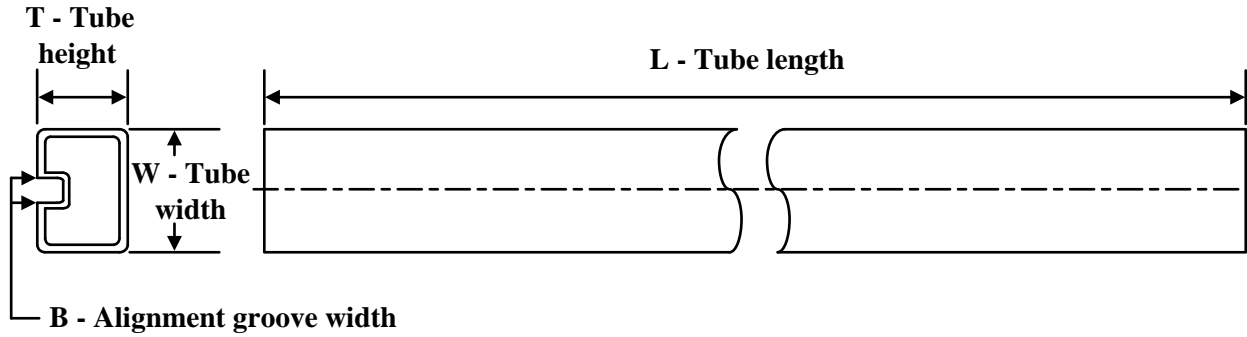


**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT543ADBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74ABT543ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74ABT543APWR	TSSOP	PW	24	2000	356.0	356.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT543ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT543APW	PW	TSSOP	24	60	530	10.2	3600	3.5

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

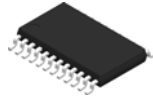


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. Falls within JEDEC MS-004

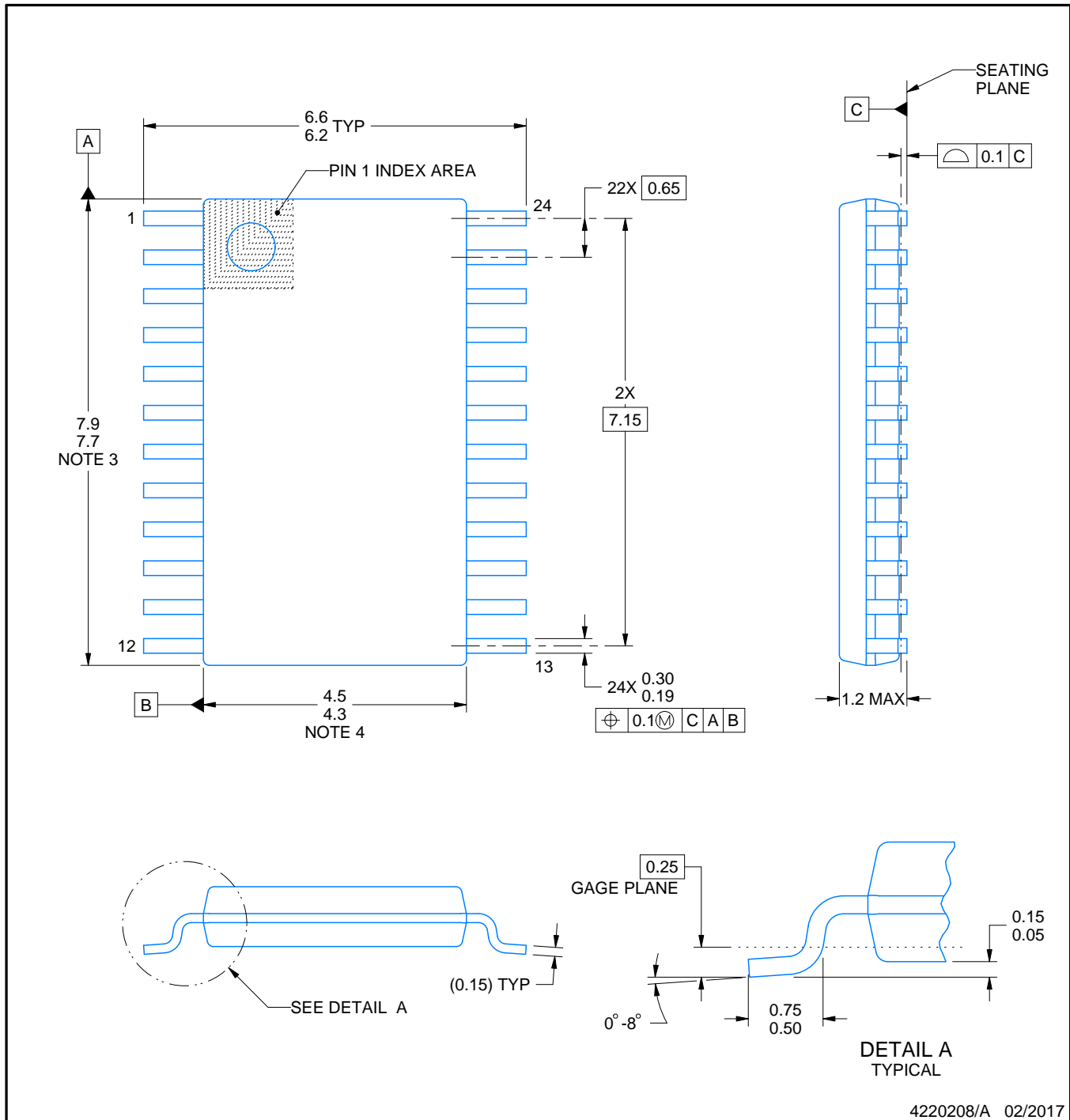


## PACKAGE OUTLINE

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

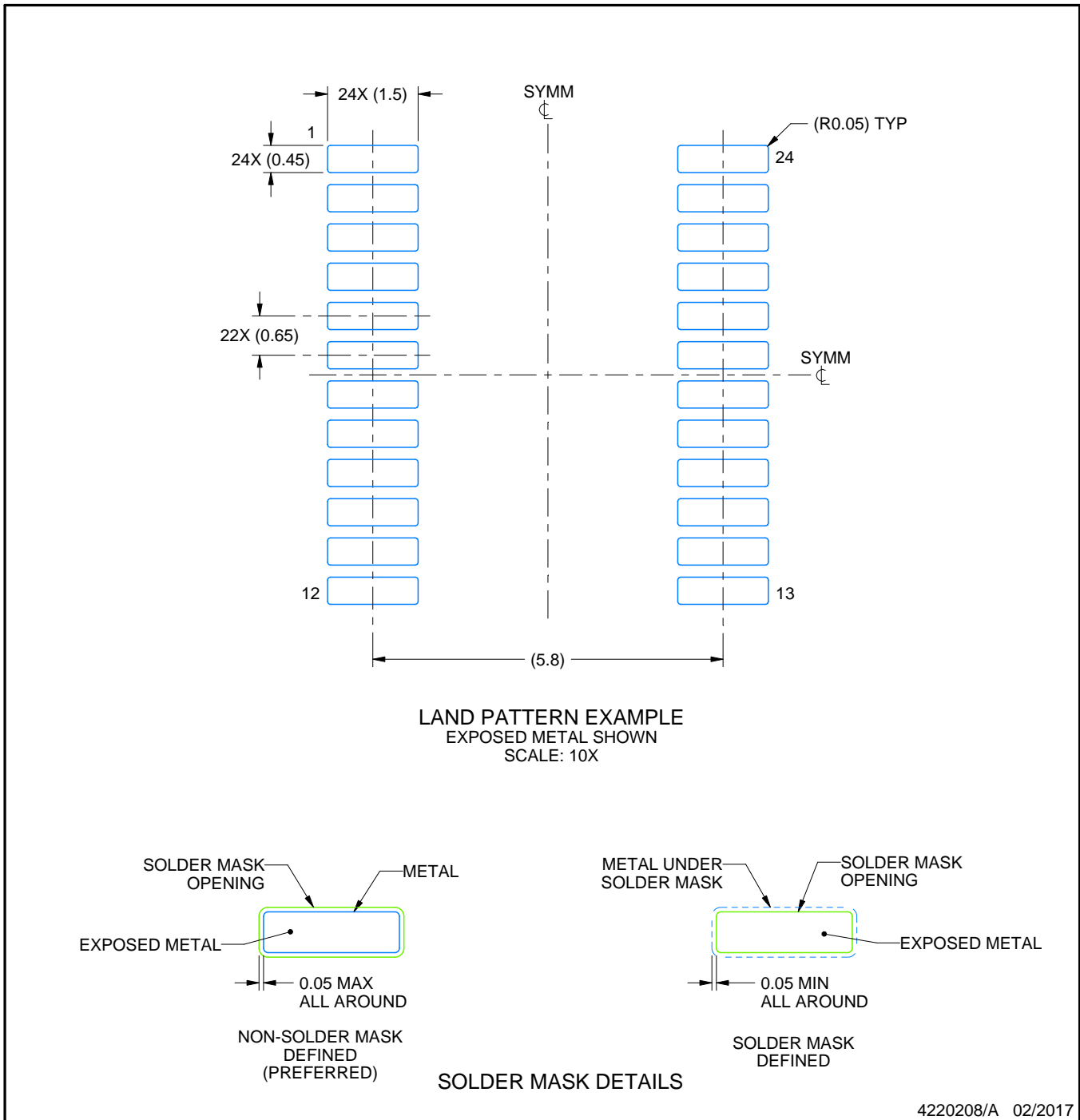


# EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

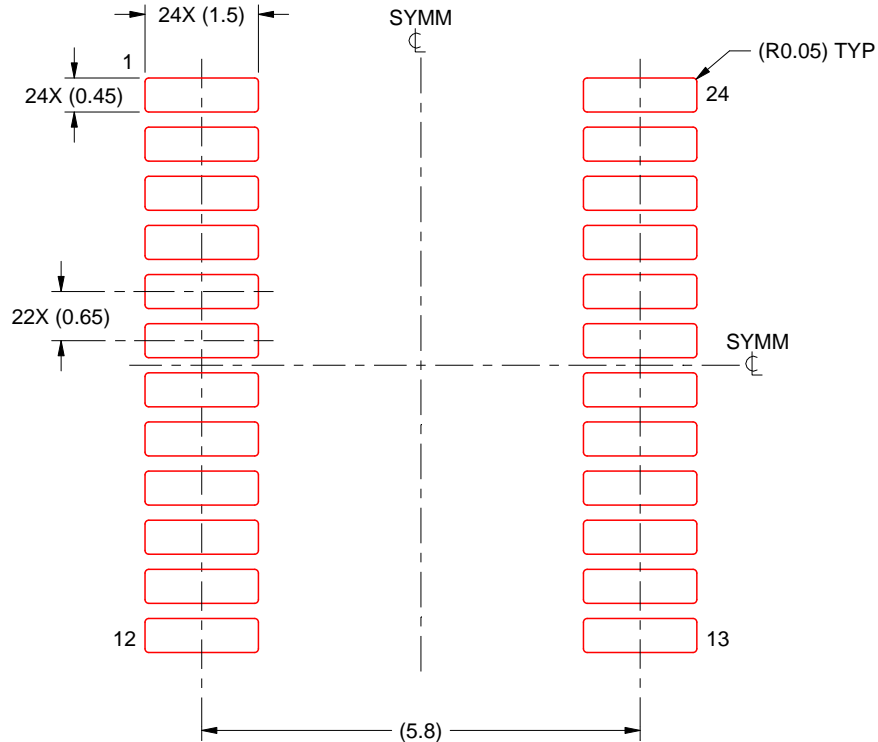


NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****PW0024A****TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 10X

4220208/A 02/2017

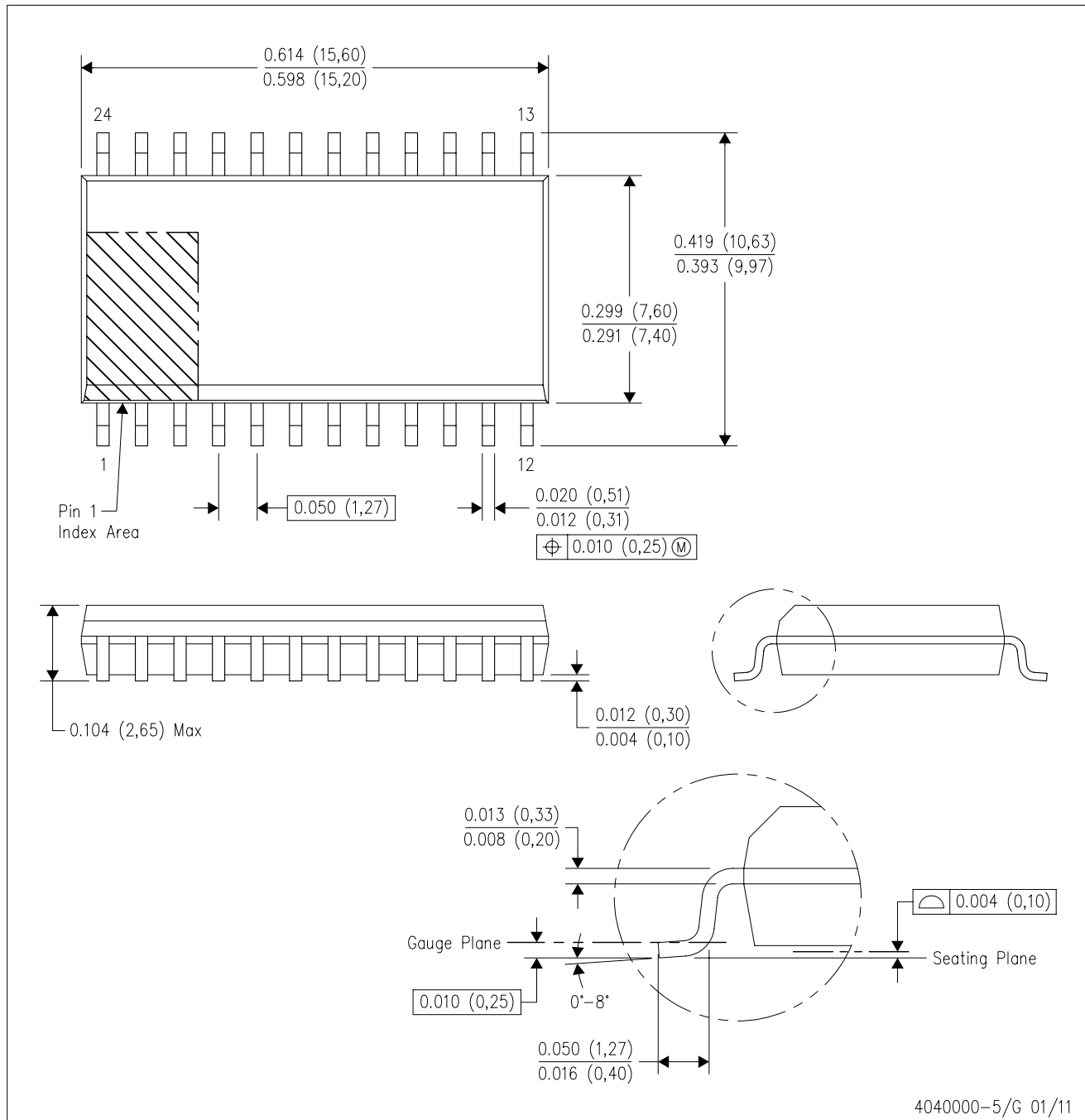
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

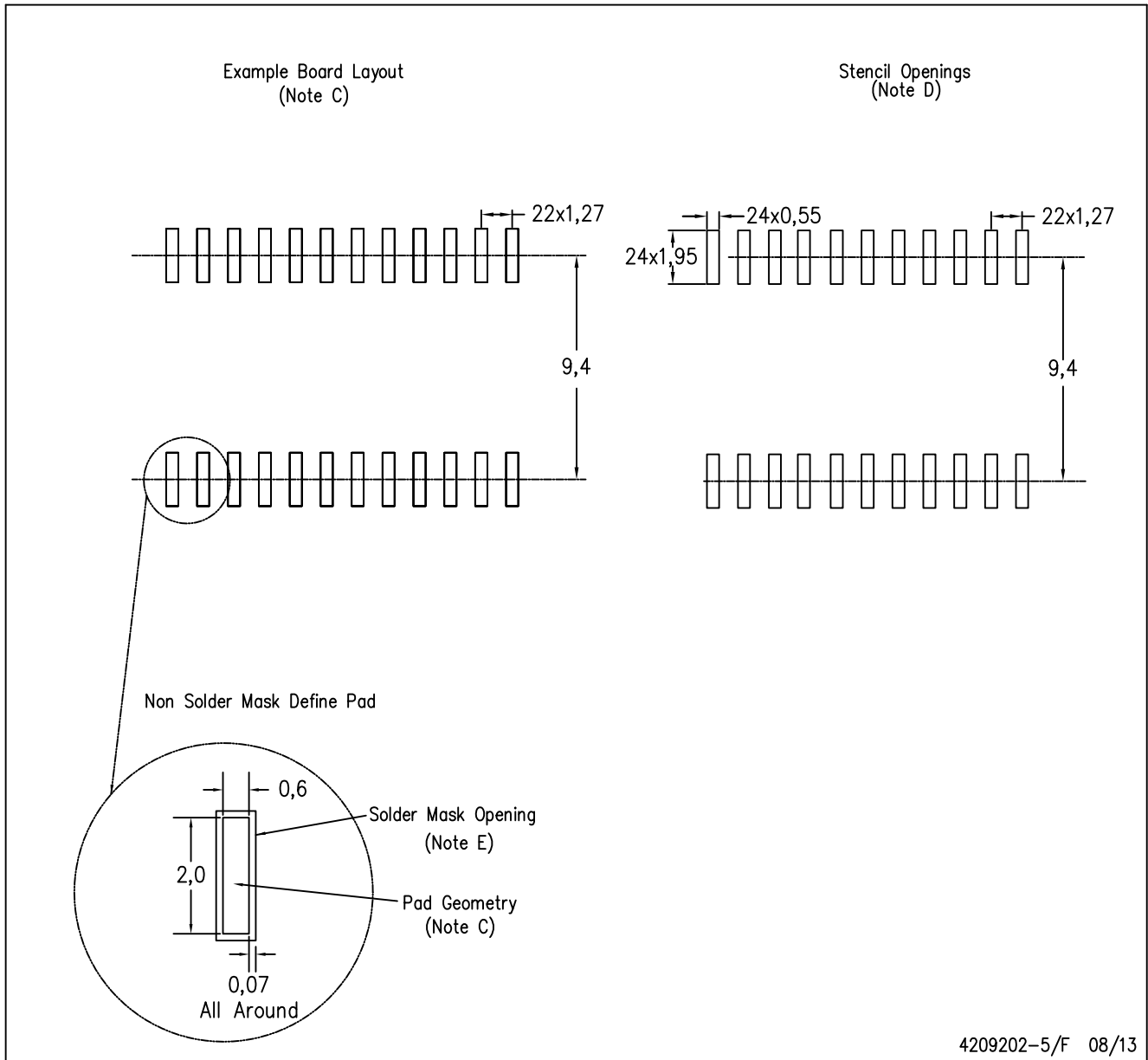


- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

## LAND PATTERN DATA

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



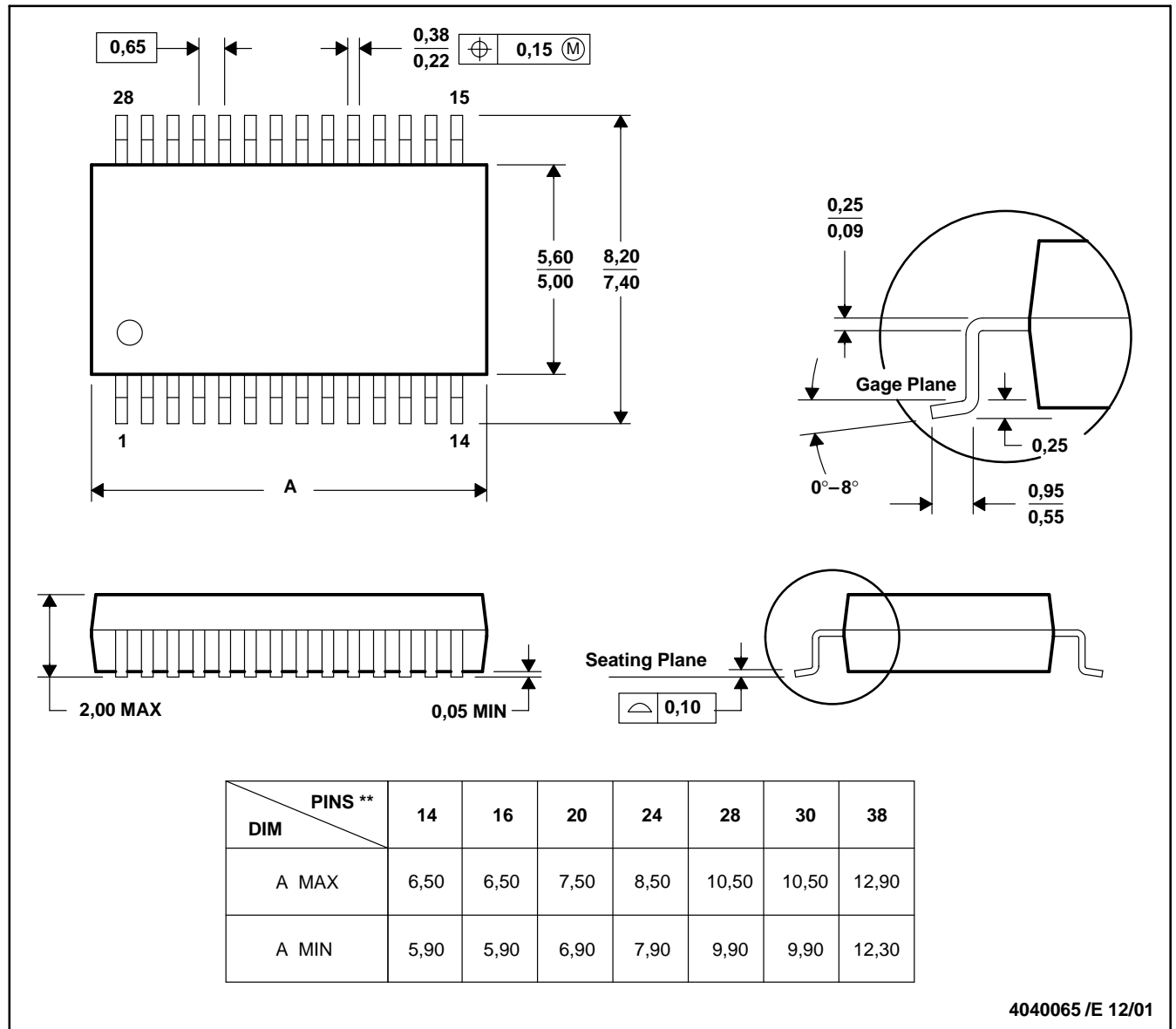
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Refer to IPC7351 for alternate board design.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



**DB (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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