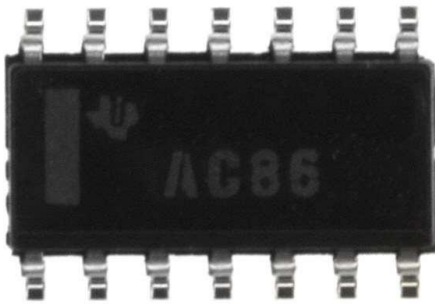


# SN74AHC32DBR Datasheet

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DiGi Electronics Part Number	SN74AHC32DBR-DG
Manufacturer	<a href="#">Texas Instruments</a>
Manufacturer Product Number	SN74AHC32DBR
Description	IC GATE OR 4CH 2-INP 14SSOP
Detailed Description	OR Gate IC 4 Channel 14-SSOP



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

SN74AHC32DBR

Series:

74AHC

Logic Type:

OR Gate

Number of Inputs:

2

Voltage - Supply:

2V ~ 5.5V

Current - Output High, Low:

8mA, 8mA

Input Logic Level - High:

1.5V ~ 3.85V

Operating Temperature:

-40°C ~ 125°C

Supplier Device Package:

14-SSOP

Base Product Number:

74AHC32

Manufacturer:

Texas Instruments

Product Status:

Active

Number of Circuits:

4

Features:

-

Current - Quiescent (Max):

2  $\mu$ A

Input Logic Level - Low:

0.5V ~ 1.65V

Max Propagation Delay @ V, Max CL:

7.5ns @ 5V, 50pF

Mounting Type:

Surface Mount

Package / Case:

14-SSOP (0.209", 5.30mm Width)

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

## SNx4AHC32 Quadruple 2-Input Positive-OR Gates

### 1 Features

- Operating range 2V to 5.5V  $V_{CC}$
- Low power consumption, 10 $\mu$ A maximum  $I_{CC}$
- $\pm 8$ mA output drive at 5V
- Latch-up performance exceeds 250mA per JESD 17

### 2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)
- [Translation between communication modules and system controllers](#)

### 3 Description

The SNx4AHC32 devices are quadruple 2-input positive-OR gates. These devices perform the Boolean function  $Y = \overline{A} \times \overline{B}$  or  $Y = A + B$  in positive logic.

#### Device Information

PART NUMBER	RATING	PACKAGE <sup>(1)</sup>
SN54AHC32	Military	FK (LCCC, 20)
		J (CDIP, 14)
		W (CFP, 14)
SN74AHC32	Commercial	DB (SSOP, 14)
		DGV (TVSOP, 14)
		D (SOIC, 14)
		N (PDIP, 14)
		NS (SO, 14)
		PW (TSSOP, 14)
		RGY (VQFN, 14)
BQA (WQFN, 14)		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)



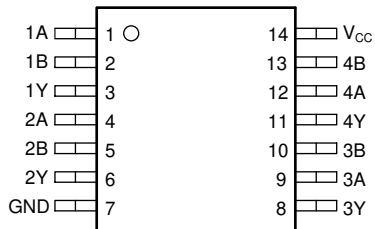
**SN74AHC32, SN54AHC32**

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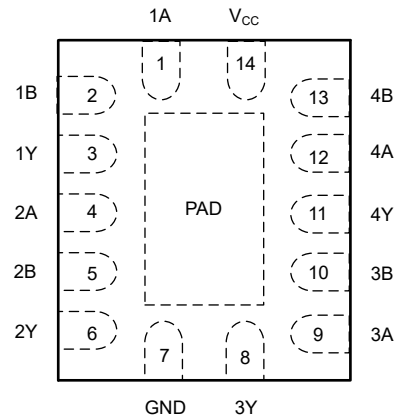
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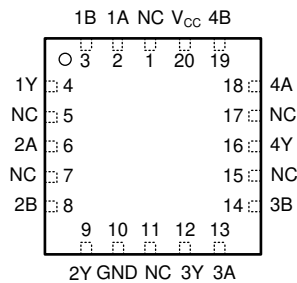
## 4 Pin Configuration and Functions



**Figure 4-1. SN54AHC32 J or W  
SN74AHC32 D, DB, DGV, N, NS or PW Package,  
14-Pin (Top View)**



**Figure 4-2. SN74AHC32 RGY or BQA Package, 14-  
Pin (Top View)**



**Figure 4-3. SN54AHC32 FK Package, 20-Pin (Top View)**

**Table 4-1. Pin Functions**

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	SN74AHC32 D, DB, DGV, N, NS, PW, RGY, BQA	SN54AHC32 J, W      FK		
1A	1	1      2	I	1A Input
1B	2	23    3	I	1B Input
1Y	3	3      4	O	1Y Output
2A	4	4      6	I	2A Input
2B	5	5      8	I	2B Input
2Y	6	6      9	O	2Y Output
3A	9	9      13	I	3A Input
3B	10	10    14	I	3B Input
3Y	8	8      12	O	3Y Output
4A	12	12    18	I	4A Input
4B	13	13    19	I	4B Input
4Y	11	11    16	O	4Y Output
GND	7	7      10	—	Ground Pin
NC	—	—      1, 5, 7, 11, 15, 17	—	No Connection

**SN74AHC32, SN54AHC32**

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**Table 4-1. Pin Functions (continued)**

NAME	PIN			TYPE <sup>(1)</sup>	DESCRIPTION
	SN74AHC32 D, DB, DGV, N, NS, PW, RGY, BQA	SN54AHC32 J, W      FK			
V <sub>CC</sub>	14	14	20	—	Power Pin
Thermal Pad <sup>(2)</sup>	–	–	–	–	Thermal Pad

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

(2) RGY and BQA Package Only

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage range, $V_{CC}$	-0.5	7	V
Input voltage range, $V_I$ <sup>(2)</sup>	-0.5	7	V
Output voltage range, $V_O$ <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		-20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )		$\pm 20$	mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )		$\pm 25$	mA
Continuous current through $V_{CC}$ or GND		$\pm 50$	mA
Storage temperature range, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	$\pm 1000$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

		SN54AHC32		SN74AHC32		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V
		$V_{CC} = 3\text{ V}$	2.1	2.1		
		$V_{CC} = 5.5\text{ V}$	3.85	3.85		
$V_{IL}$	Low-level Input voltage	$V_{CC} = 2\text{ V}$		0.5	0.5	V
		$V_{CC} = 3\text{ V}$		0.9	0.9	
		$V_{CC} = 5.5\text{ V}$		1.65	1.65	
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	-4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	20	
$T_A$	Operating free-air temperature	-55	125	-40	125	°C

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**5.4 Thermal Information**

THERMAL METRIC <sup>(1)</sup>		SNx4AHC32								UNIT
		D <sup>(2)</sup>	DB <sup>(2)</sup>	DGV <sup>(2)</sup>	N <sup>(2)</sup>	NS <sup>(2)</sup>	PW <sup>(2)</sup>	RGY <sup>(3)</sup>	BQA	
		14	14	14	14	14	14	14	14	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	124.6	96	127	80	76	147.7	47	88.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.
- (3) The package thermal impedance is calculated in accordance with JESD 51-5

**5.5 Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
					SN54AHC32		SN74AHC32		Recommended		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2	1.9		1.9		1.9		V
		3 V	2.9	3	2.9		2.9		2.9		
		4.5 V	4.4	4.5	4.4		4.4		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58		2.48		2.48		2.48		
		4.5 V	3.94		3.8		3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V	0.1		0.1		0.1		0.1		V
		3 V	0.1		0.1		0.1		0.1		
		4.5 V	0.1		0.1		0.1		0.1		
	I <sub>OH</sub> = 4 mA	3 V	0.36		0.5		0.44		0.5		
		4.5 V	0.36		0.5		0.44		0.5		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V	±0.1		±1 <sup>(1)</sup>		±1		±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	2		20		20		20		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	2 10				10				pF

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

**5.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V**over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
						SN54AHC32		SN74AHC32		Recommended		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5.5 <sup>(1)</sup>	7.9 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	1	9.5	ns
t <sub>PHL</sub>				5.5 <sup>(1)</sup>	7.9 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	1	9.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	8	11.4	1	13	1	13	1	13	ns
t <sub>PHL</sub>				8	11.4	1	13	1	13	1	13	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.



## 5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
				TYP	MAX	SN54AHC32		SN74AHC32		Recommended		
						MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	3.8 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	ns
$t_{PHL}$				3.8 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	1	8.5	1	8.5	ns
$t_{PHL}$				5.3	7.5	1	8.5	1	8.5	1	8.5	

## 5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER		SN74AHC32			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$	-0.3		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

## 5.9 Operating Characteristics

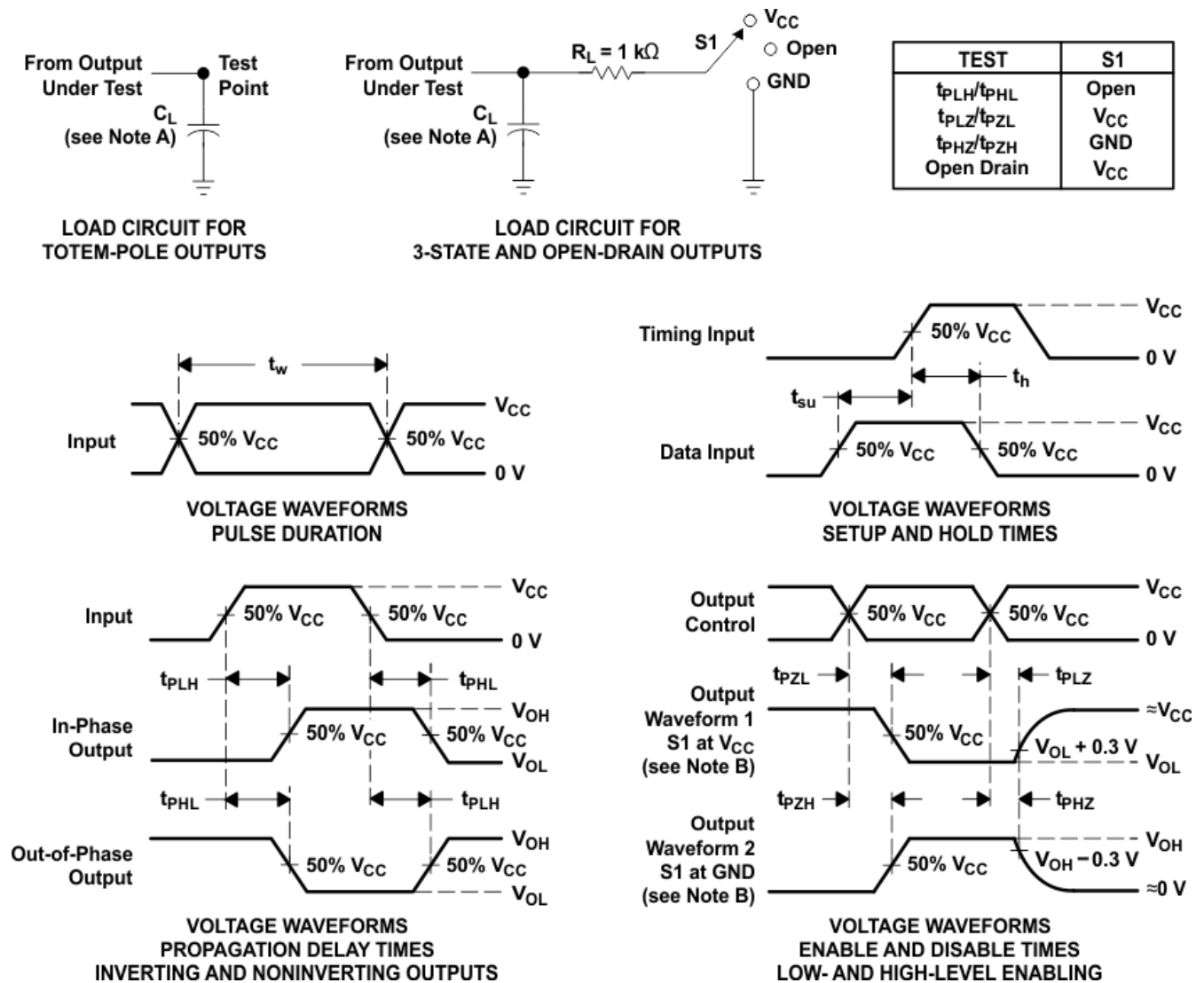
$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	No load, $f = 1\text{ MHz}$	14	pF

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## 6 Parameter Measurement Information



- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

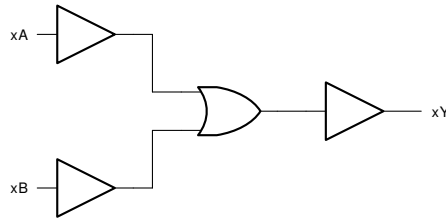
Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SNx4AHC32 contains four independent 2-input OR Gates. Each gate performs the Boolean function  $Y = A + B$  in positive logic.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

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### 7.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k $\Omega$  resistor, however, is recommended and will typically meet all requirements.

### 7.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 7.3.3 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in [Figure 7-1](#).

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

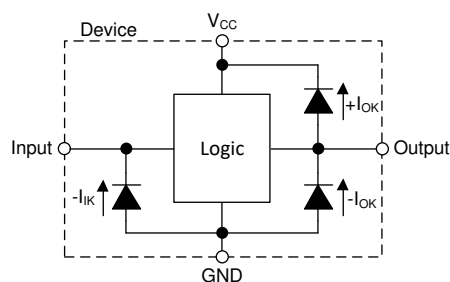


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

## 7.4 Device Functional Modes

[Table 7-1](#) lists the functional modes of the SNx4AHC32.

Table 7-1. Function Table

INPUTS <sup>(1)</sup>		OUTPUT
A	B	Y
H	H	H
L	H	H

**Table 7-1. Function Table (continued)**

INPUTS <sup>(1)</sup>		OUTPUT Y
A	B	
H	L	H
L	L	L

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

In this application, three 2-input OR gates are combined to produce a 4-input OR gate function as shown in [Figure 8-1](#). The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SNx4AHC32 is used to directly control the Enable pin of a fan driver. The fan driver requires only one input signal to be HIGH before being enabled, and should be disabled in the event that all signals go LOW. The 4-input OR gate function combines the four individual overhear signals into a single active-high enable signal.

Temperature sensors can often be spread throughout a system rather than being in a centralized location. This would mean longer length traces or wires to pass signals through leading to slower edge transitions. This makes the SNx4AHC32 useful for combining the incoming signals.

### 8.2 Typical Application

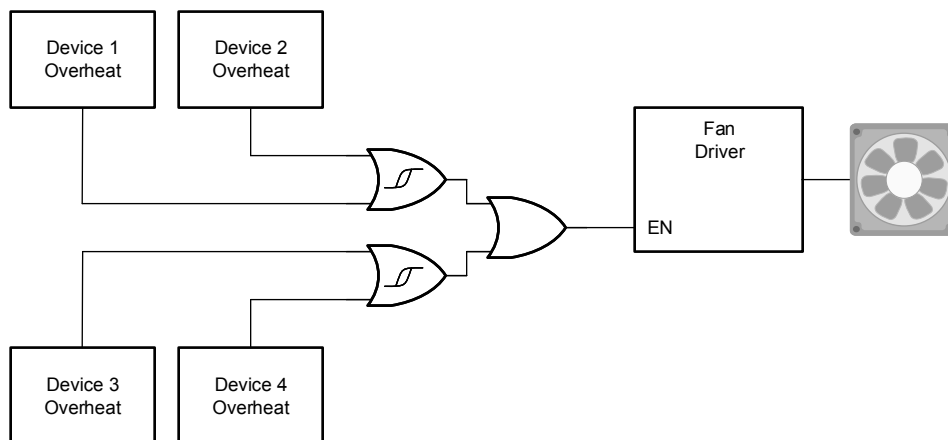


Figure 8-1. Typical Application Block Diagram

#### 8.2.1 Design Requirements

##### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4AHC32 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SNx4AHC32 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SNx4AHC32 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#) application note.

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note.

#### **CAUTION**

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4AHC32 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

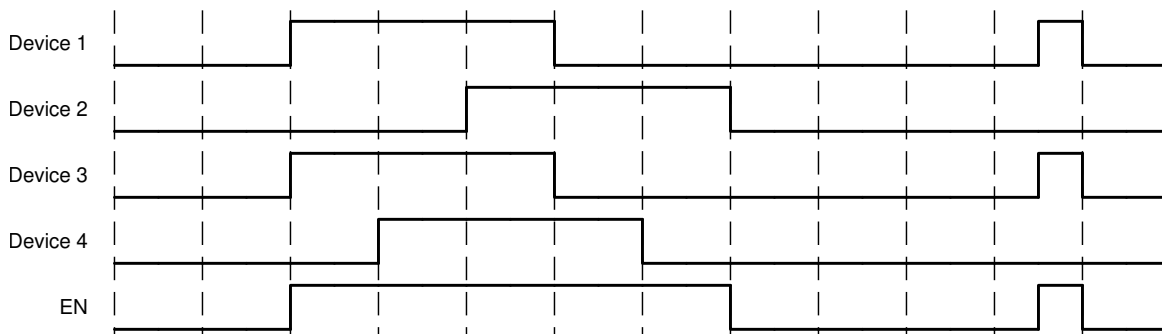
## 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$ pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4AHC32 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.

**SN74AHC32, SN54AHC32**

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4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

**8.2.3 Application Curves****Figure 8-2. Application Timing Diagram****8.3 Power Supply Recommendations**

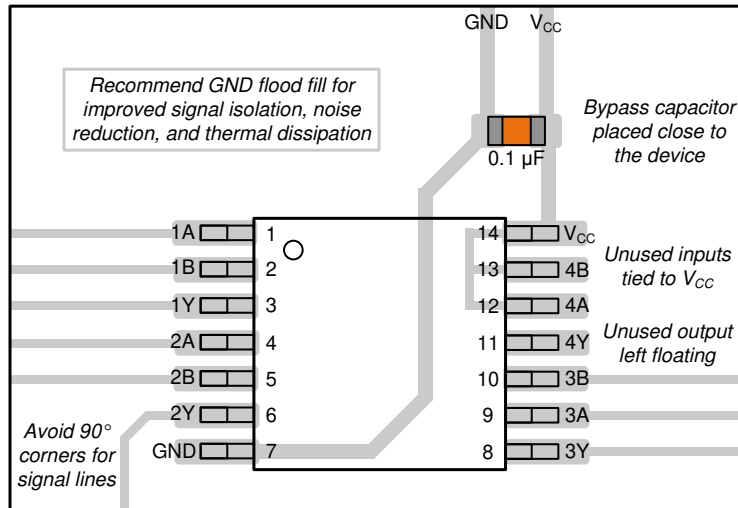
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

**8.4 Layout****8.4.1 Layout Guidelines**

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.



## 8.4.2 Layout Example



**Figure 8-3. Example Layout for the SNx4AHC32**

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

### [TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

**SN74AHC32, SN54AHC32**

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## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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### Changes from Revision K (October 2023) to Revision L (February 2024) Page

- Updated R $\theta$ JA value: D = 86 to 124.6, all values in °C/W ..... 6
- 

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### Changes from Revision J (May 2023) to Revision K (October 2023) Page

- Updated R $\theta$ JA values: PW = 113 to 147.7, all values in °C/W .....6
- 

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9682501Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682501Q2A SNJ54AHC32FK	<a href="#">Samples</a>
5962-9682501QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682501QCA SNJ54AHC32J	<a href="#">Samples</a>
5962-9682501QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682501QDA SNJ54AHC32W	<a href="#">Samples</a>
SN74AHC32BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32	<a href="#">Samples</a>
SN74AHC32D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	AHC32	
SN74AHC32DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA32	<a href="#">Samples</a>
SN74AHC32DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA32	<a href="#">Samples</a>
SN74AHC32DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32	<a href="#">Samples</a>
SN74AHC32N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC32N	<a href="#">Samples</a>
SN74AHC32NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32	<a href="#">Samples</a>
SN74AHC32PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	HA32	
SN74AHC32PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HA32	<a href="#">Samples</a>
SN74AHC32RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA32	<a href="#">Samples</a>
SNJ54AHC32FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682501Q2A SNJ54AHC32FK	<a href="#">Samples</a>
SNJ54AHC32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682501QCA SNJ54AHC32J	<a href="#">Samples</a>
SNJ54AHC32W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682501QDA SNJ54AHC32W	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54AHC32W	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHC32, SN74AHC32 :**

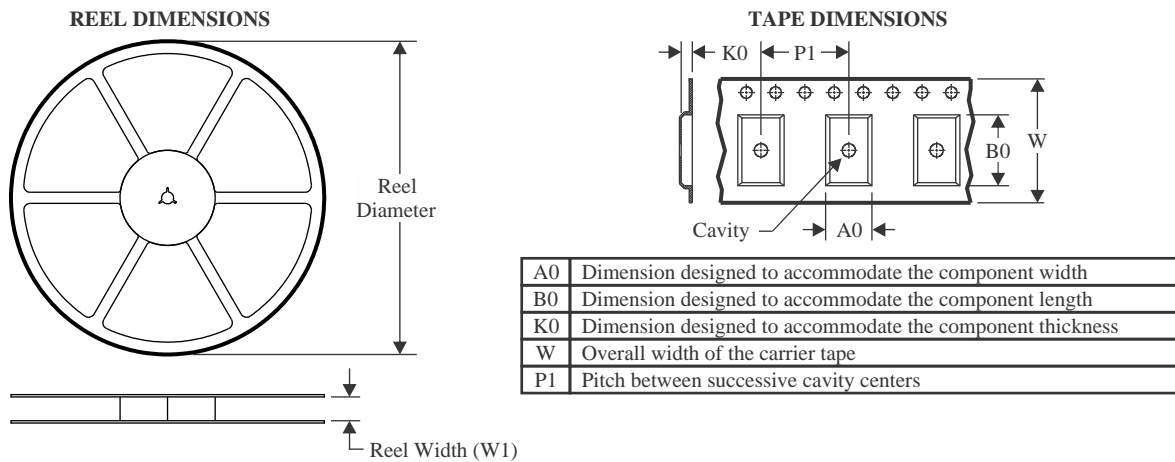
- Catalog : [SN74AHC32](#)

- Enhanced Product : [SN74AHC32-EP](#), [SN74AHC32-EP](#)
- Military : [SN54AHC32](#)

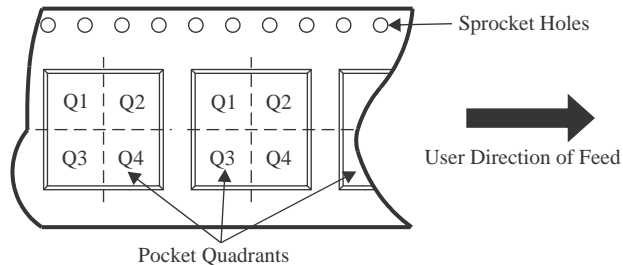
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



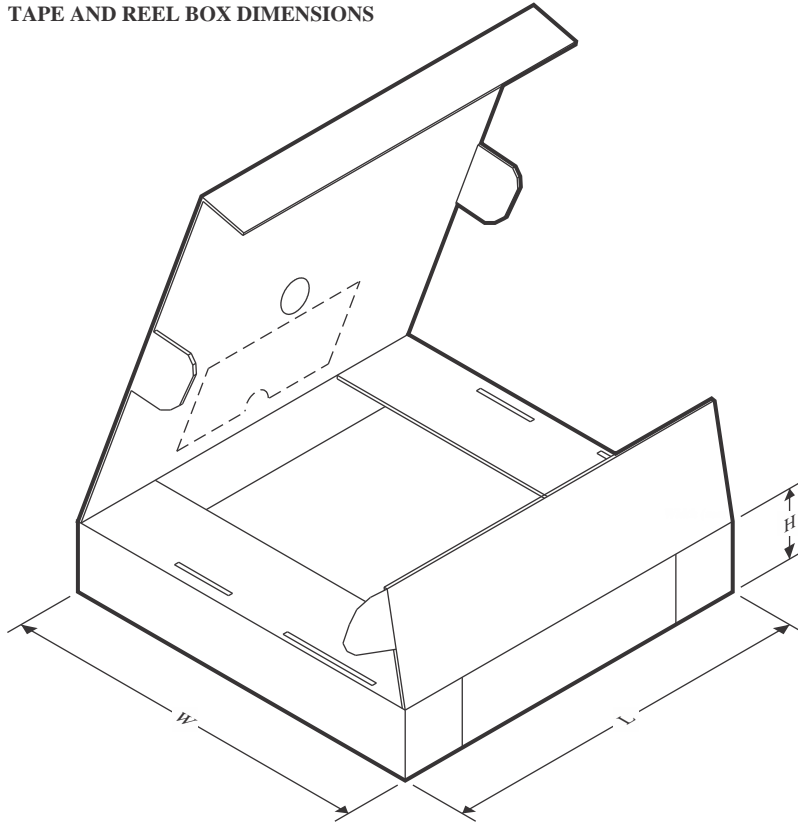
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC32BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC32DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC32DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC32DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC32NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC32PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74AHC32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC32RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

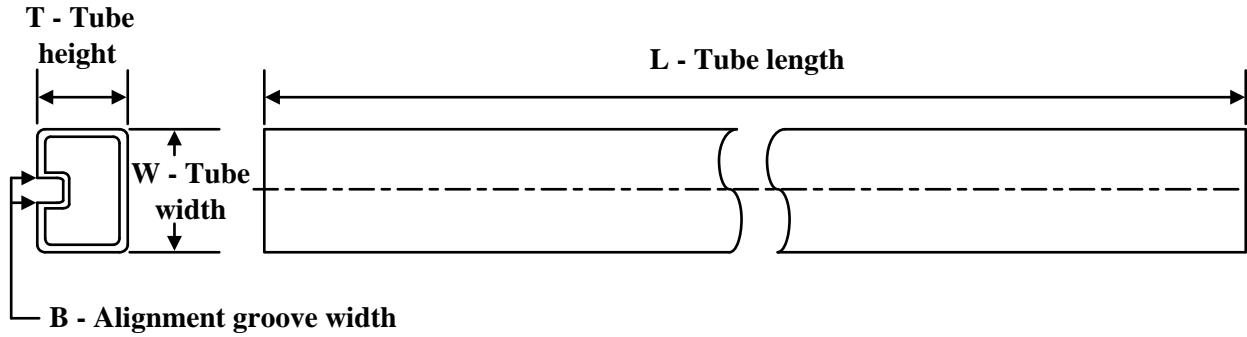
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC32BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC32DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC32DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC32DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC32DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC32DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC32NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74AHC32PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74AHC32PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC32PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC32RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

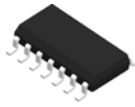
## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9682501Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9682501QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC32N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC32FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC32W	W	CFP	14	25	506.98	26.16	6220	NA



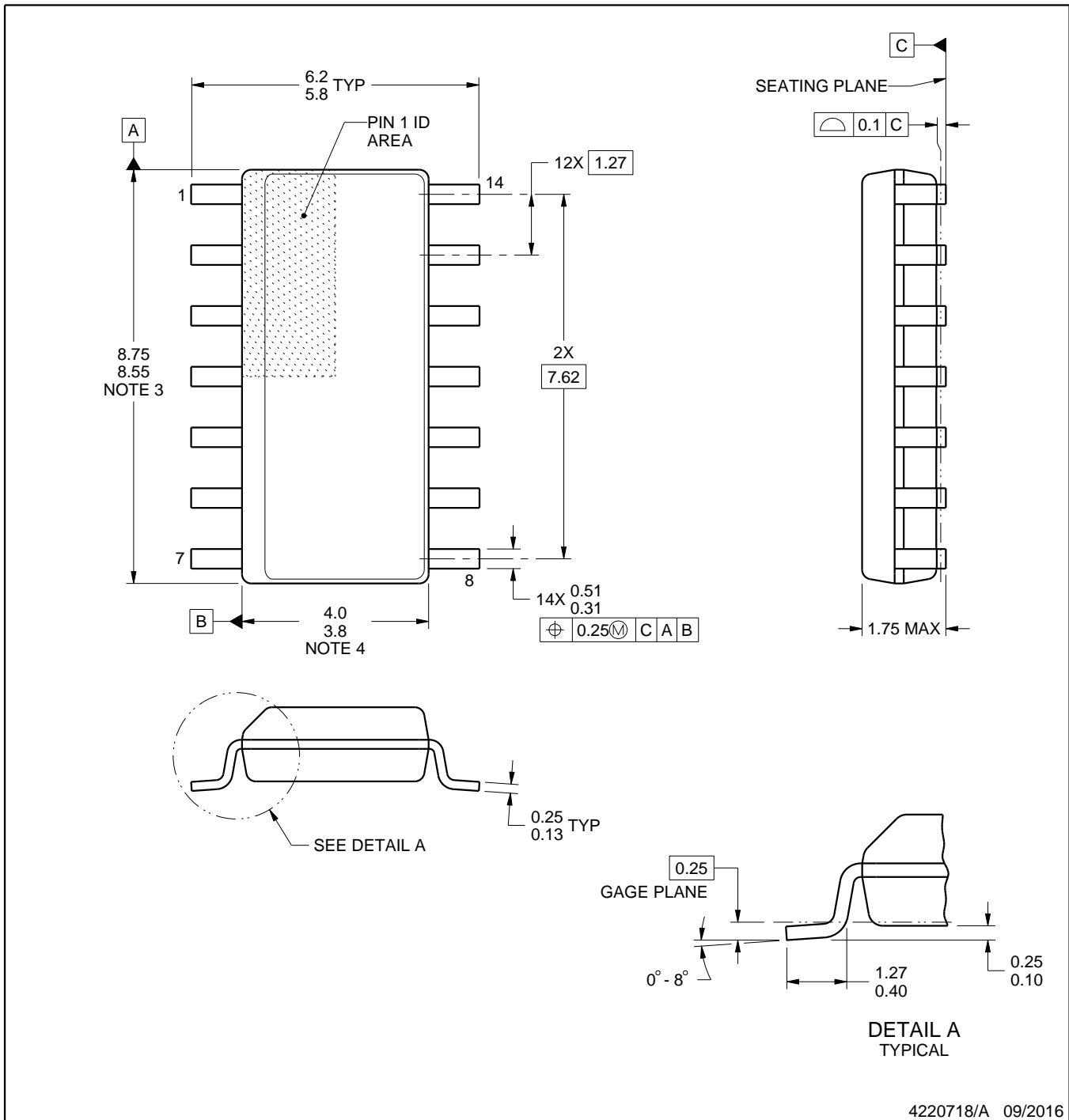


D0014A

## PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

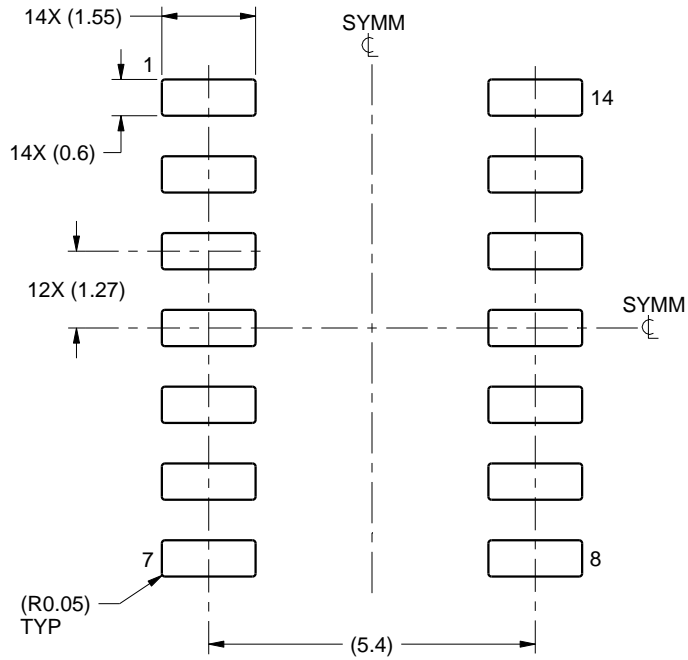
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

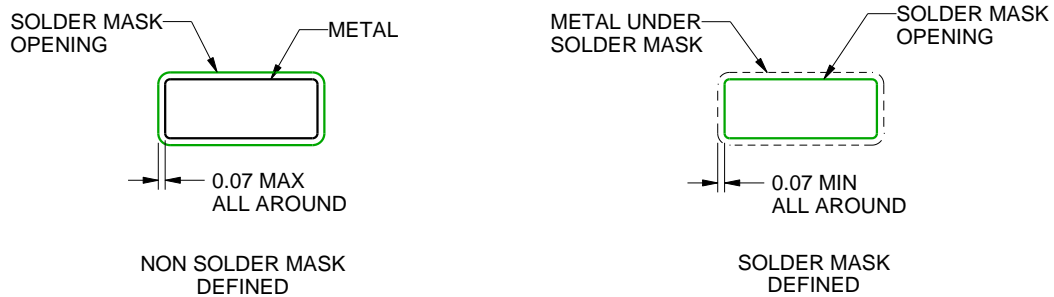
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

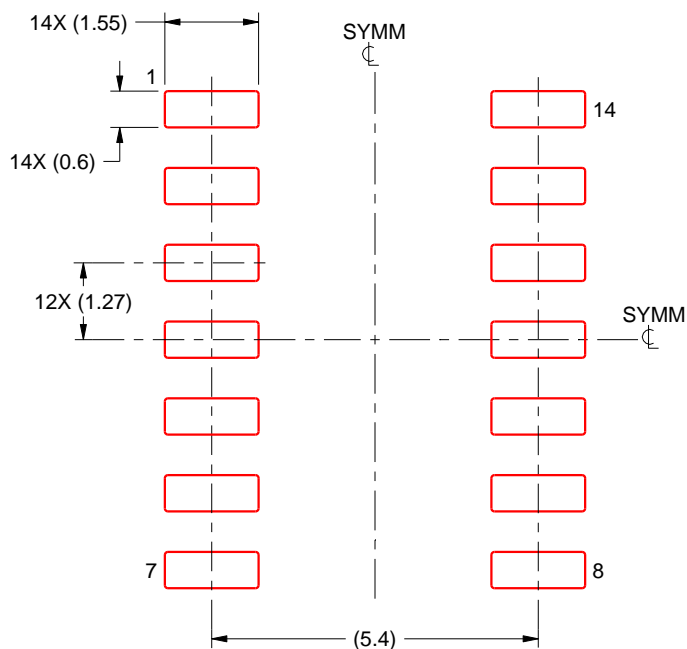
4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****D0014A****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:8X

4220718/A 09/2016

NOTES: (continued)

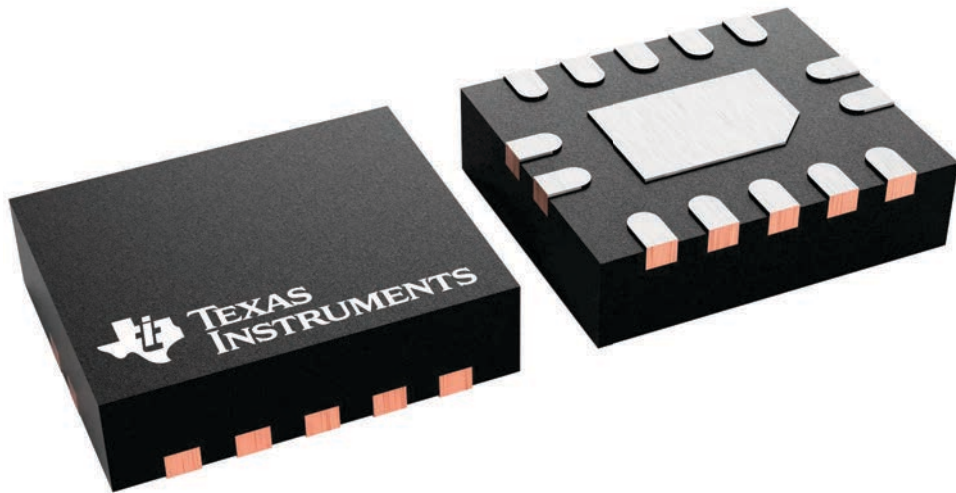
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**GENERIC PACKAGE VIEW****BQA 14****WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

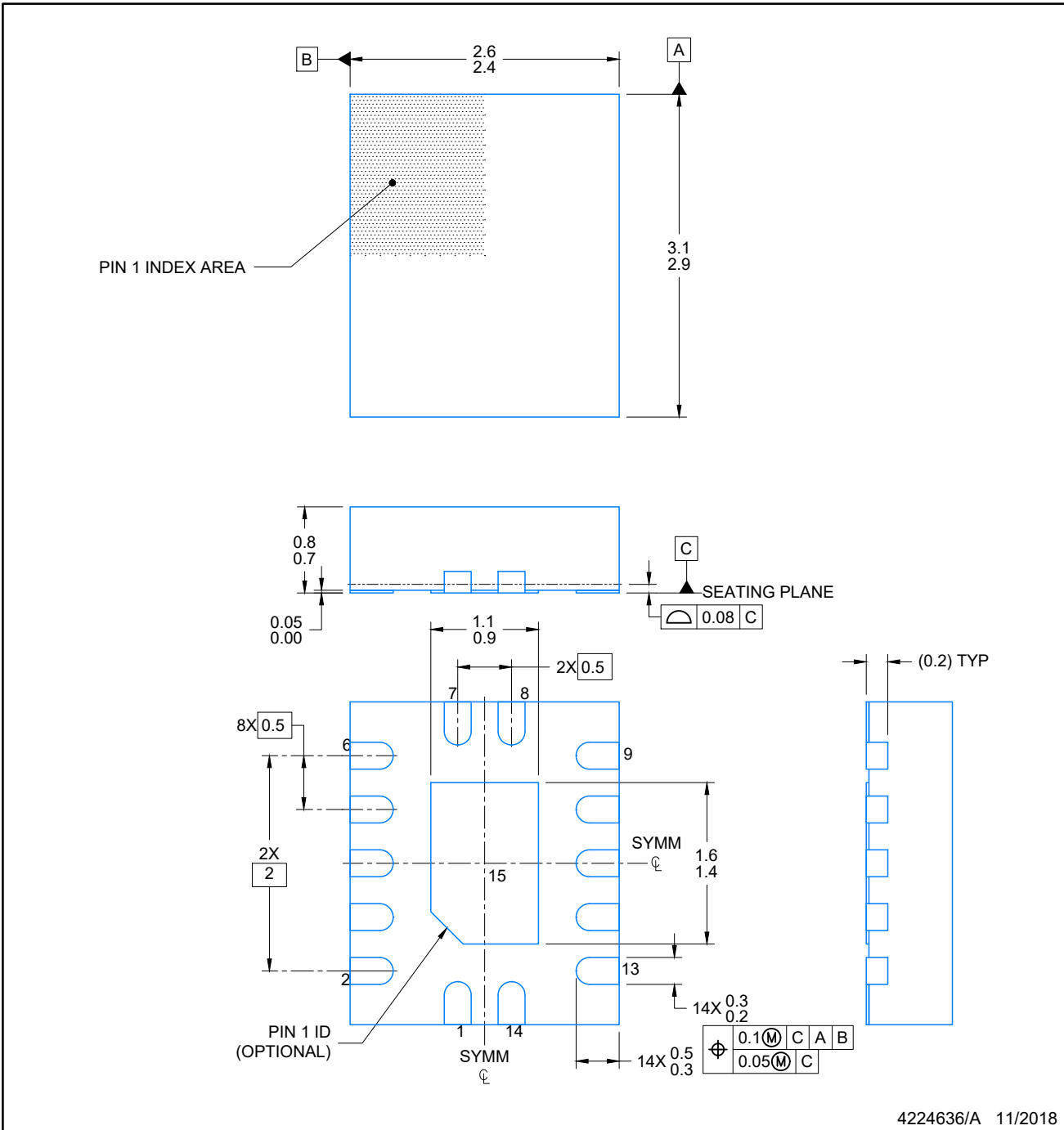


# PACKAGE OUTLINE

## BQA0014A

### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



**NOTES:**

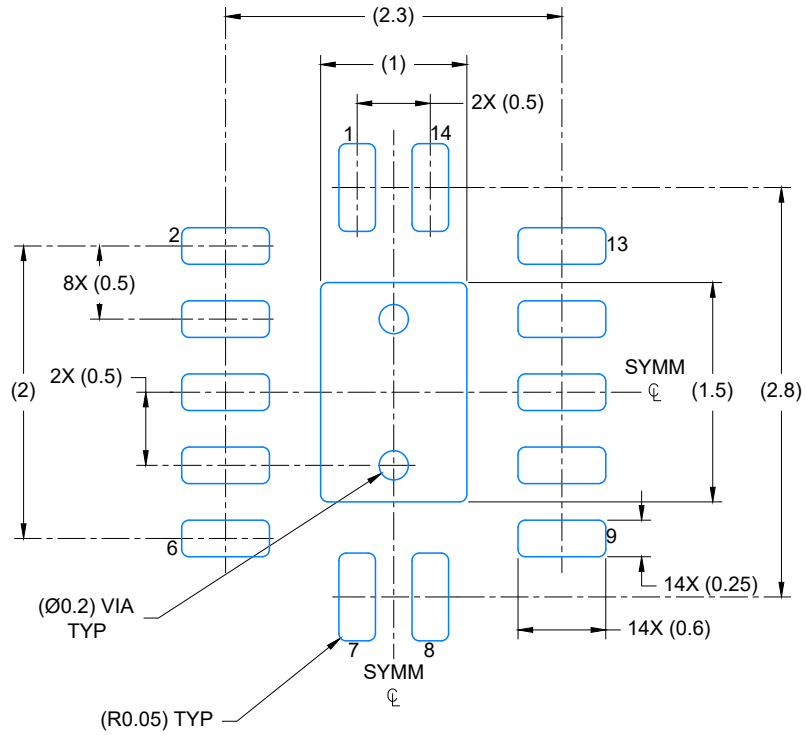
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

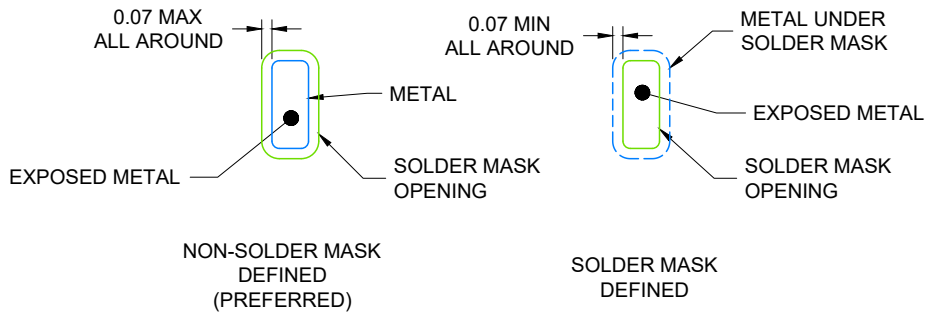
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

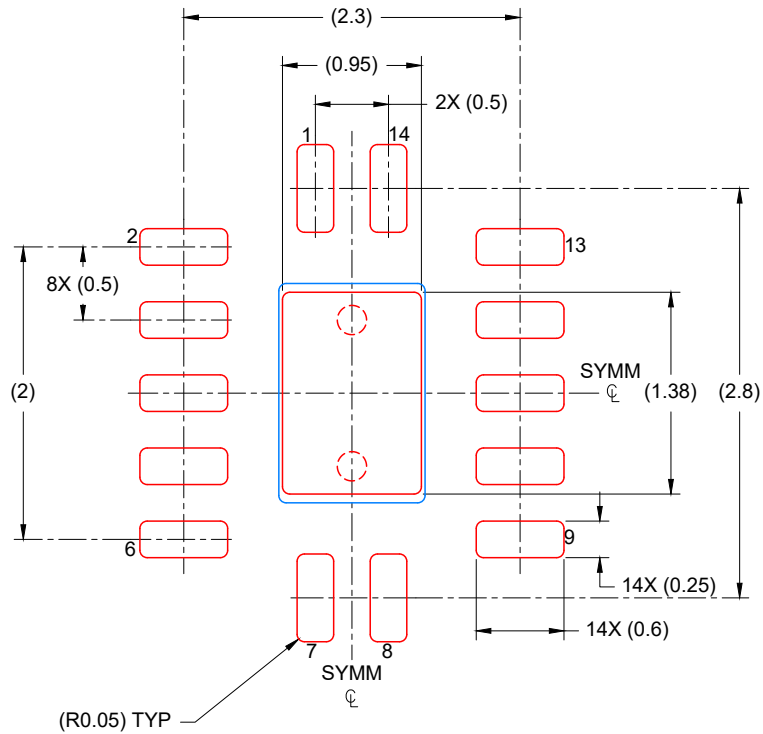
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

**BQA0014A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

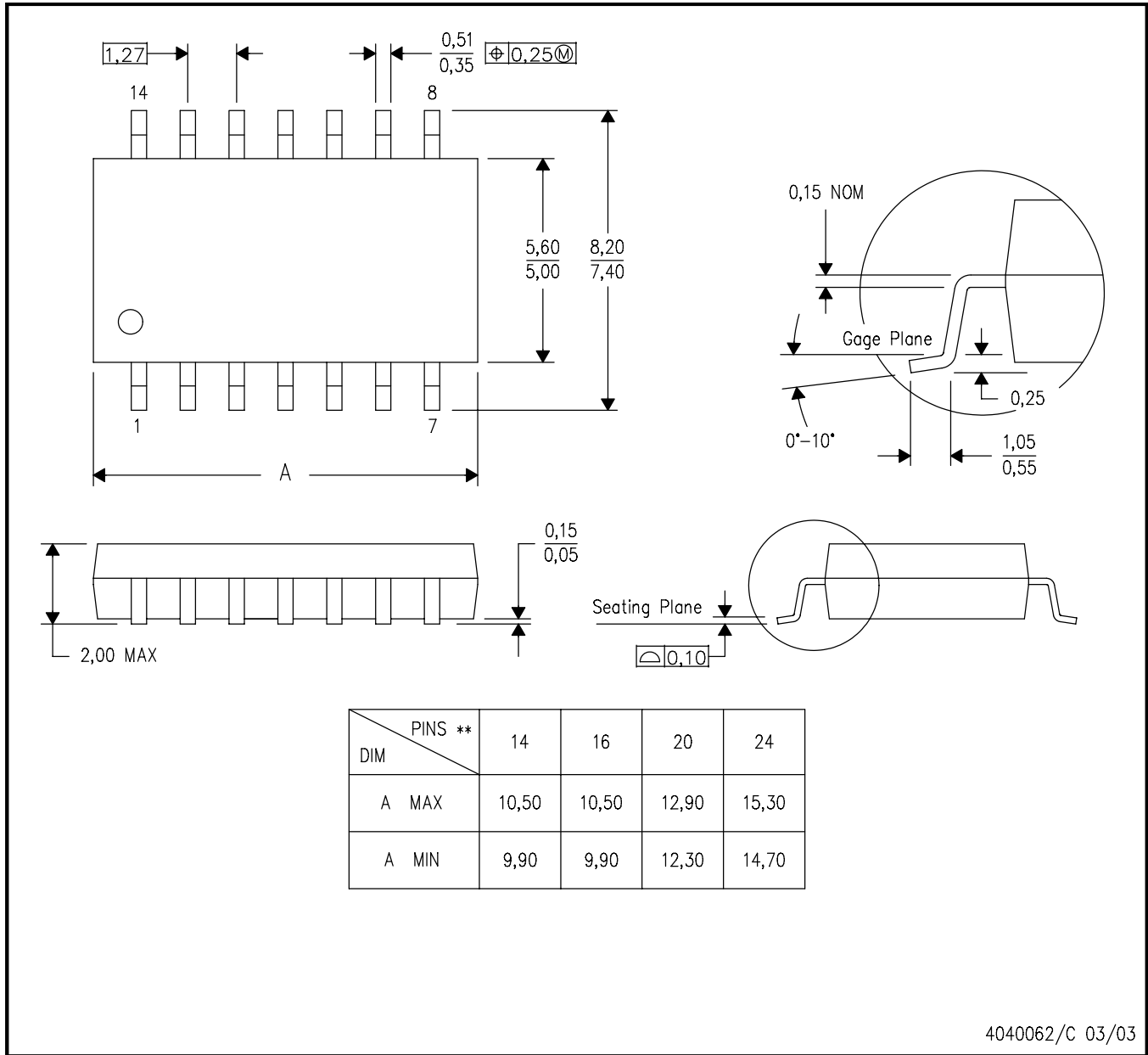
- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**MECHANICAL DATA**

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



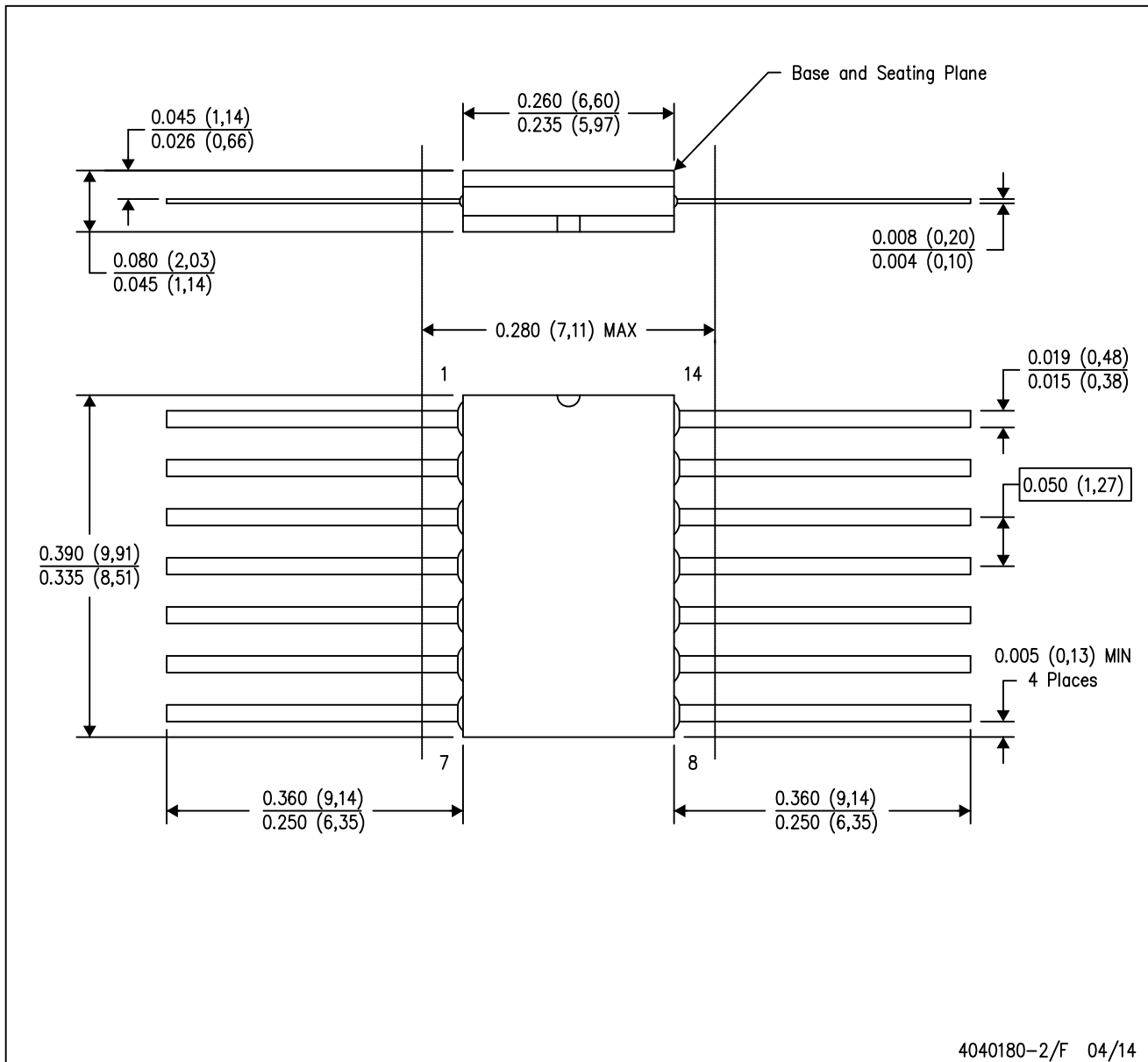
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



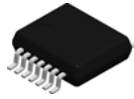
## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14

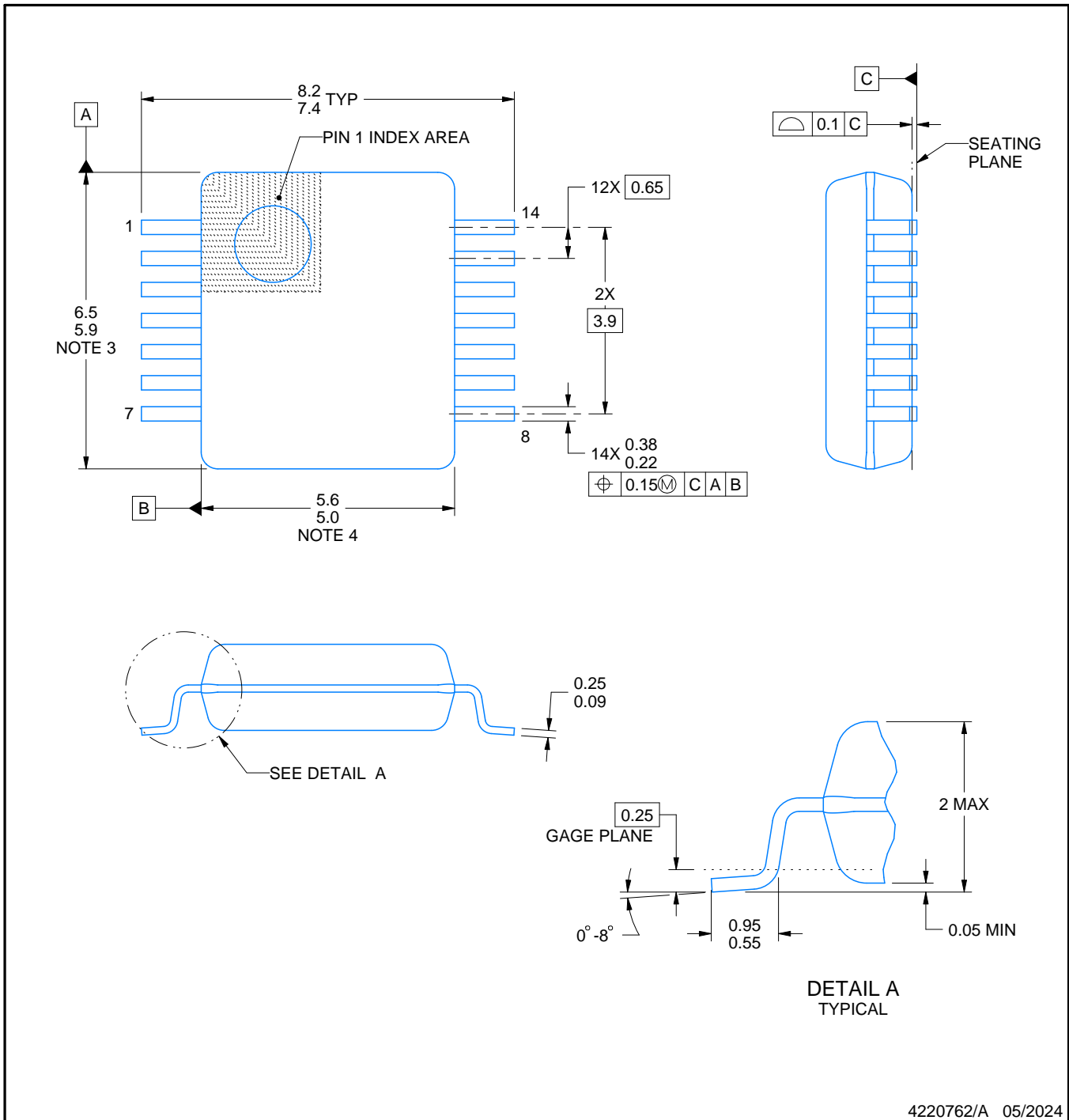


# PACKAGE OUTLINE

## DB0014A

### SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220762/A 05/2024

**NOTES:**

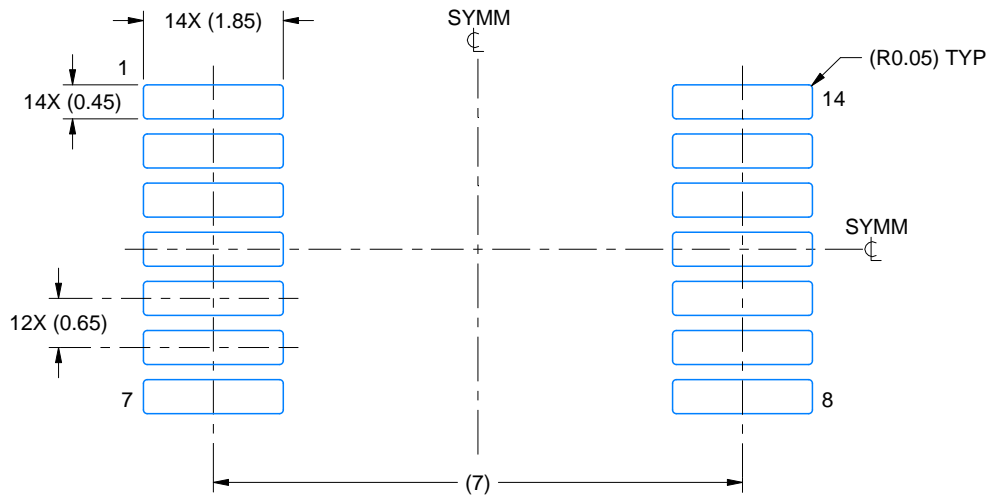
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

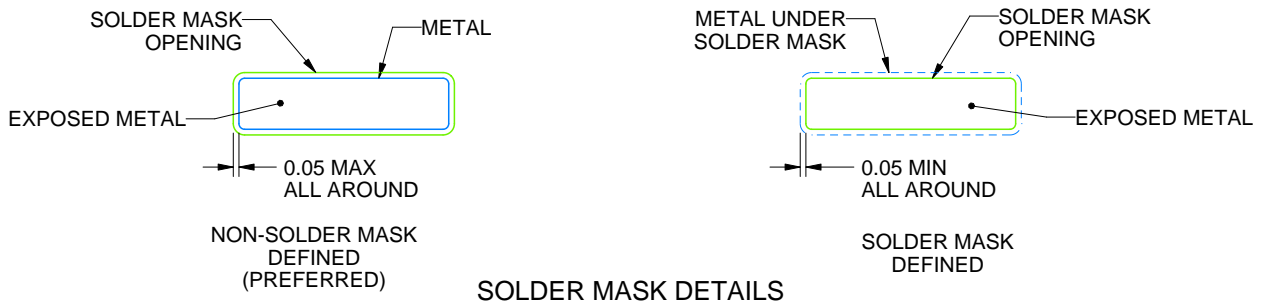
**DB0014A**

**SSOP - 2 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



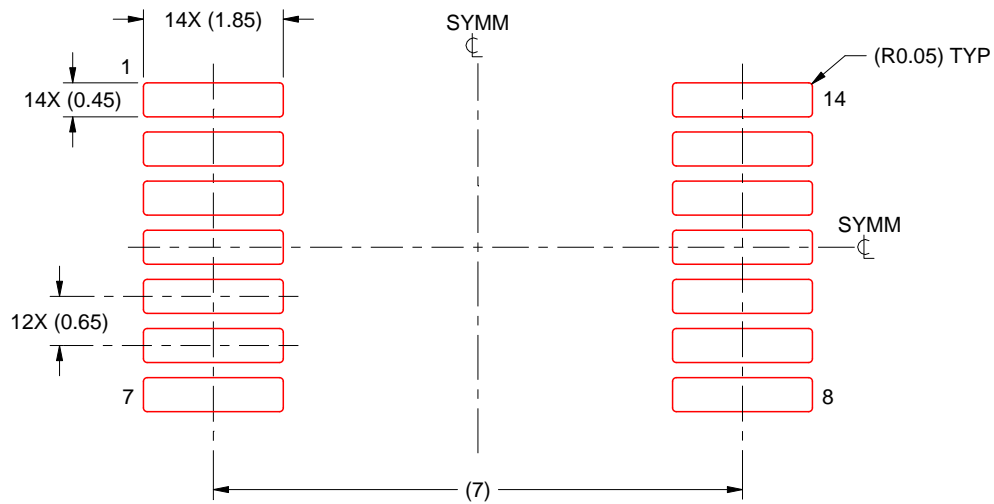
4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****DB0014A****SSOP - 2 mm max height**

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

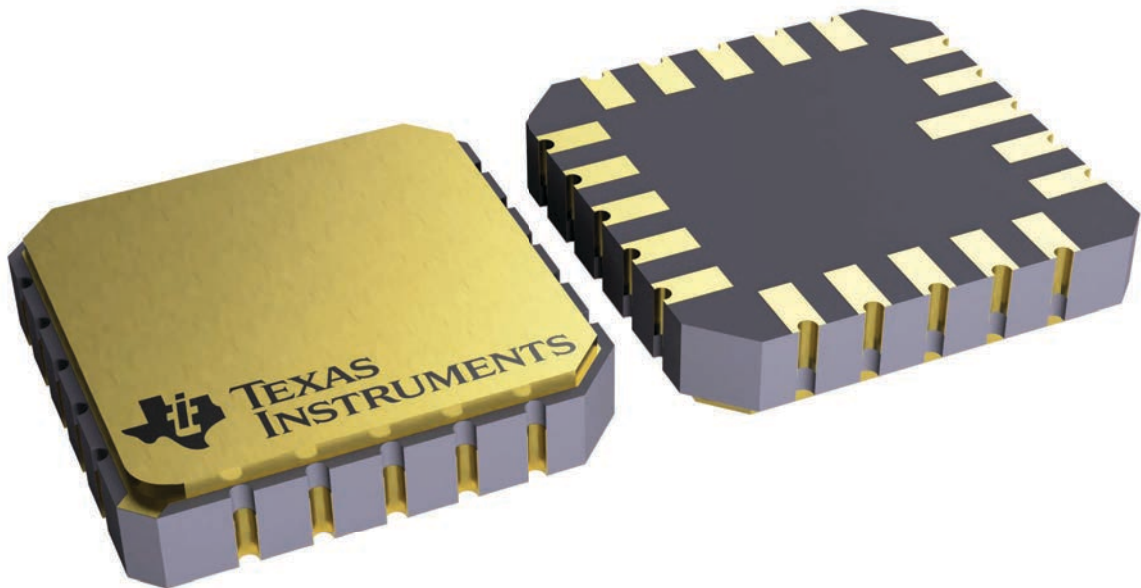
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



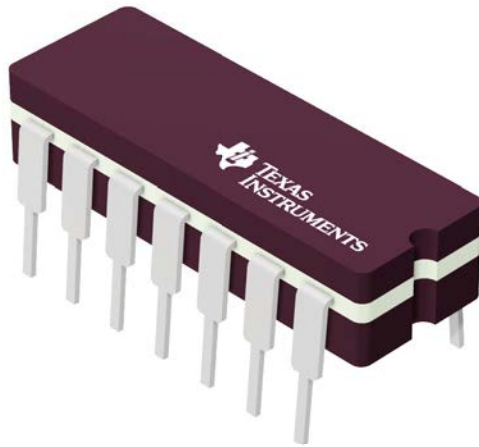
4229370VA\

## GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

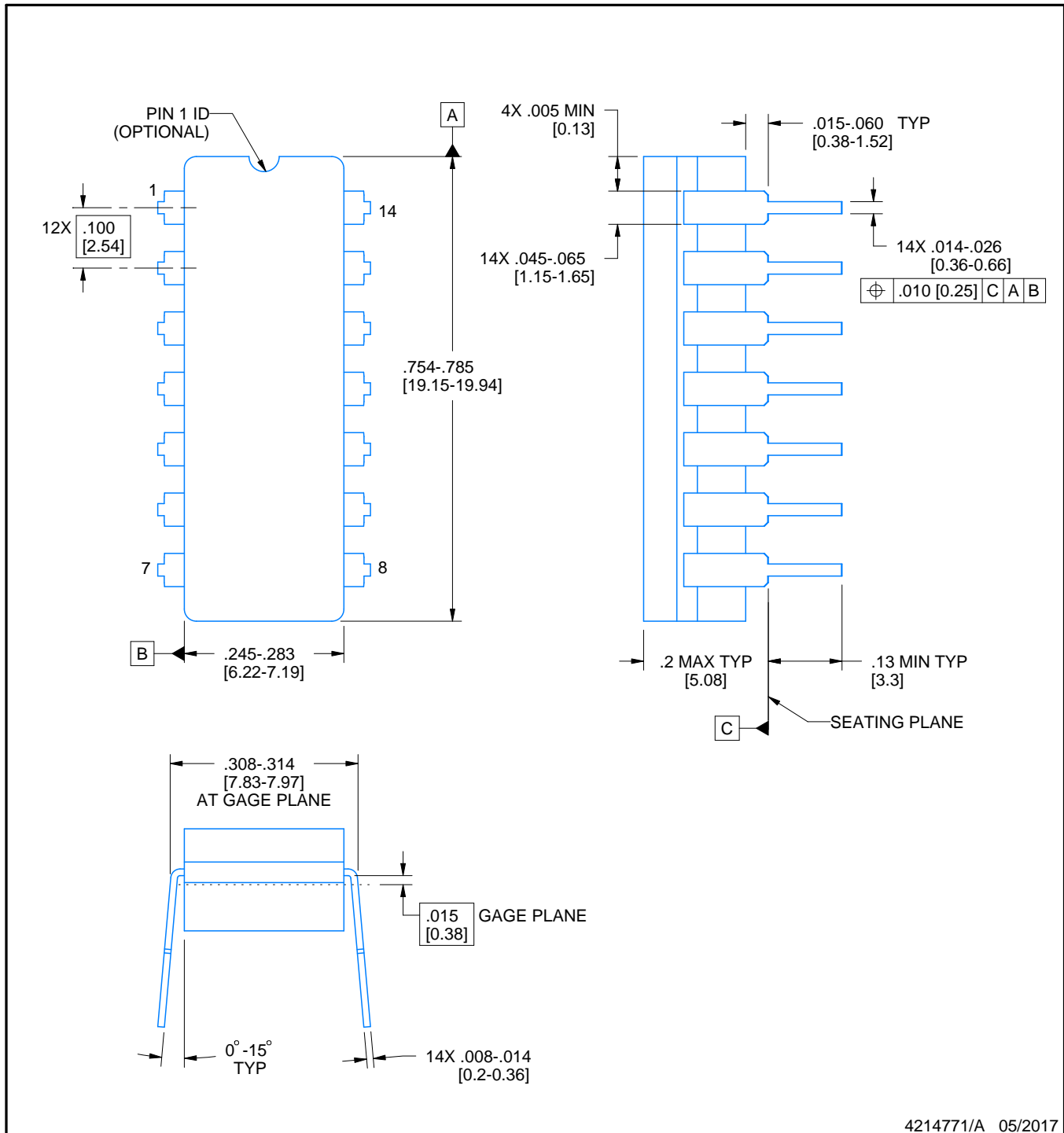


J0014A

## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

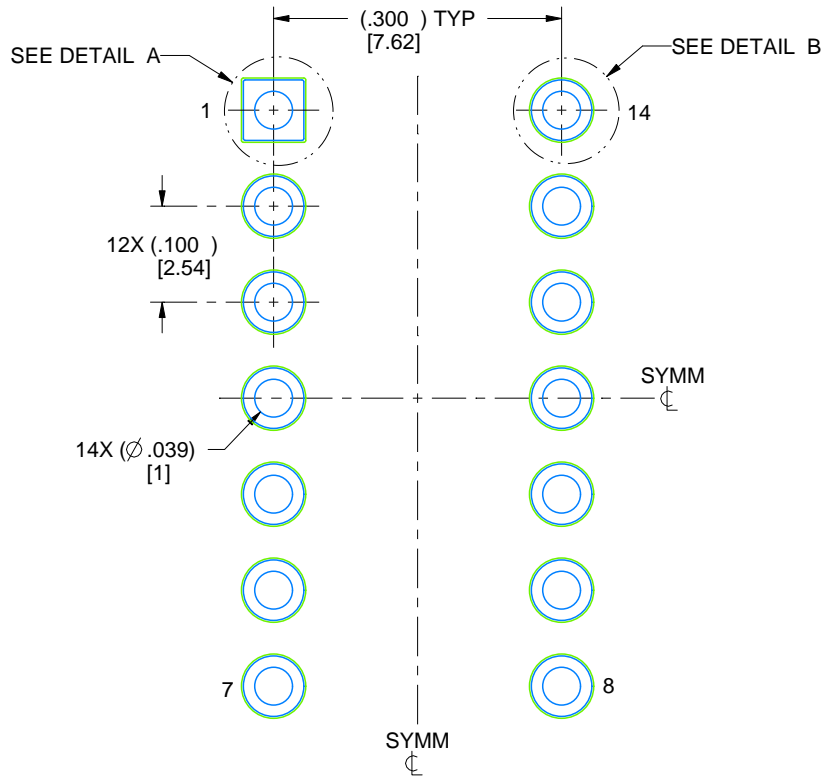
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

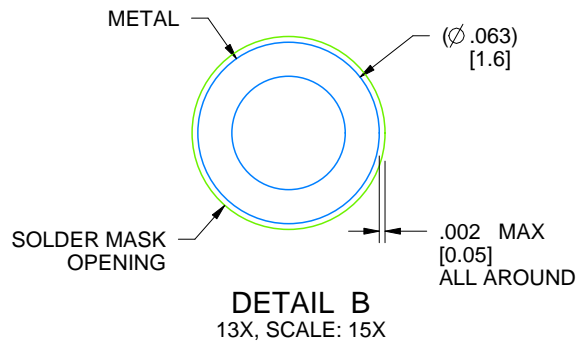
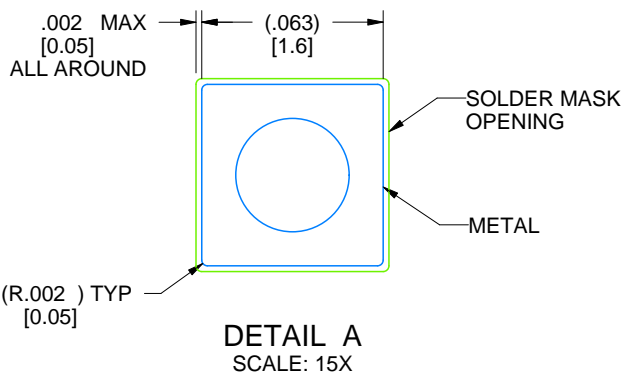
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

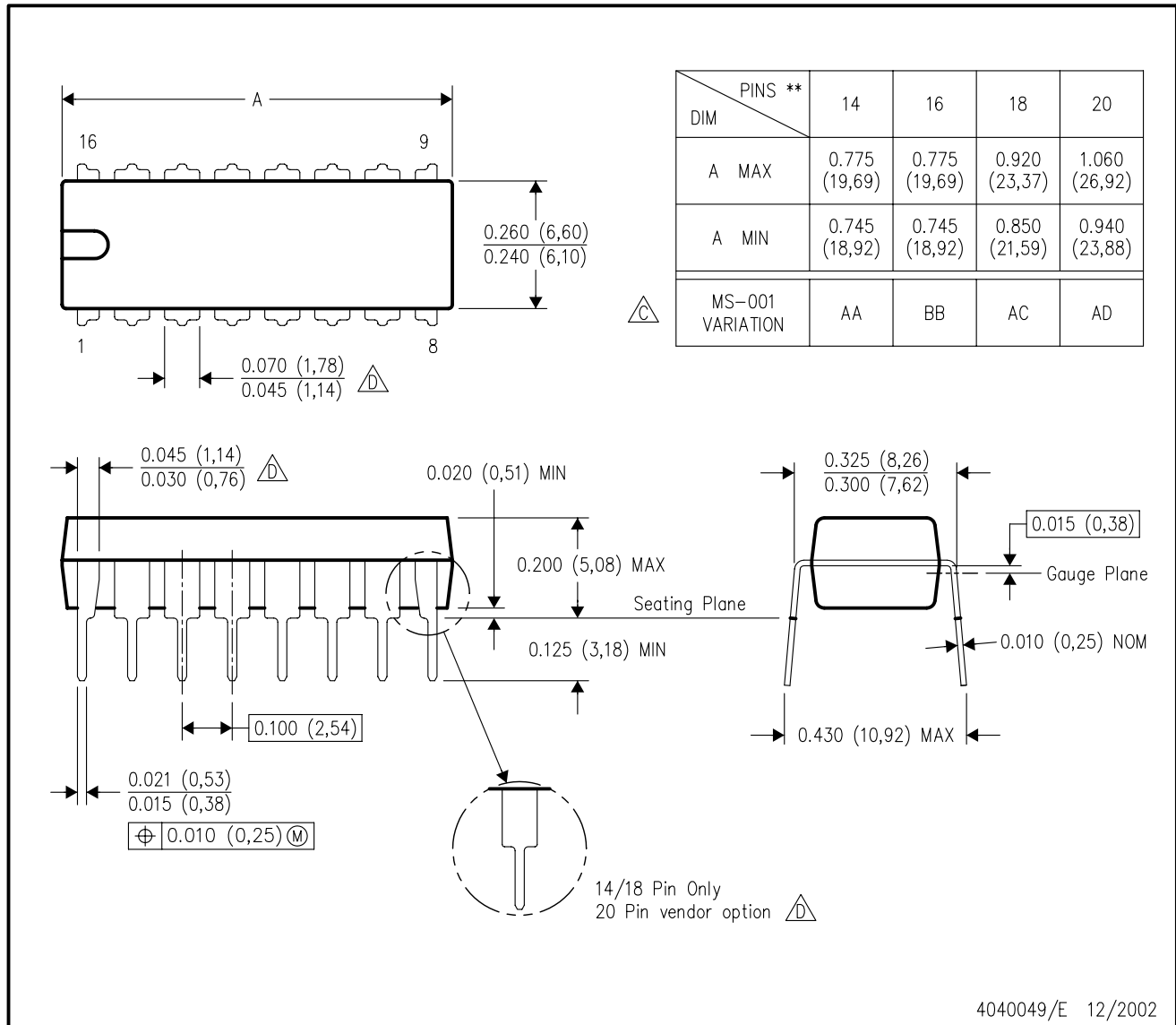


**MECHANICAL DATA**

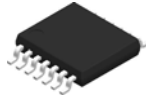
**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

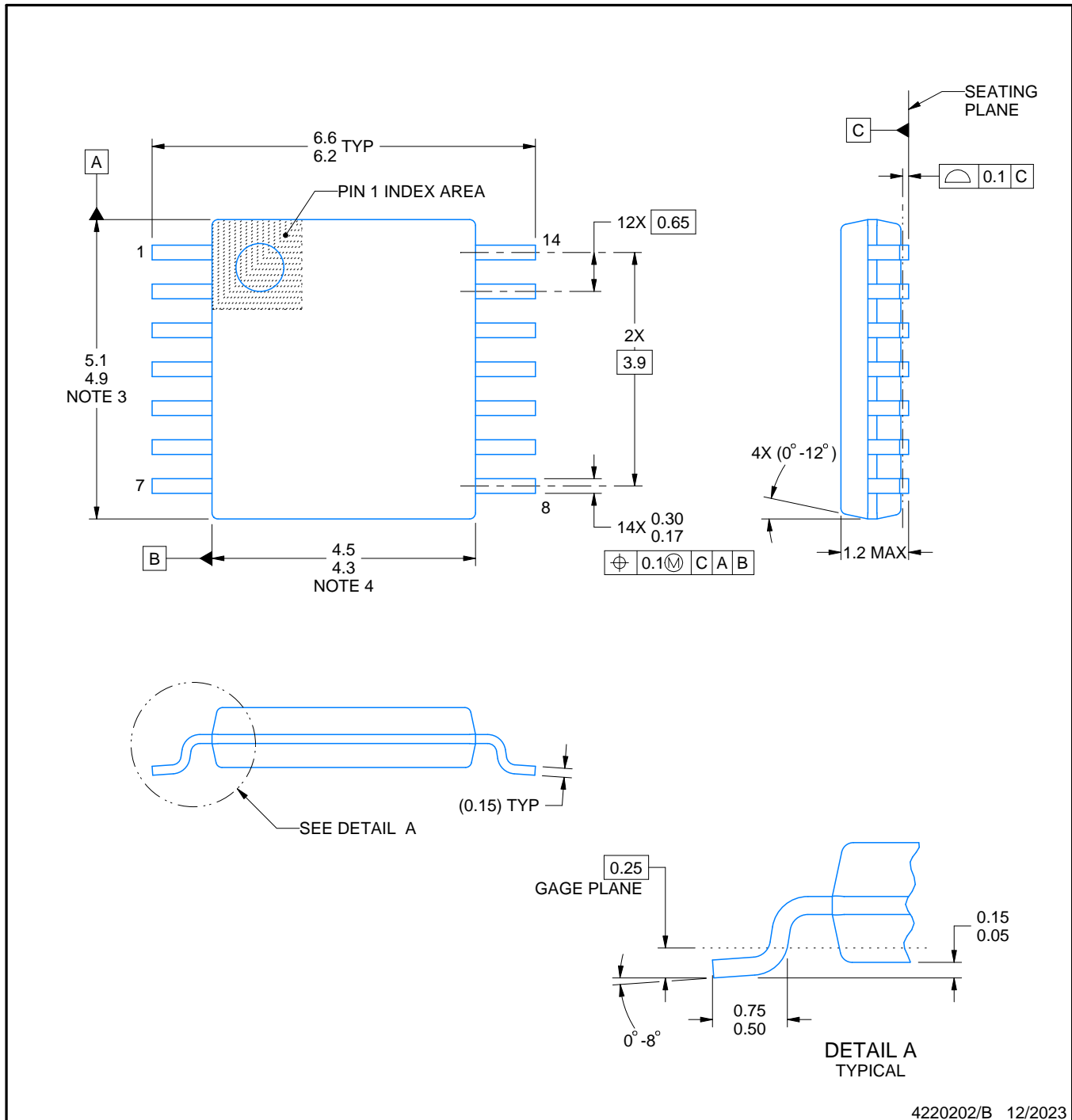


## PACKAGE OUTLINE

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

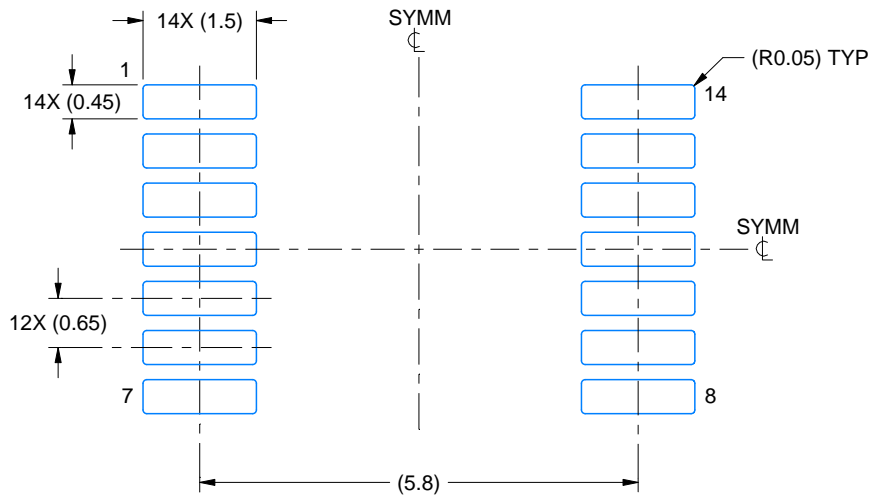
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

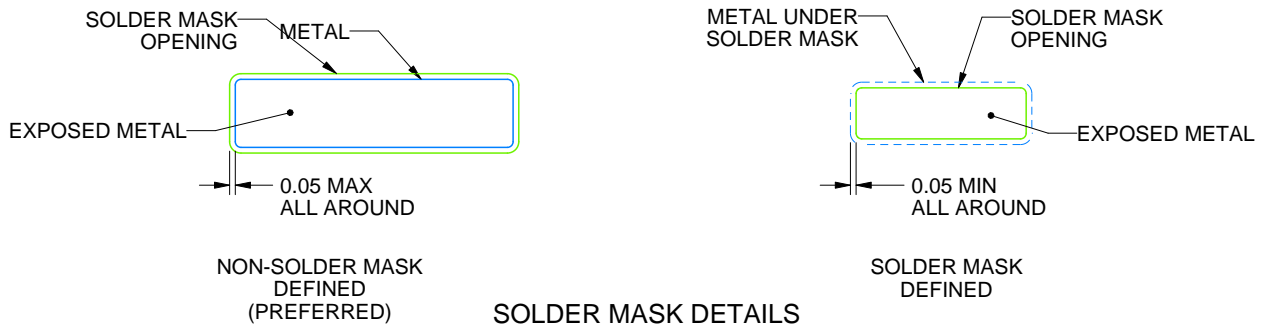
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



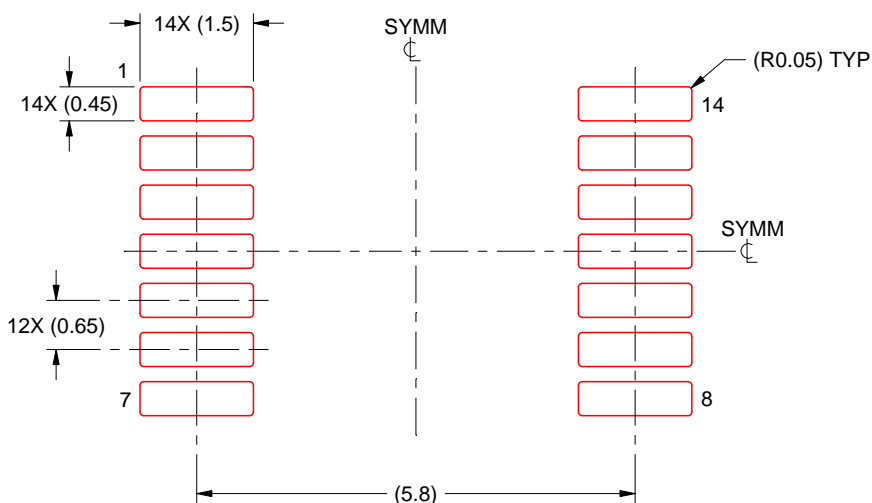
4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****PW0014A****TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

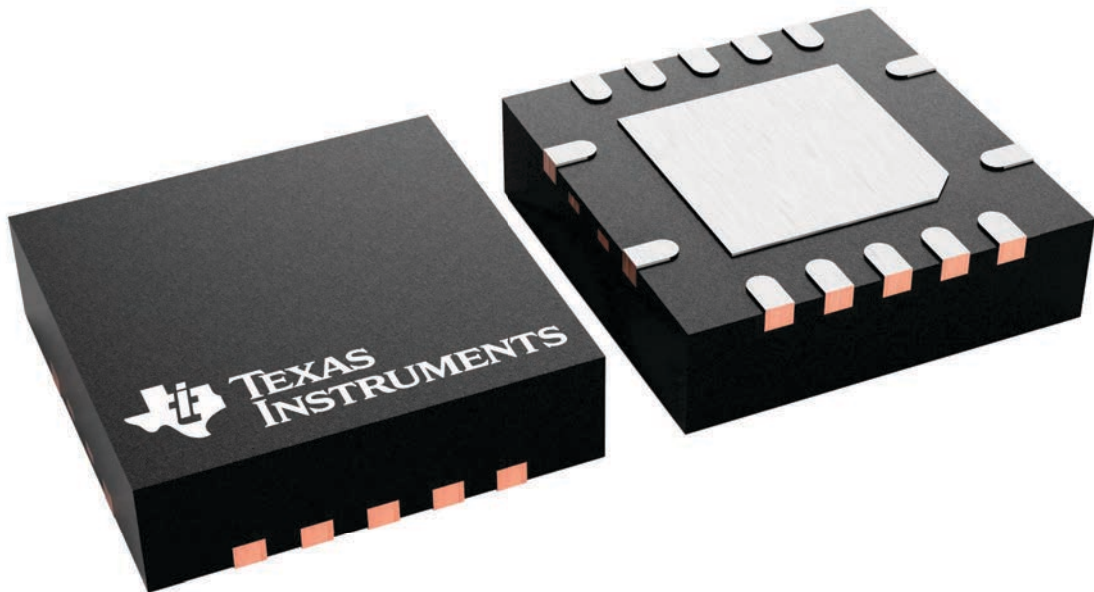
**RGY 14**

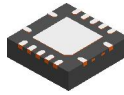
**VQFN - 1 mm max height**

**3.5 x 3.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



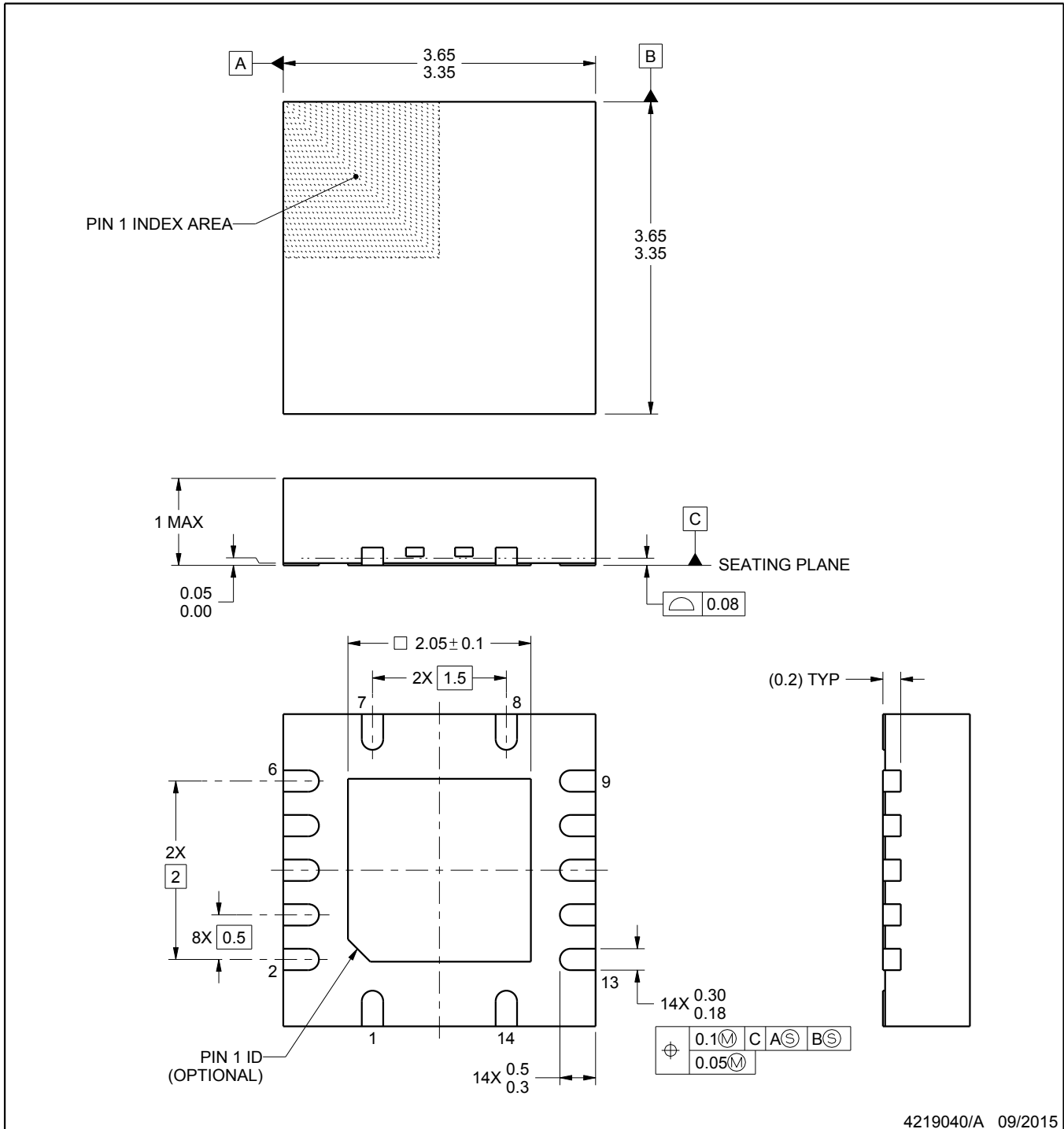


**RGY0014A**

**PACKAGE OUTLINE**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

**NOTES:**

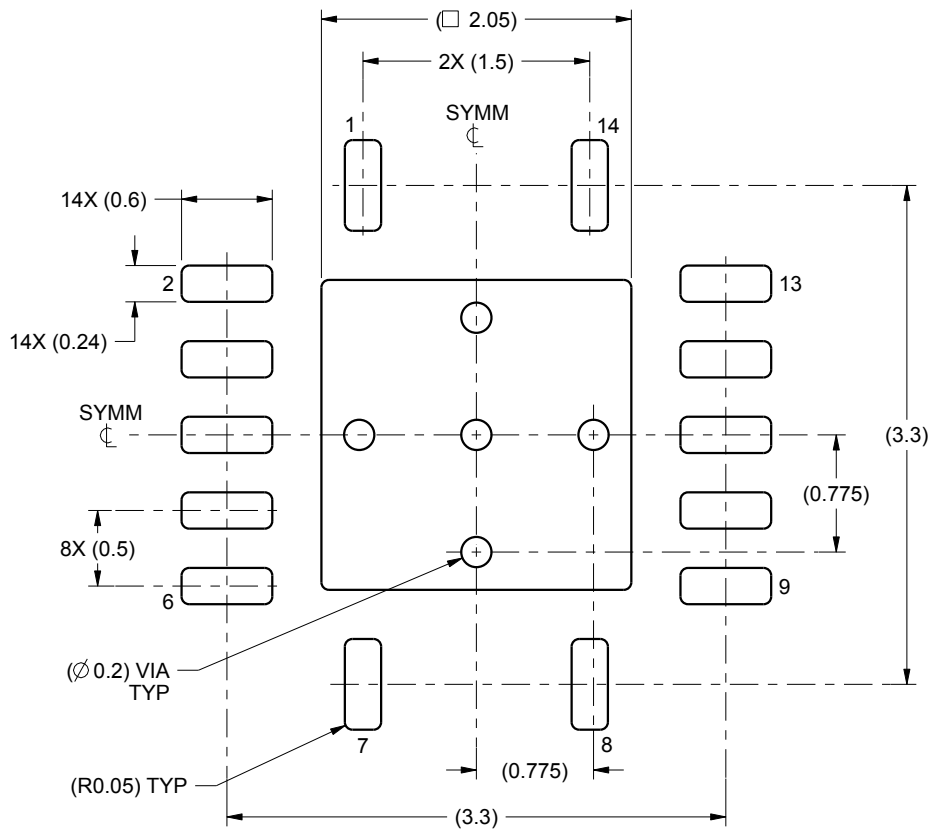
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

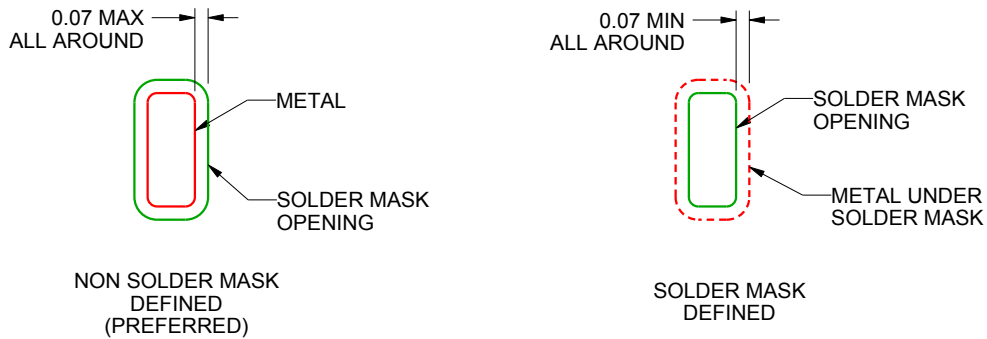
**RGY0014A**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

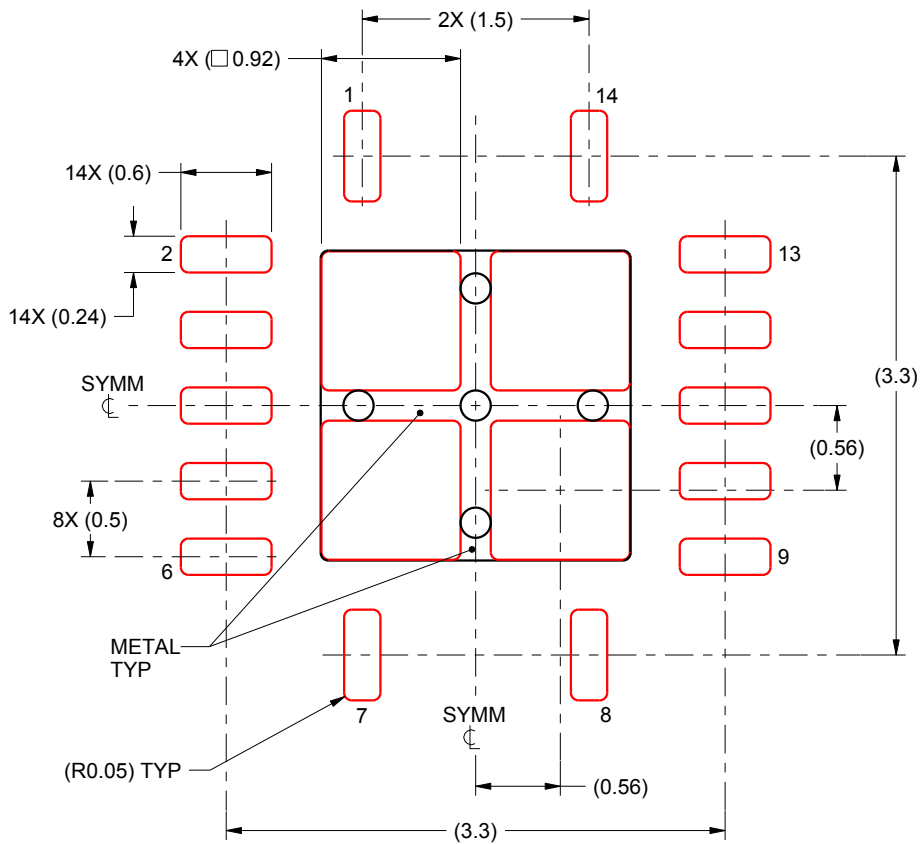
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

**RGY0014A**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 EXPOSED PAD  
 80% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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