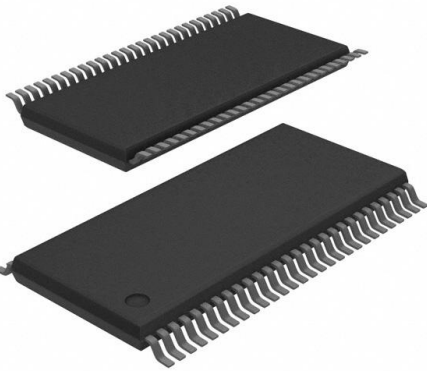


# SN74CBT16811CDGGR Datasheet

[www.digi-electronics.com](http://www.digi-electronics.com)



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	SN74CBT16811CDGGR-DG
Manufacturer	<a href="#">Texas Instruments</a>
Manufacturer Product Number	SN74CBT16811CDGGR
Description	IC BUS SWITCH 12 X 1:1 56TSSOP
Detailed Description	Bus Switch 12 x 1:1 56-TSSOP

This model SN74CBT16811CDGGR is available at DiGi Electronics.

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## Purchase and inquiry

Manufacturer Product Number:

SN74CBT16811CDGGR

Series:

74CBT

Type:

Bus Switch

Independent Circuits:

2

Voltage Supply Source:

Single Supply

Operating Temperature:

-40°C ~ 85°C

Package / Case:

56-TFSOP (0.240", 6.10mm Width)

Base Product Number:

74CBT16811

Manufacturer:

Texas Instruments

Product Status:

Active

Circuit:

12 x 1:1

Current - Output High, Low:

-

Voltage - Supply:

4V ~ 5.5V

Mounting Type:

Surface Mount

Supplier Device Package:

56-TSSOP

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

# SN74CBT16811C

## 24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

### 5-V BUS SWITCH WITH $-2$ -V UNDERSHOOT PROTECTION

SCDS118C – JANUARY 2003 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- Undershoot Protection for Off-Isolation on A and B Ports Up To  $-2$  V
- B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging
- Supports PCI Hot Plug
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3 \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 5.5$  pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 3 \mu A$  Max)
- $V_{CC}$  Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)

BIASV	1	56	1OE
1A1	2	55	2OE
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
$V_{CC}$	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12

### description/ordering information

The SN74CBT16811C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16811C provides protection for undershoot up to  $-2$  V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.



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**SN74CBT16811C****24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS****5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

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**description/ordering information (continued)**

The SN74CBT16811C is organized as two 12-bit bus switches with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When  $\overline{OE}$  is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-k $\Omega$  resistor when  $\overline{OE}$  is high, or if the device is powered down ( $V_{CC} = 0$  V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16811CDL	CBT16811C
		Tape and reel	SN74CBT16811CDLR	
	TSSOP – DGG	Tube	SN74CBT16811CDGG	CBT16811C
		Tape and reel	SN74CBT16811CDGGR	
	TVSOP – DGV	Tape and reel	SN74CBT16811CDGVR	CY811C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**  
(each 12-bit bus switch)

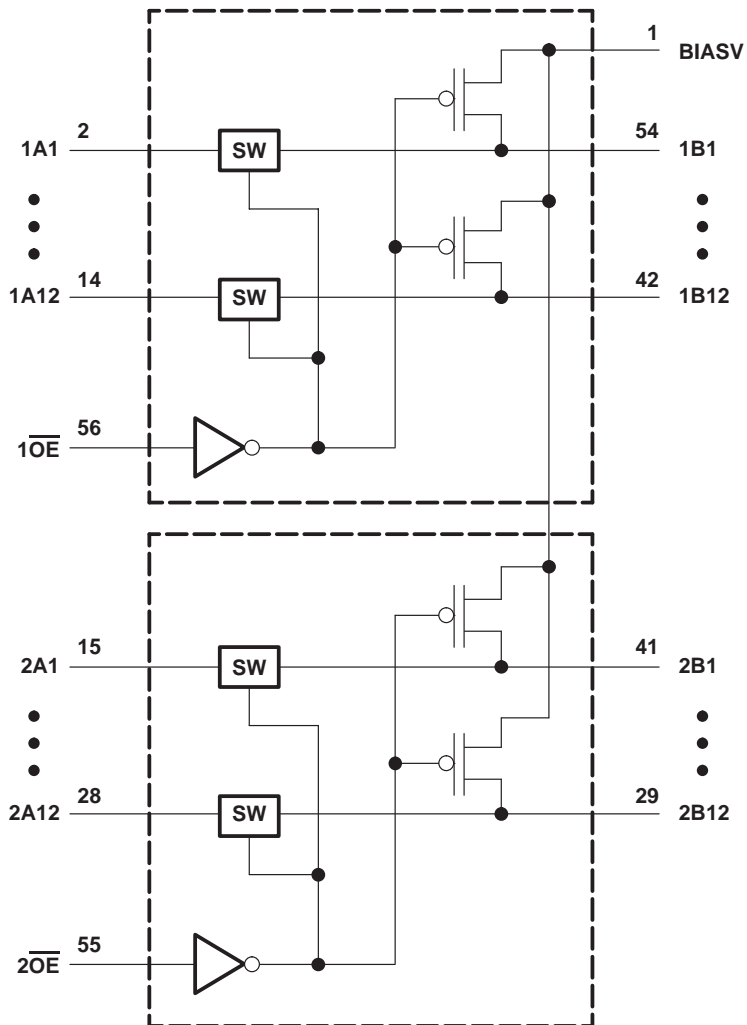
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

# SN74CBT16811C

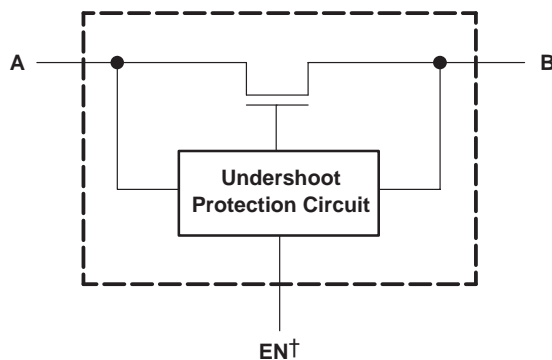
## 24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

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logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

**SN74CBT16811C****24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS****5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

SCDS118C – JANUARY 2003 – REVISED OCTOBER 2003

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Bias supply voltage range, BIASV	-0.5 V to 7 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	-0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	-0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	-50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )	-50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	$\pm 128$ mA
Continuous current through $V_{CC}$ or GND terminals	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 6)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
BIASV Bias supply voltage	0	$V_{CC}$	V
$V_{IH}$ High-level control input voltage	2	5.5	V
$V_{IL}$ Low-level control input voltage	0	0.8	V
$V_{I/O}$ Data input/output voltage	0	5.5	V
$T_A$ Operating free-air temperature	-40	85	°C

NOTE 6: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

# SN74CBT16811C

## 24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

### 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS118C – JANUARY 2003 – REVISED OCTOBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Control inputs	$V_{CC} = 4.5\text{ V}$ ,	$I_{IN} = -18\text{ mA}$			-1.8	V
$V_{IKU}$	Data inputs	$V_{CC} = 5\text{ V}$ ,	$0\text{ mA} > I_I \geq -50\text{ mA}$ , $V_{IN} = V_{CC}$ or GND, Switch OFF			-2	V
$V_{O(USP)}^\ddagger$		$V_{CC} = \text{BIASV} = 5\text{ V}$ ,	$I_I = -10\text{ mA}$ , $V_{IN} = V_{CC}$ or GND, Switch OFF	3			V
$V_O$	B port	$V_{CC} = 0\text{ V}$ ,	$\text{BIASV} = V_X$ , $I_O = 0$	$V_X - 0.1$		$V_X$	V
$I_{IN}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_{IN} = V_{CC}$ or GND			$\pm 1$	$\mu\text{A}$
$I_O$	B port	$V_{CC} = 4.5\text{ V}$ ,	$\text{BIASV} = 2.4\text{ V}$ , $V_O = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND		0.25		mA
$I_{OZ}^\S$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND			$\pm 10$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$			10	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$I_{I/O} = 0$ , $V_{IN} = V_{CC}$ or GND, Switch ON or OFF			3	$\mu\text{A}$
$\Delta I_{CC}^\parallel$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	One input at $3.4\text{ V}$ , Other inputs at $V_{CC}$ or GND			2.5	mA
$C_{in}$	Control inputs	$V_{IN} = 3\text{ V}$ or 0			4.5		pF
$C_{iO(OFF)}$	A port	$V_{I/O} = 3\text{ V}$ or 0, Switch OFF, $V_{IN} = V_{CC}$ or GND			5.5		pF
$C_{iO(ON)}$		$V_{I/O} = 3\text{ V}$ or 0, Switch ON, $V_{IN} = V_{CC}$ or GND			15.5		pF
$r_{on}^\#$		$V_{CC} = 4\text{ V}$ , TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$ , $I_O = -15\text{ mA}$		8	12	$\Omega$
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_O = 64\text{ mA}$	3	6	
			$I_O = 30\text{ mA}$	3	6		
			$V_I = 2.4\text{ V}$ , $I_O = -15\text{ mA}$	5	10		

$V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡  $V_{O(USP)}$  = A-port undershoot static protection.

§ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

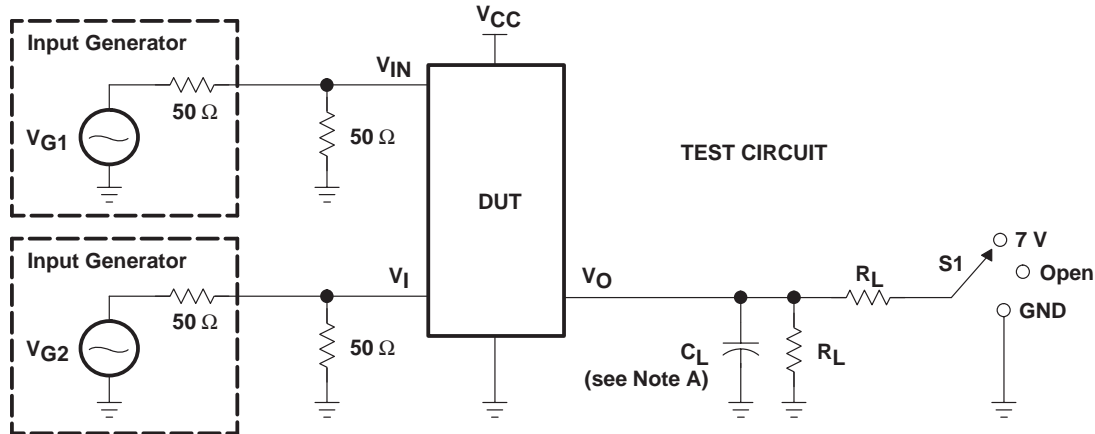
**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
$t_{pd}^{\parallel}$		A or B	B or A		0.24		0.15	ns
$t_{PZH}$	$\text{BIASV} = \text{GND}$	$\overline{\text{OE}}$	A or B		6.5	1.5	6	ns
$t_{PZL}$	$\text{BIASV} = 3\text{ V}$				6.5	1.5	6	
$t_{PHZ}$	$\text{BIASV} = \text{GND}$	$\overline{\text{OE}}$	A or B		6.5	1.5	6	ns
$t_{PLZ}$	$\text{BIASV} = 3\text{ V}$				6.5	1.5	6	

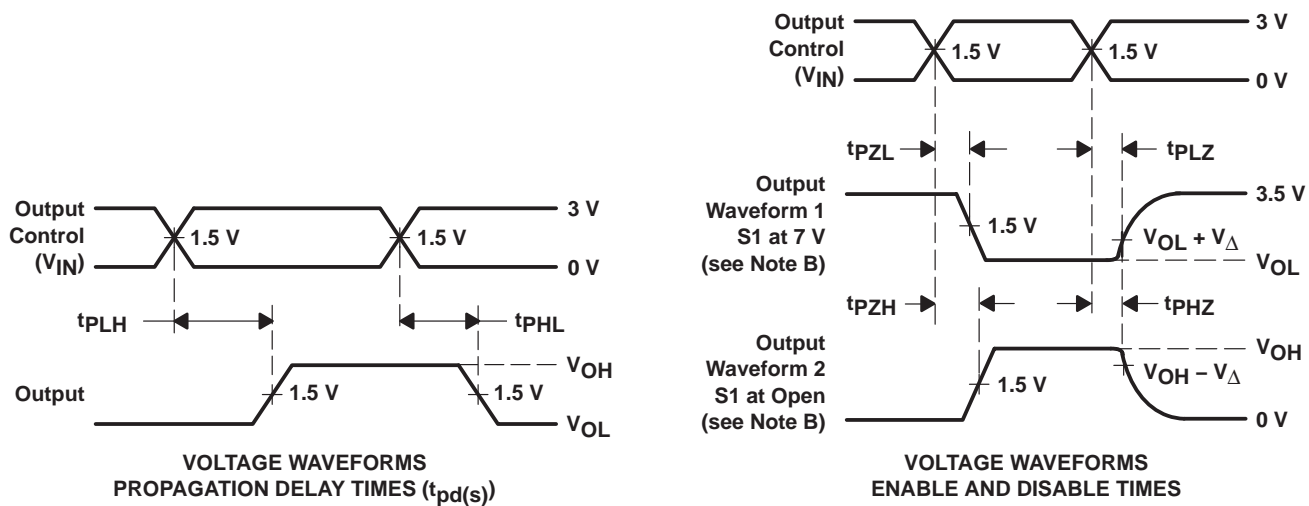
¶ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**SN74CBT16811C****24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS****5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

SCDS118C – JANUARY 2003 – REVISED OCTOBER 2003

**PARAMETER MEASUREMENT INFORMATION**

TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	5 V ± 0.5 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
	4 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.5 V	Open	500 Ω	V <sub>CC</sub>	50 pF	0.3 V
	4 V	Open	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

**Figure 1. Test Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT16811CDGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16811C	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

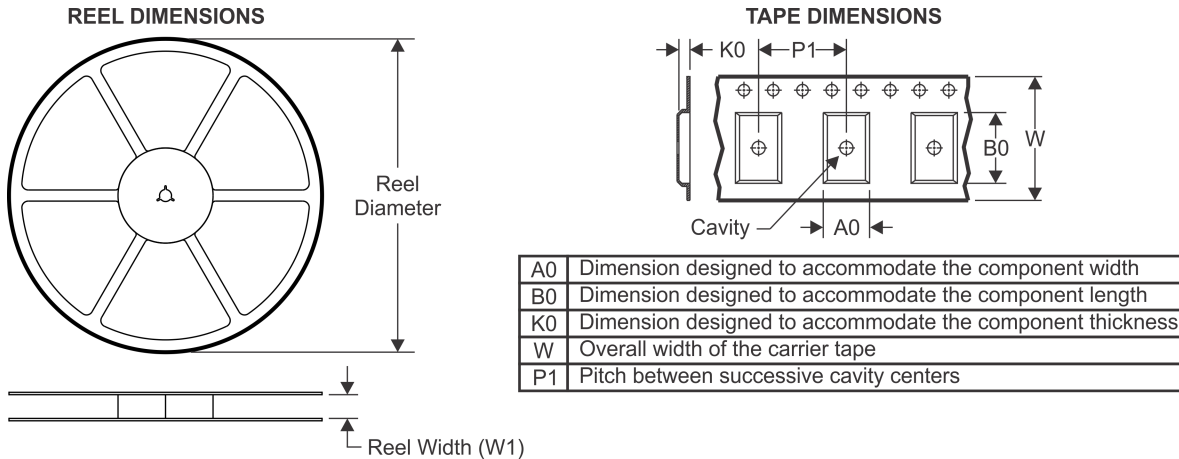
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

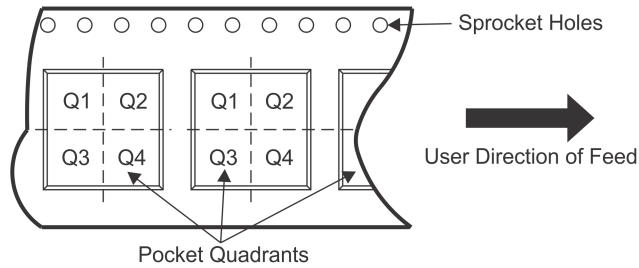
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## TAPE AND REEL INFORMATION



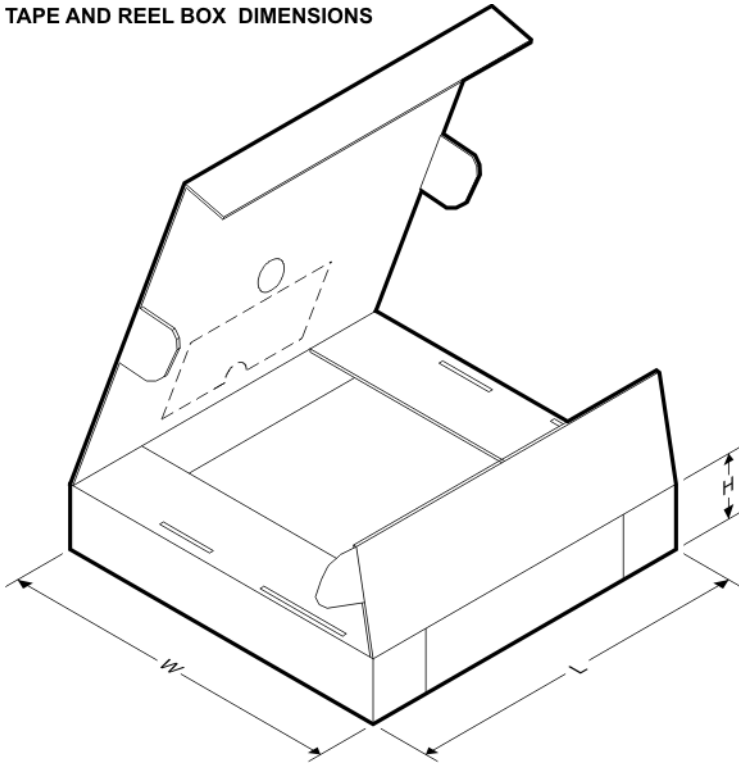
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16811CDGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16811CDGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

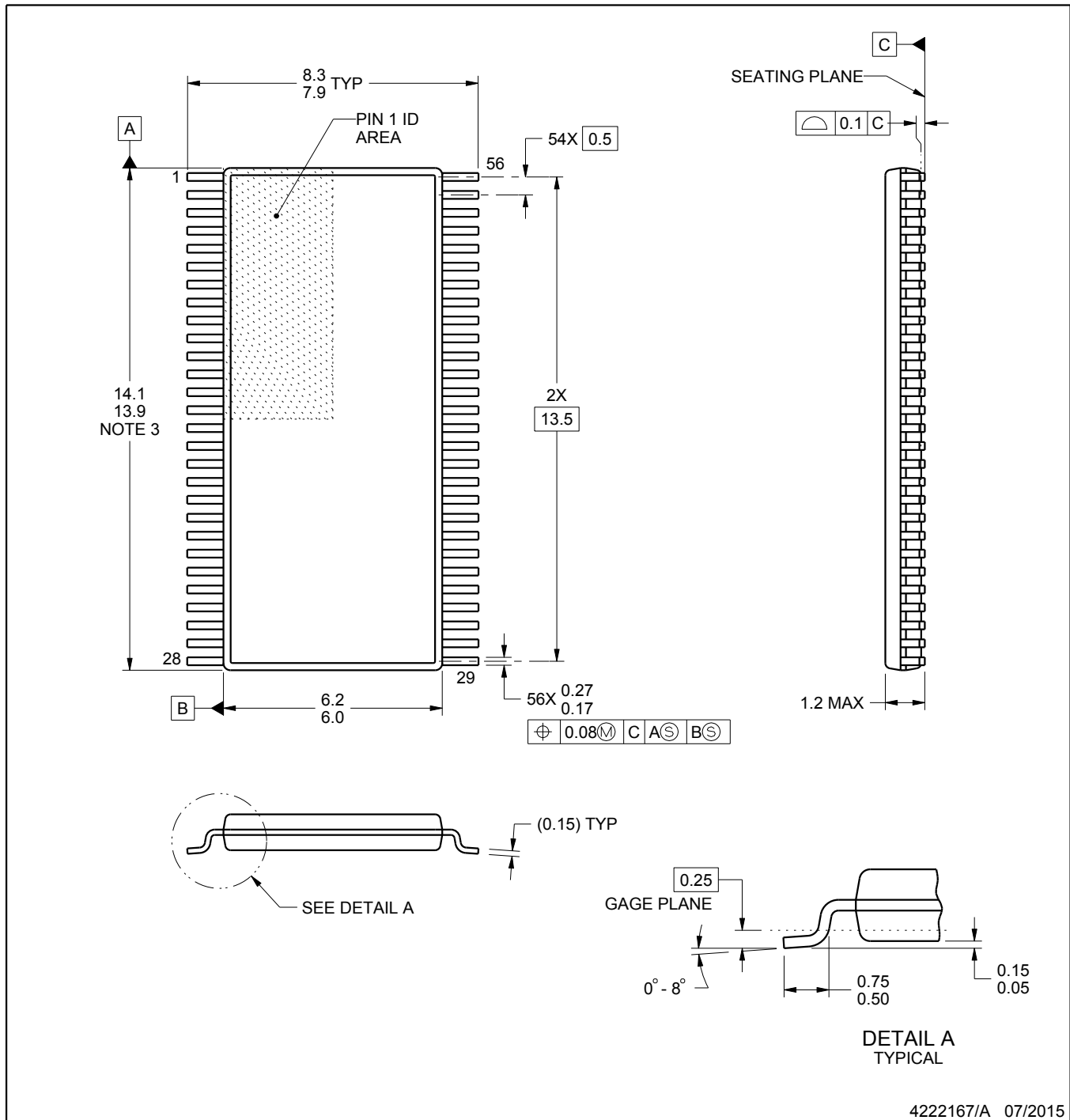


## PACKAGE OUTLINE

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

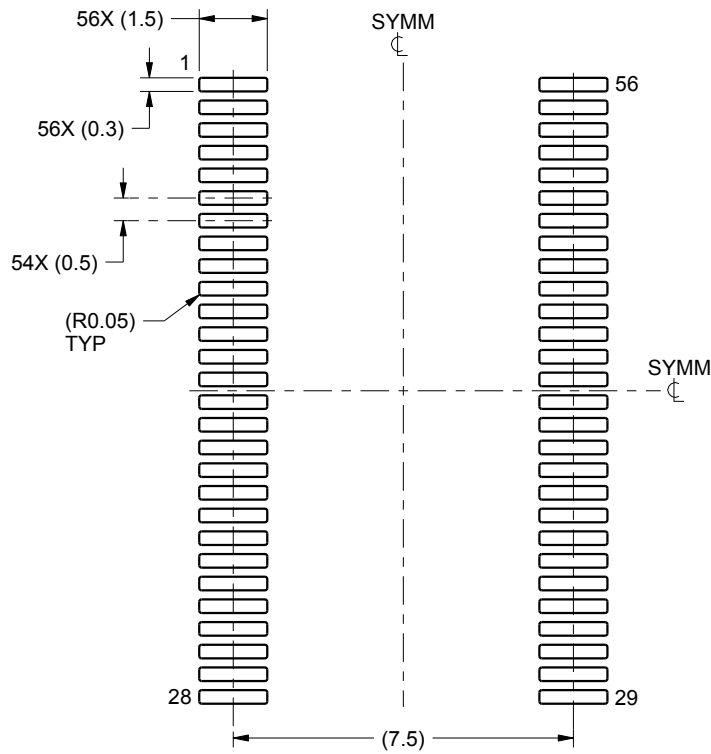


# EXAMPLE BOARD LAYOUT

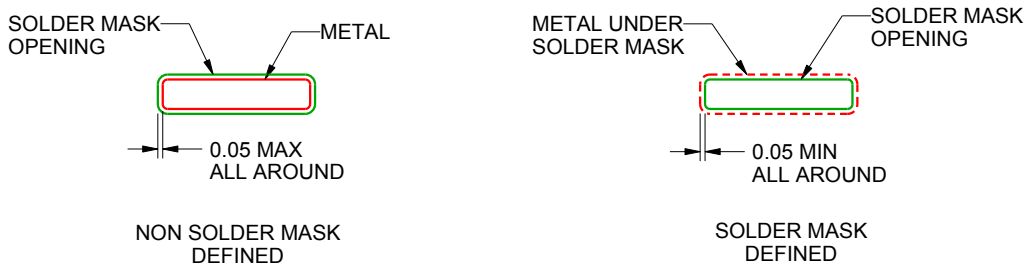
**DGG0056A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

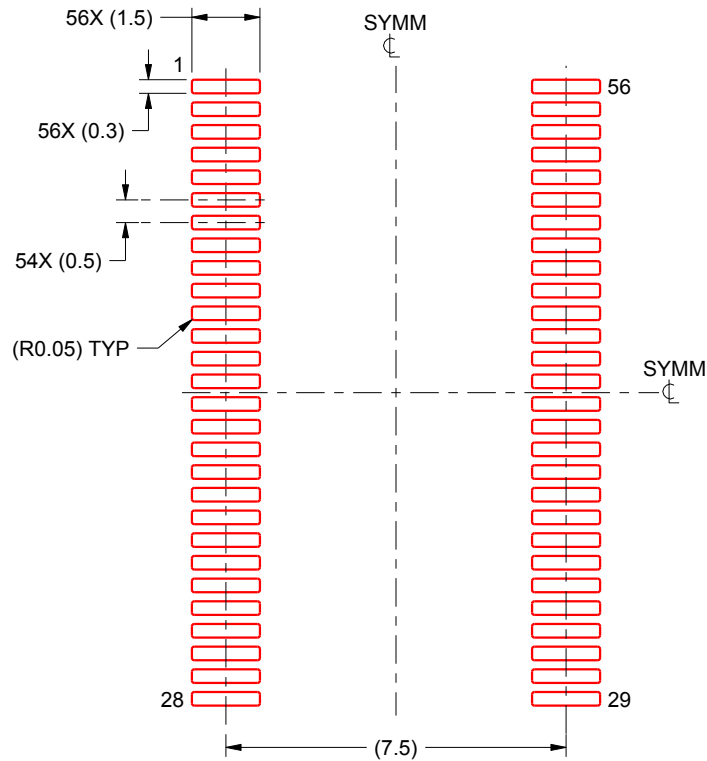
4222167/A 07/2015

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****DGG0056A****TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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