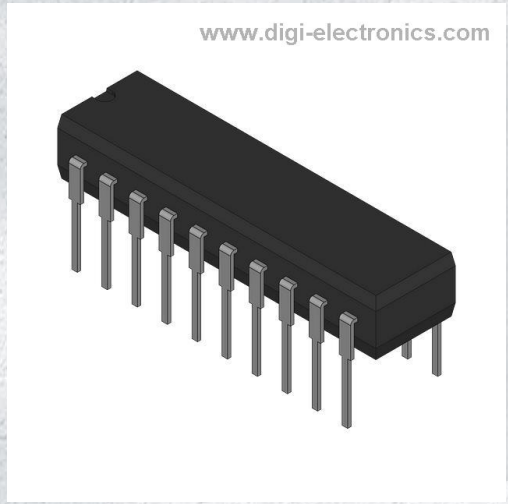
# SNJ54F240J Datasheet




| | |
|---|---|
| DiGi Electronics Part Number | SNJ54F240J-DG |
| Manufacturer | Texas Instruments |
| Manufacturer Product Number | SNJ54F240J |
| Description | 54F240 OCTAL BUFFERS/DRIVERS WIT |
| Detailed Description | Buffer, Inverting 2 Element 4 Bit per Element 3-State Output 20-CDIP |

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| SNJ54F240J | Texas Instruments |
| Series: | Product Status: |
| 54F | Active |
| Logic Type: | Number of Elements: |
| Buffer, Inverting | 2 |
| Number of Bits per Element: | Input Type: |
| 4 | - |
| Output Type: | Current - Output High, Low: |
| 3-State | 12mA, 48mA |
| Voltage - Supply: | Operating Temperature: |
| 4.5V ~ 5.5V | -55°C ~ 125°C (TA) |
| Mounting Type: | Package / Case: |
| Through Hole | 20-CDIP (0.300", 7.62mm) |
| Supplier Device Package: | Base Product Number: |
| 20-CDIP | 54F240 |

## Environmental & Export classification

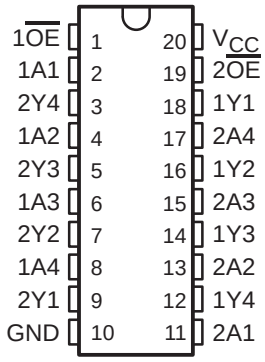
| ECCN: | HTSUS: |
| --- | --- |
| EAR99 | 8542.39.0001 |

# SN54F240, SN74F240
# OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

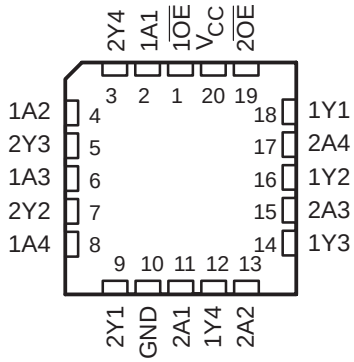
SDFS061A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

**SN54F240 . . . J PACKAGE**
**SN74F240 . . . DB, DW, OR N PACKAGE**
**(TOP VIEW)**




**SN54F240 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the ′F241 and ′F244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The ′F240 is organized as two 4-bit buffers/line drivers with separate output enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74F240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F240 is characterized for operation from 0°C to 70°C.

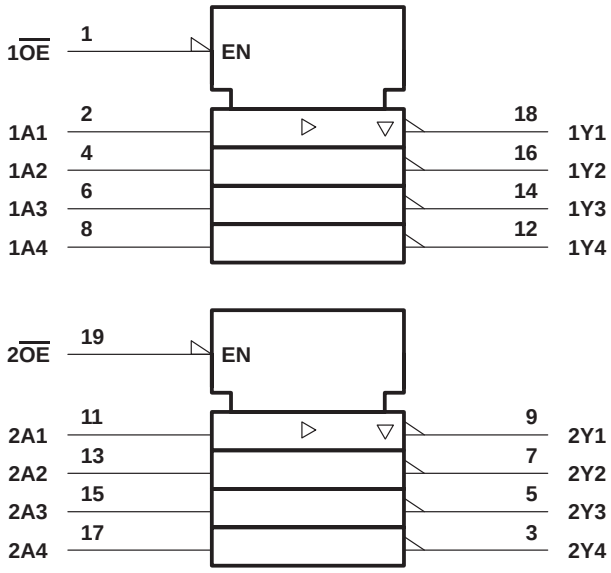
**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

# SN54F240, SN74F240
# OCTAL BUFFERS/DRIVERS
# WITH 3-STATE OUTPUTS

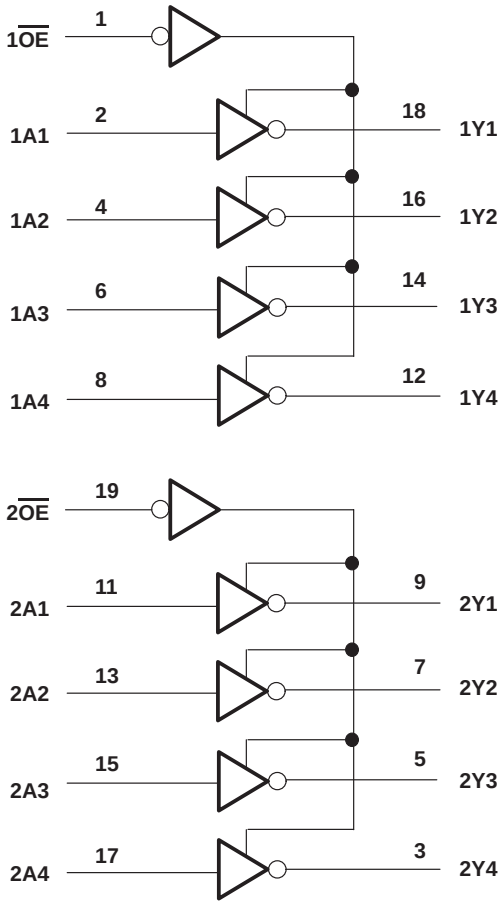
SDFS061A – D2932, MARCH 1987 – REVISED OCTOBER 1993

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to $V_{CC}$
Current into any output in the low state: SN54F240 . . . . . 96 mA
SN74F240 . . . . . 128 mA
Operating free-air temperature range: SN54F240 . . . . . –55°C to 125°C
SN74F240 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F240 | | | SN74F240 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | – 12 | | | – 15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F240 | | | SN74F240 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = – 12 mA | 2 | 3.2 | | | | | |
| | | $I_{OH}$ = – 15 mA | | | | 2 | 3.1 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | V |
| | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | | –50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 1 | | | – 1 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –100 | | –225 | –100 | | –225 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 19 | 29 | | 19 | 29 | mA |
| | | Outputs low | | 50 | 75 | | 50 | 75 | |
| | | Outputs disabled | | 42 | 63 | | 42 | 63 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | ′F240 | | | SN54F240 | | SN74F240 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any A | Y | 2.2 | 4.7 | 7 | 2.2 | 9 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 1.2 | 3.1 | 4.7 | 1.2 | 6 | 1.2 | 5.7 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.2 | 3.1 | 5.3 | 1.2 | 6.7 | 1.2 | 6.1 | ns |
| $t_{PZL}$ | | | 3.2 | 6.5 | 9 | 3.2 | 10.5 | 3.2 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.2 | 3.6 | 5.3 | 1.2 | 6.5 | 1.2 | 6.3 | ns |
| $t_{PLZ}$ | | | 1.2 | 5.6 | 8 | 1.2 | 12.5 | 1.2 | 9.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS

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# PACKAGE OPTION ADDENDUM

3-Dec-2024

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9758501Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758501Q2A SNJ54F 240FK | Samples |
| 5962-9758501QRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758501QRA SNJ54F240J | Samples |
| 5962-9758501QSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758501QSA SNJ54F240W | Samples |
| JM38510/33201B2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 33201B2A | Samples |
| JM38510/33201BRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 33201BRA | Samples |
| JM38510/33201BSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 33201BSA | Samples |
| M38510/33201B2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 33201B2A | Samples |
| M38510/33201BRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 33201BRA | Samples |
| M38510/33201BSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 33201BSA | Samples |
| SN54F240J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54F240J | Samples |
| SN74F240DW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | F240 | |
| SN74F240DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F240 | Samples |
| SN74F240N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74F240N | Samples |
| SN74F240NSR | ACTIVE | SOP | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74F240 | Samples |
| SNJ54F240FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758501Q2A SNJ54F 240FK | Samples |

# PACKAGE OPTION ADDENDUM



| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54F240J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758501QR A SNJ54F240J | Samples |
| SNJ54F240W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758501QS A SNJ54F240W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN54F240, SN74F240 :**

- Catalog : SN74F240
- Military : SN54F240

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

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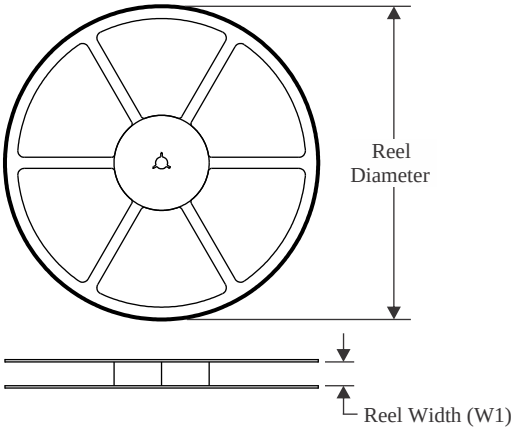
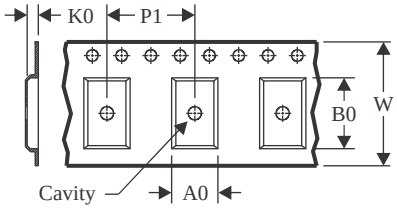
7-Dec-2024

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

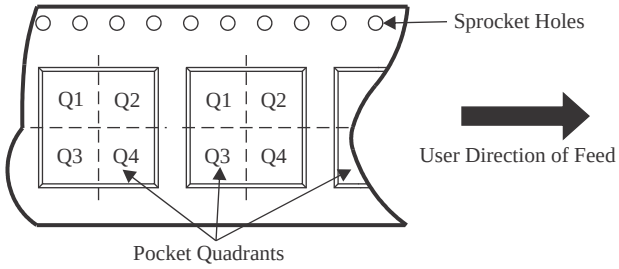



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



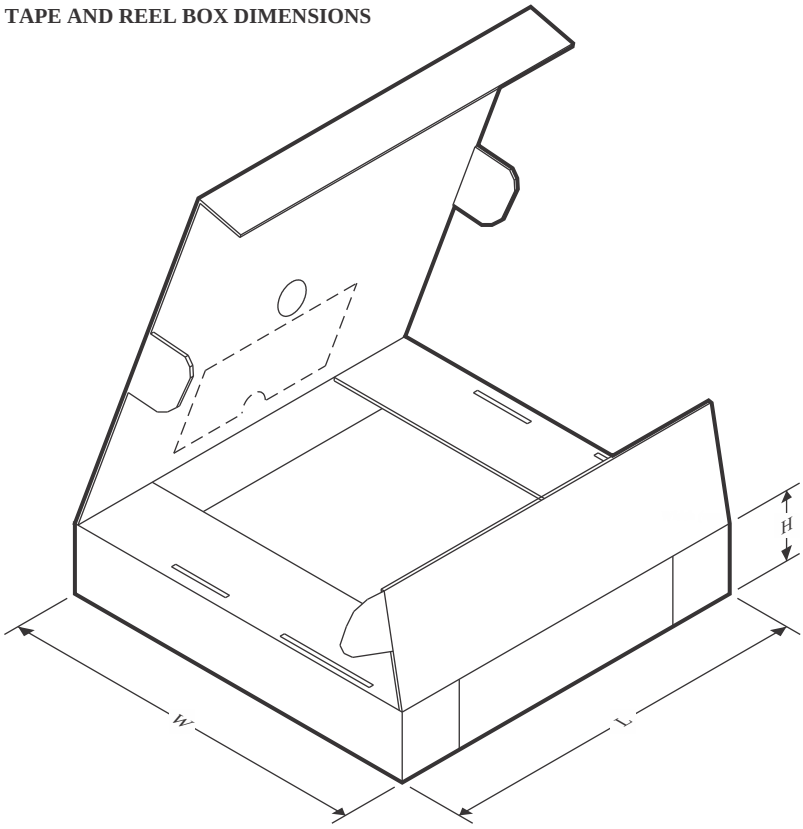

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74F240DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74F240NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

# PACKAGE MATERIALS INFORMATION



**TAPE AND REEL BOX DIMENSIONS**



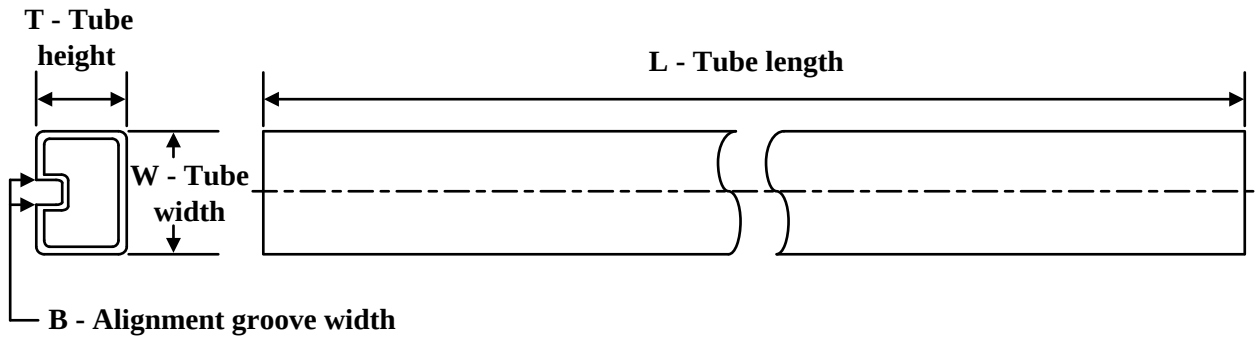

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74F240DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74F240NSR | SOP | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

# PACKAGE MATERIALS INFORMATION



## TUBE



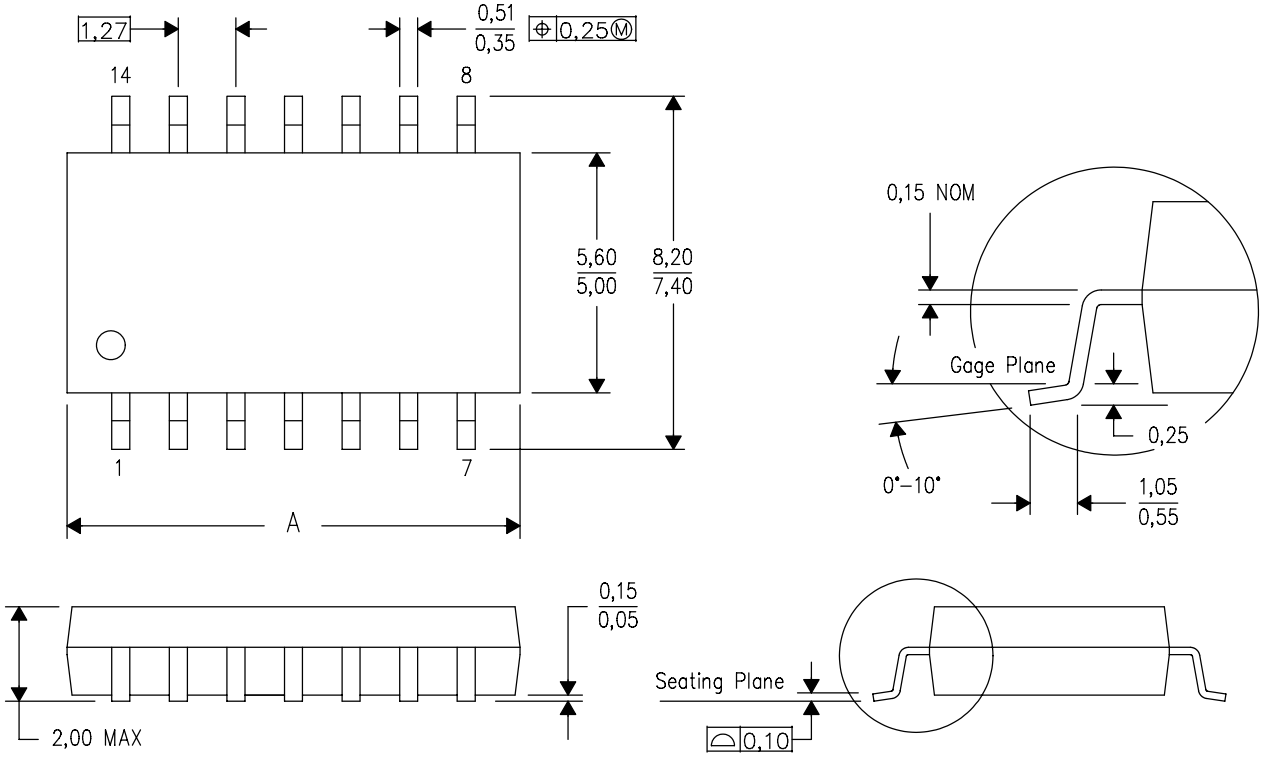

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9758501Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9758501QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/33201B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/33201BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/33201B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/33201BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74F240N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54F240FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54F240W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



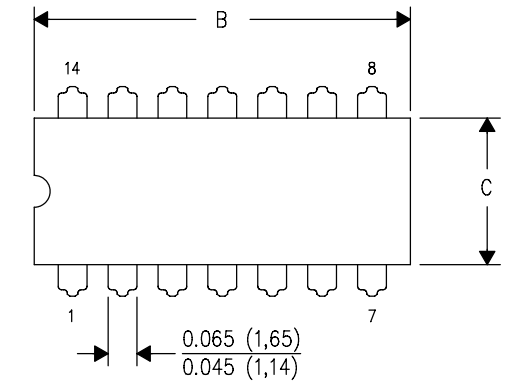

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

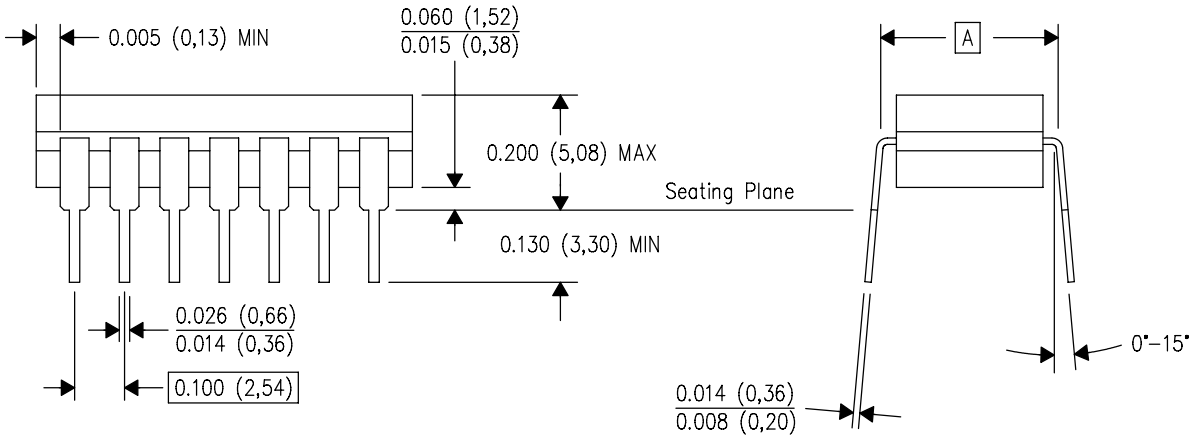
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

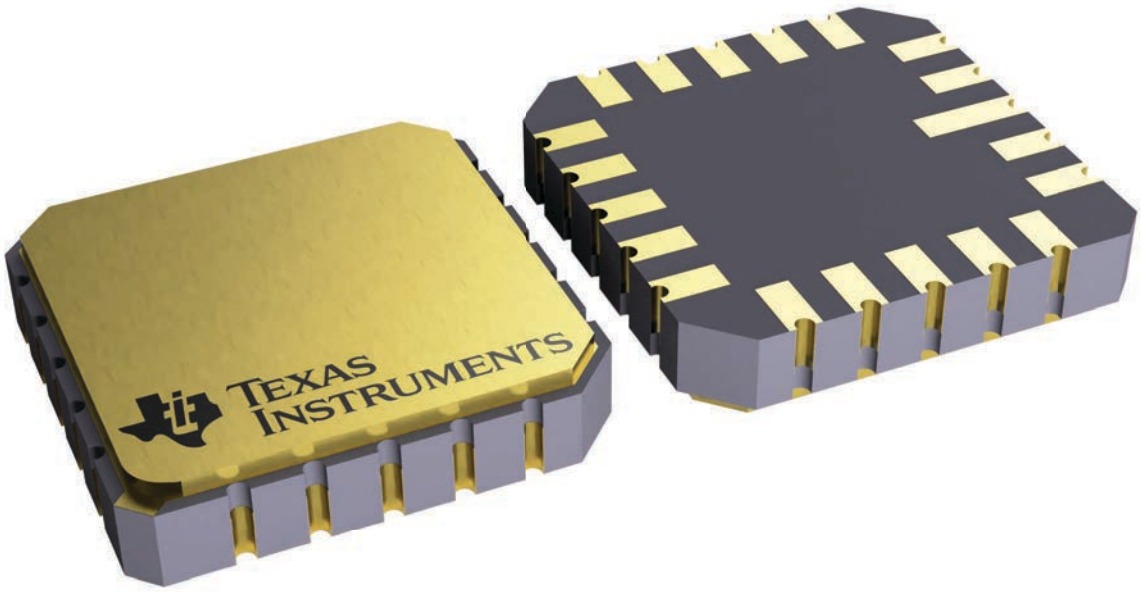
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



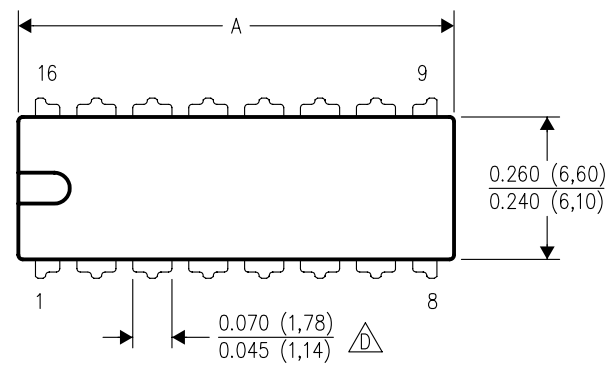

4229370VA\

**MECHANICAL DATA**

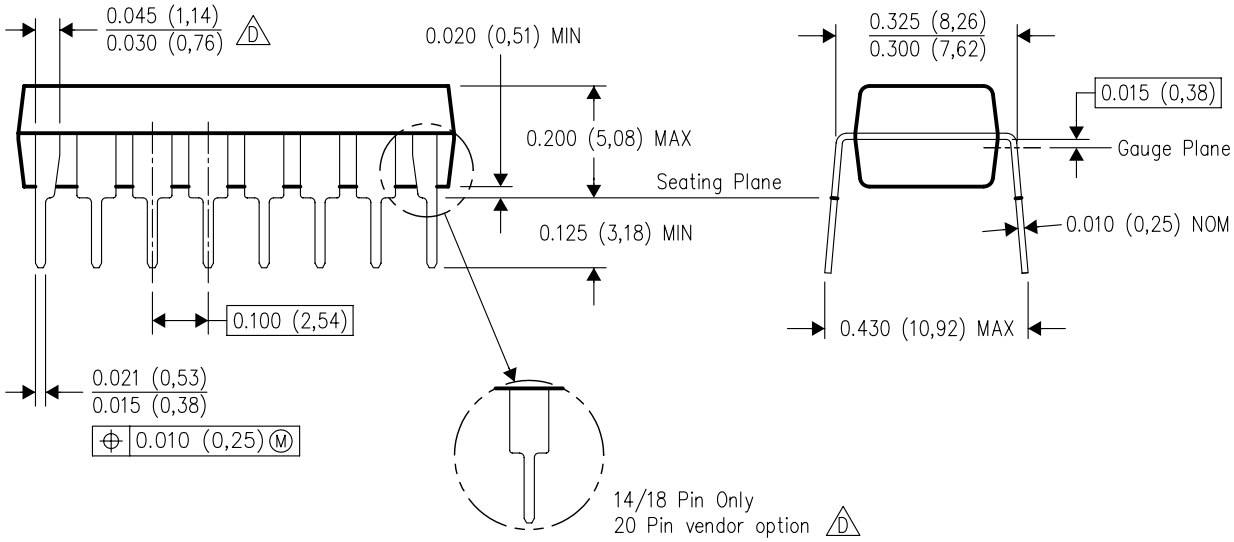
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

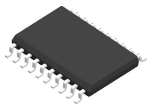



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

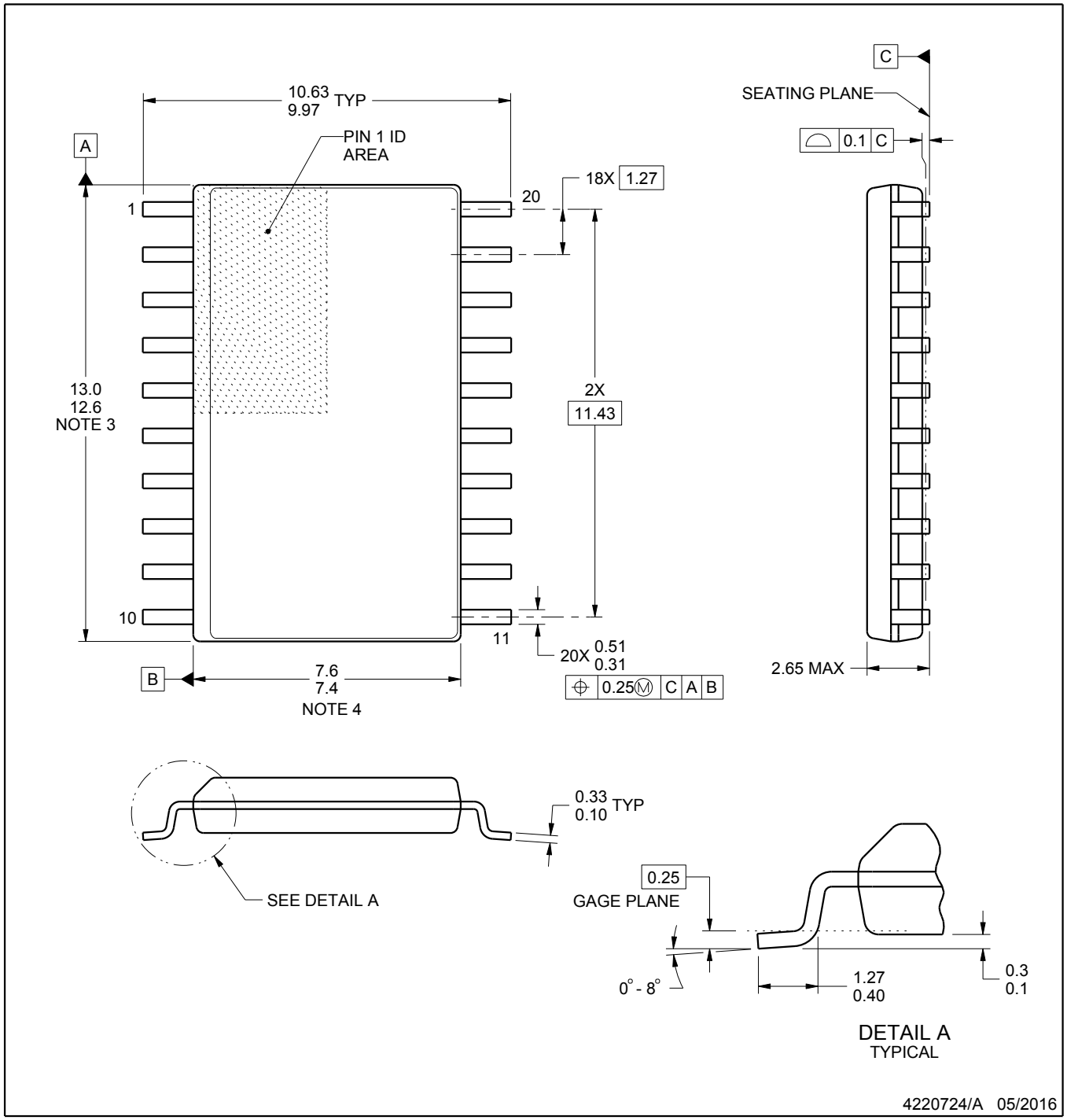


# PACKAGE OUTLINE

## DW0020A

## SOIC - 2.65 mm max height

SOIC




NOTES:

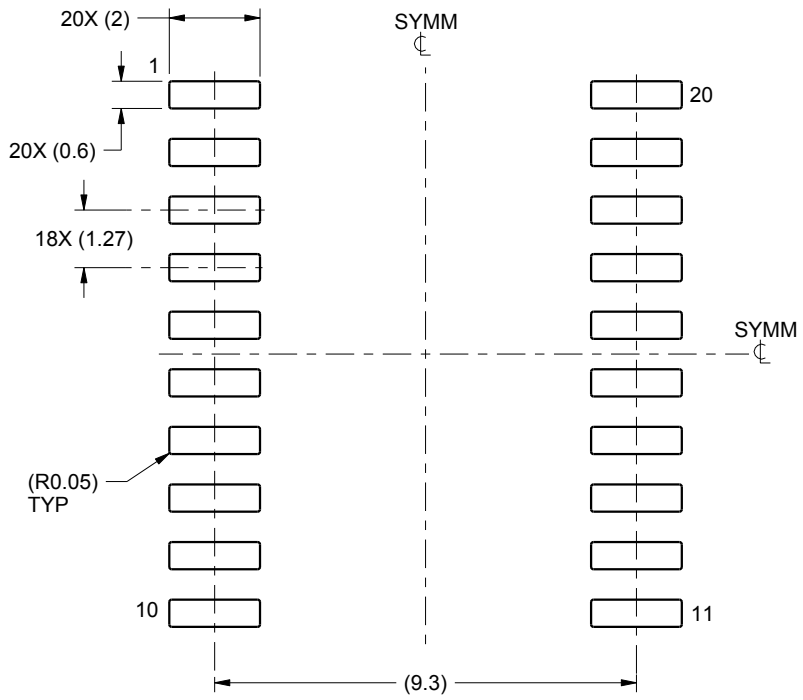
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

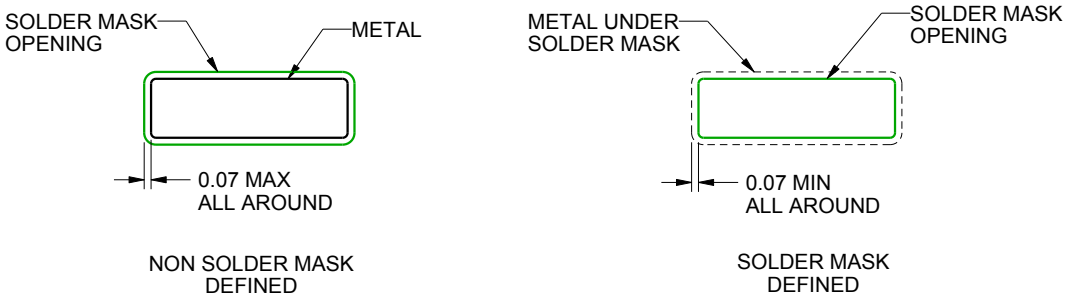
## DW0020A

## SOIC - 2.65 mm max height

SOIC




LAND PATTERN EXAMPLE
SCALE:6X




SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

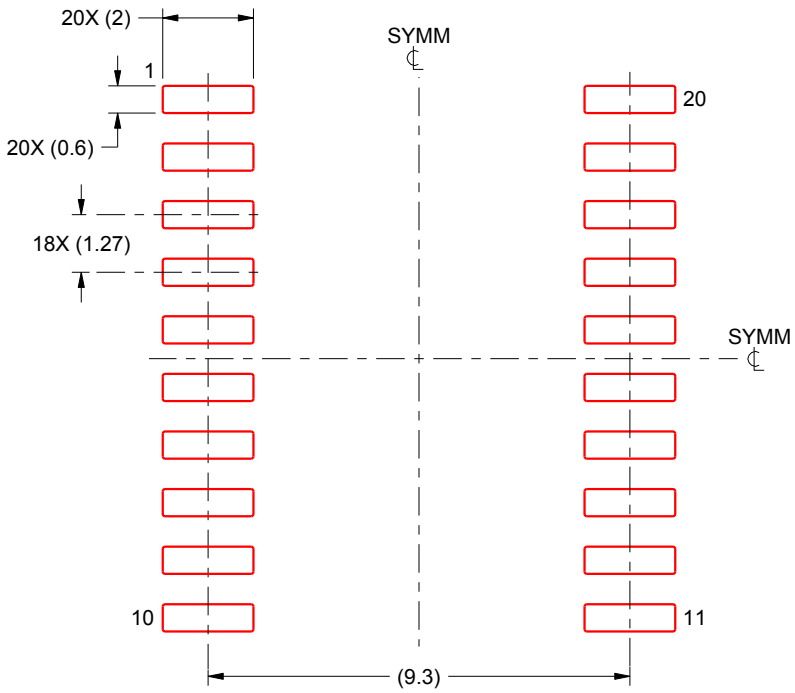
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DW0020A

## SOIC - 2.65 mm max height

SOIC




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

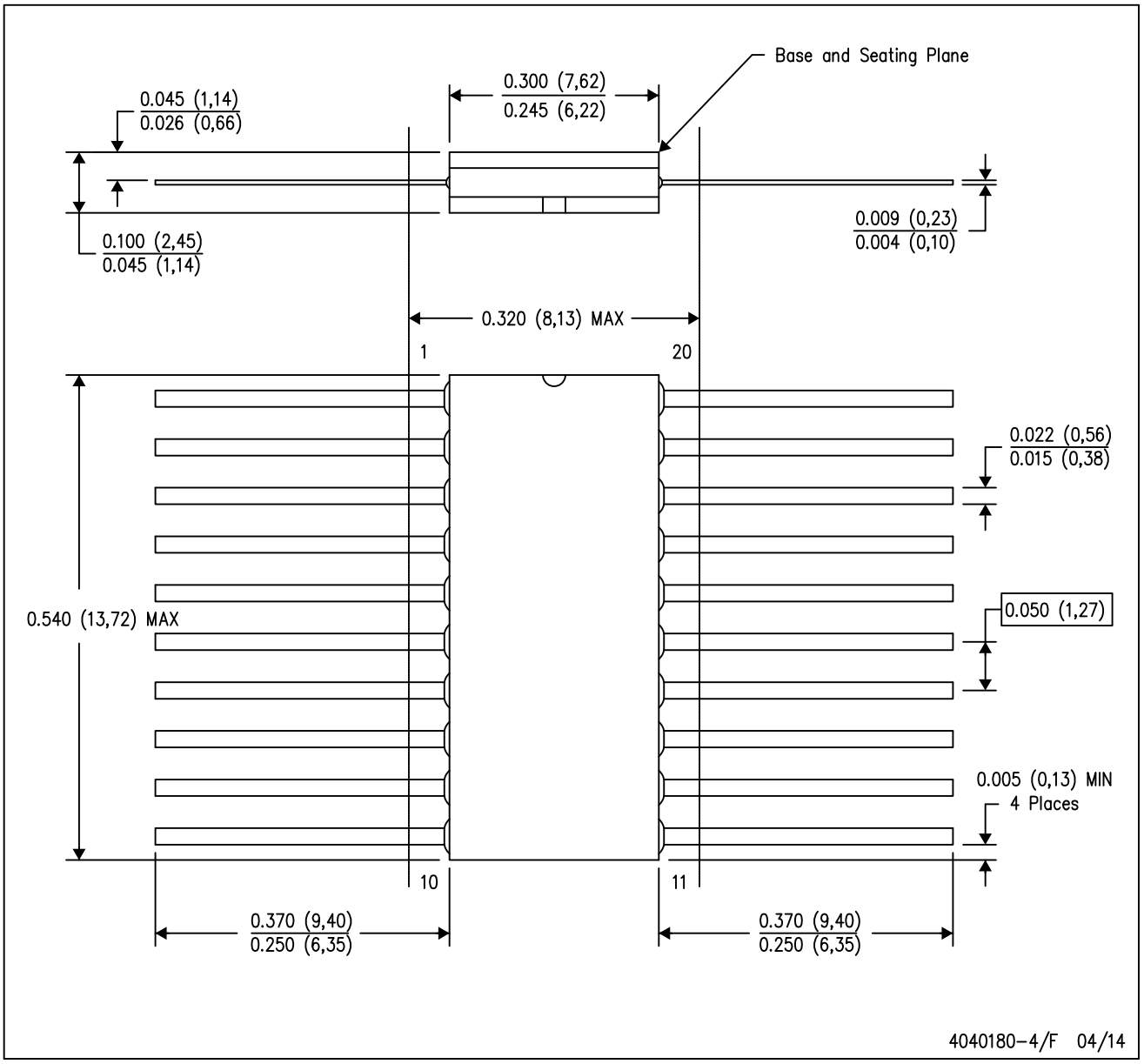
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**MECHANICAL DATA**

W (R–GDFP–F20) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

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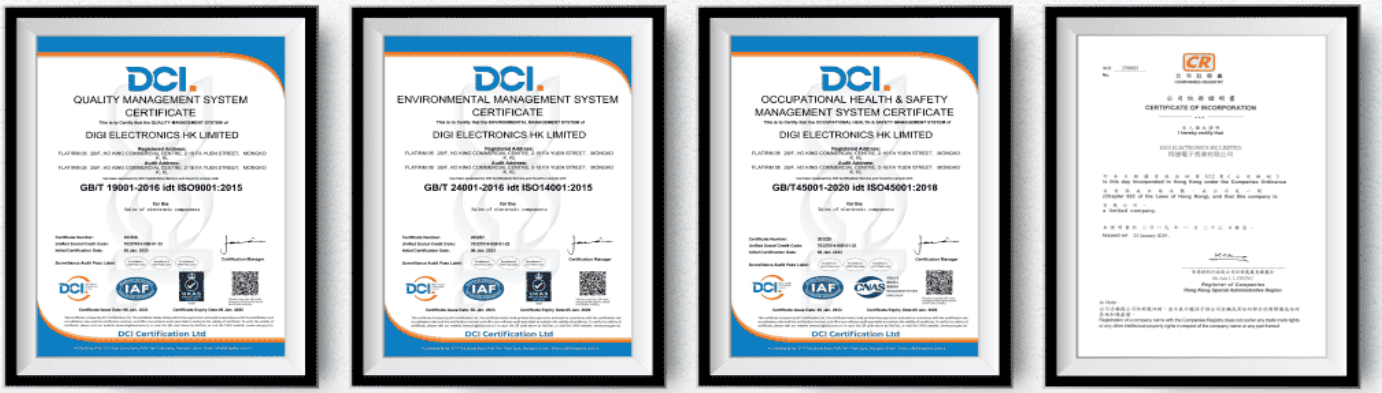



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