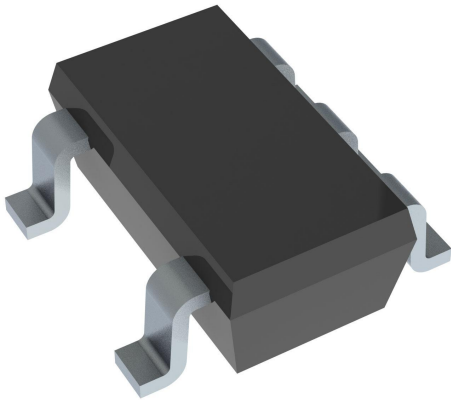


TL331MDBVTEP Datasheet

www.digi-electronics.com



TL331MDBVTEP

<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	TL331MDBVTEP-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	TL331MDBVTEP
Description	IC COMPARATOR 1 GEN PUR SOT23-5
Detailed Description	Comparator General Purpose Open-Collector, Rail-to-Rail SOT-23-5



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

TL331MDBVTEP

Series:

-

Type:

General Purpose

Output Type:

Open-Collector, Rail-to-Rail

Voltage - Input Offset (Max):

5mV

Current - Output (Typ):

-

CMRR, PSRR (Typ):

-

Hysteresis:

-

Package / Case:

SC-74A, SOT-753

Supplier Device Package:

SOT-23-5

Manufacturer:

Texas Instruments

Product Status:

Active

Number of Elements:

1

Voltage - Supply, Single/Dual (\pm):

2V ~ 36V, \pm 1V ~ 18V

Current - Input Bias (Max):

0.25 μ A @ 5V

Current - Quiescent (Max):

700 μ A

Propagation Delay (Max):

-

Operating Temperature:

-55°C ~ 125°C

Mounting Type:

Surface Mount

Base Product Number:

TL331

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

SINGLE DIFFERENTIAL COMPARATOR

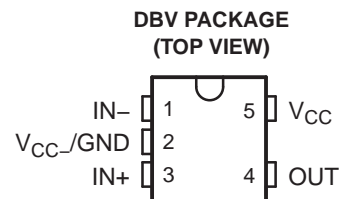
Check for Samples: [TL331-EP](#)

FEATURES

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage: 2 V to 36 V
- Low Supply-Current Drain Independent of Supply Voltage: 0.4 mA Typ.
- Low Input Bias Current: 25 nA Typ.
- Low Input Offset Voltage: 2 mV Typ.
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ± 36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military (-55°C to 125°C) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



DESCRIPTION/ORDERING INFORMATION

This device consists of a single voltage comparator designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible if the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. To achieve wired-AND relationships, one can connect the output to other open-collector outputs.

ORDERING INFORMATION⁽¹⁾

T_A	$V_{IO(MAX)}$ at 25°C	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-55°C to 125°C	5 mV	SOT-23 (DBV)	Reel of 250	TL331MDBVTEP	TEPU	V62/13611-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

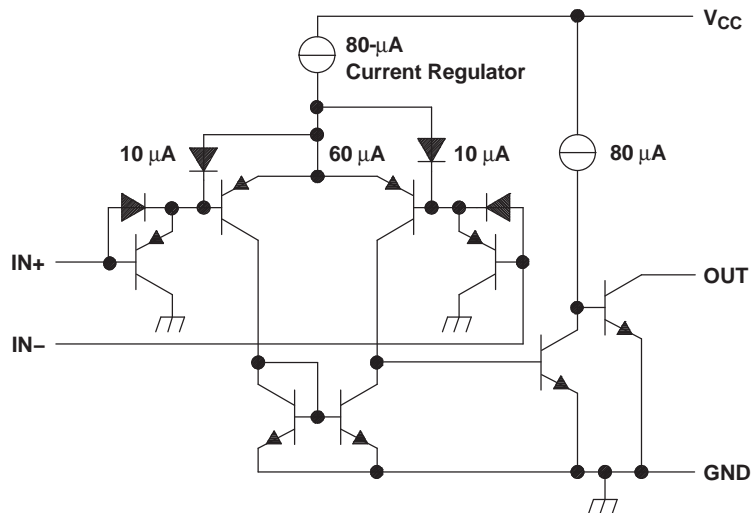


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM



SCHEMATIC



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Note: Current values shown are nominal.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage ⁽²⁾	36 V
V_{ID}	Differential input voltage ⁽³⁾	± 36 V
V_I	Input voltage range (either input)	-0.3 V to 36 V
V_O	Output voltage	36 V
I_O	Output current	20 mA
	Duration of output short-circuit to ground ⁽⁴⁾	Unlimited
T_J	Operating virtual junction temperature	150°C
T_{stg}	Storage temperature range	-65°C to 150°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TL331-EP		UNITS
		DBV		
		5 PINS		
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	299		°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	65.4		
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	97.1		
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.8		
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	95.5		
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC} = 5\text{ V}$ to 30 V , $V_O = 1.4\text{ V}$, $V_{IC} = V_{IC(min)}$	25°C		2	5	mV
			–55°C to 125°C			9	
I_{IO}	Input offset current	$V_O = 1.4\text{ V}$	25°C		5	50	nA
			–55°C to 125°C			250	
I_{IB}	Input bias current	$V_O = 1.4\text{ V}$	25°C		–25	–250	nA
			–55°C to 125°C			–400	
V_{ICR}	Common-mode input voltage range ⁽²⁾		25°C		0 to $V_{CC} - 1.5$		V
			–55°C to 125°C		0 to $V_{CC} - 2$		
A_{VD}	Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V}$ to 11.4 V , $R_L \geq 15\text{ k}\Omega$ to V_{CC}	25°C		50	200	V/mV
I_{OH}	High-level output current	$V_{OH} = 5\text{ V}$, $V_{ID} = 1\text{ V}$ $V_{OH} = 30\text{ V}$, $V_{ID} = 1\text{ V}$	25°C		0.1	50	nA
			–55°C to 125°C			1	μA
V_{OL}	Low-level output voltage	$I_{OL} = 4\text{ mA}$, $V_{ID} = -1\text{ V}$	25°C		150	400	mV
			–55°C to 125°C			700	
I_{OL}	Low-level output current	$V_{OL} = 1.5\text{ V}$, $V_{ID} = -1\text{ V}$	25°C		6		mA
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 5\text{ V}$	25°C		0.4	0.7	mA

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$, but either or both inputs can go to 30 V without damage.

SWITCHING CHARACTERISTICS $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}$ ^{(1) (2)}	100-mV input step with 5-mV overdrive	1.3
		TTL-level input step	0.3

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL331MDBVTEP	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU
TL331MDBVTEP.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU
V62/13611-01XE	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TL331-EP :

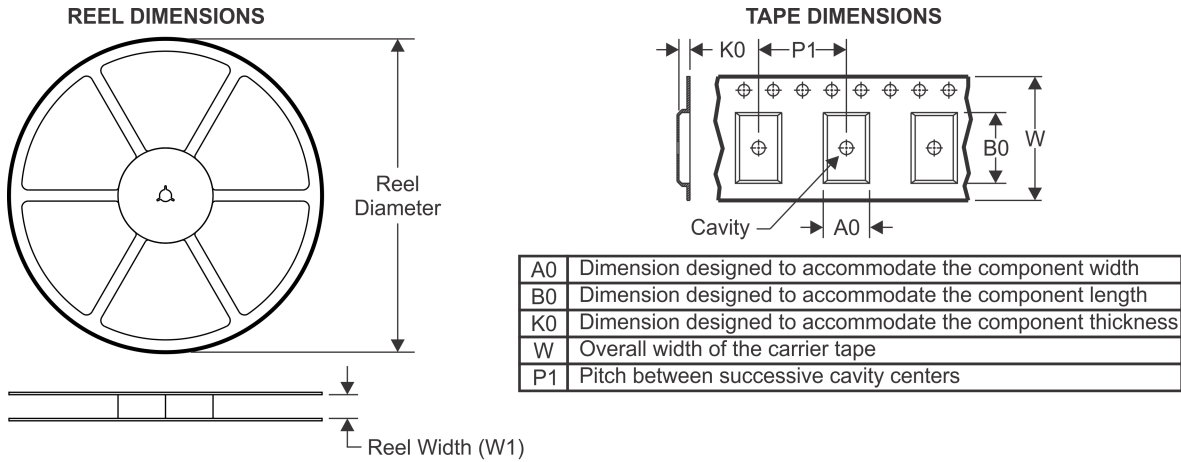
- Catalog : [TL331](#)

- Automotive : [TL331-Q1](#)

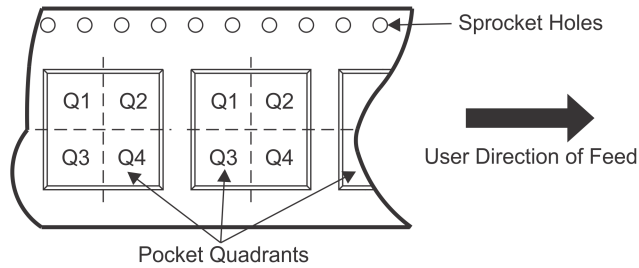
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



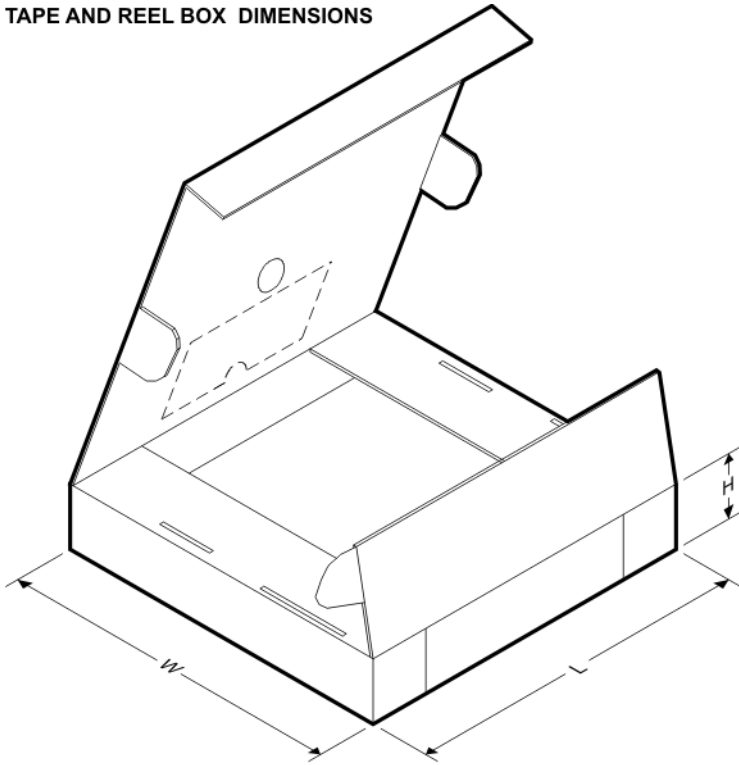
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL331MDBVTEP	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

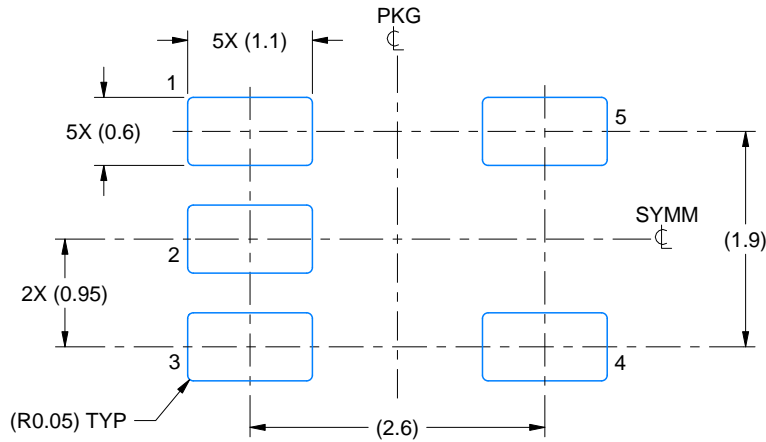
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL331MDBVTEP	SOT-23	DBV	5	250	200.0	183.0	25.0

EXAMPLE BOARD LAYOUT

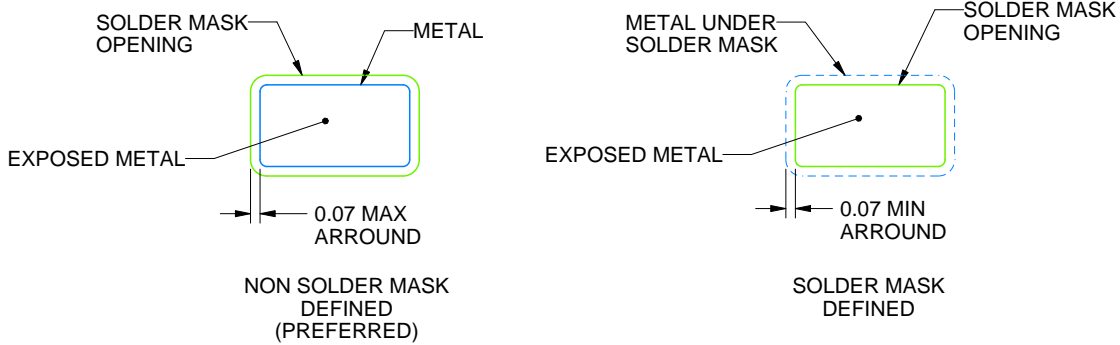
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

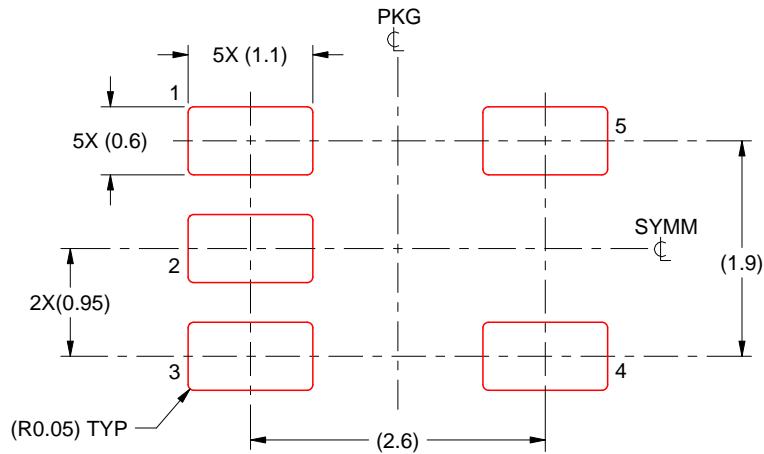
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:15X

4214839/K 08/2024

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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