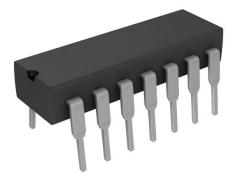


## **TLC25L4BCN Datasheet**

www.digi-electronics.com



DiGi Electronics Part Number	TLC25L4BCN-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	TLC25L4BCN
Description	IC CMOS 4 CIRCUIT 14DIP
Detailed Description	CMOS Amplifier 4 Circuit Single-Ended 14-PDIP

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### Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
TLC25L4BCN	Texas Instruments
Series:	Product Status:
LinCMOS™	Obsolete
Amplifier Type:	Number of Circuits:
CMOS	4
Output Type:	Slew Rate:
Single-Ended	0.04V/µs
Gain Bandwidth Product:	Current - Input Bias:
110 kHz	0.2 pA
Voltage - Input Offset:	Current - Supply:
340 µV	2.7mA (x4 Channels)
Voltage - Supply Span (Min):	Voltage - Supply Span (Max):
1.4 V	16 V
Operating Temperature:	Mounting Type:
0°C ~ 70°C	Through Hole
Package / Case:	Supplier Device Package:
14-DIP (0.300", 7.62mm)	14-PDIP
Base Product Number:	
TLC25L4	

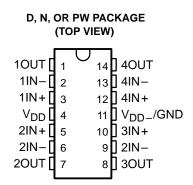
### **Environmental & Export classification**

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.33.0001	

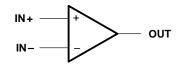
- A-Suffix Versions Offer 5-mV VIO
- B-Suffix Versions Offer 2-mV V<sub>IO</sub>
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise ... 25 nV/\(\vee{Hz}\) Typ at f = 1 kHz (High-Bias Version)

#### description

The TLC254, TLC254A, TLC254B, TLC25L4, TLC254L4A, TLC254L4B, TLC25M4, TLC25M4A and TL25M4B are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS<sup>™</sup>



symbol (each amplifier)



process, giving them stable input-offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for these devices include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices.

		Availabl	e options			
	Viemov	PAC	CHIP FORM			
	V <sub>IO</sub> max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	(Y)	
	10 mV	TLC254CD	TLC254CN	TLC254CPW	TLC254Y	
	5 mV	TLC254ACD	TLC254ACN	—	—	
	2 mV	TLC254BCD	TLC254BCN	—	—	
0°C to 70°C	10 mV	TLC25L4CD	TLC25L4CN	TLC25L4CPW	TLC25L4Y	
	5 mV	TLC25L4ACD	TLC25L4ACN	—	—	
	2 mV	TLC25L2BCD	TLC25L4BCN	—	—	
	10 mV	TLC25M4CD	TLC25M4CN	TLC25M4CPW	TLC25M4Y	
	5 mV	TLC25M4ACD	TLC25M4ACN	—	—	
	2 mV	TLC25M4BCD	TLC25M4BCN	—	—	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC254CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



#### description (continued)

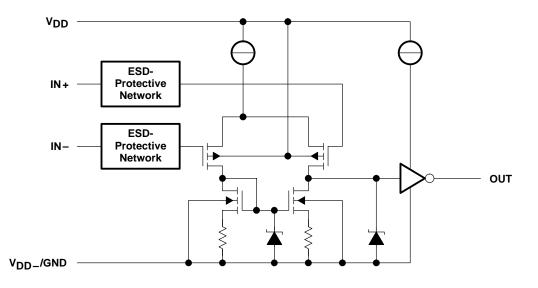
General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with these devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. These devices are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic dip and the small-outline packages. The device is also available in chip form.

These devices are characterized for operation from 0°C to 70°C.

	DEVICE FEATURES	-	-
PARAMETER	TLC25L4_C (LOW BIAS)	TLC25M4_C (MEDIUM BIAS)	TLC254_C (HIGH BIAS)
Supply current (Typ)	40 µA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μA	0.6 V/μA	4.5 V/μA
Input offset voltage (Max) TLC254C, TLC25L4C, TLC25M4C TLC254AC, TLC25L4AC, TLC25M4AC TLC254BC, TLC25L4BC, TLC25M4BC	10 mV 5 mV 2 mV	10 mV 5 mV 2 mV	10 mV 5 mV 2 mV
Offset voltage drift (Typ)	0.1 $\mu$ V/month <sup>†</sup>	0.1 μV/month <sup>†</sup>	0.1 $\mu$ V/month <sup>†</sup>
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

<sup>†</sup> The long-term drift value applies after the first month.

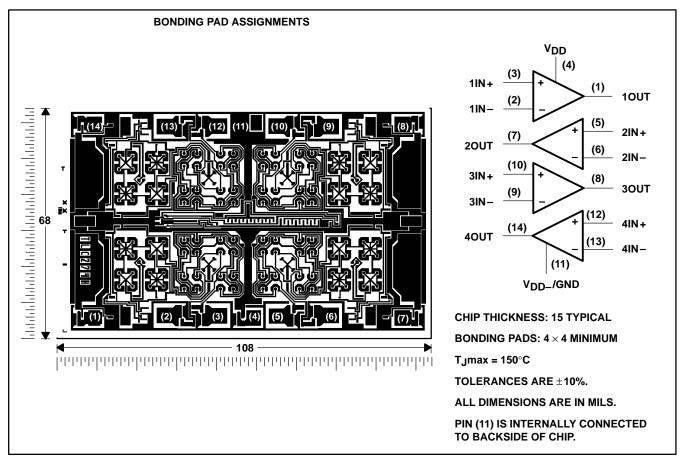
#### equivalent schematic (each amplifier)





#### chip information

These chips, when properly assembled, display characteristics similar to the TLC25\_4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>DD</sub> (see Note 1)	18 V
Differential input voltage (see Note 2)	
Input voltage range (any input)	0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	. See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to VDD-/GND.

2. Differential voltages are at IN+, with respect to IN-.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE									
PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING						
D	725 mW	5.8 mW/°C	464 mW						
N	1050 mW	9.2 mW/°C	736 mW						
PW	700 mW	5.6 mW/°C	448 mW						

#### DISSIPATION RATING TABLE

#### recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V <sub>DD</sub>		1.4	16	V
Common-mode input voltage, $V_{IC}$ $V_{DD} = 1.4 V$ $V_{DD} = 5 V$ $V_{DD} = 10 V$ $V_{DD} = 16 V$	$V_{DD} = 1.4 V$	0	0.2	
	$V_{DD} = 5 V$	-0.2	4	V
		-0.2	9	v
	-0.2	14		
Operating free-air temperature, $T_A$		0	70	°C



TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS <sup>™</sup> QUAD OPERATIONAL AMPLIFIERS SLOS003G – JUNE 1983 – REVISED MARCH 2001
TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC2 TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC2 LinCMOS <sup>TM</sup> QUAD OPERATIONAL AMPLIF

		PARAMETER		st   TA		.C254_C	:	TLC25L4_C			TLC25M4_C			UNIT
	PARAMETER		TEST CONDITIONS <sup>†</sup>	TA	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	TLC25_4C		25°C			10			10			10		
	VIO Input offset voltage	12025_40		0°C to 70°C			12			12			12	
Vio		TLC25 4AC	$V_{O} = 0.2 V, R_{S} = 50 \Omega$	25°C			5			5			5	mV
٩O	input onset voltage	16020_4A0	$V_0 = 0.2 V, V_0 = 30 S_2$	0°C to 70°C			6.5			6.5			6.5	IIIV
aVIO <sup>4</sup> ii IIO II IIB II VICR C VOM F AVD L a		TLC25_4BC		25°C			2			2			2	
		16623_460		0°C to 70°C			3			3			3	
aVIO	Average temperature input offset voltage	coefficient of		25°C to 70°C		1			1			1		μV/°C
1			N- 00V	25°C		1	60		1	60		1	60	- 4
NO	Input offset current		$V_{O} = 0.2 V$	0°C to 70°C			300			300			300	pА
lun.	Input bias current		$\lambda = 0.2 \lambda$	25°C		1	60		1	60		1	60	54
чВ	input bias current		V <sub>O</sub> = 0.2 V	0°C to 70°C			600			600			600	рА
VICR	Common-mode input	voltage range		25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
VOM	Peak output voltage s	wing‡	V <sub>ID</sub> = 100 mV	25°C	450	700		450	700		450	700		mV
A <sub>VD</sub>	Large-signal differenti amplification	al voltage	$V_{O}$ = 100 to 300 mV, R <sub>S</sub> = 50 $\Omega$	25°C		10			20			20		V/mV
CMRR	Common-mode reject	tion ratio	V <sub>O</sub> = 0.2 V, V <sub>IC</sub> = V <sub>ICR</sub> min	25°C	60	77		60	77		60	77		dB
IDD	Supply current		$V_{O} = 0.2 V$ , No load	25°C		600	750		50	68		400	500	μA

#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 1.4 V (unless otherwise noted)

<sup>†</sup> All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: for low bias,  $R_L = 1 M\Omega$ , for medium bias  $R_L = 100 k\Omega$ , and for high bias  $R_L = 10 k\Omega$ . <sup>‡</sup> The output swings to the potential of  $V_{DD}$ -/GND.

#### operating characteristics, $V_{DD}$ = 1.4 V, $T_A$ = 25°C

	PARAMETER	TEST CONDITIONS	Т	LC254_0	C	TL	C25L4_	С	TL	C25M4_	С	UNIT
	FARAMETER TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	See Figure 1		0.1			0.001			0.01		V/µs
B <sub>1</sub>	Unity-gain bandwidth	$\begin{array}{lll} A_V = 40 \mbox{ dB}, & C_L = 10 \mbox{ pF}, \\ R_S = 50 \ \Omega, & See \mbox{ Figure 1} \end{array}$		12			12			12		kHz
	Overshoot factor	See Figure 1		30%			35%			35%		

#### electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	PARAMETER		TEST CONI	DITIONS	TAT	TLC254, TLC254AC, TLC254BC			UNIT
						MIN	TYP	MAX	
		TLC254C	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		TLC254C	R <sub>S</sub> = 50 Ω,	$R_L = 10 k\Omega$	Full range			12	
\/	Input offect velteres	TLC254AC	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	mV
VIO	Input offset voltage	TLC254AC	R <sub>S</sub> = 50 Ω,	$R_L = 10 k\Omega$	Full range			6.5	mv
		TLC254BC	V <sub>O</sub> = 1.4 V,	VIC = 0,	25°C		0.34	2	
		TLC204BC	R <sub>S</sub> = 50 Ω,	$R_L = 10 \ k\Omega$	Full range			3	
αΛΙΟ	Average temperature coeffici offset voltage	ent of input			25°C to 70°C		1.8		μV/°C
	hand affect summark (see Nicks	4)	N 0.5 V		25°C		0.1	60	
10	Input offset current (see Note	4)	V <sub>O</sub> = 2.5 V,	V <sub>IC</sub> = 2.5 V	70°C		7	300	pА
	land birth and the state	4)	N 0.5 V	N 05.V	25°C		0.6	60	
IΒ	Input bias current (see Note	4)	V <sub>O</sub> = 2.5 V,	VIC = 2.5 V	70°C		40	600	pА
,, Common-mode input volta		range			25°C	-0.2 to 4	-0.3 to 4.2		
VICR	R (see Note 5)				Full range	-0.2 to 3.5			V
	High-level output voltage		V <sub>ID</sub> = 100 mV,		0°C	3	3.8		v
Vон				$R_L = 10 \ k\Omega$	25°C	3.2	3.8		
					70°C	3	3.8		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
					0°C	4	27		
AVD	Large-signal differential volta amplification	ge	$V_{O} = 0.25 V$ to 2 V,	$R_L = 10 \ k\Omega$	25°C	5	23		V/mV
	ampinioadon				70°C	4	20		
					0°C	60	84		
CMRR	Common-mode rejection ratio	)	$V_{IC} = V_{ICR}min$		25°C	65	80		dB
					70°C	60	85		
					0°C	60	94		
<b>k</b> SVR	Supply-voltage rejection ratio	$(\Delta V_{DD}/\Delta V_{IO})$	$V_{DD}$ = 5 V to 10 V,	V <sub>O</sub> = 1.4 V	25°C	65	95		dB
					70°C	60	96		
			V <sub>O</sub> = 2.5 V,	V <sub>IC</sub> = 2.5 V,	0°C		3.1	7.2	
IDD	Supply current (four amplifier	s)	$v_0 = 2.5 v$ , No load	vIC = 2.5 V,	25°C		2.7	6.4	mA
					70°C		2.3	5.2	

<sup>†</sup> Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



## TLC25L4BCN Texas Instruments IC CMOS 4 CIRCUIT 14DIP TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

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#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 10 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	TAT		C, TLC2 C254B		UNIT
						MIN	TYP	MAX	_
		TL 005 40	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		TLC254C	R <sub>S</sub> = 50 Ω,	$R_L = 10 k\Omega$	Full range			12	
Vie	Input offect voltage		V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	m\/
VIO	Input offset voltage	TLC254AC	R <sub>S</sub> = 50 Ω,	$R_L = 10 \ k\Omega$	Full range			6.5	mV
		TLC254BC	V <sub>O</sub> = 1.4 V,	VIC = 0,	25°C		0.39	2	
		1023460	R <sub>S</sub> = 50 Ω,	$R_L = 10 \text{ k}\Omega$	Full range			3	
∝VIO	Average temperature coeffi	cient of input			25°C to		2		μV/°C
NIO	offset voltage				70°C				μι, ο
١O	Input offset current (see No	ote 4)	V <sub>O</sub> = 5 V,	VIC = 5 V	25°C		0.1	60	рA
10	······································		.0,		70°C		7	300	<b>-</b>
IB	Input bias current (see Note	e 4)	V <sub>O</sub> = 5 V,	VIC = 5 V	25°C		0.7	60	рА
.ID		.,	.0,		70°C		50	600	P''
					0500	-0.2	-0.3		
	Common mode input volta				25°C	to 9	to 9.2		
VICD	Common-mode input voltage range (see Note 5)					-0.2	0.2		V
					Full range	to			
						8.5			
					0°C	7.8	8.5		
VOH	High-level output voltage		V <sub>ID</sub> = 100 mV,	$R_L = 10 \ k\Omega$	25°C	8	8.5		V
					70°C	7.8	8.4		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
		4.0.00			0°C	7.5	42		
AVD	Large-signal differential vol amplification	tage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 10 \ k\Omega$	25°C	10	36		V/mV
					70°C	7.5	32		
					0°C	60	88		
CMRR	Common-mode rejection ra	itio	$V_{IC} = V_{ICR}min$		25°C	65	85		dB
					70°C	60	88		
	Supply voltage rejection re-	i.			0°C	60	94		
ksvr	Supply-voltage rejection rat (ΔVDD/ΔVIO)	liu	$V_{DD} = 5 V$ to 10 V,	V <sub>O</sub> = 1.4 V	25°C	65	95		dB
					70°C	60	96		
			V <sub>O</sub> = 5 V,	V <sub>IC</sub> = 5 V,	0°C		4.5	8.8	
IDD	Supply current (four amplifi	ers)	No load	ν <sub>1</sub> C = 5 ν,	25°C		3.8	8	mA
					70°C		3.2	6.8	

<sup>†</sup> Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



#### operating characteristics, V<sub>DD</sub> = 5 V

	PARAMETER	Т	EST CONDITIO	NS	TA	TLC254C, TLC254AC, TLC254BC			UNIT
						MIN	TYP	MAX	
				VI(PP) = 1 V	0°C		4		
				VI(PP) = 1 V	25°C		3.6		
SR	Slew rate at unity gain	$R_L = 10 k\Omega$ ,	C <sub>L</sub> = 20 pF,	V <sub>I(PP)</sub> = 1 V	70°C	PC 3			V/µs
SK	Siew rate at unity gain	See Figure 1			0°C		3.1		v/µs
				VI(PP) = 2.5 V	25°C		2.9		
					70°C	2.5			
Vn	Equivalent input noise voltage	f = 1 kHz,	R <sub>S</sub> = 20 Ω,	See Figure 2	25°C		25		nV/√Hz
					0°C		340		
вом	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	C <sub>L</sub> = 20 pF,	R <sub>L</sub> = 10 kΩ,	25°C		320		kHz
		See Figure 1			70°C	260			
					0°C		2		
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV,	C <sub>L</sub> = 20 pF,	See Figure 1	25°C		1.7		MHz
					70°C		1.3		
			<i>,</i> , ,	0 00 5	0°C		47°		
φm	Phase margin	$V_I = 10 \text{ mV},  f = B_1,$		C <sub>L</sub> = 20 pF,	25°C		46°		
		See Figure 3			70°C		43°		

#### operating characteristics, $V_{DD} = 10 V$

	PARAMETER	т	EST CONDITIO	NS	Тд	TLC254 TL		UNIT	
						MIN	TYP	MAX	
					0°C		5.9		
				VI(PP) = 1 V	25°C		5.3		
SR	Slew rate at unity gain	$R_L = 10 k\Omega$ ,	C <sub>L</sub> = 20 pF,		70°C		4.3		V/µs
SK	Siew rate at unity gain	See Figure 1			0°C		5.1		v/µS
				VI(PP) = 5.5 V	25°C		4.6		
					70°C	3.8			
Vn	Equivalent input noise voltage	f = 1 kHz,	R <sub>S</sub> = 20 Ω,	See Figure 2	25°C		25		nV/√Hz
					0°C		220		
Вом	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	C <sub>L</sub> = 20 pF,	$R_{L} = 10 k\Omega$ ,	25°C		200		kHz
		Occ riguie i			70°C		140		
					0°C		2.5		
B <sub>1</sub>	Unity-gain bandwidth	Vj = 10 mV,	CL = 20 pF,	See Figure 1	25°C	C 2.2		MHz	
					70°C		1.8		
		10	<u> </u>	0 00 -5	0°C		50°		
φm	n Phase margin	V <sub>I</sub> = 10 mV, See Figure 3	f = B <sub>1</sub> ,	C <sub>L</sub> = 20 pF,	25°C		49°		
		See rigule S			70°C		46°		



#### TLC25L4BCN Texas Instruments IC CMOS 4 CIRCUIT 14DIP TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

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#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 5 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	τ <sub>A</sub> †	TL	LC25L40 C25L4A C25L4B	С	UNIT
		-				MIN	TYP	MAX	
		TLC25L4C	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		1023240	R <sub>S</sub> = 50 Ω,	$R_L = 1 M\Omega$	Full range			12	
VIO	Input offset voltage	TLC25L4AC	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	mV
10	input onset voltage	1202024/10	R <sub>S</sub> = 50 Ω,	$R_L = 1 M\Omega$	Full range			6.5	
		TLC25L4BC	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.24	2	
		120202480	R <sub>S</sub> = 50 Ω,	$R_L = 1 M\Omega$	Full range			3	
∝VIO	Average temperature coeff offset voltage	icient of input			25°C to 70°C		1.1		μV/°C
lio.	Input offect current (coo N	(1, 1)	V <sub>O</sub> = 2.5 V,	V <sub>IC</sub> = 2.5 V	25°C		0.1	60	pА
IIO	input onset current (see No	offset current (see Note 4)		$V_{1C} = 2.5 V_{1C}$	70°C		7	300	рА
lun.	Input bios current (coo Not	out bias current (see Note 4)		VIC = 2.5 V	25°C		0.6	60	pА
IВ	input bias current (see Not			VIC = 2.5 V	70°C		40	600	рА
	Common-mode input volta	ge range			25°C	-0.2 to 4	-0.3 to 4.2		V
VICR	(see Note 5)				Full range	-0.2 to 3.5			V
					0°C	3	4.1		
∨он	High-level output voltage		V <sub>ID</sub> = 100 mV,	$R_L = 1 M\Omega$	25°C	3.2	4.1		V
					70°C	3	4.2		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
	Leave also dell'fferentiale d				0°C	50	680		
AVD	Large-signal differential vol amplification	tage	$V_{O} = 0.25 V \text{ to } 2 V,$	$R_L = 1 M\Omega$	25°C	50	520		V/mV
	ampinoadon				70°C	50	380		
					0°C	60	95		
CMRR	Common-mode rejection ra	atio	$V_{IC} = V_{ICR}min$		25°C	65	94		dB
					70°C	60	95		
		tio			0°C	60	97		
<b>k</b> SVR	Supply-voltage rejection ra (ΔVDD/ΔVIO)	110	$V_{DD}$ = 5 V to 10 V,	V <sub>O</sub> = 1.4 V	25°C	70	98		dB
					70°C	60	97		
			$V_{0} = 25 V_{0}$	$V_{10} = 25 V$	0°C		48	84	
IDD	Supply current (four amplif	iers)	V <sub>O</sub> = 2.5 V, No load	V <sub>IC</sub> = 2.5 V,	25°C		40	68	μΑ
					70°C		31	56	

<sup>†</sup> Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 10 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	τ <sub>A</sub> †	TL	LC25L40 C25L4A C25L4B	С	UNIT
						MIN	TYP	MAX	
		TLC25L4C	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		12023240	R <sub>S</sub> = 50 Ω,	$R_L = 1 M\Omega$	Full range			12	
VIO	Input offset voltage	TLC25L4AC	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	mV
۷IO	input onset voltage	TEOZJE4AC	R <sub>S</sub> = 50 Ω,	$R_L = 1 M\Omega$	Full range			6.5	IIIV
		TLC25L4BC	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0,$	25°C		0.26	2	
		120202480	R <sub>S</sub> = 50 Ω,	$R_L = 1 M\Omega$	Full range			3	
αΛΙΟ	Average temperature coeff input offset voltage	icient of			25°C to 70°C		1		μV/°C
lio.	Input offect current (see No	(1, 1)	V <sub>O</sub> = 5 V,	VIC = 5 V	25°C		0.1	60	n۸
IO	input onset current (see No	nput offset current (see Note 4)		AIC = 2 A	70°C		7	300	pА
	Input bias current (see Note 4)		V <sub>O</sub> = 5 V,	V <sub>IC</sub> =.5 V	25°C		0.7	60	<b>n</b> A
IВ			$v_{\rm O} = 5 v$ ,	VIC =.5 V	70°C		50	600	pА
.,	Common-mode input volta	ge range (see			25°C	-0.2 to 9	-0.3 to 9.2		V
VICR	Note 5)				Full range	-0.2 to 8.5			V
					0°C	7.8	8.9		
Vон	High-level output voltage		V <sub>ID</sub> = 100 mV,	$R_L = 1 M\Omega$	25°C	8	8.9		V
					70°C	7.8	8.9		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
		_			0°C	50	1025		
AVD	Large-signal differential vol amplification	tage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 1 M\Omega$	25°C	50	870		V/mV
	ampineation				70°C	50	660		
					0°C	60	97		
CMRR	Common-mode rejection ra	atio	$V_{IC} = V_{ICR}min$		25°C	65	97		dB
					70°C	60	97		
					0°C	60	97		
<sup>k</sup> SVR	Supply-voltage rejection ra $(\Delta V_{DD}/\Delta V_{IO})$	tio	$V_{DD} = 5 V \text{ to } 10 V,$	V <sub>O</sub> = 1.4 V	25°C	70	97		dB
					70°C	60	98		
			<u> </u>	· · · · ·	0°C		72	132	
IDD	Supply current (four amplif	ers)	V <sub>O</sub> = 5 V, No load	V <sub>IC</sub> = 5 V,	25°C		57	92	μΑ
					70°C		44	80	

<sup>†</sup>Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



#### operating characteristics, $V_{DD} = 5 V$

	PARAMETER	ТЕ	EST CONDITION	NS	TA	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
						MIN	TYP	MAX	
					0°C		0.04		
				V <sub>I(PP)</sub> = 1 V	25°C		0.03		
SR	Slew rate at unity gain	$R_L = 1 M\Omega$ ,	C <sub>L</sub> = 20 pF,		70°C		0.03		V/µs
	Siew rate at unity gain	See Figure 1			0°C		0.03		ν/μ5
				V <sub>I(PP)</sub> =2.5V	25°C	5°C 0.03			
					70°C		0.02		
Vn	Equivalent input noise voltage	f = 1 kHz,	R <sub>S</sub> = 20 Ω,	See Figure 2	25°C		70		nV/√Hz
		., .,	0 00 5		0°C		6		
Вом	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	C <sub>L</sub> = 20 pF,	$R_{L} = 1 M\Omega,$	25°C	5			kHz
		occ rigure r			70°C		4.5		
					0°C		100		
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV,	C <sub>L</sub> = 20 pF,	See Figure 1	25°C		85		kHz
					70°C		65		
		10	<u> </u>	0.00.05	0°C		36°		
φm		$V_I = 10 \text{ mV},  f = B_{1,}$ ( See Figure 3		C <sub>L</sub> = 20 pF,	25°C		34°		
		2001 190100		70°C		30°			

### operating characteristics, $V_{DD}$ = 10 V

	PARAMETER	TE	EST CONDITIO	NS	TA	TL TLO TLO	C	UNIT	
						MIN	TYP	MAX	
					0°C		0.05		
				VI(PP) = 1 V	25°C		0.05		
SR	Slew rate at unity gain	$R_L = 1 M\Omega$ ,	C <sub>L</sub> = 20 pF,		70°C		0.04		V/μs
SK	Siew rate at unity gain	See Figure 1			0°C		0.05		v/µs
				V <sub>I(PP)</sub> =5.5V	25°C		0.04		
					70°C		0.04		
Vn	Equivalent input noise voltage	f = 1 kHz,	R <sub>S</sub> = 20 Ω,	See Figure 2	25°C		70		nV/√Hz
					0°C		1.3		
ВОМ	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	C <sub>L</sub> = 20 pF,	$R_{L} = 1 M\Omega,$	25°C		1		kHz
		See rigure r			70°C		0.9		
					0°C		125		
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV,	C <sub>L</sub> = 20 pF,	See Figure 1	25°C		110		kHz
					70°C		90		
			( )	0 00 - 5	0°C		40°		
φm		V <sub>I</sub> = 10 mV, See Figure 3	f = B <sub>1</sub> ,	C <sub>L</sub> = 20 pF,	25°C	38°			
				70°C		34°			



#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 5 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	т <sub>А</sub> †	TL	.C25M40 C25M4A C25M4B	С	UNIT
						MIN	TYP	MAX	
		TLC25M4C	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0,$	25°C		1.1	10	
		1202510140	R <sub>S</sub> = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range			12	
VIO	Input offset voltage	TLC25M4AC	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	mV
٩O	input onset voltage	TECZOWARC	R <sub>S</sub> = 50 Ω,	RL = 100 kΩ	Full range			6.5	IIIV
		TLC25M4BC	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0,$	25°C		0.25	2	
		TEC25W4BC	R <sub>S</sub> = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range			3	
∝VIO	Average temperature c input offset voltage	oefficient of			25°C to 70°C		1.7		μV/°C
L	Input offset current (see Note 4)		V <sub>O</sub> = 2.5 V,		25°C		0.1	60	- 4
IIO	Input onset current (se	nput offset current (see Note 4)		VIC = 2.5 V	70°C		7	300	pА
l	Input bias current (see Note 4)				25°C		0.6	60	- 0
IВ	Input bias current (see Note 4)		V <sub>O</sub> = 2.5 V,	VIC = 2.5 V	70°C		40	600	pА
	Common-mode input v	oltage range			25°C	-0.2 t0 4	-0.3 to 4.2		V
VICR	(see Note 5)				Full range	-0.2 to 3.5			V
					0°C	3	3.9		
Vон	High-level output voltage	ge	V <sub>ID</sub> = 100 mV,	$R_L = 100 \text{ k}\Omega$	25°C	3.2	3.9		V
					70°C	3	4		
					0°C		0	50	
VOL	Low-level output voltag	le	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
		l Ita			0°C	15	200		
AVD	Large-signal differentia amplification	l voltage	$V_{O}$ = 0.25 V to 2 V,	$R_L = 100 \text{ k}\Omega$	25°C	25	170		V/mV
	ampinioation				70°C	15	140		
					0°C	60	91		
CMRR	Common-mode rejection	on ratio	$V_{IC} = V_{ICR}min$		25°C	65	91		dB
					70°C	60	92		
	0 1 10 1 10				0°C	60	92		
ksvr	Supply-voltage rejectio (ΔVDD/ΔVIO)	n ratio	$V_{DD} = 5 V$ to 10 V,	V <sub>O</sub> = 1.4 V	25°C	70	93		dB
					70°C	60	94		
			N 0.5 Y		0°C		500	1280	
IDD	Supply current (four an	nplifiers)	$V_{O} = 2.5 V$ , No load	V <sub>IC</sub> = 2.5 V,	25°C		420	1120	μΑ
					70°C		340	880	

<sup>†</sup>Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



#### TLC25L4BCN Texas Instruments IC CMOS 4 CIRCUIT 14DIP TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

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#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 10 V (unless otherwise noted)

	PARAMETER		TEST COND	ITIONS	τ <sub>A</sub> †	TL	.C25M40 C25M4A C25M4B	C	UNIT
						MIN	TYP	MAX	
		TLC25M4C	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0,$	25°C		1.1	10	
		1602310140	R <sub>S</sub> = 50 Ω,	R <sub>L</sub> = 100 kΩ	Full range			12	
VIO	Input offset voltage	TLC25M4AC	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	mV
VIO	input onset voltage		R <sub>S</sub> = 50 Ω,	RL = 100 kΩ	Full range			6.5	
		TLC25M4BC	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0,$	25°C		0.26	2	
			R <sub>S</sub> = 50 Ω,	RL = 100 kΩ	Full range			3	
ανιο	Average temperature coef	ficient of input			25°C to 70°C		2.1		μV/°C
10	Input offset current (see No	(14)	V <sub>O</sub> = 5 V,	VIC = 5 V	25°C		0.1	60	pА
U	input onset current (see h			VIC = 3 V	70°C		7	300	PΛ
IB	nput bias current (see Note 4)		V <sub>O</sub> = 5 V,	VIC = 5 V	25°C		0.7	60	pА
чв					70°C		50	600	PA
	Common-mode input volta	ae range (see			25°C	-0.2 to 9	-0.3 to 9.2		V
VICR	Note 5)				Full range	-0.2 to 8.5			V
					0°C	7.8	8.7		
Vон	High-level output voltage		V <sub>ID</sub> = 100 mV,	$R_L = 100 \text{ k}\Omega$	25°C	8	8.7		V
					70°C	7.8	8.7		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	IOT = 0	25°C		0	50	mV
					70°C		0	50	
	Large-signal differential vo	ltage			0°C	15	320		
AVD	amplification	lage	$V_{O} = 1 V \text{ to } 6 V,$	RL = 100 kΩ	25°C	25	275		V/mV
					70°C	15	230		
					0°C	60	94		
CMRR	Common-mode rejection ra	atio	$V_{IC} = V_{ICR}min$		25°C	65	94		dB
					70°C	60	94		
	<b>_</b>				0°C	60	92		
<sup>k</sup> SVR	Supply-voltage rejection ra	tio ( $\Delta V DD / \Delta V IO$ )	$V_{DD} = 5 V$ to 10 V,	V <sub>O</sub> = 1.4 V	25°C	70	93		dB
				-	70°C	60	94	1005	
	<b>_</b>		V <sub>O</sub> = 5 V,	V <sub>IC</sub> = 5 V,	0°C		690	1600	
IDD	Supply current (four amplif	iers)	No load		25°C		570	1200	μA
					70°C		440	1120	

<sup>†</sup> Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



#### operating characteristics, V<sub>DD</sub> = 5 V

	PARAMETER	т	EST CONDITIO	NS	TA	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
				-		MIN	TYP	MAX	
					0°C		0.46		V/µs
				V <sub>I(PP)</sub> = 1 V	25°C		0.43		V/µs
SR	Slew rate at unity gain	$R_L = 100 \text{ k}\Omega,$	C <sub>L</sub> = 20 pF,		70°C		0.36		
SK	Siew rate at unity gain	See Figure 1			0°C		0.43		V/µs
				V <sub>I(PP)</sub> = 2.5 V	25°C	0.40 0.34			ν/μ5
					70°C				
Vn	Equivalent input noise voltage	f = 1 kHz,	R <sub>S</sub> = 20 Ω,	See Figure 2	25°C		32		nV/√Hz
				<b>B</b> ( <b>AA</b> ) <b>A</b>	0°C		60		
ВОМ	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	C <sub>L</sub> = 20 pF,	R <sub>L</sub> = 100 kΩ,	25°C		55		kHz
		See ligure l			70°C		50		
					0°C		610		
В <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV,	CL = 20 pF,	See Figure 1	25°C		525		kHz
					70°C		400		
		10	( )	0 00 - 5	0°C		41°		
фт	Pm Phase margin	V <sub>I</sub> = 10 mV, See Figure 3		C <sub>L</sub> = 20 pF,	25°C		40°		
		Gee Liguie e		70°C		39°			

### operating characteristics, $V_{DD}$ = 10 V

	PARAMETER	т	EST CONDITIO	NS	TA	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
						MIN	TYP	MAX	
					0°C		0.67		
				VI(PP) = 1 V	25°C		0.62		
SR	Slow roto of unity goin	R <sub>L</sub> = 100 kΩ,	C <sub>L</sub> = 20 pF,		70°C	0.51			\//uo
	Slew rate at unity gain	See Figure 1			0°C		0.61		V/μs
				V <sub>I(PP)</sub> = 5.5 V	25°C				
					70°C		0.46		
Vn	Equivalent input noise voltage	f = 1 kHz,	R <sub>S</sub> = 20 Ω,	See Figure 2	25°C		32		nV/√Hz
				<b>D</b>	0°C		40		
Вом	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	CL = 20 pF,	R <sub>L</sub> = 100 kΩ,	25°C		35		kHz
		Occ rigure r			70°C		30		
					0°C		710		
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV,	C <sub>L</sub> = 20 pF,	See Figure 1	25°C		635		kHz
					70°C		510		
		10	<u> </u>	0. 00 = 5	0°C		44°		
φm		V <sub>I</sub> = 10 mV, f = B <sub>1</sub> , C See Figure 3		C <sub>L</sub> = 20 pF,	25°C		43°		
					70°C		42°		



## TLC25L4BCN Texas Instruments IC CMOS 4 CIRCUIT 14DIP TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

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	DADAMETED	TEST	Т	LC254Y	(	Т	LC25L4	Y	TI	_C25M4	Y	UNIT
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIO	Input offset voltage	$V_{O} = 1.4 V,$ $V_{IC} = 0 V,$ $R_{S} = 50 \Omega,$ See Note 6		1.1	10		1.1	10		1.1	10	mV
αVIO	Average temperature coefficient of input offset voltage			1.8			1.1			1.7		μV/°C
IIO	Input offset current (see Note 4)	$V_{O} = V_{DD}/2,$ $V_{IC} = V_{DD}/2$		0.1	60		0.1	60		0.1	60	pА
I <sub>IB</sub>	Input bias current (see Note 4)	$V_{O} = V_{DD}/2,$ $V_{IC} = V_{DD}/2$		0.6	60		0.6	60		0.6	60	pА
VICR	Common-mode input voltage range (see Note 5)		-0.2 to 4	-0.3 to 4.2		-0.2 to 4	-0.3 to 4.2		-0.2 to 4	-0.3 to 4.2		V
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $R_L = 100 \text{ k}\Omega$	3.2	3.8		3.2	4.1		3.2	3.9		V
V <sub>OL</sub>	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 0$		0	50		0	50		0	50	mV
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>O</sub> = 0.25 V, See Note 6	5	23		50	520		25	170		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	65	80		65	94		65	91		dB
ksvr	Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	V <sub>DD</sub> = 5 V to 10 V, V <sub>O</sub> = 1.4 V	65	95		70	97		70	93		dB
I <sub>DD</sub>	Supply current	$V_O = V_{DD}/2,$ $V_{IC} = V_{DD}/2,$ No load		2.7	6.4		0.04	0.068		0.42	1.12	mA

#### electrical characteristics, $V_{DD} = 5 V$ , $T_A = 25^{\circ}C$ (unless otherwise noted)

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically. 5. This range also applies to each input individually.

6. For low-bias mode, R<sub>L</sub> = 1 MΩ, for medium-bias mode, R<sub>L</sub> = 100 kΩ, and for high-bias mode, R<sub>L</sub> = 10 kΩ.

#### operating characteristics, $V_{DD}$ = 5 V, $T_A$ = 25°C

PARAMETER		TEST CO	TLC254Y			TLC25L4Y			TLC25M4Y			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain	CL = 20 pF,	VI(PP) = 1 V	3.			0.03				0.43	\//uo	
SK		See Note 6	V <sub>I(PP)</sub> = 2.5 V		2.9			0.03			0.40		V/µs
Vn	Equivalent input noise voltage	f = 1 kHz,	R <sub>S</sub> = 20 Ω		2.5			70			32		nV/√ <del>Hz</del>
BOM	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , R <sub>L</sub> = 10 kΩ	C <sub>L</sub> = 20 pF,		320			5			55		kHz
В <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV,	C <sub>L</sub> = 20 pF		1.7			0.085			0.525		MHz
<sup>¢</sup> m	Phase margin	f = B <sub>1</sub> , C <sub>L</sub> = 20 pF	V <sub>I</sub> = 10 mV,		46°			34°			40°		

NOTE 6: For low-bias mode,  $R_L = 1 M\Omega$ , for medium-bias mode,  $R_L = 100 k\Omega$ , and for high-bias mode,  $R_L = 10 k\Omega$ .

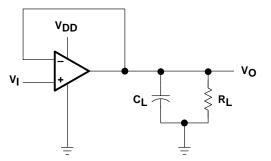
#### TLC25L4BCN Texas Instruments IC CMOS 4 CIRCUIT 14DIP TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y inCMOS™ QUAD OPERATIONAL AMPLIFIERS

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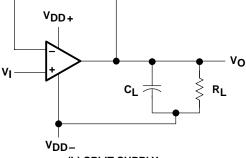
#### PARAMETER MEASUREMENT INFORMATION

#### single-supply versus split-supply test circuits

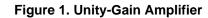
Because the TLC25\_4, TLC25\_4A, and TLC25\_4B are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

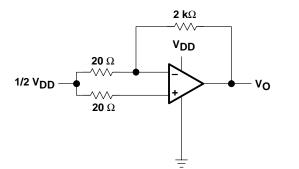


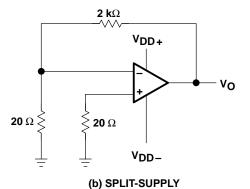
(a) SINGLE-SUPPLY





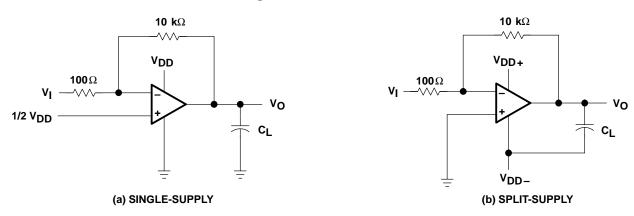






(a) SINGLE-SUPPLY









#### TLC25L4BCN Texas Instruments IC CMOS 4 CIRCUIT 14DIP TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLĆ25L4Y, TLĆ25M4, TLĆ25M4A, TLĆ25M4B, TLĆ25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

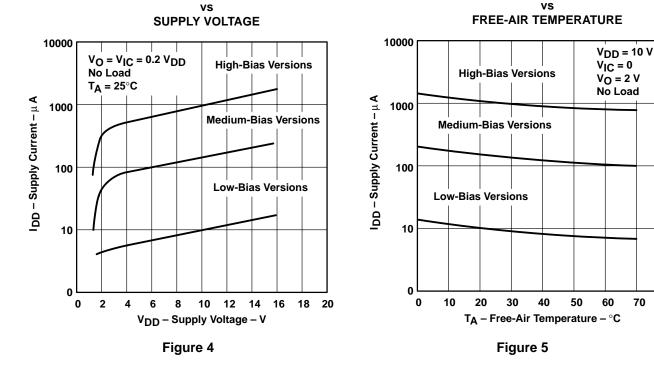
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SUPPLY CURRENT

#### **TYPICAL CHARACTERISTICS**

#### **Table of Graphs**

				FIGURE
IDD	Supply current		vs Supply voltage vs Free-air temperature	4 5
		Low bias	vs Frequency	6
AVD	Large-signal differential voltage amplification	Medium bias	vs Frequency	7
		High bias	vs Frequency	8
		Low bias	vs Frequency	6
	Phase shift	Medium bias	vs Frequency	7
		High bias	vs Frequency	8

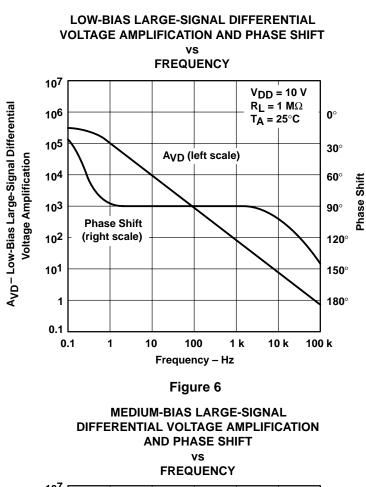


SUPPLY CURRENT



70

80





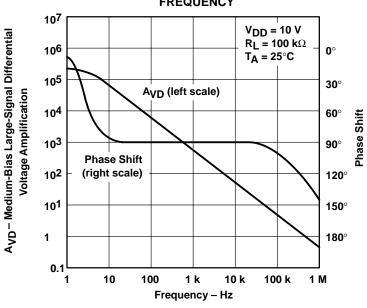


Figure 7



#### **TYPICAL CHARACTERISTICS**

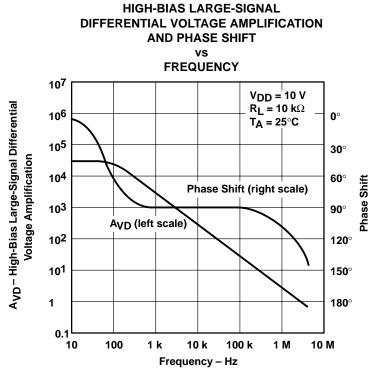


Figure 8



#### APPLICATION INFORMATION

#### latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifiers supplies should be established simultaneously with, or before, application of any input signals.

#### output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (VOH) is virtually independent of the IDD selection and increases with higher values of V<sub>DD</sub> and reduced output loading. The low-level output voltage (V<sub>OL</sub>) decreases with reduced output current and higher input common-mode voltage. With no load, VOL is essentially equal to the potential of V<sub>DD</sub>\_/GND.

#### supply configurations

Even though the TLC25\_4C series is are characterized for single-supply operation, they can be used effectively in a split-supply configuration if the input common-mode voltage ( $V_{ICR}$ ), output swing ( $V_{OI}$  and  $V_{OH}$ ), and supply voltage limits are not exceeded.

#### circuit layout precautions

Whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup as well as excessive dc leakages.





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#### PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC254ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254AC	Samples
TLC254BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254BC	Samples
TLC254BCN	ACTIVE	PDIP	Ν	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC254BCN	Samples
TLC254CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254C	Samples
TLC254CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	Samples
TLC254CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	Samples
TLC25L4BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	25L4BC	Samples
TLC25L4CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25L4C	Samples
TLC25M4CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25M4C	Samples
TLC25M4CN	ACTIVE	PDIP	Ν	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC25M4CN	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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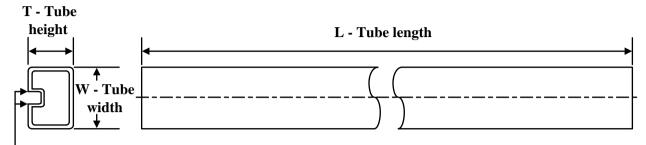


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## PACKAGE MATERIALS INFORMATION

9-Aug-2022

#### TUBE



#### - B - Alignment groove width

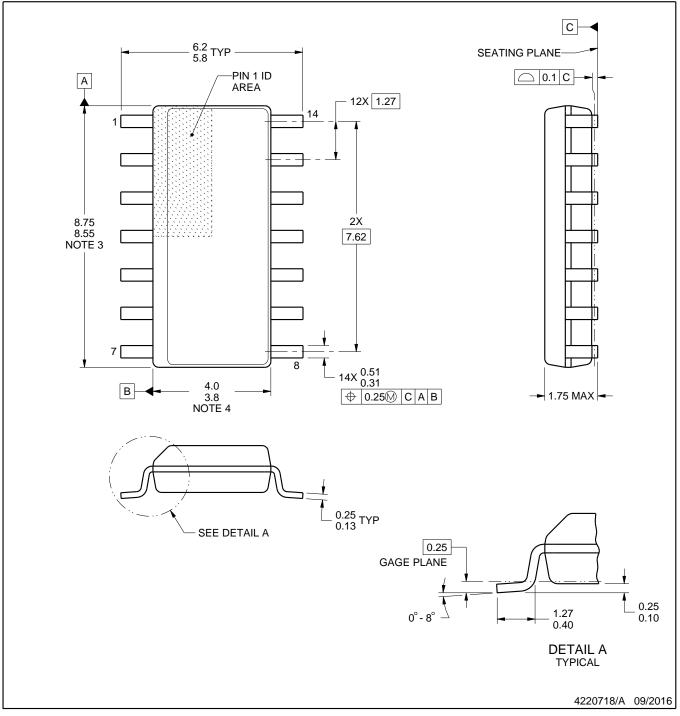
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
TLC254ACD	D	SOIC	14	50	505.46	6.76	3810	4
TLC254BCD	D	SOIC	14	50	505.46	6.76	3810	4
TLC254BCN	N	PDIP	14	25	506	13.97	11230	4.32
TLC254CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC254CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC254CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLC25L4BCD	D	SOIC	14	50	505.46	6.76	3810	4
TLC25L4CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC25M4CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC25M4CN	N	PDIP	14	25	506	13.97	11230	4.32

## **D0014A**

## **PACKAGE OUTLINE**

#### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

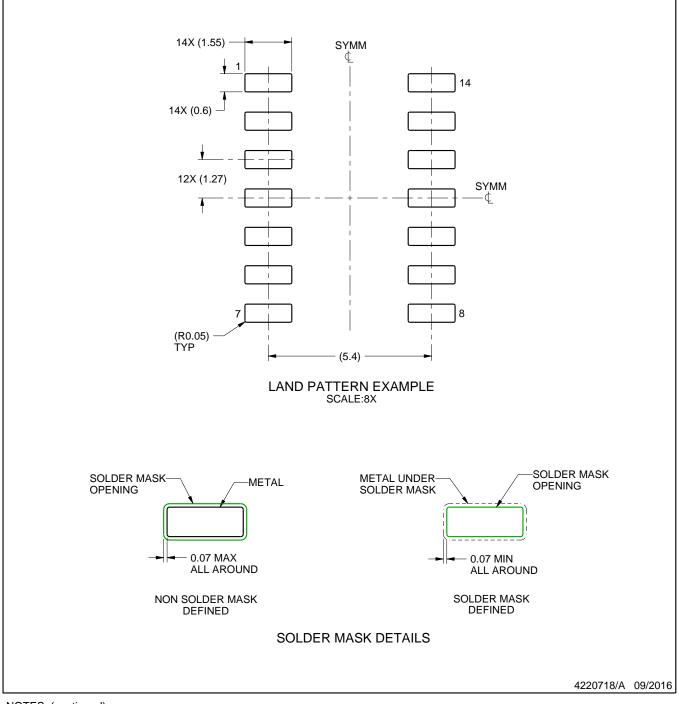
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



## **EXAMPLE BOARD LAYOUT**

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

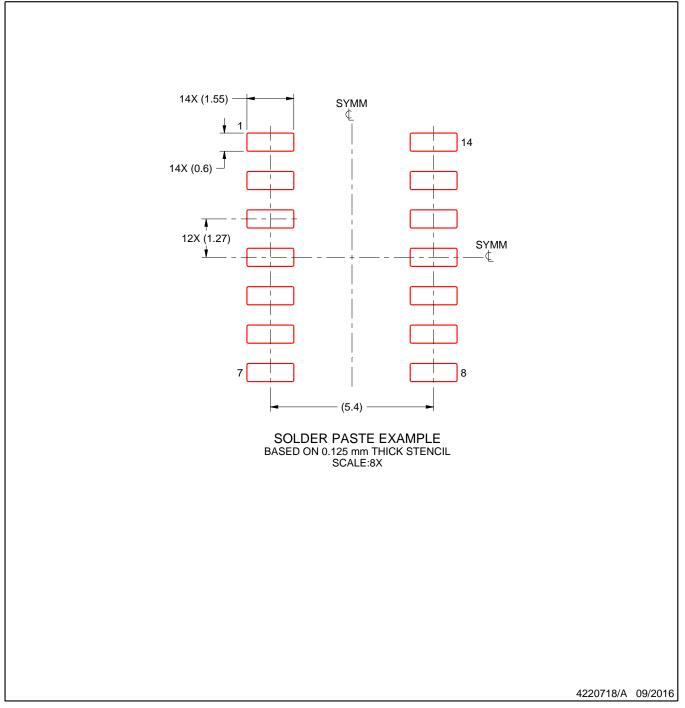
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## **EXAMPLE STENCIL DESIGN**

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



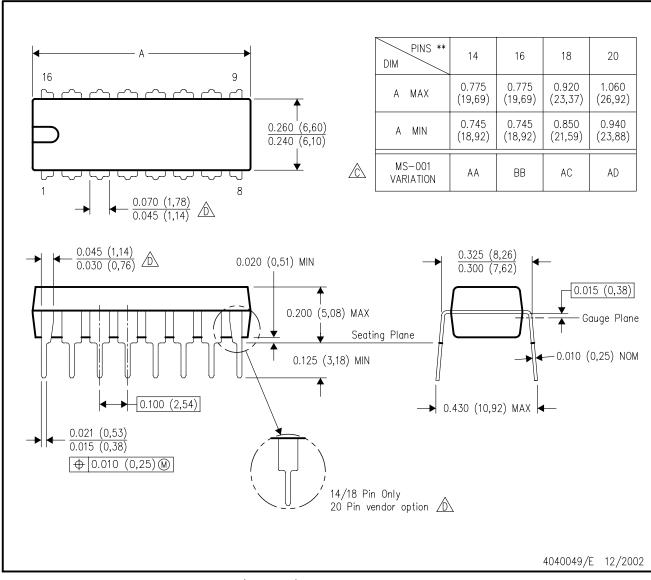
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



#### N (R-PDIP-T\*\*) 16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



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