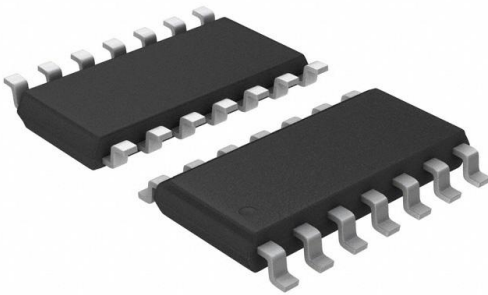


# TLC25M4CD Datasheet

[www.digi-electronics.com](http://www.digi-electronics.com)



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DiGi Electronics Part Number	TLC25M4CD-DG
Manufacturer	<a href="#">Texas Instruments</a>
Manufacturer Product Number	TLC25M4CD
Description	IC CMOS 4 CIRCUIT 14SOIC
Detailed Description	CMOS Amplifier 4 Circuit Open Drain 14-SOIC



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

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## Purchase and inquiry

Manufacturer Product Number:

TLC25M4CD

Series:

LinCMOST™

Amplifier Type:

CMOS

Output Type:

Open Drain

Gain Bandwidth Product:

1.7 MHz

Voltage - Input Offset:

1.1 mV

Voltage - Supply Span (Min):

1.4 V

Operating Temperature:

0°C ~ 70°C

Package / Case:

14-SOIC (0.154", 3.90mm Width)

Base Product Number:

TLC25M4

Manufacturer:

Texas Instruments

Product Status:

Last Time Buy

Number of Circuits:

4

Slew Rate:

0.6V/μs

Current - Input Bias:

0.6 pA

Current - Supply:

2.7mA (x4 Channels)

Voltage - Supply Span (Max):

16 V

Mounting Type:

Surface Mount

Supplier Device Package:

14-SOIC

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.33.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

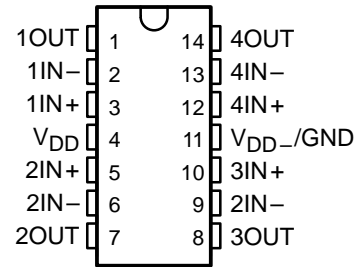
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TLC25M4CD Texas Instruments IC CMOS 4 CIRCUIT 14SOIC  
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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- **A-Suffix Versions Offer 5-mV  $V_{IO}$**
- **B-Suffix Versions Offer 2-mV  $V_{IO}$**
- **Wide Range of Supply Voltages**  
1.4 V to 16 V
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 25 nV/ $\sqrt{\text{Hz}}$  Typ at  $f = 1$  kHz (High-Bias Version)**

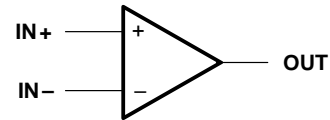
**D, N, OR PW PACKAGE  
(TOP VIEW)**



**description**

The TLC254, TLC254A, TLC254B, TLC25L4, TLC25L4A, TLC25L4B, TLC25M4, TLC25M4A and TLC25M4B are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™

**symbol (each amplifier)**



process, giving them stable input-offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for these devices include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices.

**Available options**

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	10 mV	TLC254CD	TLC254CN	TLC254CPW	TLC254Y
	5 mV	TLC254ACD	TLC254ACN	—	—
	2 mV	TLC254BCD	TLC254BCN	—	—
	10 mV	TLC25L4CD	TLC25L4CN	TLC25L4CPW	TLC25L4Y
	5 mV	TLC25L4ACD	TLC25L4ACN	—	—
	2 mV	TLC25L2BCD	TLC25L4BCN	—	—
	10 mV	TLC25M4CD	TLC25M4CN	TLC25M4CPW	TLC25M4Y
	5 mV	TLC25M4ACD	TLC25M4ACN	—	—
	2 mV	TLC25M4BCD	TLC25M4BCN	—	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC254CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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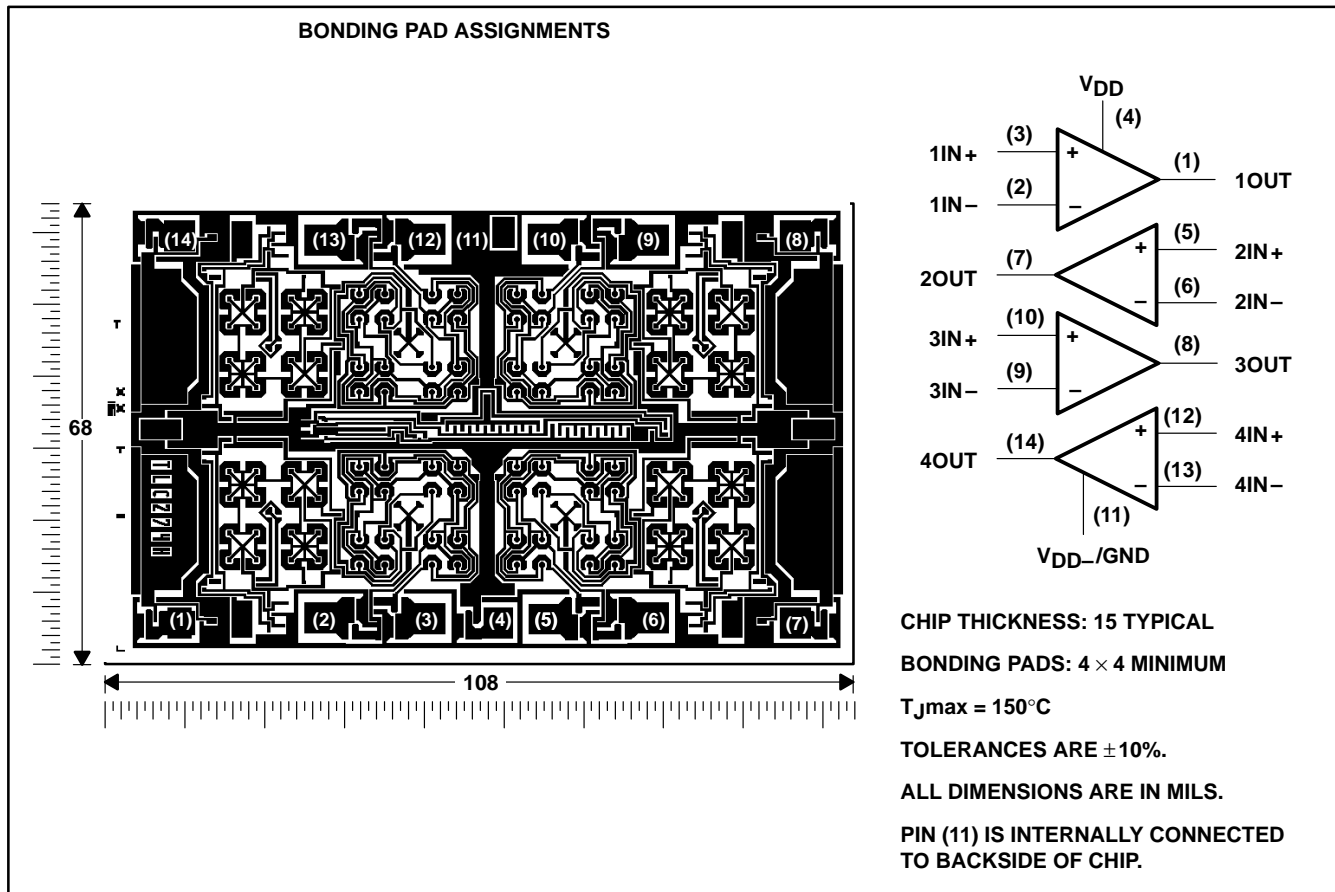


TLC25M4CD Texas Instruments IC CMOS 4 CIRCUIT 14SOIC  
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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**chip information**

These chips, when properly assembled, display characteristics similar to the TLC25\_4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



# TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm 18$ V
Input voltage range (any input)	-0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to  $V_{DD-}/GND$ .

2. Differential voltages are at  $IN+$ , with respect to  $IN-$ .

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
N	1050 mW	9.2 mW/°C	736 mW
PW	700 mW	5.6 mW/°C	448 mW

## recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$		1.4	16	V
Common-mode input voltage, $V_{IC}$	$V_{DD} = 1.4$ V	0	0.2	V
	$V_{DD} = 5$ V	-0.2	4	
	$V_{DD} = 10$ V	-0.2	9	
	$V_{DD} = 16$ V	-0.2	14	
Operating free-air temperature, $T_A$		0	70	°C

**electrical characteristics at specified free-air temperature,  $V_{DD} = 1.4\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONST	$T_A$	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_O = 0.2\text{ V}, R_S = 50\ \Omega$	25°C			10			10			10	mV
			0°C to 70°C			12			12			12	
			25°C			5			5			5	
			0°C to 70°C			6.5			6.5			6.5	
			25°C			2			2			2	
			0°C to 70°C			3			3			3	
$a_{VIO}$	Average temperature coefficient of input offset voltage		25°C to 70°C		1			1			1	$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current	$V_O = 0.2\text{ V}$	25°C		1	60		1	60		1	60	pA
			0°C to 70°C			300			300			300	
$I_{IB}$	Input bias current	$V_O = 0.2\text{ V}$	25°C		1	60		1	60		1	60	pA
			0°C to 70°C			600			600			600	
$V_{ICR}$	Common-mode input voltage range		25°C	0 to 0.2			0 to 0.2			0 to 0.2		V	
$V_{OM}$	Peak output voltage swing‡	$V_{ID} = 100\text{ mV}$	25°C	450	700		450	700		450	700	mV	
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 100\text{ to }300\text{ mV}, R_S = 50\ \Omega$	25°C		10			20			20	V/mV	
CMRR	Common-mode rejection ratio	$V_O = 0.2\text{ V}, V_{IC} = V_{ICRmin}$	25°C	60	77		60	77		60	77	dB	
$I_{DD}$	Supply current	$V_O = 0.2\text{ V}, \text{ No load}$	25°C		600	750		50	68		400	500	$\mu\text{A}$

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: for low bias,  $R_L = 1\text{ M}\Omega$ , for medium bias  $R_L = 100\text{ k}\Omega$ , and for high bias  $R_L = 10\text{ k}\Omega$ .

‡ The output swings to the potential of  $V_{DD-}/\text{GND}$ .

**operating characteristics,  $V_{DD} = 1.4\text{ V}, T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	See Figure 1		0.1			0.001			0.01		$\text{V}/\mu\text{s}$
$B_1$	Unity-gain bandwidth	$A_V = 40\text{ dB}, R_S = 50\ \Omega, C_L = 10\text{ pF}, \text{ See Figure 1}$		12			12			12		kHz
	Overshoot factor	See Figure 1		30%			35%			35%		

**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		$T_A$ †	TLC254, TLC254AC, TLC254BC			UNIT
					MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	TLC254C	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 10\text{ k}\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC254AC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 10\text{ k}\Omega$	25°C	0.9	5	
					Full range		6.5	
		TLC254BC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 10\text{ k}\Omega$	25°C	0.34	2	
					Full range		3	
$\alpha_{VIO}$	Average temperature coefficient of input offset voltage			25°C to 70°C	1.8		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current (see Note 4)	$V_O = 2.5\text{ V}$ ,	$V_{IC} = 2.5\text{ V}$	25°C	0.1	60	pA	
				70°C	7	300		
$I_{IB}$	Input bias current (see Note 4)	$V_O = 2.5\text{ V}$ ,	$V_{IC} = 2.5\text{ V}$	25°C	0.6	60	pA	
				70°C	40	600		
$V_{ICR}$	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2	V	
				Full range	-0.2 to 3.5			
$V_{OH}$	High-level output voltage	$V_{ID} = 100\text{ mV}$ ,	$R_L = 10\text{ k}\Omega$	0°C	3	3.8	V	
				25°C	3.2	3.8		
				70°C	3	3.8		
$V_{OL}$	Low-level output voltage	$V_{ID} = -100\text{ mV}$ ,	$I_{OL} = 0$	0°C	0	50	mV	
				25°C	0	50		
				70°C	0	50		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 0.25\text{ V to }2\text{ V}$ ,	$R_L = 10\text{ k}\Omega$	0°C	4	27	V/mV	
				25°C	5	23		
				70°C	4	20		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		0°C	60	84	dB	
				25°C	65	80		
				70°C	60	85		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V}$ ,	$V_O = 1.4\text{ V}$	0°C	60	94	dB	
				25°C	65	95		
				70°C	60	96		
$I_{DD}$	Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , No load	$V_{IC} = 2.5\text{ V}$ ,	0°C	3.1	7.2	mA	
				25°C	2.7	6.4		
				70°C	2.3	5.2		

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



TLC25M4CD Texas Instruments IC CMOS 4 CIRCUIT 14SOIC  
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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**electrical characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		$T_A$ †	TLC254C, TLC254AC, TLC254BC			UNIT
					MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	TLC254C	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 10\text{ k}\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC254AC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 10\text{ k}\Omega$	25°C	0.9	5	
					Full range		6.5	
		TLC254BC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 10\text{ k}\Omega$	25°C	0.39	2	
					Full range		3	
$\epsilon_{VIO}$	Average temperature coefficient of input offset voltage			25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current (see Note 4)	$V_O = 5\text{ V}$ ,	$V_{IC} = 5\text{ V}$	25°C	0.1	60	pA	
				70°C	7	300		
$I_{IB}$	Input bias current (see Note 4)	$V_O = 5\text{ V}$ ,	$V_{IC} = 5\text{ V}$	25°C	0.7	60	pA	
				70°C	50	600		
$V_{ICR}$	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 9	-0.3 to 9.2	V	
				Full range	-0.2 to 8.5			
$V_{OH}$	High-level output voltage	$V_{ID} = 100\text{ mV}$ ,	$R_L = 10\text{ k}\Omega$	0°C	7.8	8.5	V	
				25°C	8	8.5		
				70°C	7.8	8.4		
$V_{OL}$	Low-level output voltage	$V_{ID} = -100\text{ mV}$ ,	$I_{OL} = 0$	0°C	0	50	mV	
				25°C	0	50		
				70°C	0	50		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 1\text{ V to }6\text{ V}$ ,	$R_L = 10\text{ k}\Omega$	0°C	7.5	42	V/mV	
				25°C	10	36		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		0°C	60	88	dB	
				25°C	65	85		
				70°C	60	88		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V}$ ,	$V_O = 1.4\text{ V}$	0°C	60	94	dB	
				25°C	65	95		
				70°C	60	96		
$I_{DD}$	Supply current (four amplifiers)	$V_O = 5\text{ V}$ , No load	$V_{IC} = 5\text{ V}$ ,	0°C	4.5	8.8	mA	
				25°C	3.8	8		
				70°C	3.2	6.8		

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



operating characteristics,  $V_{DD} = 5\text{ V}$ 

PARAMETER	TEST CONDITIONS	$T_A$	TLC254C, TLC254AC, TLC254BC			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , See Figure 1 $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	0°C	4		V/ $\mu$ s
			25°C	3.6		
		$V_{I(PP)} = 1\text{ V}$	70°C	3		
			$V_{I(PP)} = 2.5\text{ V}$	0°C	3.1	
		25°C		2.9		
		70°C		2.5		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 20\ \Omega$ , See Figure 2	25°C	25		nV/ $\sqrt{\text{Hz}}$	
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$ , See Figure 1 $C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$	0°C	340		kHz	
		25°C	320			
		70°C	260			
B <sub>1</sub> Unity-gain bandwidth	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , See Figure 1	0°C	2		MHz	
		25°C	1.7			
		70°C	1.3			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , See Figure 3 $f = B_1$ , $C_L = 20\text{ pF}$	0°C	47°			
		25°C	46°			
		70°C	43°			

operating characteristics,  $V_{DD} = 10\text{ V}$ 

PARAMETER	TEST CONDITIONS	$T_A$	TLC254C, TLC254AC, TLC254BC			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , See Figure 1 $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	0°C	5.9		V/ $\mu$ s
			25°C	5.3		
			70°C	4.3		
		$V_{I(PP)} = 5.5\text{ V}$	0°C	5.1		
			25°C	4.6		
			70°C	3.8		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 20\ \Omega$ , See Figure 2	25°C	25		nV/ $\sqrt{\text{Hz}}$	
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$ , See Figure 1 $C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$	0°C	220		kHz	
		25°C	200			
		70°C	140			
B <sub>1</sub> Unity-gain bandwidth	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , See Figure 1	0°C	2.5		MHz	
		25°C	2.2			
		70°C	1.8			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , See Figure 3 $f = B_1$ , $C_L = 20\text{ pF}$	0°C	50°			
		25°C	49°			
		70°C	46°			

TLC25M4CD Texas Instruments IC CMOS 4 CIRCUIT 14SOIC  
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
					MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	TLC25L4C	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ , $R_L = 1\text{ M}\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC25L4AC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ , $R_L = 1\text{ M}\Omega$	25°C	0.9	5	
					Full range		6.5	
		TLC25L4BC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ , $R_L = 1\text{ M}\Omega$	25°C	0.24	2	
					Full range		3	
$\infty V_{IO}$	Average temperature coefficient of input offset voltage			25°C to 70°C	1.1		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current (see Note 4)	$V_O = 2.5\text{ V}$	$V_{IC} = 2.5\text{ V}$	25°C	0.1	60	pA	
				70°C	7	300		
$I_{IB}$	Input bias current (see Note 4)	$V_O = 2.5\text{ V}$	$V_{IC} = 2.5\text{ V}$	25°C	0.6	60	pA	
				70°C	40	600		
$V_{ICR}$	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2	V	
				Full range	-0.2 to 3.5		V	
$V_{OH}$	High-level output voltage	$V_{ID} = 100\text{ mV}$	$R_L = 1\text{ M}\Omega$	0°C	3	4.1	V	
				25°C	3.2	4.1		
				70°C	3	4.2		
$V_{OL}$	Low-level output voltage	$V_{ID} = -100\text{ mV}$	$I_{OL} = 0$	0°C	0	50	mV	
				25°C	0	50		
				70°C	0	50		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 0.25\text{ V to }2\text{ V}$	$R_L = 1\text{ M}\Omega$	0°C	50	680	V/mV	
				25°C	50	520		
				70°C	50	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		0°C	60	95	dB	
				25°C	65	94		
				70°C	60	95		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V}$	$V_O = 1.4\text{ V}$	0°C	60	97	dB	
				25°C	70	98		
				70°C	60	97		
$I_{DD}$	Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , No load	$V_{IC} = 2.5\text{ V}$	0°C	48	84	$\mu\text{A}$	
				25°C	40	68		
				70°C	31	56		

$^\dagger$  Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



# TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

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**electrical characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	$T_A$ †	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
				MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	TLC25L4C $V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 1\text{ M}\Omega$	25°C	1.1	10	mV
				Full range		12	
		TLC25L4AC $V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 1\text{ M}\Omega$	25°C	0.9	5	
				Full range		6.5	
		TLC25L4BC $V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 1\text{ M}\Omega$	25°C	0.26	2	
				Full range		3	
$\alpha_{VIO}$	Average temperature coefficient of input offset voltage		25°C to 70°C	1		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current (see Note 4)	$V_O = 5\text{ V}$ ,	$V_{IC} = 5\text{ V}$	25°C	0.1	60	pA
				70°C	7	300	
$I_{IB}$	Input bias current (see Note 4)	$V_O = 5\text{ V}$ ,	$V_{IC} = 5\text{ V}$	25°C	0.7	60	pA
				70°C	50	600	
$V_{ICR}$	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 9	-0.3 to 9.2	V
				Full range	-0.2 to 8.5		V
$V_{OH}$	High-level output voltage	$V_{ID} = 100\text{ mV}$ ,	$R_L = 1\text{ M}\Omega$	0°C	7.8	8.9	V
				25°C	8	8.9	
				70°C	7.8	8.9	
$V_{OL}$	Low-level output voltage	$V_{ID} = -100\text{ mV}$ ,	$I_{OL} = 0$	0°C	0	50	mV
				25°C	0	50	
				70°C	0	50	
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 1\text{ V to }6\text{ V}$ ,	$R_L = 1\text{ M}\Omega$	0°C	50	1025	V/mV
				25°C	50	870	
				70°C	50	660	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		0°C	60	97	dB
				25°C	65	97	
				70°C	60	97	
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V}$ ,	$V_O = 1.4\text{ V}$	0°C	60	97	dB
				25°C	70	97	
				70°C	60	98	
$I_{DD}$	Supply current (four amplifiers)	$V_O = 5\text{ V}$ , No load	$V_{IC} = 5\text{ V}$ ,	0°C	72	132	$\mu\text{A}$
				25°C	57	92	
				70°C	44	80	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



TLC25M4CD Texas Instruments IC CMOS 4 CIRCUIT 14SOIC  
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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**operating characteristics,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , See Figure 1 $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	0°C	0.04		V/ $\mu$ s
			25°C	0.03		
			70°C	0.03		
		$V_{I(PP)} = 2.5\text{ V}$	0°C	0.03		
			25°C	0.03		
			70°C	0.02		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 20\ \Omega$ , See Figure 2	25°C	70		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , See Figure 1 $C_L = 20\text{ pF}$ , $R_L = 1\text{ M}\Omega$	0°C	6		kHz	
		25°C	5			
		70°C	4.5			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , See Figure 1	0°C	100		kHz	
		25°C	85			
		70°C	65			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , See Figure 3 $f = B_1$ , $C_L = 20\text{ pF}$	0°C	36°			
		25°C	34°			
		70°C	30°			

**operating characteristics,  $V_{DD} = 10\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , See Figure 1 $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	0°C	0.05		V/ $\mu$ s
			25°C	0.05		
			70°C	0.04		
		$V_{I(PP)} = 5.5\text{ V}$	0°C	0.05		
			25°C	0.04		
			70°C	0.04		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 20\ \Omega$ , See Figure 2	25°C	70		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , See Figure 1 $C_L = 20\text{ pF}$ , $R_L = 1\text{ M}\Omega$	0°C	1.3		kHz	
		25°C	1			
		70°C	0.9			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , See Figure 1	0°C	125		kHz	
		25°C	110			
		70°C	90			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , See Figure 3 $f = B_1$ , $C_L = 20\text{ pF}$	0°C	40°			
		25°C	38°			
		70°C	34°			



**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B  
 TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y  
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**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	$T_A$ †	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
				MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	TLC25M4C $V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ , $R_L = 100\text{ k}\Omega$	25°C	1.1	10	mV
				Full range		12	
	TLC25M4AC $V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ , $R_L = 100\text{ k}\Omega$	25°C	0.9	5		
			Full range		6.5		
	TLC25M4BC $V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ , $R_L = 100\text{ k}\Omega$	25°C	0.25	2		
			Full range		3		
$^{\circ}V_{IO}$	Average temperature coefficient of input offset voltage		25°C to 70°C	1.7		$\mu\text{V}/^{\circ}\text{C}$	
$I_{IO}$	Input offset current (see Note 4)	$V_O = 2.5\text{ V}$	$V_{IC} = 2.5\text{ V}$	25°C	0.1	60	pA
				70°C	7	300	
$I_{IB}$	Input bias current (see Note 4)	$V_O = 2.5\text{ V}$	$V_{IC} = 2.5\text{ V}$	25°C	0.6	60	pA
				70°C	40	600	
$V_{ICR}$	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2	V
				Full range	-0.2 to 3.5		V
$V_{OH}$	High-level output voltage	$V_{ID} = 100\text{ mV}$	$R_L = 100\text{ k}\Omega$	0°C	3	3.9	V
				25°C	3.2	3.9	
				70°C	3	4	
$V_{OL}$	Low-level output voltage	$V_{ID} = -100\text{ mV}$	$I_{OL} = 0$	0°C		0 50	mV
				25°C		0 50	
				70°C		0 50	
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 0.25\text{ V to }2\text{ V}$	$R_L = 100\text{ k}\Omega$	0°C	15	200	V/mV
				25°C	25	170	
				70°C	15	140	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		0°C	60	91	dB
				25°C	65	91	
				70°C	60	92	
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V}$	$V_O = 1.4\text{ V}$	0°C	60	92	dB
				25°C	70	93	
				70°C	60	94	
$I_{DD}$	Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , No load	$V_{IC} = 2.5\text{ V}$	0°C	500	1280	$\mu\text{A}$
				25°C	420	1120	
				70°C	340	880	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



TLC25M4CD Texas Instruments IC CMOS 4 CIRCUIT 14SOIC  
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
					MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	TLC25M4C	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 100\text{ k}\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC25M4AC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 100\text{ k}\Omega$	25°C	0.9	5	
					Full range		6.5	
		TLC25M4BC	$V_O = 1.4\text{ V}$ , $R_S = 50\ \Omega$ ,	$V_{IC} = 0$ , $R_L = 100\text{ k}\Omega$	25°C	0.26	2	
					Full range		3	
$\alpha_{VIO}$	Average temperature coefficient of input offset voltage			25°C to 70°C	2.1		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current (see Note 4)	$V_O = 5\text{ V}$ ,	$V_{IC} = 5\text{ V}$	25°C	0.1	60	pA	
				70°C	7	300		
$I_{IB}$	Input bias current (see Note 4)	$V_O = 5\text{ V}$ ,	$V_{IC} = 5\text{ V}$	25°C	0.7	60	pA	
				70°C	50	600		
$V_{ICR}$	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 9	-0.3 to 9.2	V	
				Full range	-0.2 to 8.5		V	
$V_{OH}$	High-level output voltage	$V_{ID} = 100\text{ mV}$ ,	$R_L = 100\text{ k}\Omega$	0°C	7.8	8.7	V	
				25°C	8	8.7		
				70°C	7.8	8.7		
$V_{OL}$	Low-level output voltage	$V_{ID} = -100\text{ mV}$ ,	$I_{OL} = 0$	0°C	0	50	mV	
				25°C	0	50		
				70°C	0	50		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 1\text{ V to }6\text{ V}$ ,	$R_L = 100\text{ k}\Omega$	0°C	15	320	V/mV	
				25°C	25	275		
				70°C	15	230		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		0°C	60	94	dB	
				25°C	65	94		
				70°C	60	94		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V}$ ,	$V_O = 1.4\text{ V}$	0°C	60	92	dB	
				25°C	70	93		
				70°C	60	94		
$I_{DD}$	Supply current (four amplifiers)	$V_O = 5\text{ V}$ , No load	$V_{IC} = 5\text{ V}$ ,	0°C	690	1600	$\mu\text{A}$	
				25°C	570	1200		
				70°C	440	1120		

$^\dagger$  Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B  
 TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y  
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**operating characteristics,  $V_{DD} = 5\text{ V}$** 

PARAMETER	TEST CONDITIONS			$T_A$	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
					MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , See Figure 1	$C_L = 20\text{ pF}$ ,	$V_{I(PP)} = 1\text{ V}$	0°C	0.46		V/ $\mu\text{s}$	
				25°C	0.43		V/ $\mu\text{s}$	
				70°C	0.36			
			$V_{I(PP)} = 2.5\text{ V}$	0°C	0.43		V/ $\mu\text{s}$	
				25°C	0.40			
				70°C	0.34			
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ ,	$R_S = 20\ \Omega$ ,	See Figure 2	25°C	32		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , See Figure 1	$C_L = 20\text{ pF}$ ,	$R_L = 100\text{ k}\Omega$ ,	0°C	60		kHz	
				25°C	55			
				70°C	50			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ ,	$C_L = 20\text{ pF}$ ,	See Figure 1	0°C	610		kHz	
				25°C	525			
				70°C	400			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , See Figure 3	$f = B_1$ ,	$C_L = 20\text{ pF}$ ,	0°C	41°			
				25°C	40°			
				70°C	39°			

**operating characteristics,  $V_{DD} = 10\text{ V}$** 

PARAMETER	TEST CONDITIONS			$T_A$	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
					MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , See Figure 1	$C_L = 20\text{ pF}$ ,	$V_{I(PP)} = 1\text{ V}$	0°C	0.67		V/ $\mu\text{s}$	
				25°C	0.62			
				70°C	0.51			
			$V_{I(PP)} = 5.5\text{ V}$	0°C	0.61			
				25°C	0.56			
				70°C	0.46			
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ ,	$R_S = 20\ \Omega$ ,	See Figure 2	25°C	32		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , See Figure 1	$C_L = 20\text{ pF}$ ,	$R_L = 100\text{ k}\Omega$ ,	0°C	40		kHz	
				25°C	35			
				70°C	30			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ ,	$C_L = 20\text{ pF}$ ,	See Figure 1	0°C	710		kHz	
				25°C	635			
				70°C	510			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , See Figure 3	$f = B_1$ ,	$C_L = 20\text{ pF}$ ,	0°C	44°			
				25°C	43°			
				70°C	42°			



TLC25M4CD Texas Instruments IC CMOS 4 CIRCUIT 14SOIC  
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B**  
**TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y**  
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**electrical characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TLC254Y			TLC25L4Y			TLC25M4Y			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 1.4\text{ V}$ , $V_{IC} = 0\text{ V}$ , $R_S = 50\ \Omega$ , See Note 6		1.1	10		1.1	10		1.1	10	mV
$\alpha_{VIO}$ Average temperature coefficient of input offset voltage			1.8			1.1			1.7		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$ Input offset current (see Note 4)	$V_O = V_{DD}/2$ , $V_{IC} = V_{DD}/2$		0.1	60		0.1	60		0.1	60	pA
$I_{IB}$ Input bias current (see Note 4)	$V_O = V_{DD}/2$ , $V_{IC} = V_{DD}/2$		0.6	60		0.6	60		0.6	60	pA
$V_{ICR}$ Common-mode input voltage range (see Note 5)		-0.2 to 4	-0.3 to 4.2		-0.2 to 4	-0.3 to 4.2		-0.2 to 4	-0.3 to 4.2		V
$V_{OH}$ High-level output voltage	$V_{ID} = 100\text{ mV}$ , $R_L = 100\text{ k}\Omega$	3.2	3.8		3.2	4.1		3.2	3.9		V
$V_{OL}$ Low-level output voltage	$V_{ID} = -100\text{ mV}$ , $I_{OL} = 0$		0	50		0	50		0	50	mV
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 0.25\text{ V}$ , See Note 6	5	23		50	520		25	170		V/mV
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	65	80		65	94		65	91		dB
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V}$ , $V_O = 1.4\text{ V}$	65	95		70	97		70	93		dB
$I_{DD}$ Supply current	$V_O = V_{DD}/2$ , $V_{IC} = V_{DD}/2$ , No load		2.7	6.4		0.04	0.068		0.42	1.12	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
5. This range also applies to each input individually.  
6. For low-bias mode,  $R_L = 1\text{ M}\Omega$ , for medium-bias mode,  $R_L = 100\text{ k}\Omega$ , and for high-bias mode,  $R_L = 10\text{ k}\Omega$ .

**operating characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TLC254Y			TLC25L4Y			TLC25M4Y			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$C_L = 20\text{ pF}$ , See Note 6	$V_I(PP) = 1\text{ V}$	3.6		0.03		0.43				V/ $\mu\text{s}$
		$V_I(PP) = 2.5\text{ V}$	2.9		0.03		0.40				
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 20\ \Omega$		2.5			70			32		$\text{nV}/\sqrt{\text{Hz}}$
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10\text{ k}\Omega$		320			5			55		kHz
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$		1.7			0.085			0.525		MHz
$\phi_m$ Phase margin	$f = B_1$ , $C_L = 20\text{ pF}$		46°			34°			40°		

NOTE 6: For low-bias mode,  $R_L = 1\text{ M}\Omega$ , for medium-bias mode,  $R_L = 100\text{ k}\Omega$ , and for high-bias mode,  $R_L = 10\text{ k}\Omega$ .



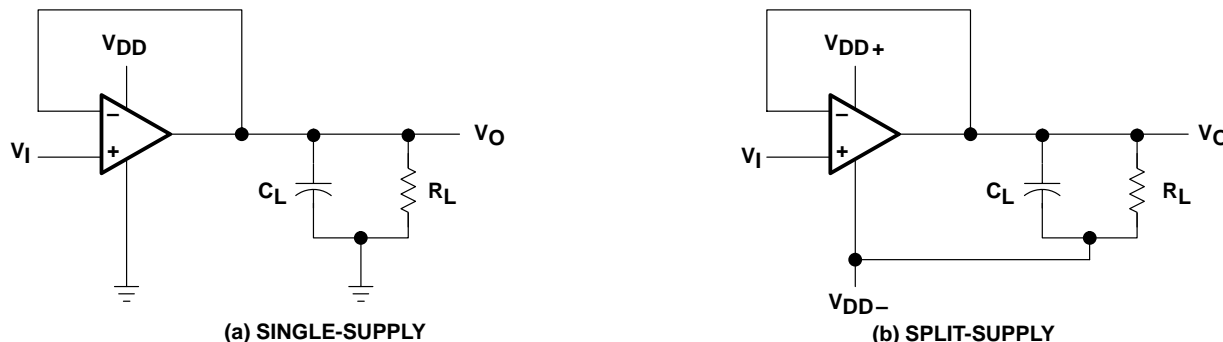
**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B  
TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y  
LinCMOS™ QUAD OPERATIONAL AMPLIFIERS**

SLOS003G – JUNE 1983 – REVISED MARCH 2001

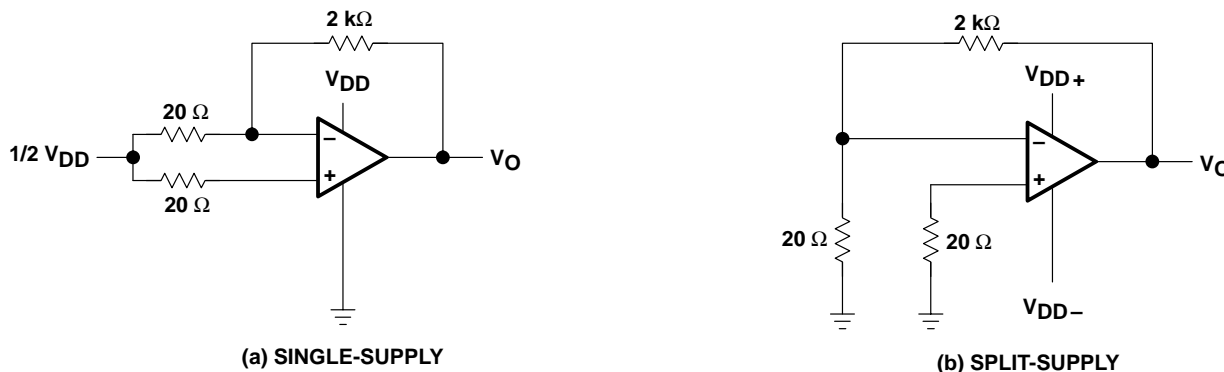
**PARAMETER MEASUREMENT INFORMATION**

**single-supply versus split-supply test circuits**

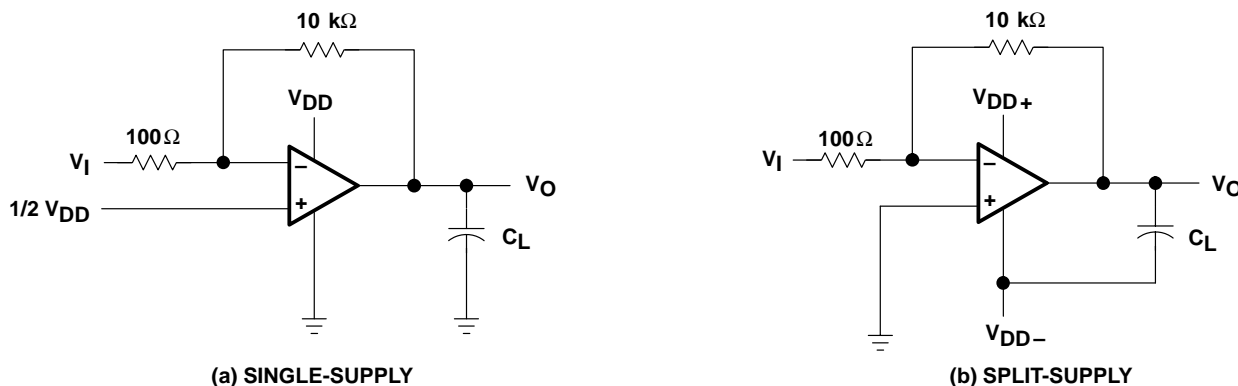
Because the TLC25\_4, TLC25\_4A, and TLC25\_4B are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



**Figure 1. Unity-Gain Amplifier**



**Figure 2. Noise-Test Circuit**



**Figure 3. Gain-of-100 Inverting Amplifier**

**TYPICAL CHARACTERISTICS**

Table of Graphs

			FIGURE	
I <sub>DD</sub>	Supply current		vs Supply voltage	4
			vs Free-air temperature	5
A <sub>VD</sub>	Large-signal differential voltage amplification	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8
	Phase shift	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

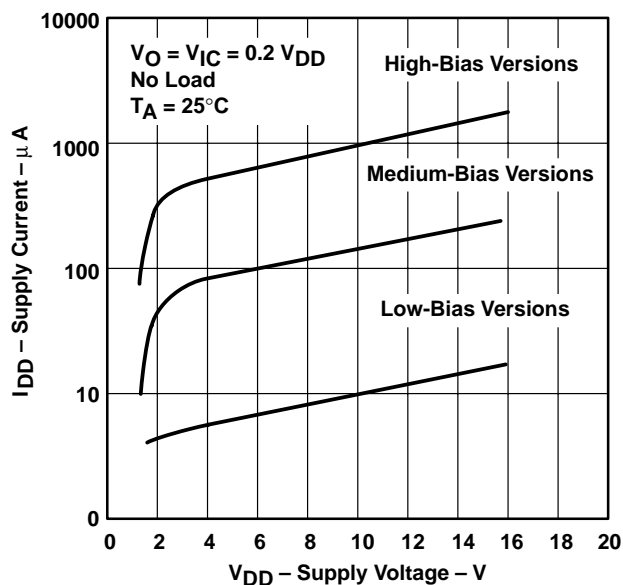


Figure 4

**SUPPLY CURRENT  
vs  
FREE-AIR TEMPERATURE**

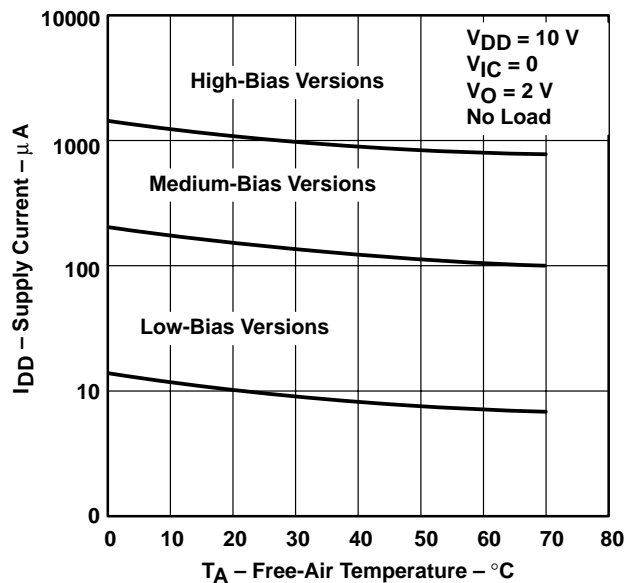
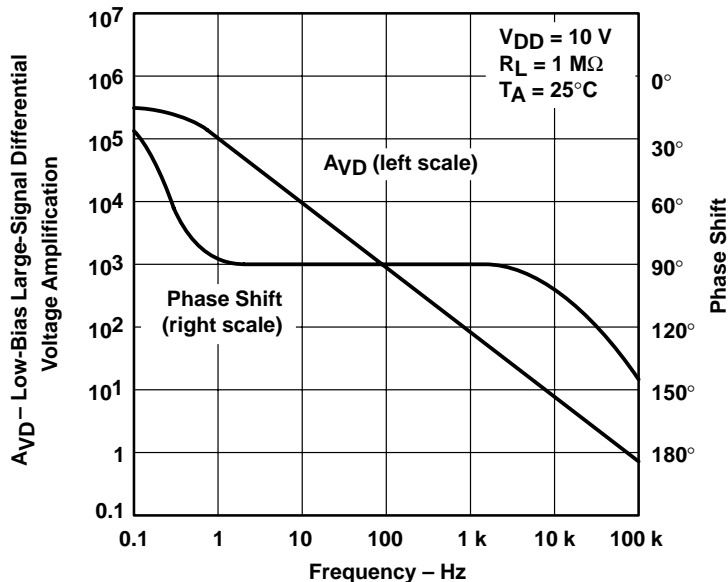


Figure 5

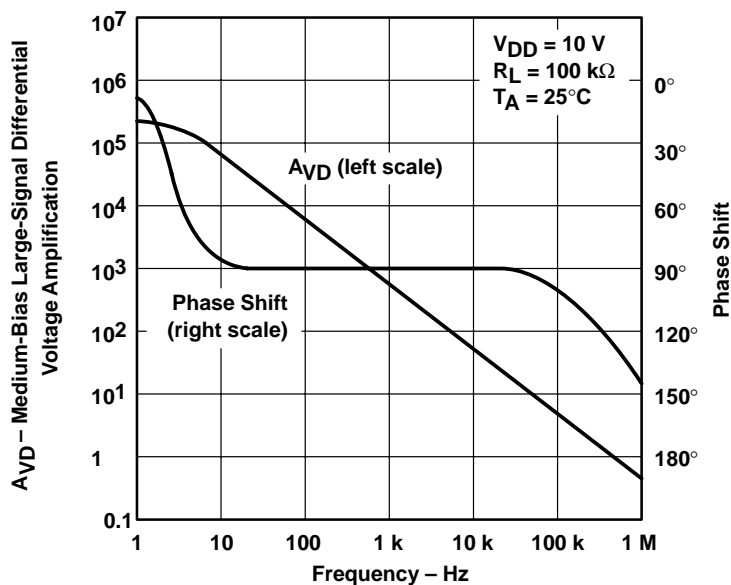
**TYPICAL CHARACTERISTICS**

**LOW-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT**  
**vs**  
**FREQUENCY**



**Figure 6**

**MEDIUM-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT**  
**vs**  
**FREQUENCY**

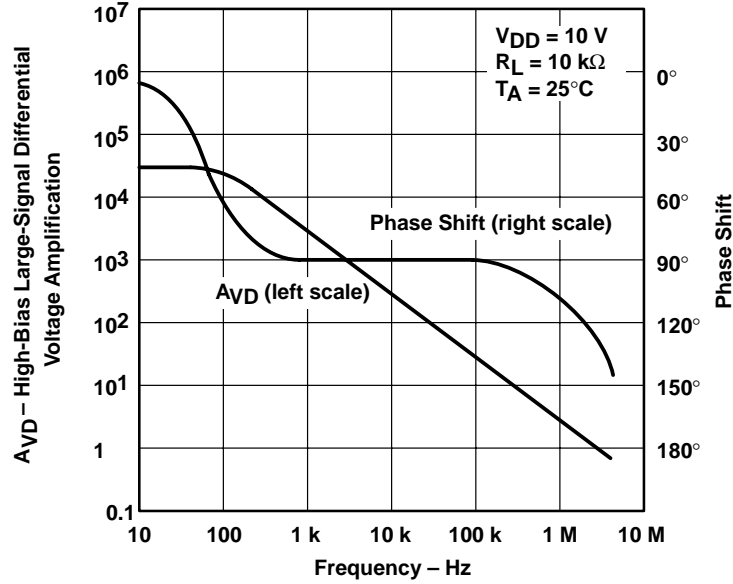


**Figure 7**



**TYPICAL CHARACTERISTICS**

**HIGH-BIAS LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 AND PHASE SHIFT  
 VS  
 FREQUENCY**



**Figure 8**

**TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B  
TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y  
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**APPLICATION INFORMATION****latch-up avoidance**

Junction-isolated CMOS circuits have an inherent parasitic PNP structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifiers supplies should be established simultaneously with, or before, application of any input signals.

**output stage considerations**

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage ( $V_{OH}$ ) is virtually independent of the  $I_{DD}$  selection and increases with higher values of  $V_{DD}$  and reduced output loading. The low-level output voltage ( $V_{OL}$ ) decreases with reduced output current and higher input common-mode voltage. With no load,  $V_{OL}$  is essentially equal to the potential of  $V_{DD-}/GND$ .

**supply configurations**

Even though the TLC25\_4C series is characterized for single-supply operation, they can be used effectively in a split-supply configuration if the input common-mode voltage ( $V_{ICR}$ ), output swing ( $V_{OL}$  and  $V_{OH}$ ), and supply voltage limits are not exceeded.

**circuit layout precautions**

Whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup as well as excessive dc leakages.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC254ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254AC	<a href="#">Samples</a>
TLC254BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254BC	<a href="#">Samples</a>
TLC254BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC254BCN	<a href="#">Samples</a>
TLC254CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254C	<a href="#">Samples</a>
TLC254CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	<a href="#">Samples</a>
TLC254CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	<a href="#">Samples</a>
TLC25L4BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	25L4BC	<a href="#">Samples</a>
TLC25L4CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25L4C	<a href="#">Samples</a>
TLC25M4CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25M4C	<a href="#">Samples</a>
TLC25M4CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC25M4CN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

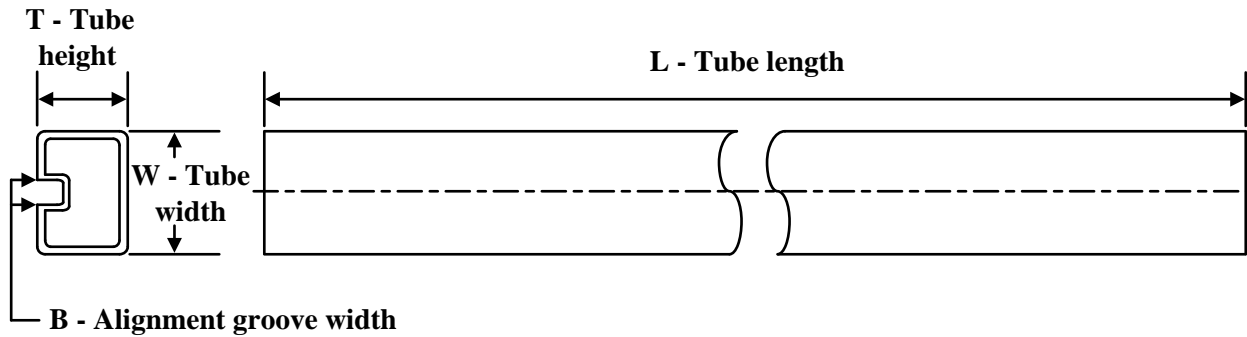
<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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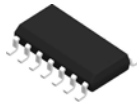


## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC254ACD	D	SOIC	14	50	505.46	6.76	3810	4
TLC254BCD	D	SOIC	14	50	505.46	6.76	3810	4
TLC254BCN	N	PDIP	14	25	506	13.97	11230	4.32
TLC254CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC254CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC254CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLC25L4BCD	D	SOIC	14	50	505.46	6.76	3810	4
TLC25L4CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC25M4CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC25M4CN	N	PDIP	14	25	506	13.97	11230	4.32

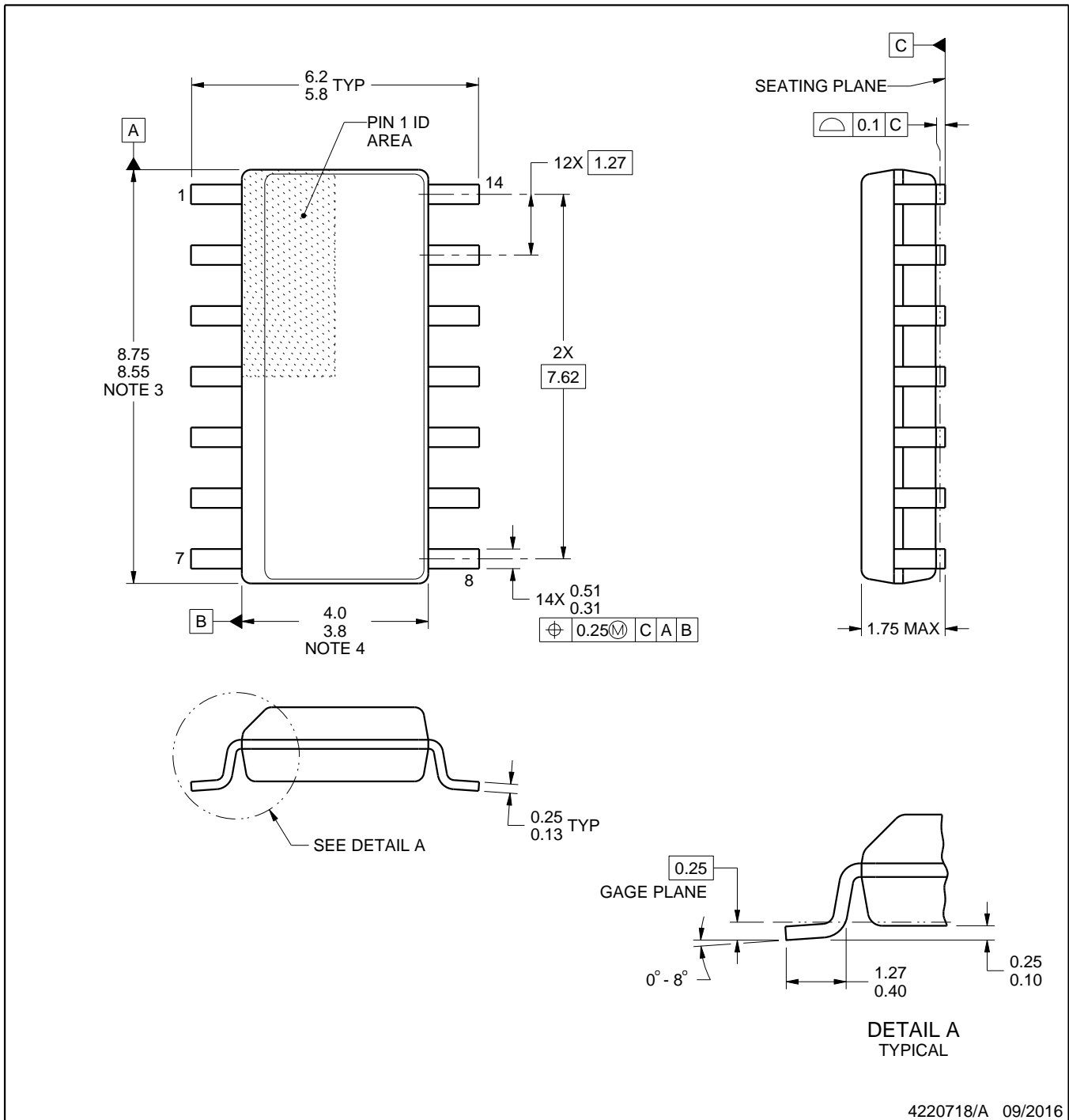


D0014A

## PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

## NOTES:

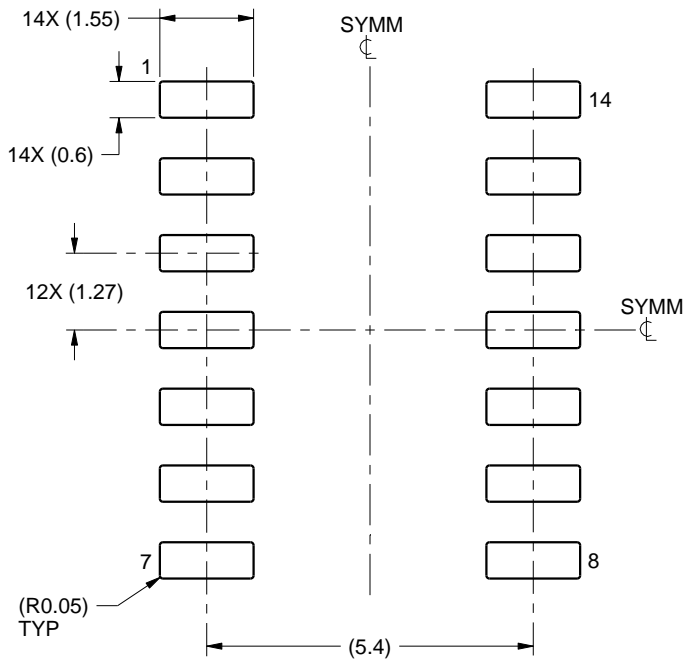
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

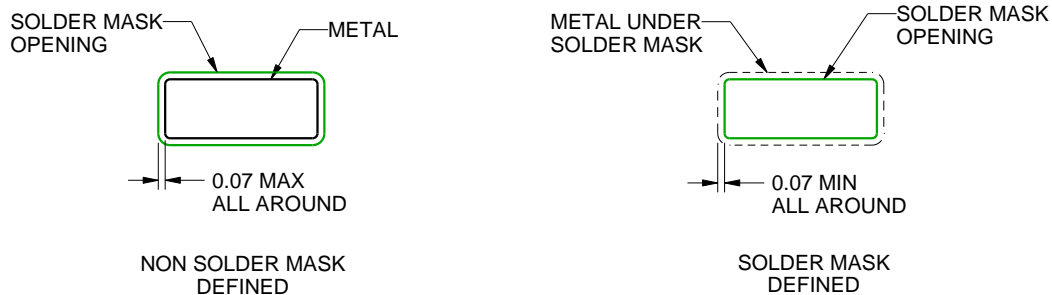
**D0014A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

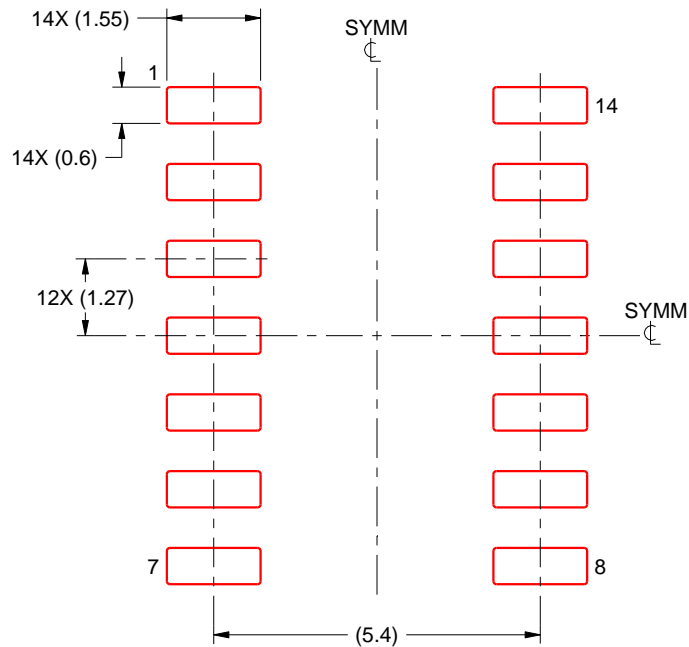
4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****D0014A****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:8X

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NOTES: (continued)

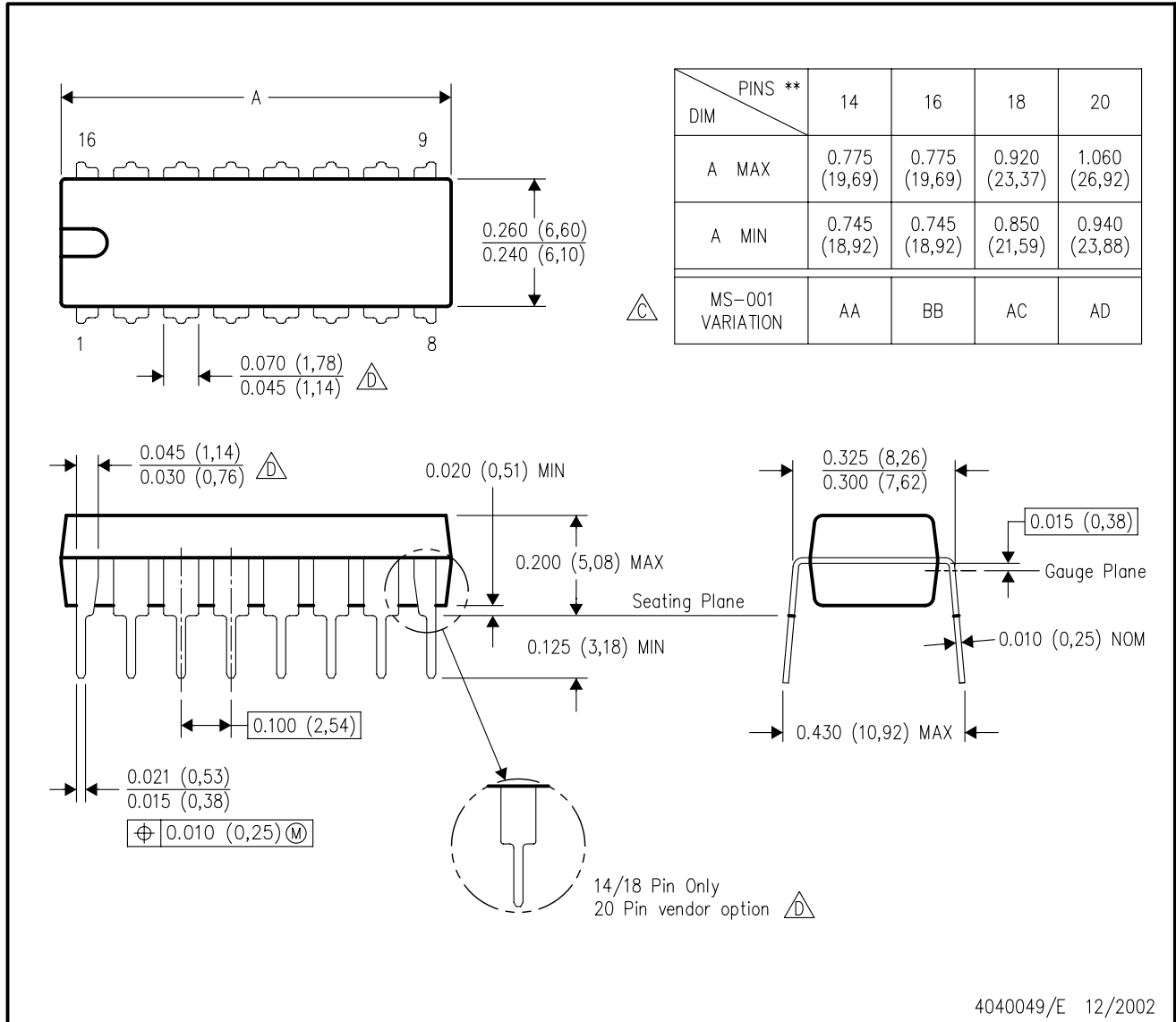
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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