

TLC352IDR Datasheet

www.digi-electronics.com

Ν



DiGi Electronics Part Number	TLC352IDR-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	TLC352IDR
Description	IC COMPARATOR 2 DIFF 850IC
Detailed Description	Comparator Differential CMOS, MOS, Open-Drain, T TL 8-SOIC

https://www.DiGi-Electronics.com



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
TLC352IDR	Texas Instruments
Series:	Product Status:
LinCMOS™	Active
Туре:	Number of Elements:
Differential	2
Output Type:	Voltage - Supply, Single/Dual (±):
CMOS, MOS, Open-Drain, TTL	1.4V ~ 16V, ±0.7V ~ 8V
Voltage - Input Offset (Max):	Current - Input Bias (Max):
5mV @ 5V	5pA @ 5V
Current - Output (Typ):	Current - Quiescent (Max):
20mA	400µA
CMRR, PSRR (Typ):	Propagation Delay (Max):
Hysteresis:	Operating Temperature:
	-40°C ~ 85°C
Package / Case:	Mounting Type:
8-SOIC (0.154", 3.90mm Width)	Surface Mount
Supplier Device Package:	Base Product Number:
8-SOIC	TLC352

Environmental & Export classification

RoHS Status:
ROHS3 Compliant
REACH Status:
REACH Unaffected
HTSUS:
8542.39.0001

Moisture Sensitivity Level (MSL):
1 (Unlimited)
ECCN:
EAR99

.. . .

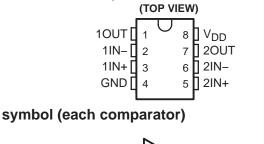
LinCMOS[™] DUAL DIFFERENTIAL COMPARATOR

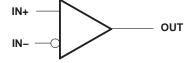
SLCS016A - SEPTEMBER 1985 - REVISED SEPTEMBER 2002

TLC352C, TLC352I . . . D OR P PACKAGE

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages 1.5 V to 18 V
- Very Low Supply Current Drain 150 μA Typ at 5 V 65 μA Typ at 1.4 V
- Built-In ESD Protection
- High Input Impedance . . . $10^{12} \Omega$ Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/ Month, Including the First 30 Days
- Common-Mode Input Voltage Range Includes Ground
- Outputs Compatible With TTL, MOS, and CMOS
- Pin-Compatible With LM393

description





This device is fabricated using LinCMOS[™] technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10¹² Ω), which allows direct interface to high-impedance sources. The output are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC352C is characterized for operation from 0° C to 70° C. The TLC352I is characterized for operation over the industrial temperature range of -40° C to 85° C.

	, ((), (12) (12)		
	Mar mov	PACH	AGE
Τ _Α	V _{IO} max AT 25°C	SMALL-OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC352CD	TLC352CP
– 40°C to 85°C	5 mV	TLC352ID	TLC352IP

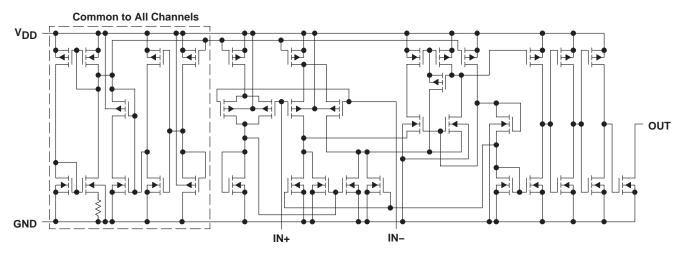
AVAILABLE OPTIONS

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC352 CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

SLCS016A - SEPTEMBER 1985 - REVISED SEPTEMBER 2002

equivalent schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1)	18 V
Differential input voltage, VID (see Note 2)	± 18 V
Input voltage, V _I	
Input voltage range, V _I	– 0.3 V to 18 V
Output voltage, V _O	18 V
Input current, I	$\ldots \pm 5 \text{ mA}$
Output current, I _O	
Duration of output short circuit to ground (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, TA TLC352C	0°C to 70°C
TLC352I	– 40°C to 85°C
Storage temperature range	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P p	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values except differential voltages are with respect to the network ground.
 - 2. Differential voltages are at IN+ with respect to IN -.
 - 3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T _A	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW
P	500 mW	N/A	N/A	500 mW	500 mW



					TLC352C	52C	TLC352	121	
					NIW	MAX	MIN	MAX	UNIT
Supply	Supply voltage, VDD				1.4	16	1.4	16	>
	VDD = 5 V				0	3.5	0	3.5	>
E muon	Common-mode input vortage, vIC				0	8.5	0	8.5	>
Operat	Operating free-air temperature, TA				0	70	- 40	85	ů
electr	electrical characteristics at specified free-air ten	free-air temperature, V _{DD} = 1.4 V (unless otherwise noted)	(unless o	therwise no	ted)				
			+	TLC352C		F	TLC352I		
	PARAMETER	TEST CONDITIONS	TAT	ΜΙΝ ΤΥΡ	MAX	MIN	ТҮР	MAX	LIND
			25°C	2	5		2	5	
01/	Input onset vonage	VIC = VICR MIN, See Note 4	Full range		6.5			7	> E
-			25°C	1			٢		рA
0	Input onset current		MAX		0.3			1	hA
_			25°C	5			5		рA
8	Input plas current		MAX		0.6			2	hA
VICR	Common-mode input voltage range		Full range	0 to 0.2		0 to 0.2			>
	المنبد المنبعا منطعينات المستعلمين		25°C	100	200		100	200	//
NOL	Low-level output voltage		Full range		200			200	> E
loL	Low-level output current	$V_{ID} = -0.5 V$, $V_{OL} = 0.3 V$	25°C	1 1.6		٦	1.6		mА
(Cumply Auron (Auro componentare)		25°C	65	150		65	150	۷.,
מטי	ouppry current (two comparators)		Full range		200			200	ς μ
† All ch ⁱ See P NOTE 4	† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, – 40°C to 85°C for TLC352I. IMPORTANT: See Parameter Measurement Information. NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and Vnn. They	e unless otherwise noted. Full ran ed to drive the output above 1.25 \	ige is 0°C to 7 V or below 150	0°C for TLC352C mV with a 10-kΩ	t, - 40°C 2 resistor	to 85°C fo between t	or TLC35 the outpu	21. IMPC t and Vr	DRTANT: DD. They
	can be verified by applying the limit value to the input and checking for the appropriate output state.	ecking for the appropriate output s	state.				-	1	,

recommended operating conditions



TLC352 LinCMOS™ DUAL DIFFERENTIAL COMPARATOR

SLCS016A - SEPTEMBER 1985 - REVISED SEPTEMBER 2002

Template Release Date: 7–11–94 TLC352IDR Texas Instruments IC COMPARATOR 2 DIFF 8SOIC TLC352

LinCMOSTM DUAL DIFFERENTIAL COMPARATOR

SLCS016A - SEPTEMBER 1985 - REVISED SEPTEMBER 2002

	elect	electrical characteristics at specified		free-air temperature, V _{DD} = 5 V (unless otherwise noted)	ure, V _{DD} =	5 V (unle	ss otherw	ise note	(þ			
FARAMELEX IEST COMUTIONS AI MIN TYP V[O< Input offset voltage V[C = V[CR min, See Note 5 Edit range 1 I/O Input offset voltage V[C = V[CR min, See Note 5 Edit range 1 I/O Input offset voltage N/AX 25°C 0.0 V[CR Common-mode input voltage range 25°C VDD-1 V[CR Common-mode input voltage range 25°C VDD-1 V[CR Common-mode input voltage range 25°C VDD-1 V[D V V[D = 1 V, VDI = 25°C 0.0 VOL Low-level output voltage range VID = 1 V, 25°C 0.0 VID VID = 1 V, VDI = 25°C 6 10 Low-level output voltage VID = 1 V, 25°C 6 10 Low-level output voltage VID = 1 V, 25°C 6 10 Low-level output voltage mater VID = 1 V, 25°C 6 10 See Stander Massavered with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C						+	TLC:	352C		TLC352I		
VIC Input offset voltage		PAKAM	IE I EK	IESI CON	SNOILIG	IAI	MIN	TYP MAX		MIN TYP	MAX	
VIO Input offset current VIC = VICR min, see Note 5 Full range Full range Full range Input offset current Io Input offset current ES°C VDD ES°C 010 VIC Romon-mode input voltage range ES°C VDD<-1	;					25°C		t	5	Ļ	5	
Input offset current 25° C 10 Input bias current 100 100 100 Input bias current 25° C 010 Input bias current 25° C 010 VICR Common-mode input voltage range 25° C 010 VICR Common-mode input voltage range 10° 25° C 010 VICR Common-mode input voltage range 10° 25° C 010 VIL Low-level output voltage 10° 25° C 010° VOL Low-level output voltage 10° 25° C 010° Indicateristics VID 10° 10° 25° C 010° Indicateristics VID 10° 10° 25° C 015° Indicateristics VID 10° 10° 25° C 015° Indicateristics VID 10° 10° 15° 15° C Indicateristics VID 10° 10° 15° 15° C Indicateristics VID 10° 10° 10° 10° Indicaterintic VID 10° 10°	0/2	Input offset voltage		VIC = VICR min,	See Note 5	Full range		9	6.5		7	> E
Ino Input bias current MAX MAX Input bias current 25° C 0 to Input bias current 25° C 0 to VICR Common-mode input voltage range 25° C 0 to VICR Common-mode input voltage range 10° 25° C 0 to VICR Common-mode input voltage range 10° 25° C 0° D VICR Low-level output current $VD = 1^{\circ}$ $VD = 1^{\circ}$ 0° VOL Low-level output current $VD = 1^{\circ}$ 0° 0° Vol Low-level output current $VD = 1^{\circ}$ 0° 0° Ioi Low-level output current $VD = 1^{\circ}$ 0° 0° Vol Low-level output current $VD = 1^{\circ}$ 0° 0° Ioi Suppt current $VD = 1^{\circ}$ $VD = 2^{\circ}$ 0° 0° Ioi Low-level output current $VD = 2^{\circ}$ $VD = 2^{\circ}$ 0° 0° Ioi Suppt current $VD = 2^{\circ}$ $VD = 2^{\circ}$ 0° 0° Ioi Ese Parameter Measurener Information. $VD = 2^{\circ}$ 0° 0° Ioi Constererere <td></td> <td></td> <td></td> <td></td> <td></td> <td>25°C</td> <td></td> <td>Ł</td> <td></td> <td>~</td> <td></td> <td>рА</td>						25°C		Ł		~		рА
Input blas current 25°C 5 MAX MAX MAX 6 VICR Common-mode input voltage range 25°C 0 to 0 to VICR Common-mode input voltage range 25°C 0 to 0 to 0 to VICR Common-mode input voltage range VID<=1V	0	Input offset current				MAX		C	0.3		1	nA
IIB Input bias outrent MAX						25°C		5		5		рА
Vick Common-mode input voltage range 25°C 010 0 to 0 to 0 to 0 to 0 to 0 to 0 to 0 t	8	Input blas current				MAX		C	0.6		2	hA
VICR Common-mode input votage range Full range 0 to $D_{DD} - 1.5$ IOH High-level output current VID = 1 V VOH = 5 V 25° C 0.1 IOH High-level output vottage VID = 1 V VDH = 15 V 25° C 6 160 VOL Low-level output voltage VID = 1 V, VDL = 4 mA 25° C 6 16 VOL Low-level output voltage VID = 1 V, VDL = 1.5 V 25° C 6 16 ID Supply current VID = 1 V, VDL = 1.5 V 25° C 6 16 ID Kitwo comparators) VID = 1 V, No load 25° C 6 16 ID Kitwo comparators) VID = 1 V, No load 25° C 6 16 TAI characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0° C to 70°C for TLC See Parameter Measurement Information. NDE = 5 7 A 25° C 6 76 TAI characteristics are measured with zero common-mode input voltage unless ofherwise noted. Full range is 0° C to 70°C for TLC See Parameter Measurement Information. NDE = 5 7 A 25° C 6	;					25°C	0 to VDD - 1		0 to VDD -	0 to DD - 1		:
	VICR		voltage range			Full range	0 to VDD - 1.5		0 VDD	0 to VDD - 1.5		>
IOH Tight-evel output current VID = 1 V VOH = 15 V Full range VOL Low-level output voltage VID = 1 V, IOL = 4 mA 25° C 6 16 VOL Low-level output current VID = 1 V, VID = 1.5 V 25° C 6 16 IoL Low-level output current VID = 1 V, VOL = 1.5 V 25° C 6 16 IbD Supply current VID = 1 V, No load 25° C 6 16 IbD Supply current VID = 1 V, No load 25° C 6 16 TAIL characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC 25°C 0.15 Tall characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC 25°C 0.15 Tall characteristics are measured with zero common-mode input add checking for the appropriate output state. 25°C 0.15 Supply output Tall characteristics are measured with zero common-mode input add checking for the appropriate output state. 25°C 0.15 Supply of the input add checking for the appropriate output state. 25°C 100-mV input step <t< td=""><td></td><td></td><td></td><td></td><td>11</td><td>25°C</td><td></td><td>0.1</td><td></td><td>0.1</td><td></td><td>hA</td></t<>					11	25°C		0.1		0.1		hA
VOL Low-level output voltage VID 1 V, IOL 4 MI range 55° c 160 IOL Low-level output current VID VID 1 V , 25° c 6 16 IOL Low-level output current VID 1 V , 10 Lev 25° c 6 16 IDD Supply current VID 1 V , No load 25° c 6 16 IDD Supply current VID 1 V , No load 25° c 6 16 Indo (wo comparators) VID 1 V , No load 25° c 6 16 Tall characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0° C to 70° C for TLC See Parameter Measurement Information. No load 25° c 70° C for 70° C for TLC State Parameter Measurement Information. No load 10° Full range is 0° C to 70° C for TLC See Parameter Measurement Information. 70° Full range is 0° C to 70° C for TLC State Parameter Measurement Information. No load 10° Full range is 0° C to 70° C for TLC	НО	High-level output curre		$\Lambda I = OI \Lambda$	VOH = 15 V	Full range			4		4	μA
VOL Low-terror output voltage VID = 1 V, IOL = 4 mA Full range IoL Low-tevel output current VID = 1 V, VOL = 1.5 V 25° C 6 16 IoL Low-tevel output current VID = 1 V, VoL = 1.5 V 25° C 6 16 IbD Supply current (two comparators) VID = 1 V, No load 25° C 6 16 T All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC See Parameter Measurement Information. No load 25° C 6 76 Te All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC See Parameter Measurement Information. No load 25° C 6 76 To be effect by applying the limit value to the input and checking for the appropriate output state. No noted to 5 V, TA = 25°C Full range is 0°C to 70°C to 70°						25°C			400	150	400	, , , , , , , , , , , , , , , , , , , ,
Iol_ Low-level output current VID = -1 V, VOL = 1.5 V 25°C 6 16 IbD Supply current (two comparators) VID = 1 V, No load 25° C 6 16 T All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC See Parameter Measurement Information. NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input and checking for the appropriate output state. NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input and checking for the appropriate output state. POCE 5. NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input above 4 V or below 400 mV with a 10-can be verified by th	VOL	LOW-IEVEI OUIDUI VOILA	le	VID = 1 V,	10L = 4 IIIA	Full range		7(700		700	NII N
$\begin{tabular}{ l]{l} ll l$	loL	Low-level output curre	nt		VOL = 1.5 V	25°C	9	16	•	6 16		mA
DD (two comparators) VID = 1 v, VID = 1 v, Full range 1 All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC: See Parameter Measurement Information. Full characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC: See Parameter Measurement Information. NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input and checking for the appropriate output state. Full characteristics, VDD = 5 V, TA = 25°C Switching characteristics, VDD = 5 V, TA = 25°C Test conditions Test conditions Response time RL connected to 5 V through 5.1 kQ, Test conditions Response time CL = 15 pF‡, See Note 6 TL-level input step with 5-mV overdrive		Supply current		\\ F =\\		25°C			0.3	0.15	0.3	< *
¹ All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC. See Parameter Measurement Information. NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input and checking for the appropriate output state. NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-can be verified by applying the limit value to the input and checking for the appropriate output state. Switching characteristics, VDD = 5 V, T _A = 25°C Response time TEST CONDITIONS Response time RL connected to 5 V through 5.1 kΩ, TeST CONDITIONS CL = 15 pF‡, See Note 6 TL-level input step with 5-mV overdrive	מחי	(two comparators)		VID = 1 V,		Full range		C	0.4		0.4	
switching characteristics, V _{DD} = 5 V, T _A = 25°C PARAMETER PARAMETER TEST CONDITIONS Response time RL connected to 5 V through 5.1 kQ, not input step with 5-mV overdrive CL = 15 pF‡, See Note 6 100-mV input step with 5-mV overdrive ‡CL includes probe and jig capacitance. An input step with 5-mV overdrive	† All ch See F NOTE	aracteristics are measur. Parameter Measurement 5: The offset voltage lim can be verified by ap	ed with zero common-mode in Information. its given are the maximum val plying the limit value to the inp	nput voltage unless lues required to driv put and checking fo	otherwise noted e the output abc r the appropriate	 Full range is ove 4 V or belc e output state. 	0°C to 70°C fr w 400 mV with	or TLC352C h a 10-kΩ re	, – 40°C t sistor bet	o 85°C for TLC ween the outpu	352I. IMP	ORTANT: . They
PARAMETER TEST CONDITIONS Parameter TEST CONDITIONS Response time RL connected to 5 V through 5.1 kΩ,, Response time 0.2 = 15 pF‡, CL = 15 pF‡, See Note 6 ‡ CL includes probe and jig capacitance.	swite	thing characteris	5 <,	= 25∘C								
PARAMETER TEST CONDITIONS Response time RL connected to 5 V through 5.1 kΩ, 100-mV input step with 5-mV overdrive Response time CL = 15 pF‡, See Note 6 TTL-level input step ‡ CL includes probe and jig capacitance. ************************************										TLC352C, TLC352I	C352I	
RL connected to 5 V through 5.1 kΩ, 100-mV input step with 5-mV overdrive Response time CL = 15 pF‡, See Note 6 TTL-level input step [‡] CL includes probe and jig capacitance. Nontr for the include the inc		PARAMETER		TE	EST CONDITIO	NS			<u> </u>	MIN TYP	MAX	LIND
* Composition of the spectrum	Doc	time		jh 5.1 kΩ,,	100-mV inpu	it step with 5-r	nV overdrive			650		ů
t CL includes probe and jig capacitance.			CL = 15 pF‡,	See Note 6	TTL-level inp	out step				200		2
NUTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.	‡ c∟ in NOTE	cludes probe and jig cap 3: The response time s	acitance. pecified is the interval betweer	in the input step fun	ction and the ins	stant when the) output crosse	s 1.4 V.				



SLCS016A - SEPTEMBER 1985 - REVISED SEPTEMBER 2002

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

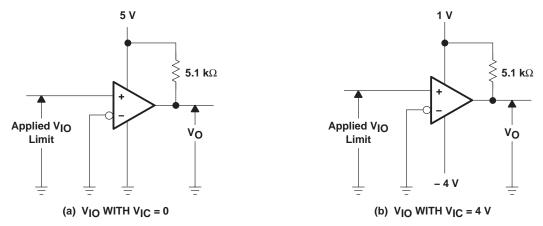


Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits



SLCS016A - SEPTEMBER 1985 - REVISED SEPTEMBER 2002

PARAMETER INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

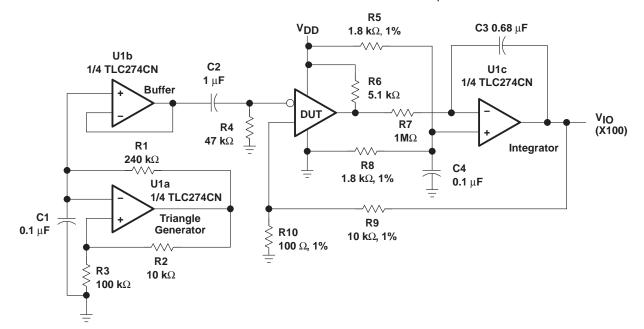


Figure 2. Circuit for Input Offset Voltage Measurement



SLCS016A - SEPTEMBER 1985 - REVISED SEPTEMBER 2002

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.

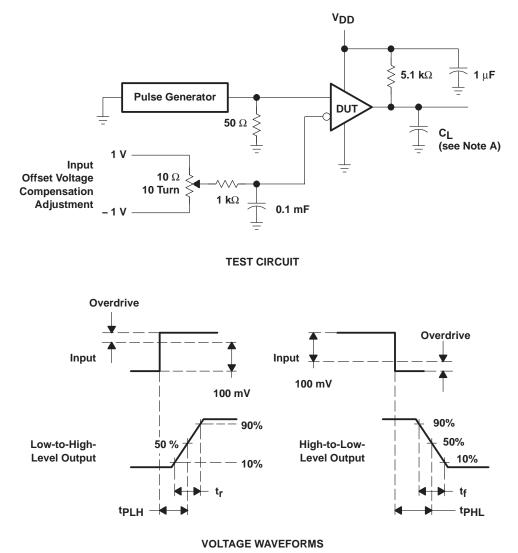




Figure 3. Response, Rise, and Fall Times Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
TLC352CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	352C	
TLC352CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	352C	Samples
TLC352CP	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC352CP	Samples
TLC352ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	3521	
TLC352IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3521	Samples
TLC352IDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TLC352IP	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC352IP	Samples
TLC352IPW	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	P352I	
TLC352IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P352I	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

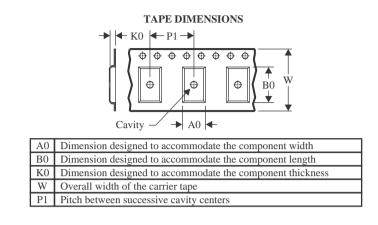
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



25-Sep-2024

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	-	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC352CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

25-Sep-2024



*All dimensions are nominal

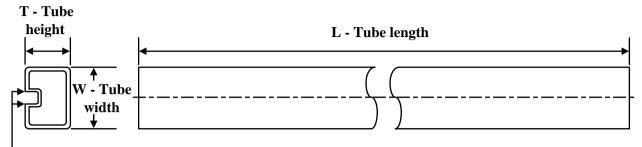
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC352CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC352IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC352IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC352IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0



PACKAGE MATERIALS INFORMATION

25-Sep-2024

TUBE



- B - Alignment groove width

*All dimensions are nominal

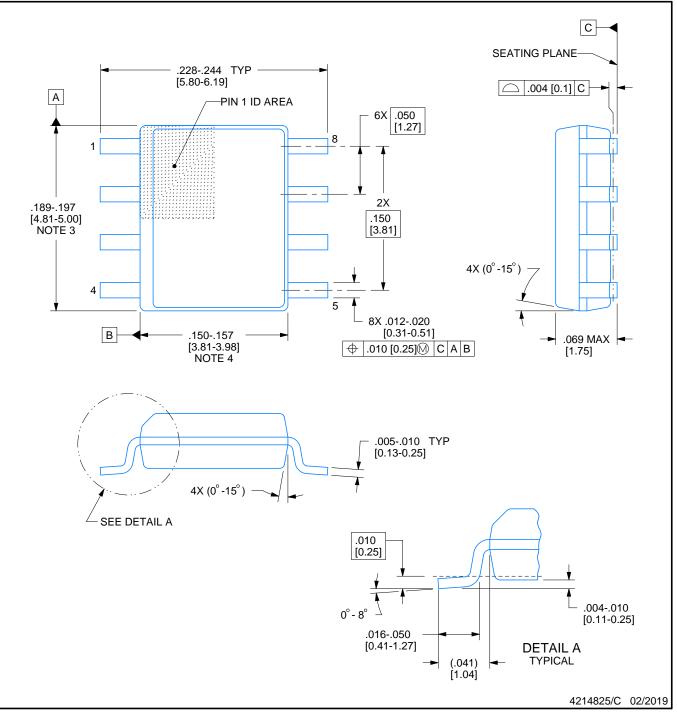
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
TLC352CP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC352IP	Р	PDIP	8	50	506	13.97	11230	4.32



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.

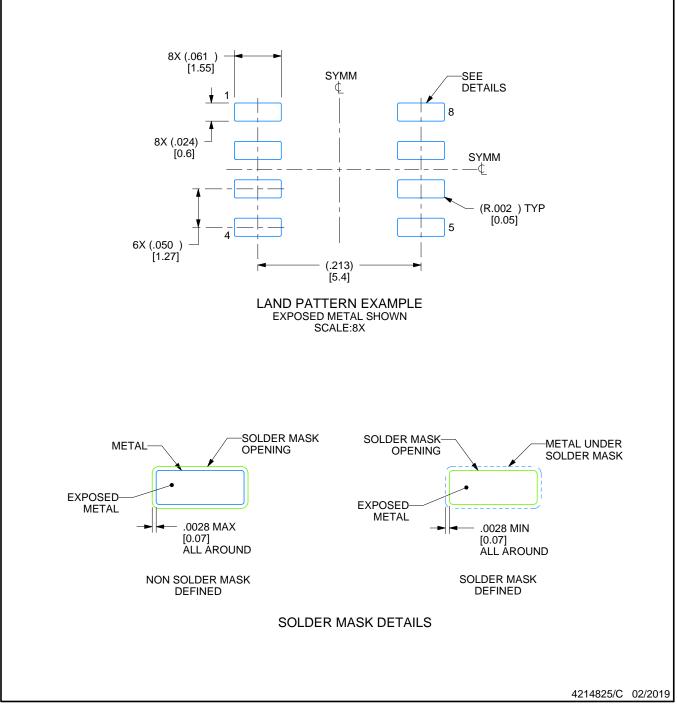


D0008A

EXAMPLE BOARD LAYOUT

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

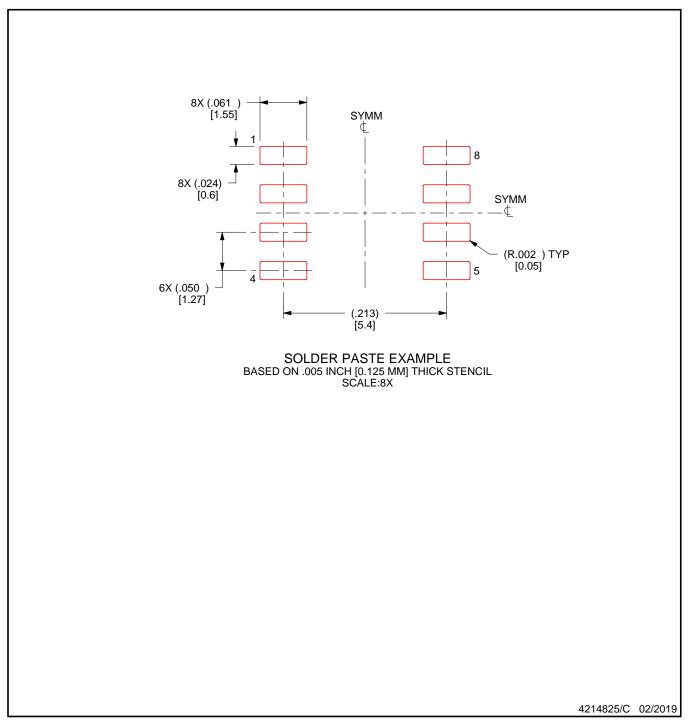


D0008A

EXAMPLE STENCIL DESIGN

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

P(R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear almensions are in incres (millimeters).B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

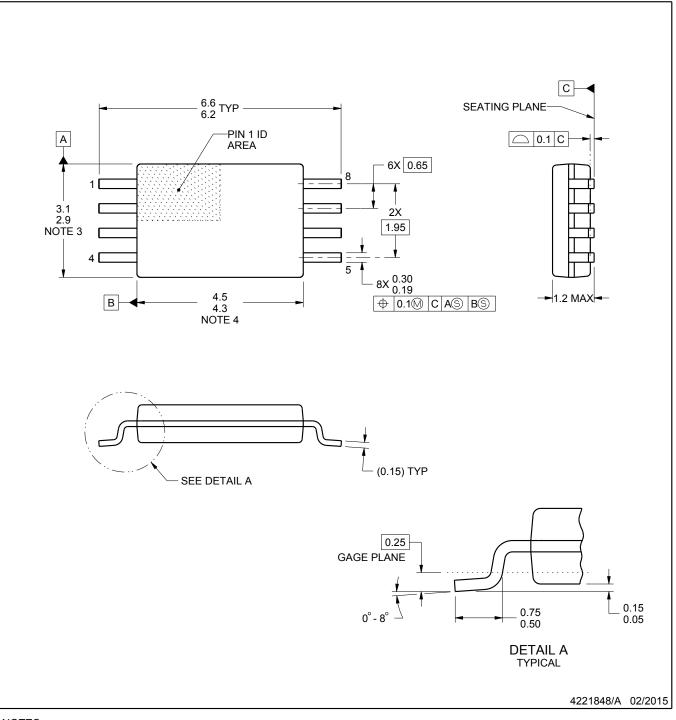


PW0008A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

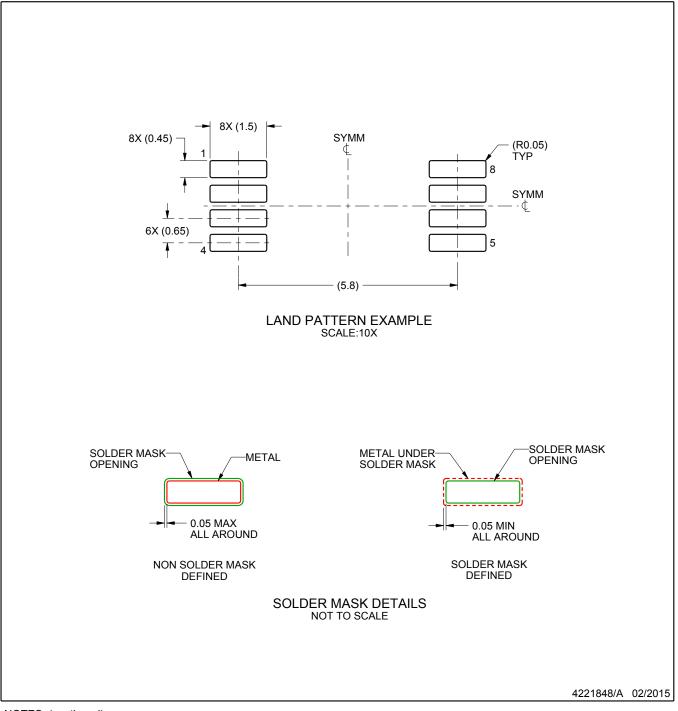
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

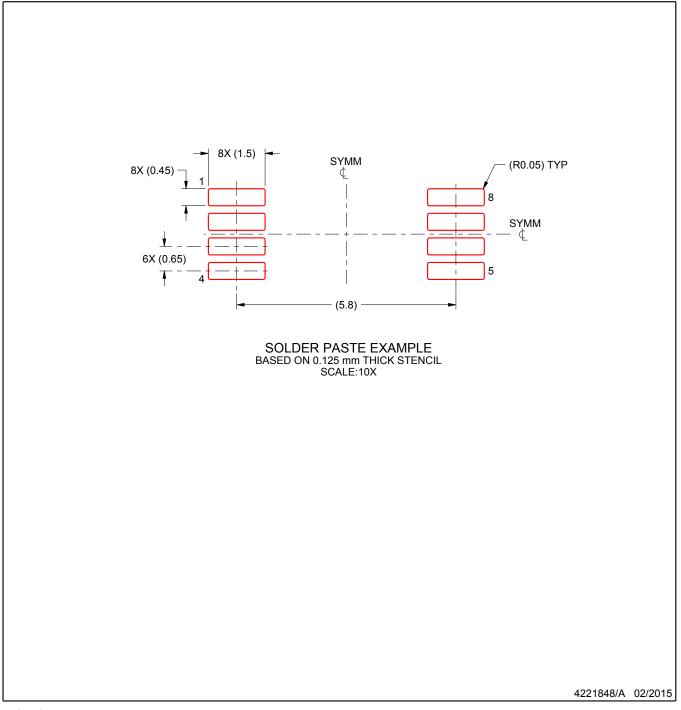
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

9. Board assembly site may have different recommendations for stencil design.



^{8.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2024, Texas Instruments Incorporated



OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we striciy control the quality of products and services. Welcome your RFQ to Email: Info@DiGi-Electronics.com

	<section-header></section-header>		
Marginary Marginary Marginary	Market	Marchine Marchine Image: Control of the sector of the sec	





Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.