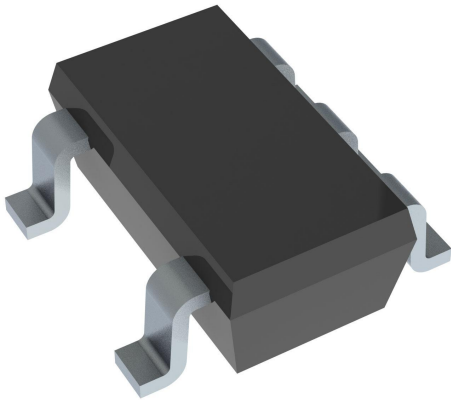


TLV2211CDBVT Datasheet

www.digi-electronics.com



TLV2211CDBVT

<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	TLV2211CDBVT-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	TLV2211CDBVT
Description	IC OPAMP GP 1 CIRCUIT SOT23-5
Detailed Description	General Purpose Amplifier 1 Circuit Rail-to-Rail SOT-23-5



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

TLV2211CDBVT

Series:

LinCMOST™

Amplifier Type:

General Purpose

Output Type:

Rail-to-Rail

Gain Bandwidth Product:

65 kHz

Voltage - Input Offset:

450 μ V

Current - Output / Channel:

50 mA

Voltage - Supply Span (Max):

10 V

Mounting Type:

Surface Mount

Supplier Device Package:

SOT-23-5

Manufacturer:

Texas Instruments

Product Status:

Last Time Buy

Number of Circuits:

1

Slew Rate:

0.025V/ μ s

Current - Input Bias:

1 pA

Current - Supply:

13 μ A

Voltage - Supply Span (Min):

2.7 V

Operating Temperature:

0°C ~ 70°C

Package / Case:

SC-74A, SOT-753

Base Product Number:

TLV2211

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.33.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

TLV2211, TLV2211Y

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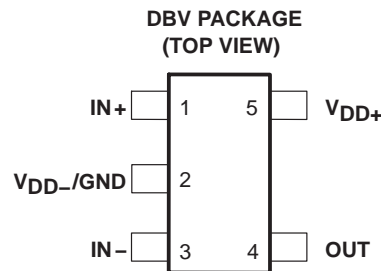
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- Output Swing Includes Both Supply Rails
- Low Noise . . . 21 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Very Low Power . . . 11 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Wide Supply Voltage Range 2.7 V to 10 V
- Available in the SOT-23 Package
- Macromodel Included

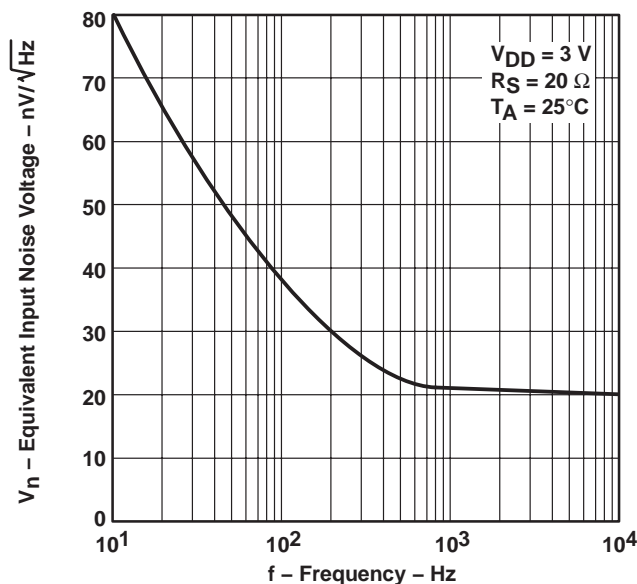
description

The TLV2211 is a single low-voltage operational amplifier available in the SOT-23 package. It consumes only 11 μA (typ) of supply current and is ideal for battery-power applications. Looking at Figure 1, the TLV2211 has a 3-V noise level of 22 nV/√Hz at 1kHz; 5 times lower than competitive SOT-23 micropower solutions. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2211 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2211, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).



EQUIVALENT INPUT NOISE VOLTAGE†
VS
FREQUENCY



† All loads are referenced to 1.5 V.

Figure 1. Equivalent Input Noise Voltage Versus Frequency

AVAILABLE OPTIONS

T _A	V _{IOMax} AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM‡ (Y)
		SOT-23 (DBV)†		
0°C to 70°C	3 mV	TLV2211CDBV	VACC	TLV2211Y
-40°C to 85°C	3 mV	TLV2211IDBV	VACI	

† The DBV package available in tape and reel only.

‡ Chip forms are tested at T_A = 25°C only.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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description (continued)

With a total area of 5.6mm², the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces. TI has also taken special care to provide a pinout that is optimized for board layout (see Figure 2). Both inputs are separated by GND to prevent coupling or leakage paths. The OUT and IN– terminals are on the same end of the board to provide negative feedback. Finally, gain setting resistors and decoupling capacitor are easily placed around the package.

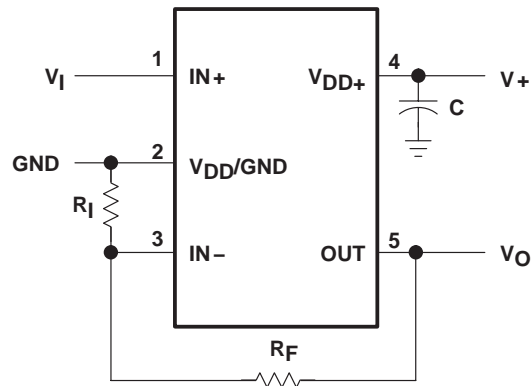
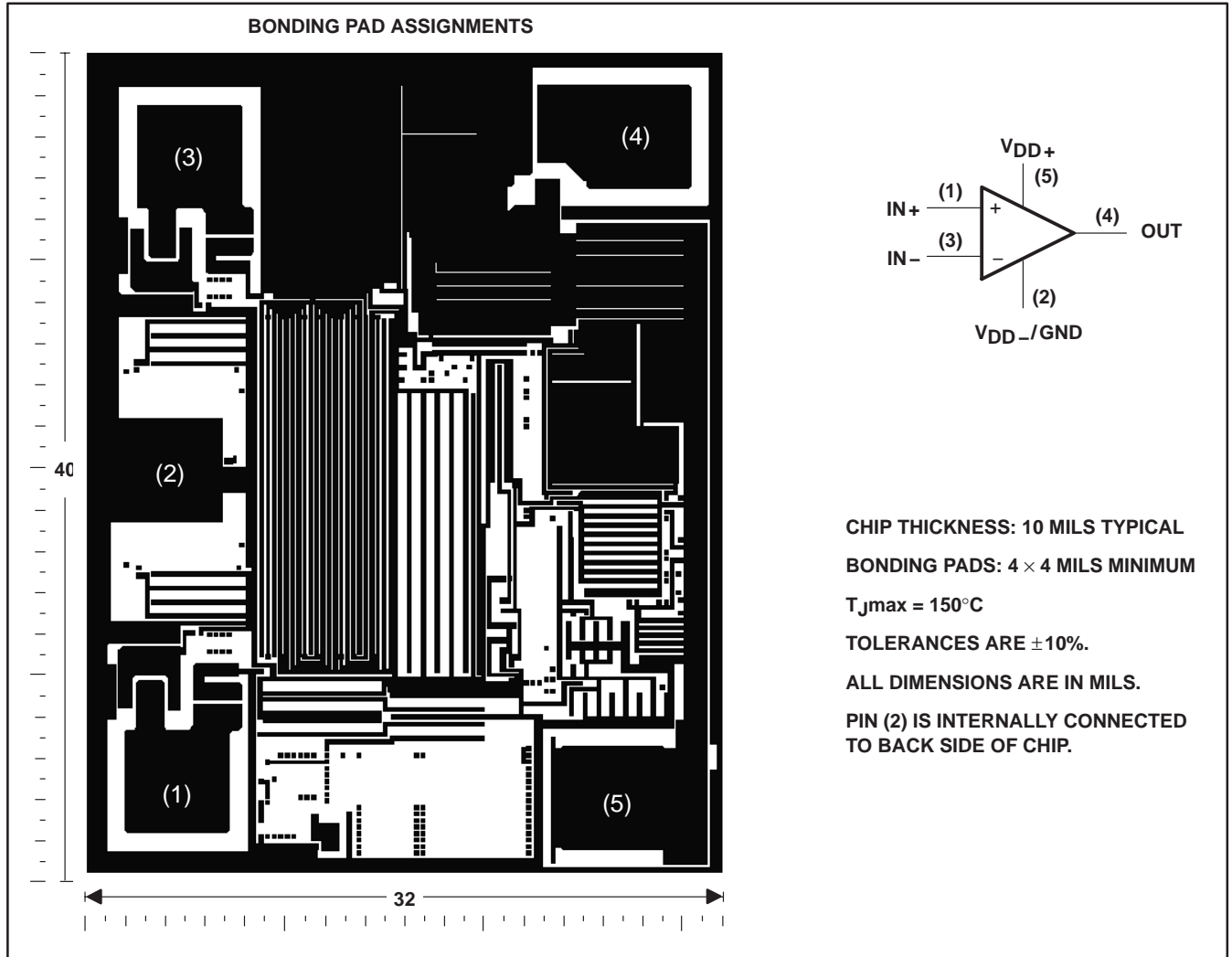


Figure 2. Typical Surface Mount Layout for a Fixed-Gain Noninverting Amplifier

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TLV2211Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2211C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.



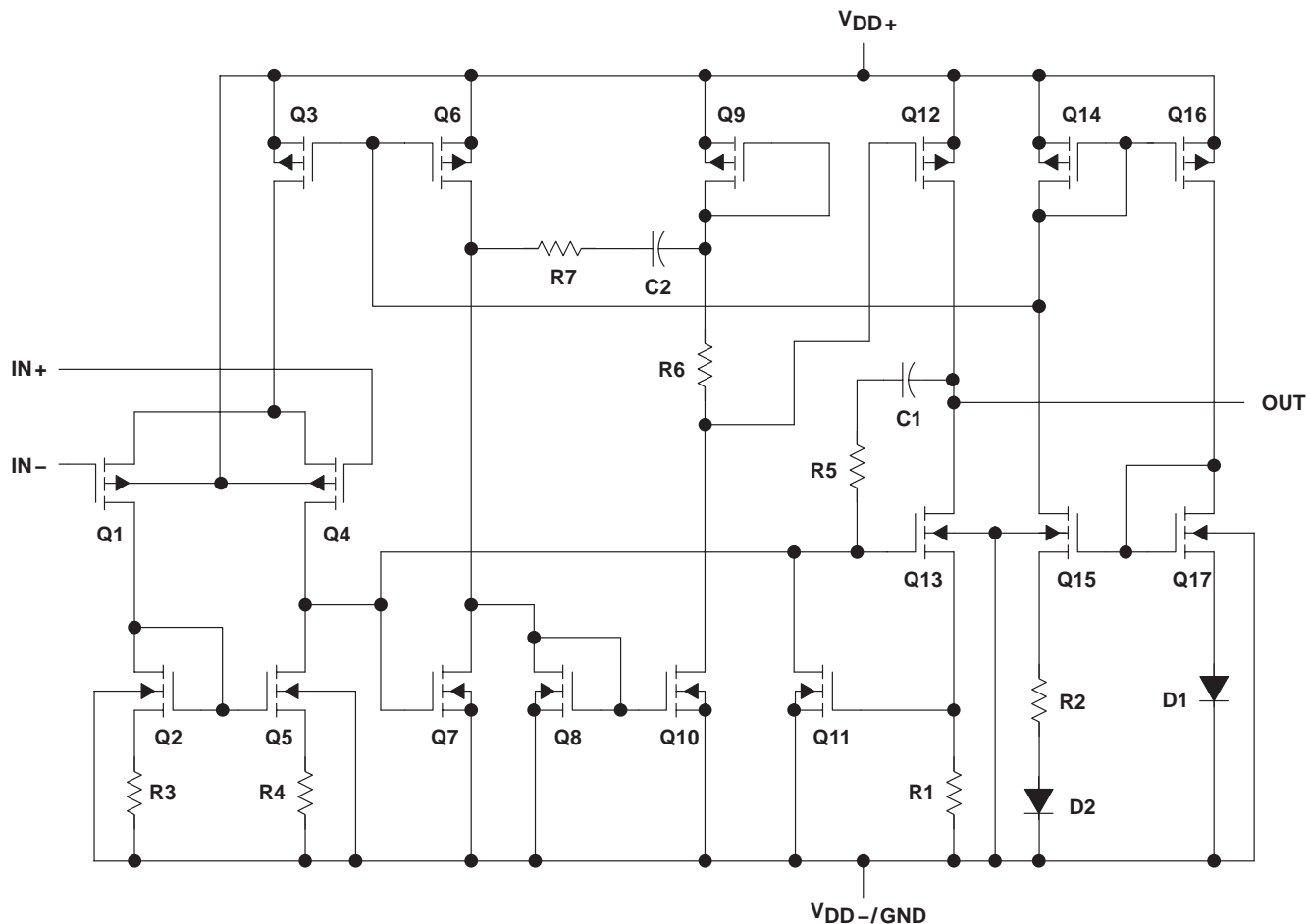
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equivalent schematic



COMPONENT COUNT†	
Transistors	23
Diodes	6
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	-0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLV2211C	0°C to 70°C
TLV2211I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values, except differential voltages, are with respect to V_{DD-} .
 - Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
 - The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2211C		TLV2211I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	-40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .

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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2211C			TLV2211I			UNIT		
			MIN	TYP	MAX	MIN	TYP	MAX			
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	Full range	0.47		3	0.47		3	mV		
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage			1		1		$\mu\text{V}/^\circ\text{C}$				
Input offset voltage long-term drift (see Note 4)			25°C		0.003		0.003		$\mu\text{V}/\text{mo}$		
I_{IO} Input offset current			Full range		0.5		60	0.5		60	pA
I_{IB} Input bias current			Full range		1		60	1		60	pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2		V		
		Full range	0 to 1.7		0 to 1.7						
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -250\ \mu\text{A}$	25°C	2.94		2.94				V		
		25°C	2.85		2.85						
		Full range	2.5		2.5						
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	15		15				mV		
		25°C	150		150						
		Full range	500		500						
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to } 2\text{ V}$	25°C	3		7	3		7	V/mV		
			Full range	1		1					
		25°C	600		600						
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²		10 ¹²				Ω		
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²		10 ¹²				Ω		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	5		5				pF		
z_o Closed-loop output impedance	$f = 7\text{ kHz}$, $A_V = 1$	25°C	200		200				Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$, $R_S = 50\ \Omega$, $V_O = 1.5\text{ V}$	25°C	65	83		65	83		dB		
		Full range	60		60						
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, No load, $V_{IC} = V_{DD}/2$	25°C	80	95		80	95		dB		
		Full range	80		80						
I_{DD} Supply current	$V_O = 1.5\text{ V}$, No load	25°C	11	25		11	25		μA		
		Full range	30		30						

† Full range for the TLV2211C is 0°C to 70°C. Full range for the TLV2211I is -40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2211C			TLV2211I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 1.1\text{ V to }1.9\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.01	0.025		0.01	0.025		V/ μ s
		Full range	0.005			0.005			
V_n	Equivalent input noise voltage	f = 10 Hz	80			80			nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz	22			22			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	660			660			nV
		f = 0.1 Hz to 10 Hz	880			880			
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
	Gain-bandwidth product	f = 10 kHz, $C_L = 100\text{ pF}$ ‡	$R_L = 10\text{ k}\Omega$ ‡,	25°C		56			kHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡,	$A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C		7			kHz
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C		56°			
	Gain margin			25°C		20			dB

† Full range is -40°C to 85°C .

‡ Referenced to 1.5 V

TLV2211, TLV2211Y

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2211C			TLV2211I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	Full range	0.45 3			0.45 3			mV
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage			0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 5)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5 60			0.5 60			pA
		Full range	150			150			
I_{IB} Input bias current		25°C	1 60			1 60			pA
	Full range	150			150				
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$ $R_S = 50\ \Omega$	25°C	0 to 4 –0.3 to 4.2		0 to 4 –0.3 to 4.2		V		
		Full range	0 to 3.5		0 to 3.5				
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -250\ \mu\text{A}$	25°C	4.95			4.95			V
		25°C	4.875			4.875			
		Full range	4.5			4.5			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	12			12			mV
		25°C	120			120			
		Full range	500			500			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	25°C	$R_L = 10\text{ k}\Omega$ ‡		6 12		6 12		V/mV
			Full range		3		3		
		25°C	$R_L = 1\text{ M}\Omega$ ‡		800		800		
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²			Ω
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²			Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$,	25°C	5			5			pF
z_o Closed-loop output impedance	$f = 7\text{ kHz}$, $A_V = 1$	25°C	200			200			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $R_S = 50\ \Omega$, $V_O = 2.5\text{ V}$	25°C	70 83			70 83			dB
		Full range	70			70			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, No load, $V_{IC} = V_{DD}/2$	25°C	80 95			80 95			dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C	13 25			13 25			μA
		Full range	30			30			

† Full range for the TLV2211C is 0°C to 70°C. Full range for the TLV2211I is –40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2211, TLV2211Y

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2211C			TLV2211I			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = 1.5\text{ V to }3.5\text{ V}, R_L = 10\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$	25°C	0.01	0.025		0.01	0.025		V/ μs	
		Full range	0.005			0.005				
V_n	Equivalent input noise voltage	f = 10 Hz	72			72			nV/ $\sqrt{\text{Hz}}$	
		f = 1 kHz	21			21				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	600			600			nV	
		f = 0.1 Hz to 10 Hz	800			800				
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$	
	Gain-bandwidth product	f = 10 kHz, $C_L = 100\text{ pF}^\ddagger$	$R_L = 10\text{ k}\Omega^\ddagger,$ 25°C			65			kHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 10\text{ k}\Omega^\ddagger,$	$A_V = 1,$ $C_L = 100\text{ pF}^\ddagger$			25°C			7	kHz
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega^\ddagger,$	$C_L = 100\text{ pF}^\ddagger$			25°C			56°	56°
			25°C			22			22	
	Gain margin	25°C			22			22	dB	

† Full range is -40°C to 85°C .

‡ Referenced to 1.5 V

electrical characteristics at $V_{DD} = 3\text{ V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2211Y			UNIT	
		MIN	TYP	MAX		
V_{IO}	Input offset voltage	0.47			mV	
I_{IO}	Input offset current	0.5			60	
I_{IB}	Input bias current	1			60	
V_{ICR}	Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV},$ $R_S = 50\ \Omega$			-0.3 to 2.2	V
V_{OH}	High-level output voltage	$I_{OH} = -100\ \mu\text{A}$			2.94	V
		$I_{OH} = -200\ \mu\text{A}$			2.85	
V_{OL}	Low-level output voltage	$V_{IC} = 0,$ $I_{OL} = 50\ \mu\text{A}$			15	mV
		$V_{IC} = 0,$ $I_{OL} = 500\ \mu\text{A}$			150	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V},$ $V_O = 1\text{ V to }2\text{ V}$		$R_L = 10\text{ k}\Omega^\ddagger$	7	V/mV
				$R_L = 1\text{ M}\Omega^\ddagger$	600	
$r_{i(d)}$	Differential input resistance				10^{12}	Ω
$r_{i(c)}$	Common-mode input resistance				10^{12}	Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz			5	pF
z_o	Closed-loop output impedance	f = 7 kHz, $A_V = 1$		200		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V},$ $V_O = 1.5\text{ V},$ $R_S = 50\ \Omega$		83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load		95		dB
I_{DD}	Supply current	$V_O = 1.5\text{ V},$ No load		11		μA

† Referenced to 1.5 V

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electrical characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2211Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm = \pm 2.5\text{ V}$, $R_S = 50\ \Omega$ $V_{IC} = 0$, $V_O = 0$,	0.45			mV
I_{IO} Input offset current		0.5	60		pA
I_{IB} Input bias current		1	60		pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	-0.3 to 4.2			V
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$	4.95			V
	$I_{OH} = -250\ \mu\text{A}$	4.875			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	12			mV
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	120			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\dagger$	12		V/mV
		$R_L = 1\text{ M}\Omega^\dagger$	800		
$r_{i(d)}$ Differential input resistance		10^{12}			Ω
$r_{i(c)}$ Common-mode input resistance		10^{12}			Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	5			pF
z_o Closed-loop output impedance	$f = 7\text{ kHz}$, $A_V = 1$	200			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	83			dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	95			dB
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	13			μA

† Referenced to 1.5 V

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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2211
INPUT OFFSET VOLTAGE**

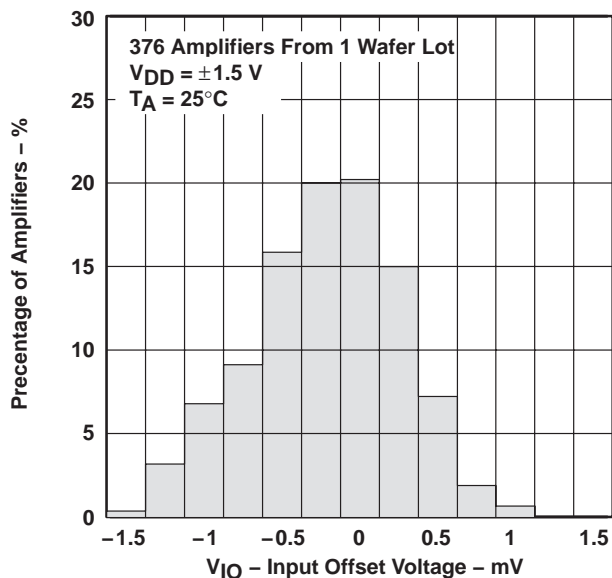


Figure 3

**DISTRIBUTION OF TLV2211
INPUT OFFSET VOLTAGE**

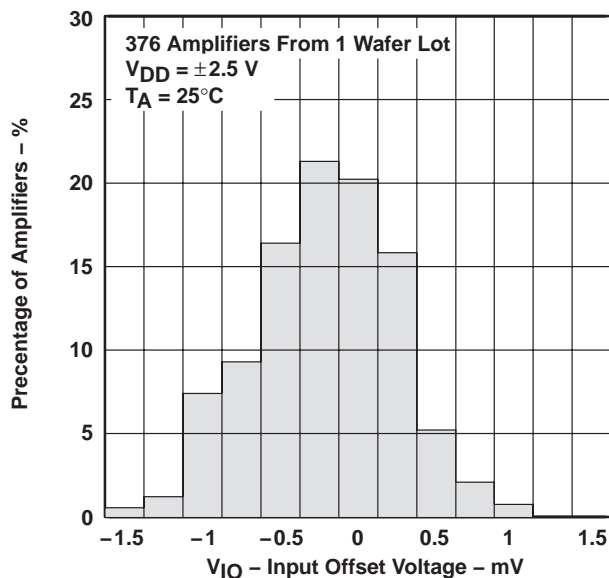


Figure 4

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

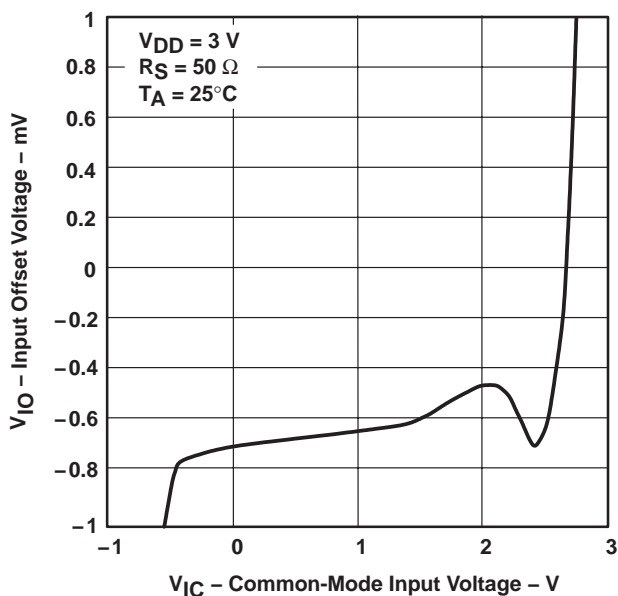


Figure 5

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

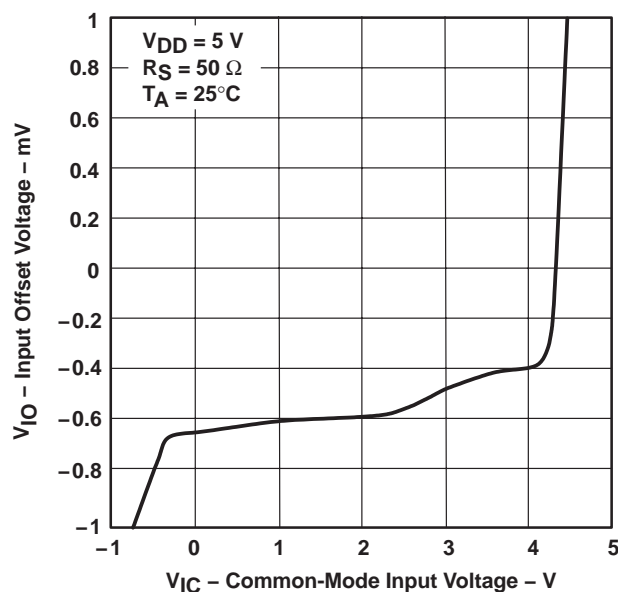


Figure 6

† For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

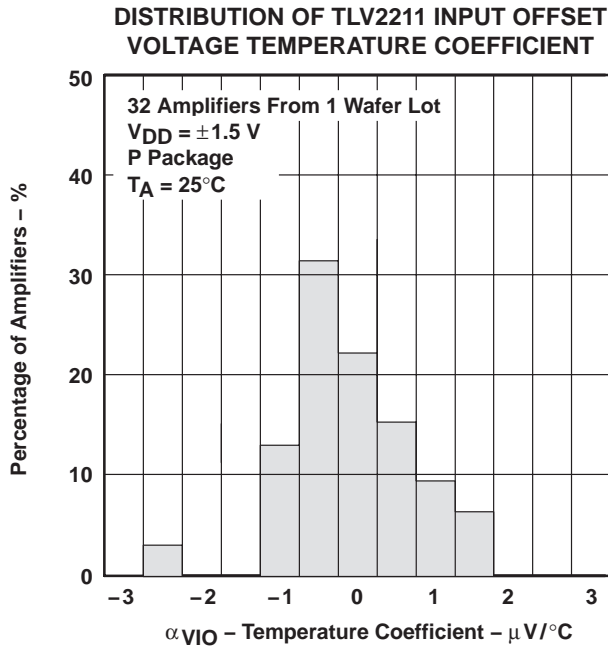


Figure 7

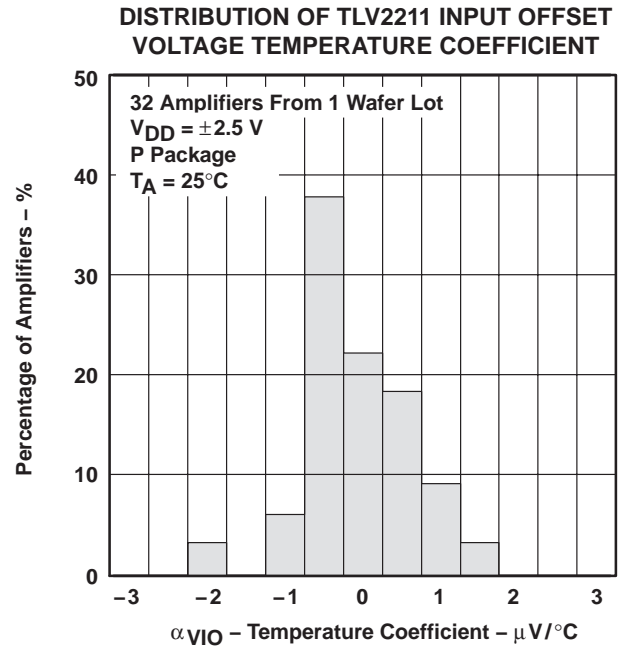


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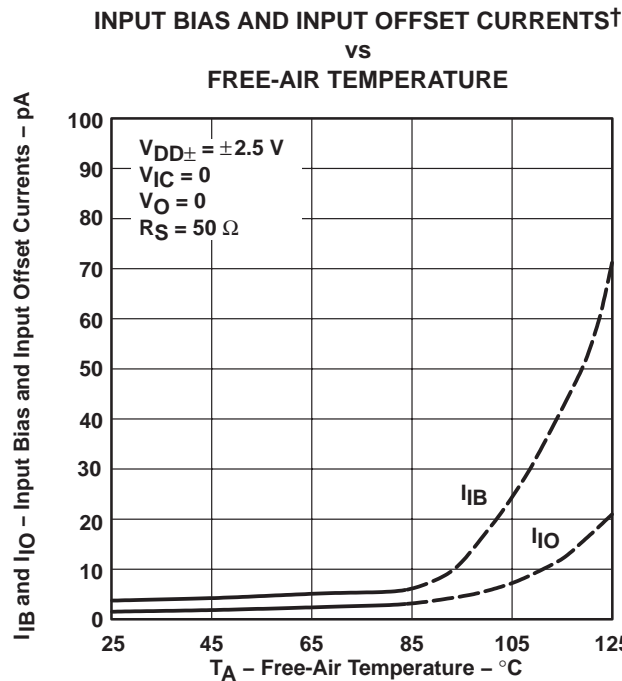


Figure 9

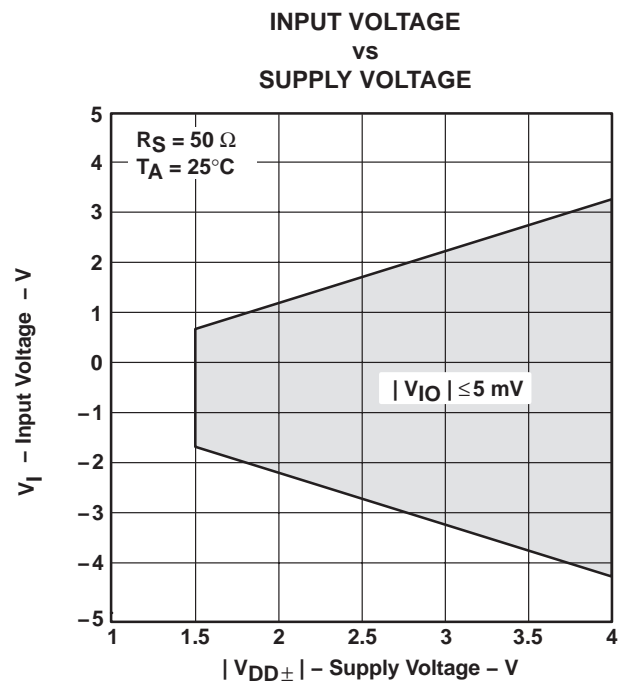


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

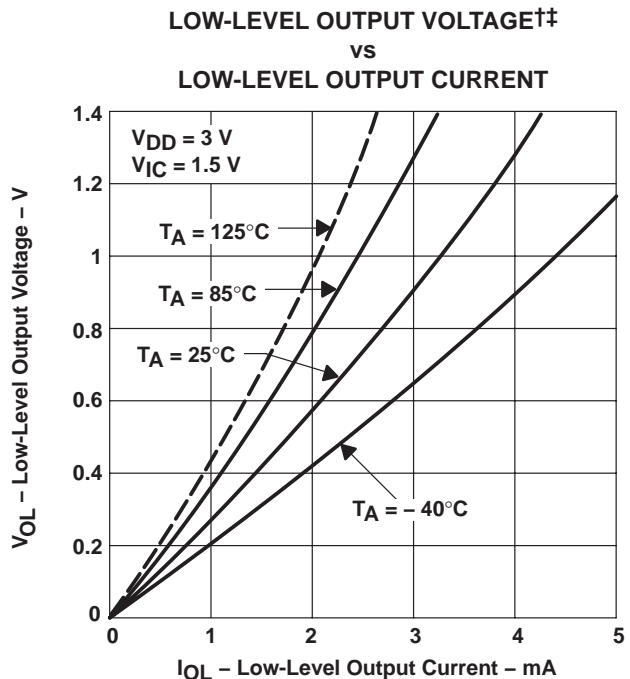
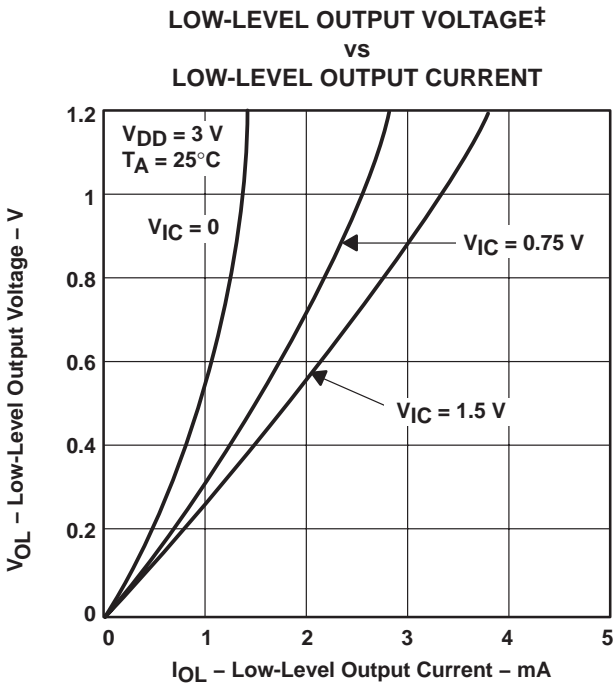
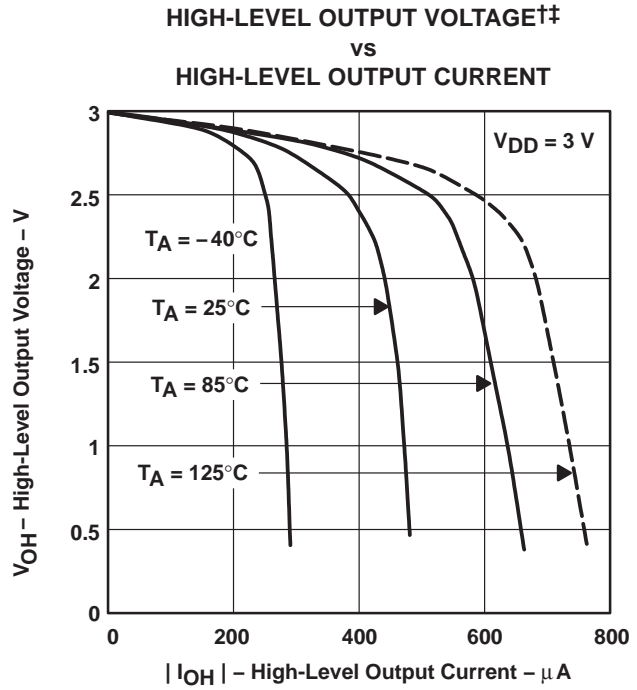
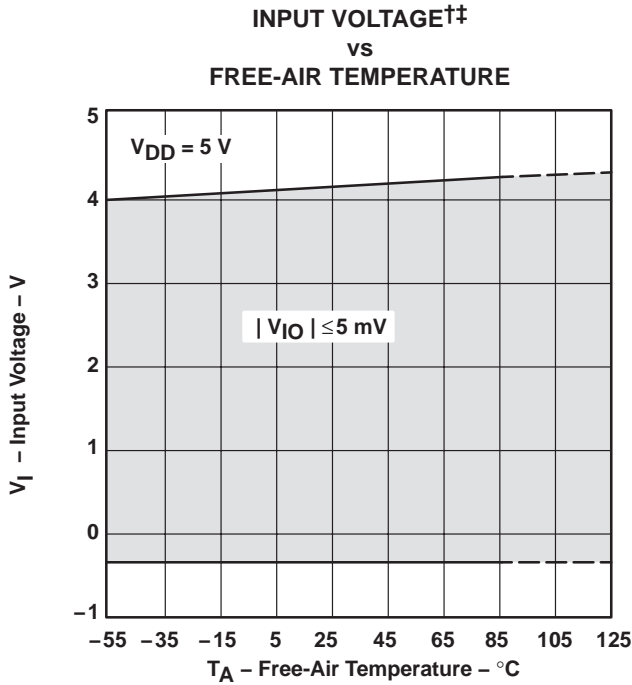
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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

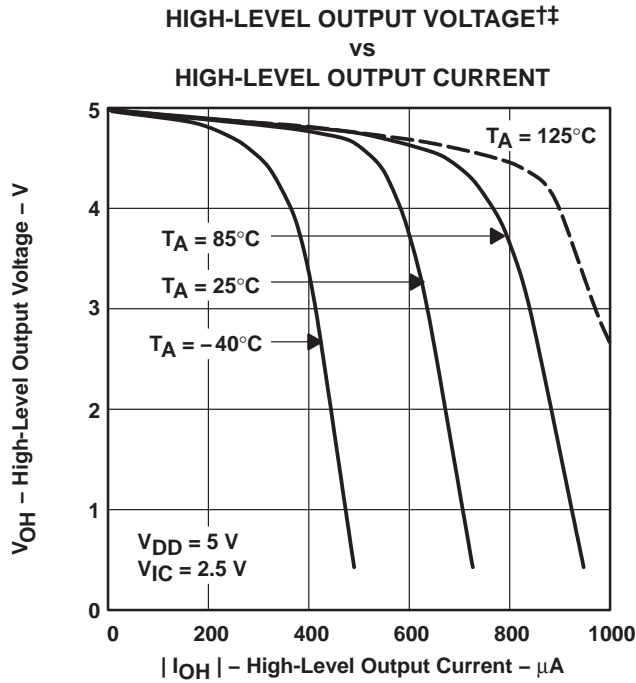


Figure 15

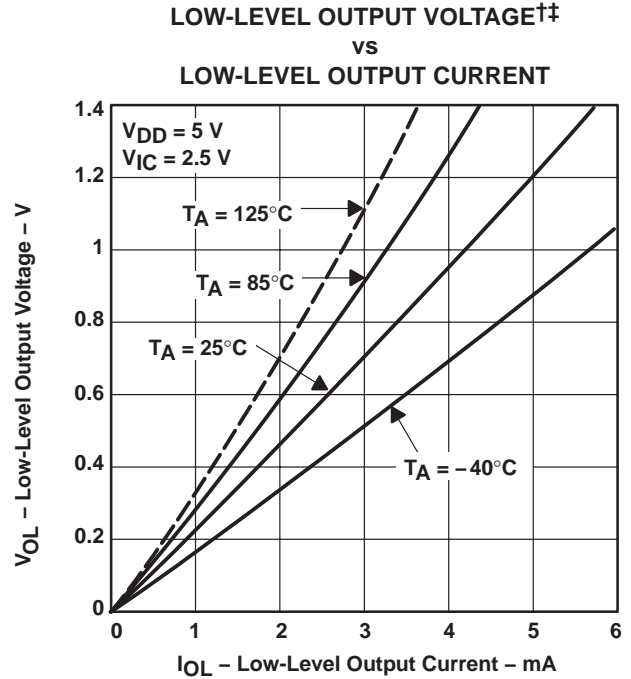


Figure 16

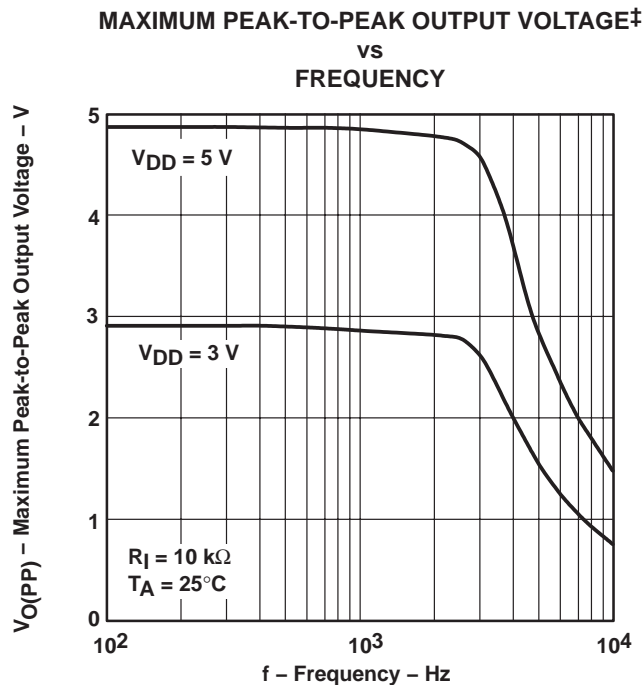


Figure 17

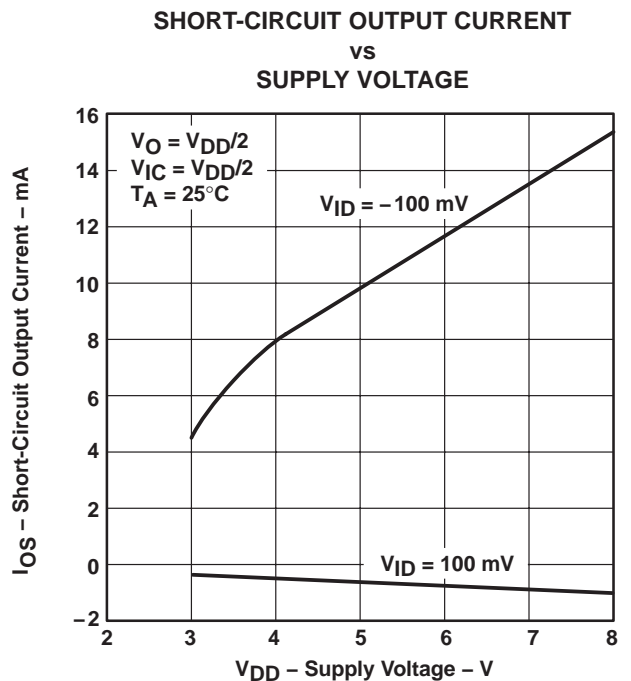


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5 V$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 V$, all loads are referenced to 1.5 V.

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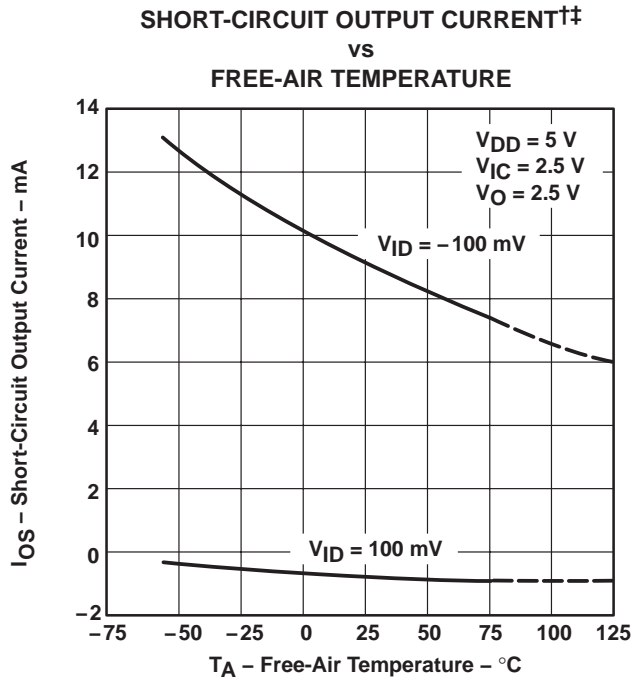


Figure 19

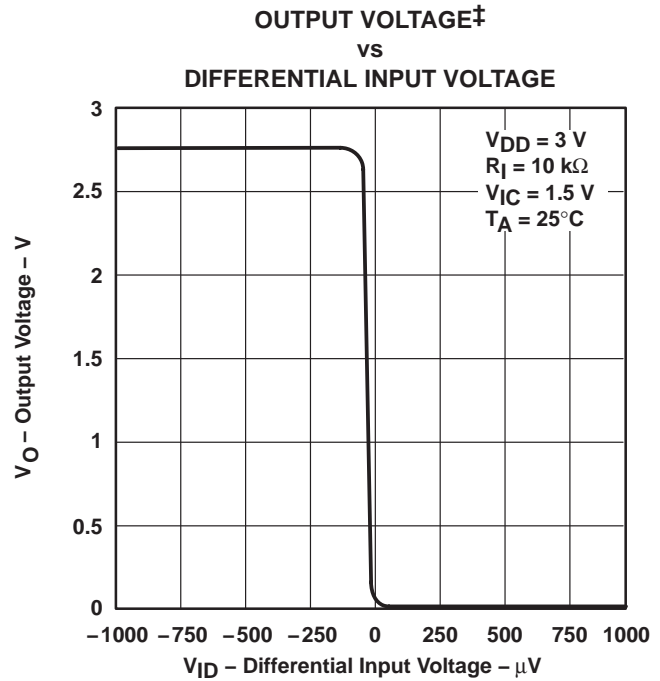


Figure 20

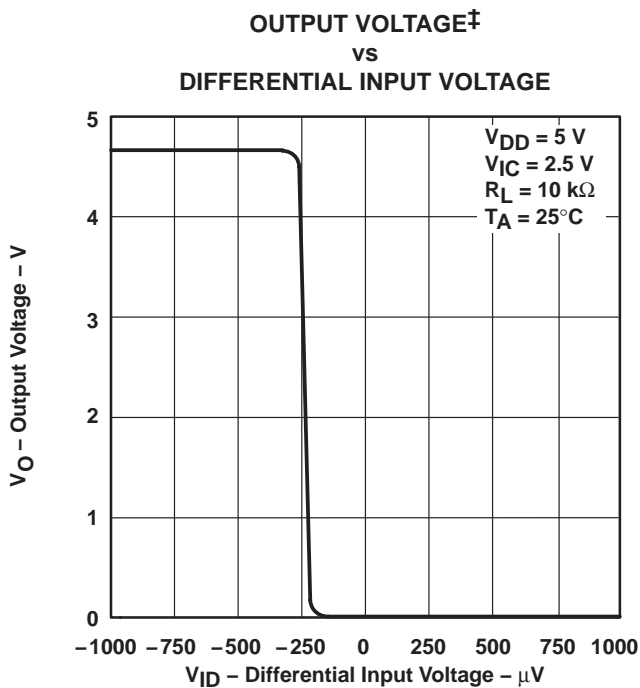


Figure 21

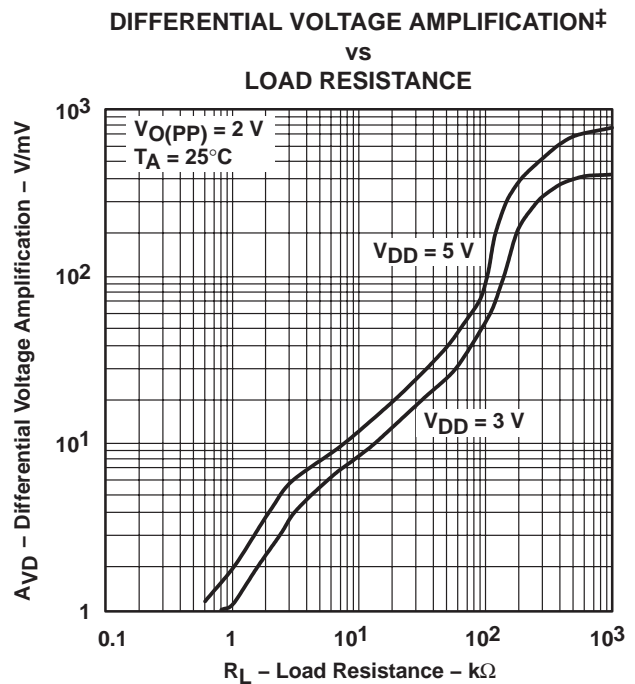


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.



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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†

vs

FREQUENCY

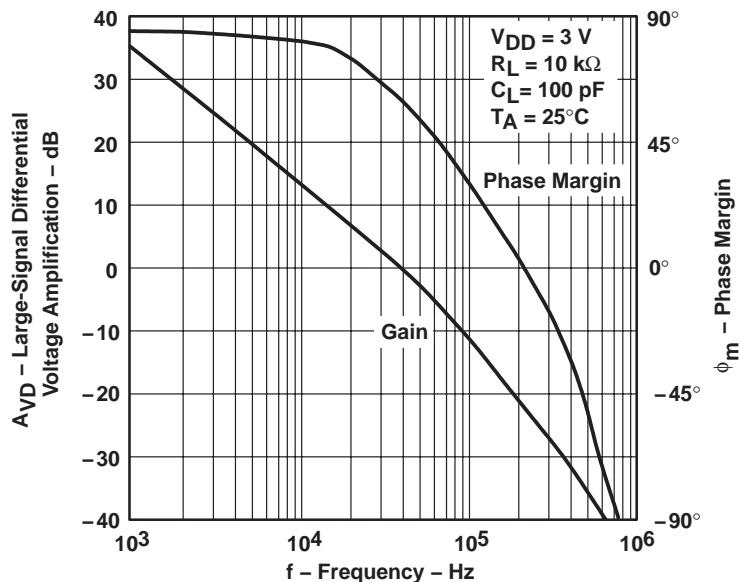


Figure 23

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†

vs

FREQUENCY

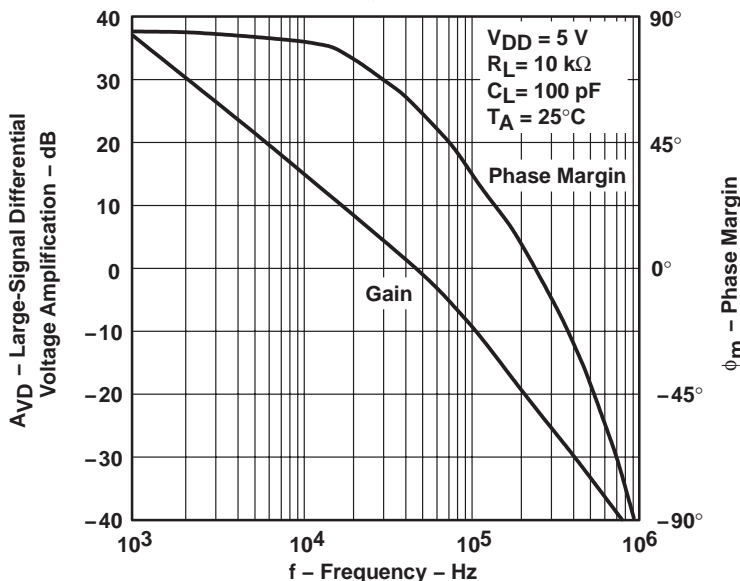


Figure 24

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡
 vs
FREE-AIR TEMPERATURE

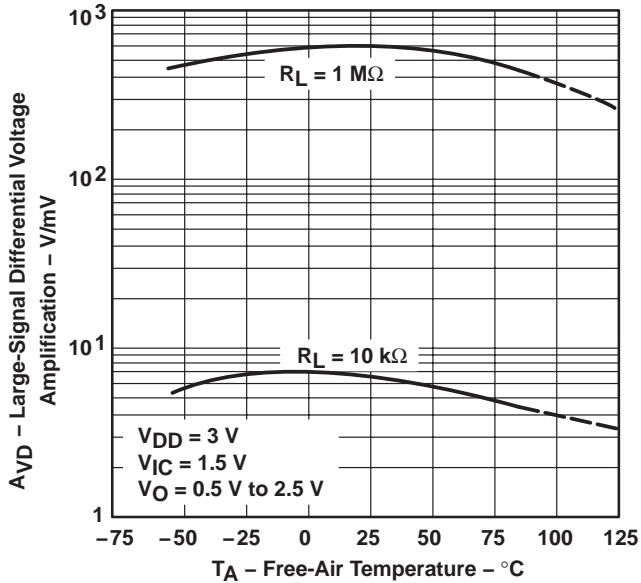


Figure 25

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡
 vs
FREE-AIR TEMPERATURE

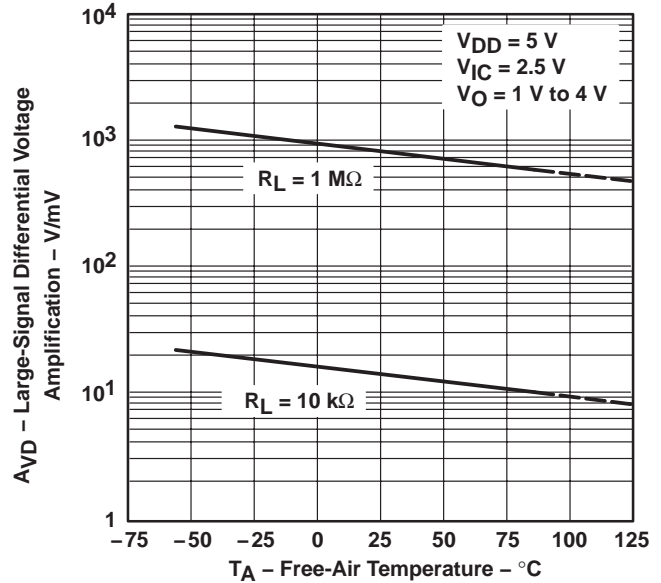


Figure 26

OUTPUT IMPEDANCE‡
 vs
FREQUENCY

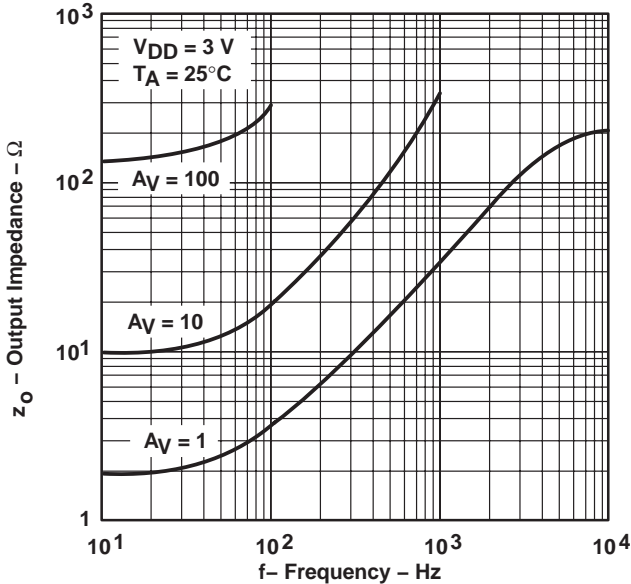


Figure 27

OUTPUT IMPEDANCE‡
 vs
FREQUENCY

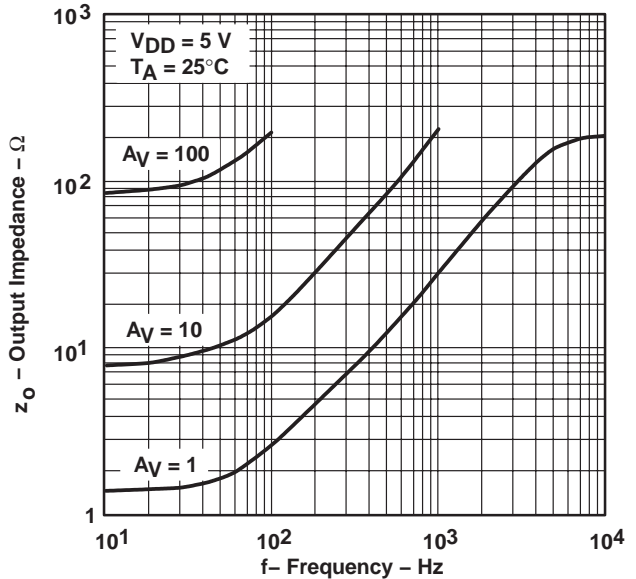
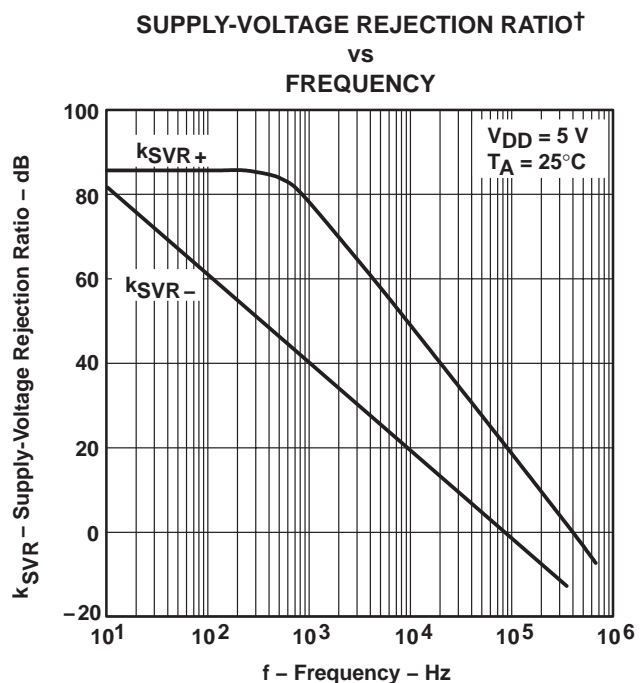
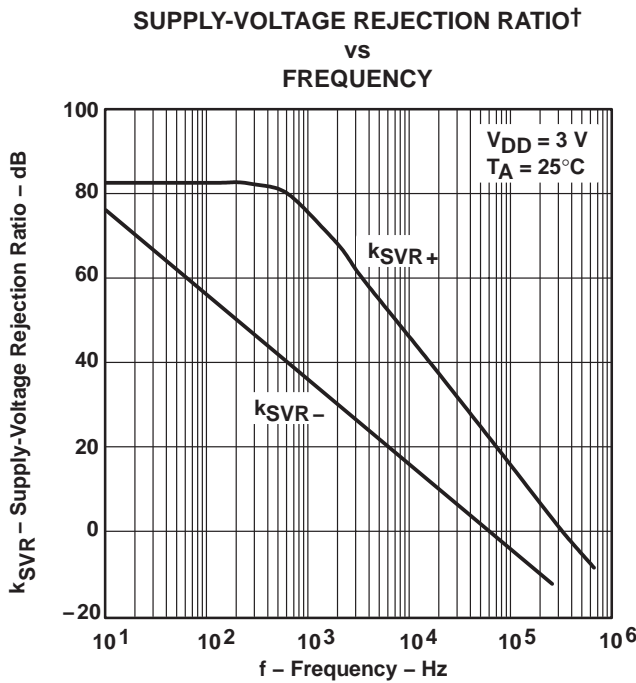
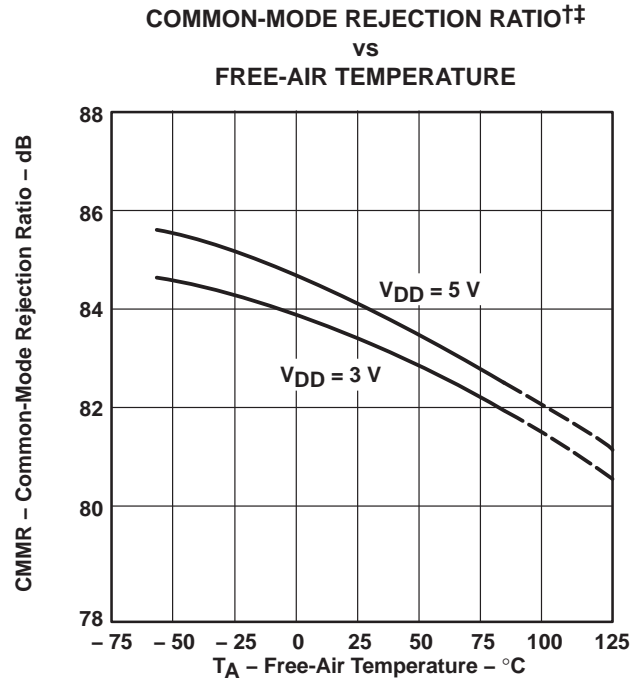
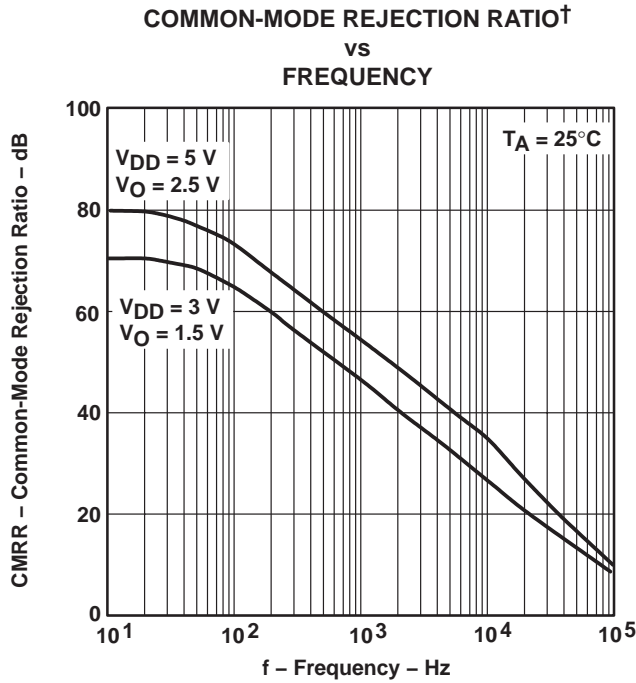


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.



TYPICAL CHARACTERISTICS



† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
 †† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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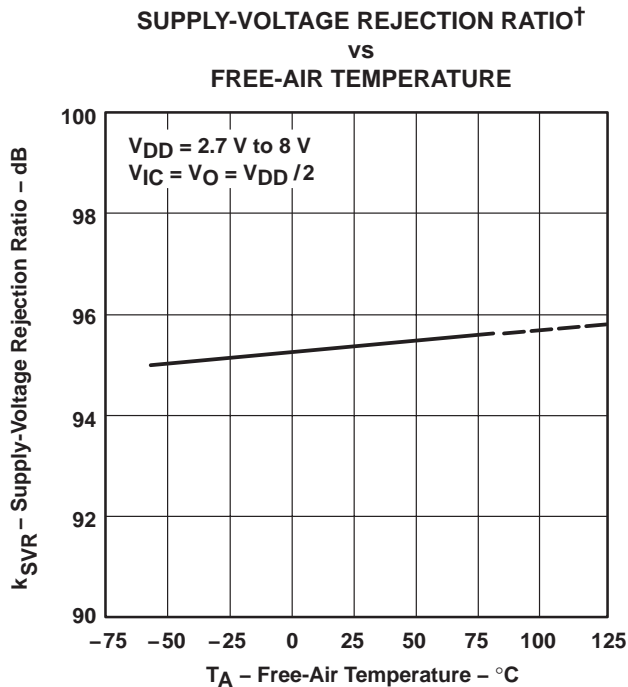


Figure 33

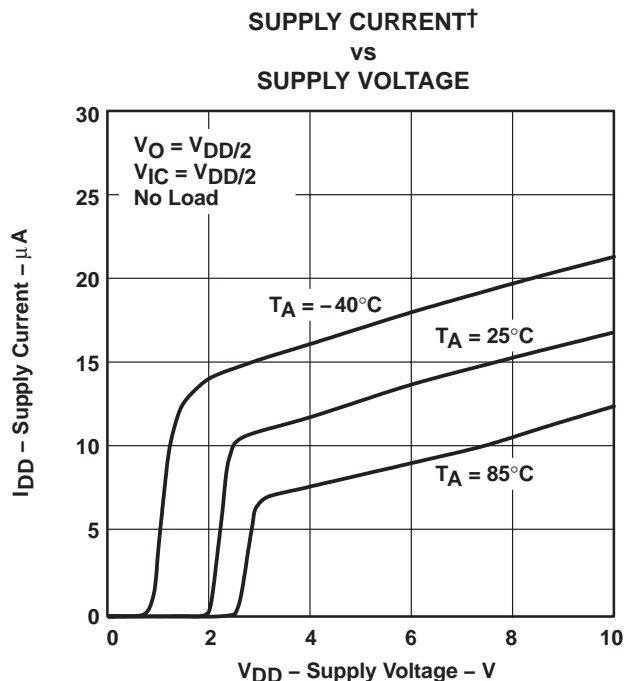


Figure 34

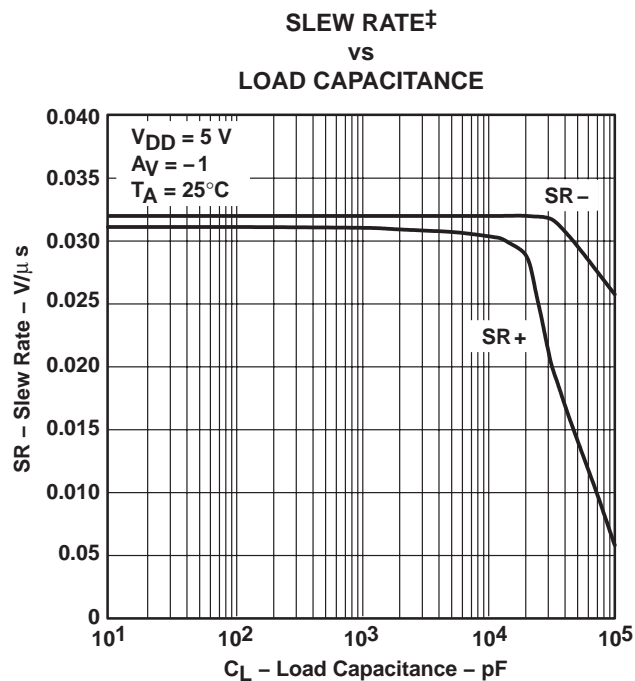


Figure 35

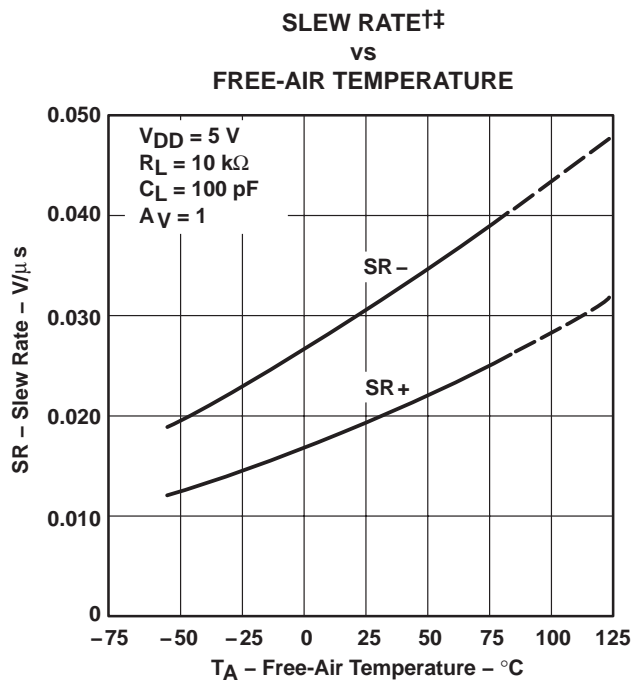


Figure 36

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.



TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

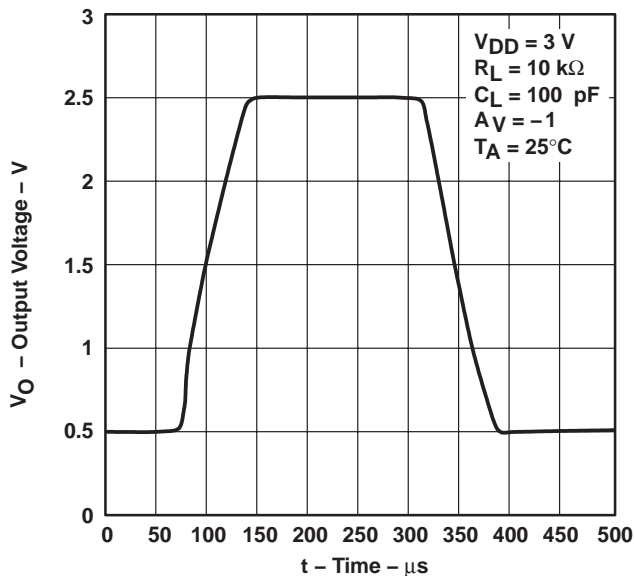


Figure 37

INVERTING LARGE-SIGNAL PULSE RESPONSE†

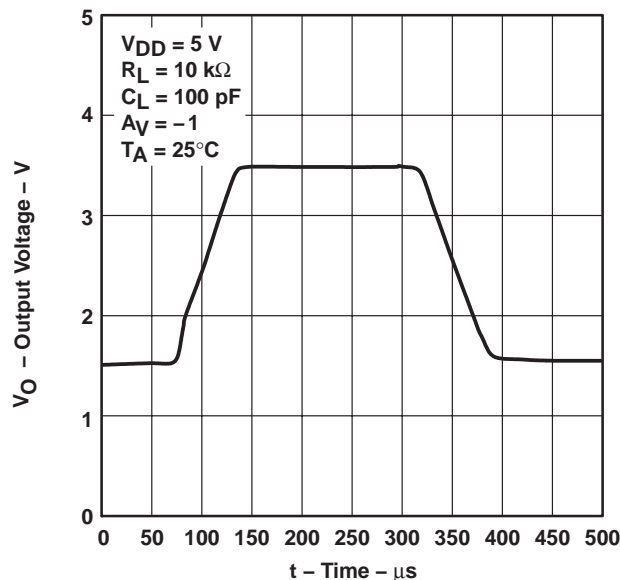


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

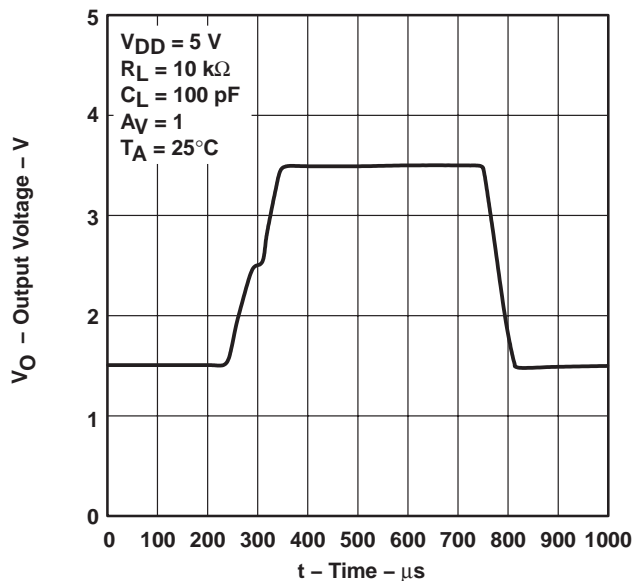


Figure 39

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

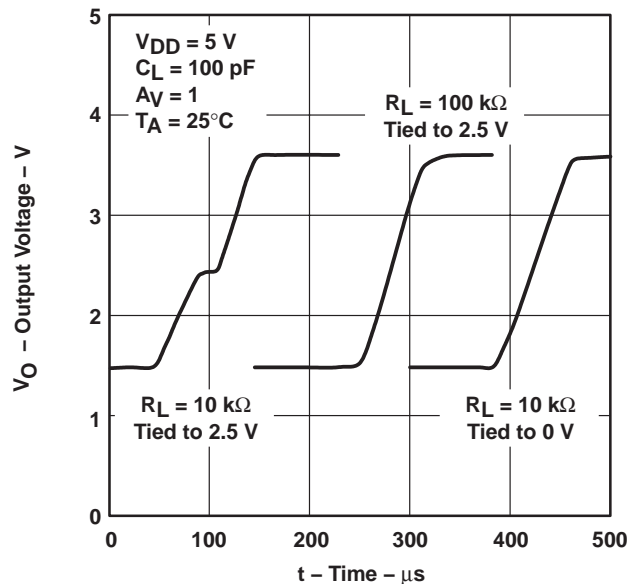


Figure 40

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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INVERTING SMALL-SIGNAL PULSE RESPONSE†

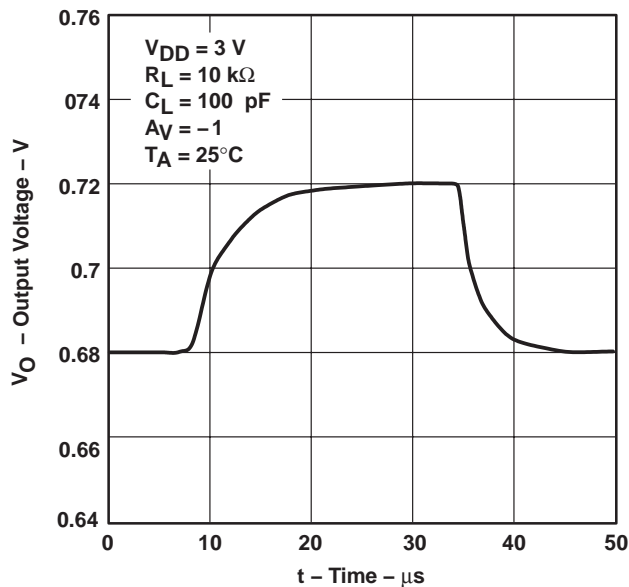


Figure 41

INVERTING SMALL-SIGNAL PULSE RESPONSE†

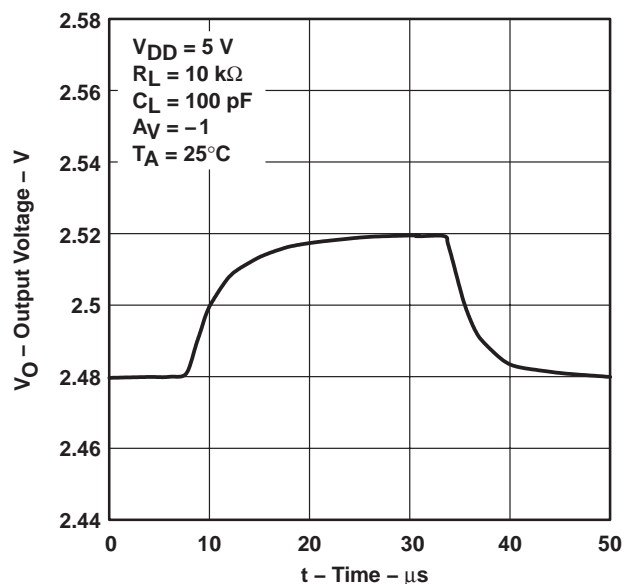


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

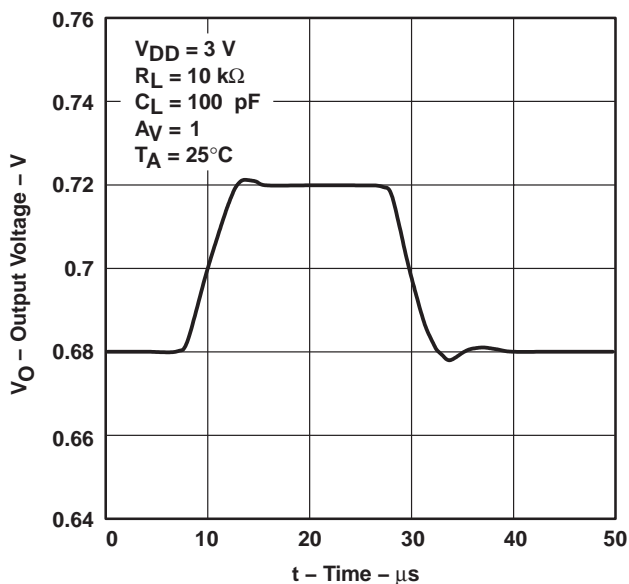


Figure 43

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

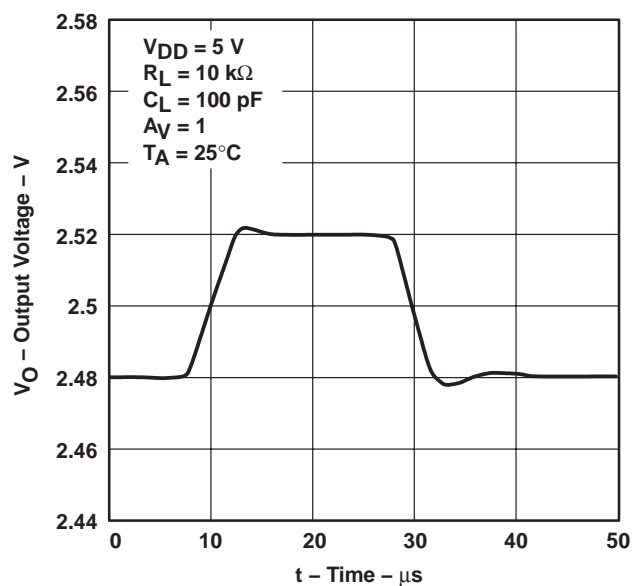
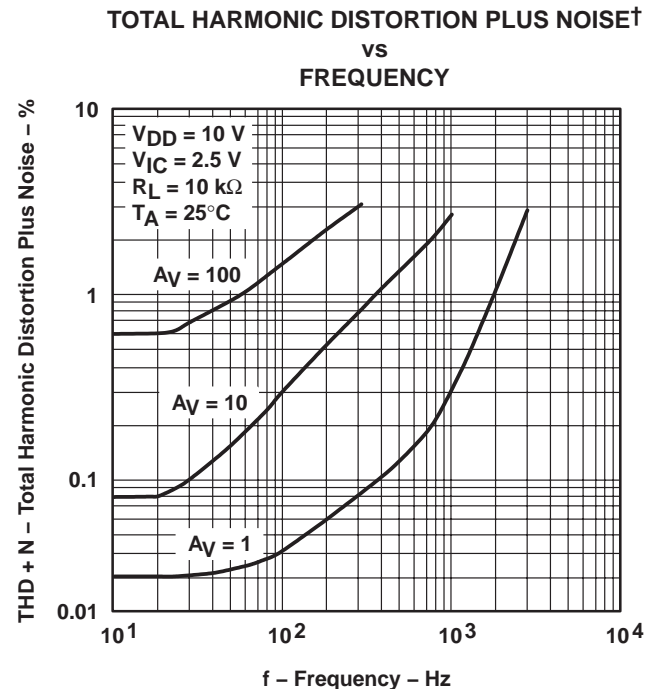
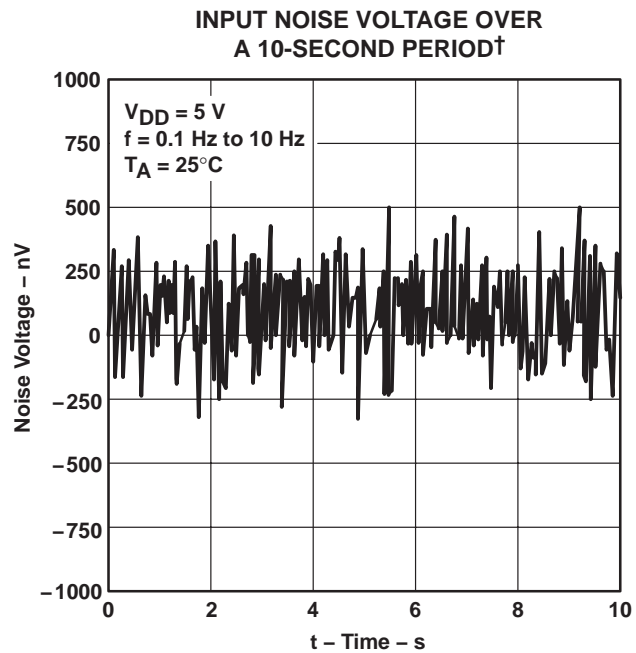
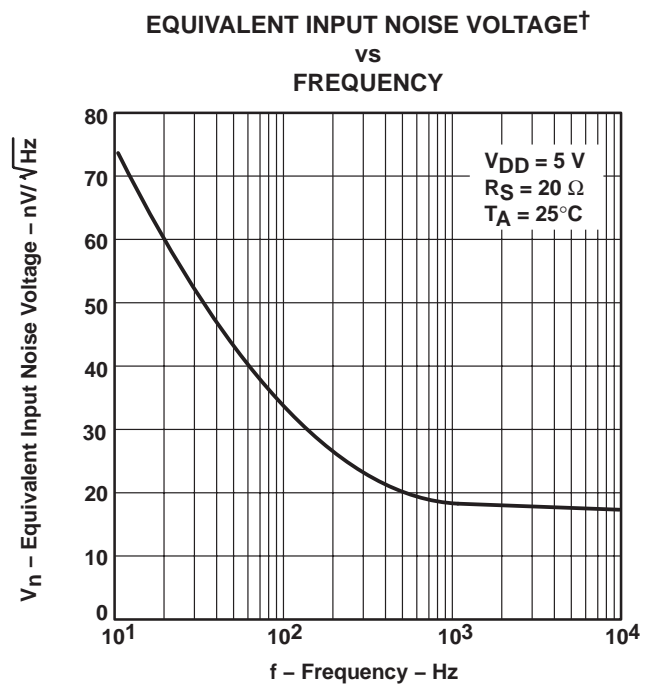
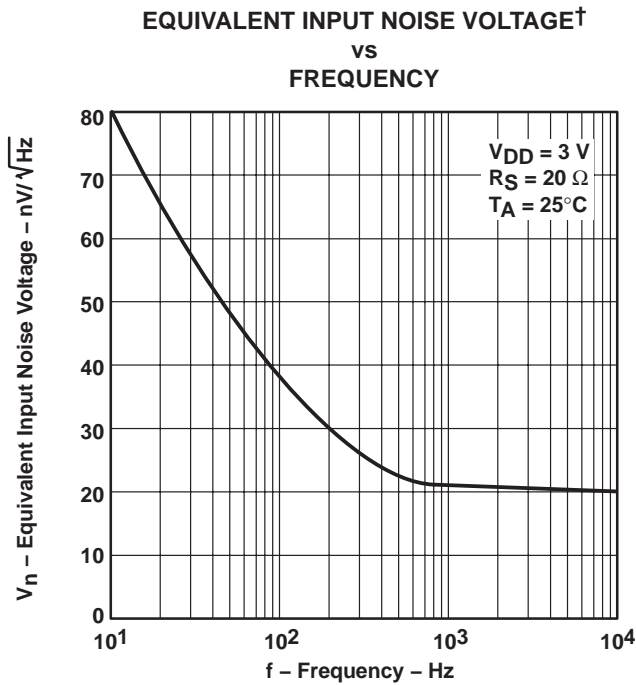


Figure 44

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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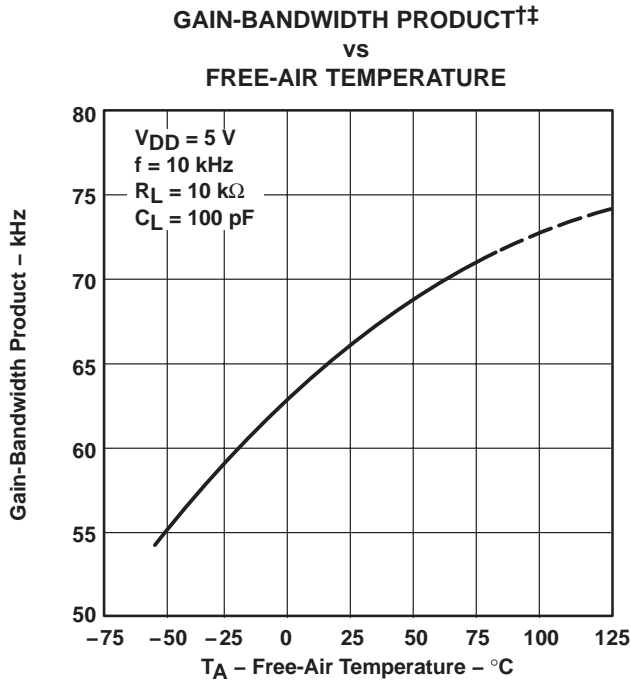


Figure 49

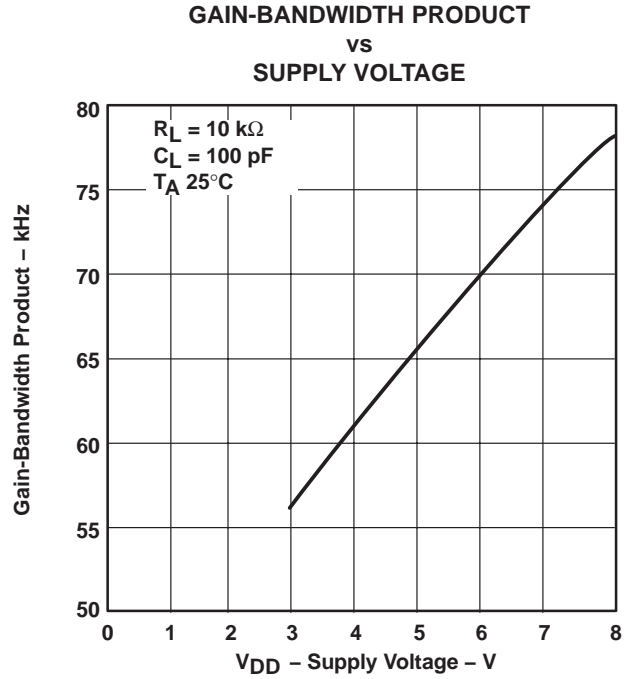


Figure 50

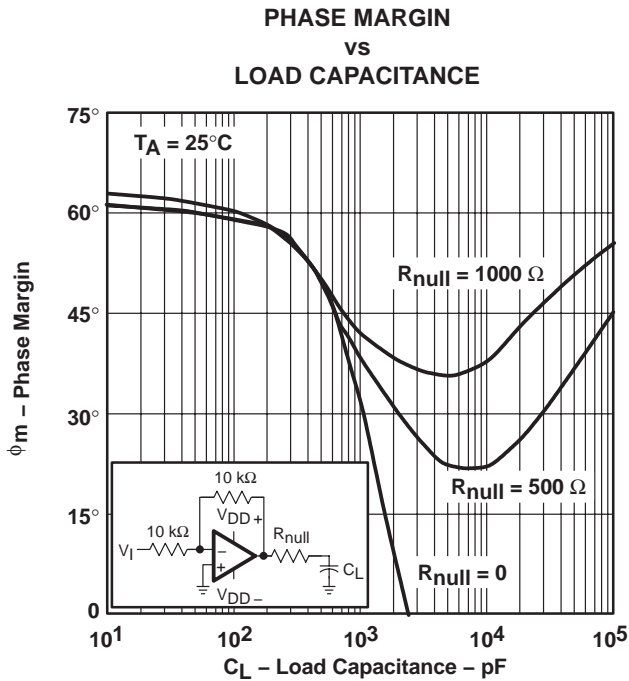


Figure 51

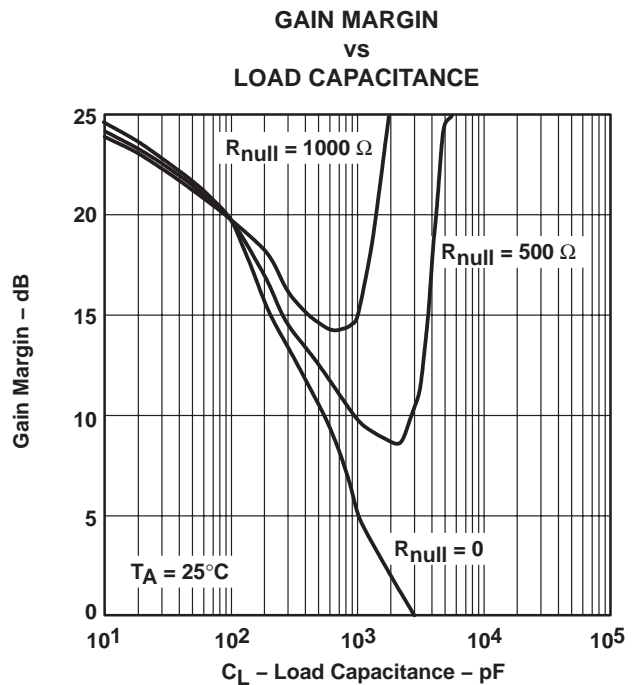


Figure 52

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

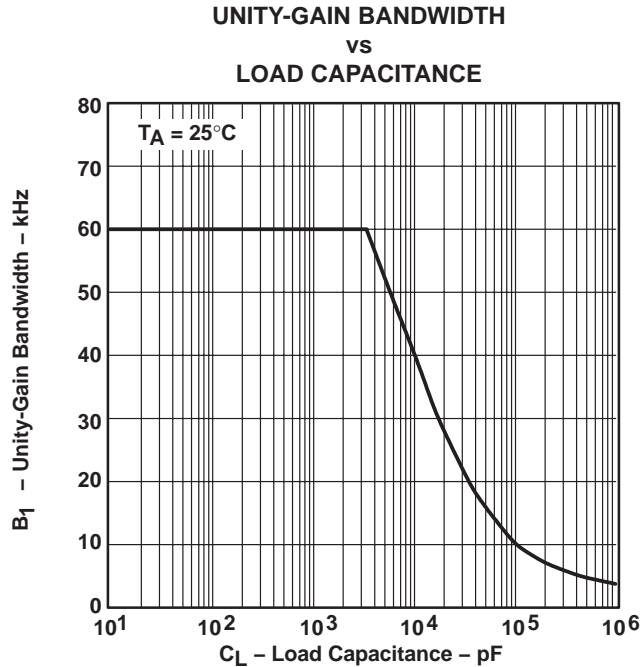


Figure 53

APPLICATION INFORMATION

driving large capacitive loads

The TLV2211 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figures 51 and 52 illustrate its ability to drive loads up to 600 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 54) improves the gain and phase margins when driving large capacitive loads. Figures 51 and 52 show the effects of adding series resistances of 500 Ω and 1000 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

$\Delta\phi_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

C_L = load capacitance

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APPLICATION INFORMATION

driving large capacitive loads (continued)

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 54). To use equation 1, UGBW must be approximated from Figure 54.

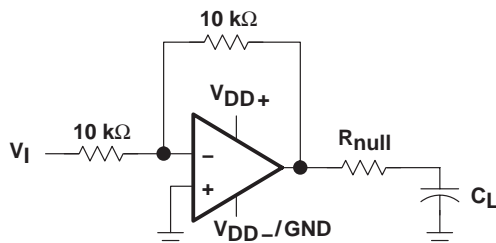


Figure 54. Series-Resistance Circuit

driving heavy dc loads

The TLV2211 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 μA and source 250 μA at $V_{\text{DD}} = 3\text{ V}$ and $V_{\text{DD}} = 5\text{ V}$ at a maximum quiescent I_{DD} of 25 μA . This provides a greater than 90% power efficiency.

When driving heavy dc loads, such as 10 k Ω , the positive edge can experience some distortion under slewing conditions. This condition can be seen in Figure 39. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 40 illustrates two 10-k Ω load conditions. The first load condition shows the distortion seen for a 10-k Ω load tied to 2.5 V. The third load condition shows no distortion for a 10-k Ω load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 40 illustrates the difference seen on the output for a 10-k Ω load and a 100-k Ω load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

TLV2211, TLV2211Y

Advanced LinCMOS™ RAIL-TO-RAIL MICROPOWER SINGLE OPERATIONAL AMPLIFIERS

SLOS156E – MAY 1996 – REVISED SEPTEMBER 2006

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 54 are generated using the TLV2211 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

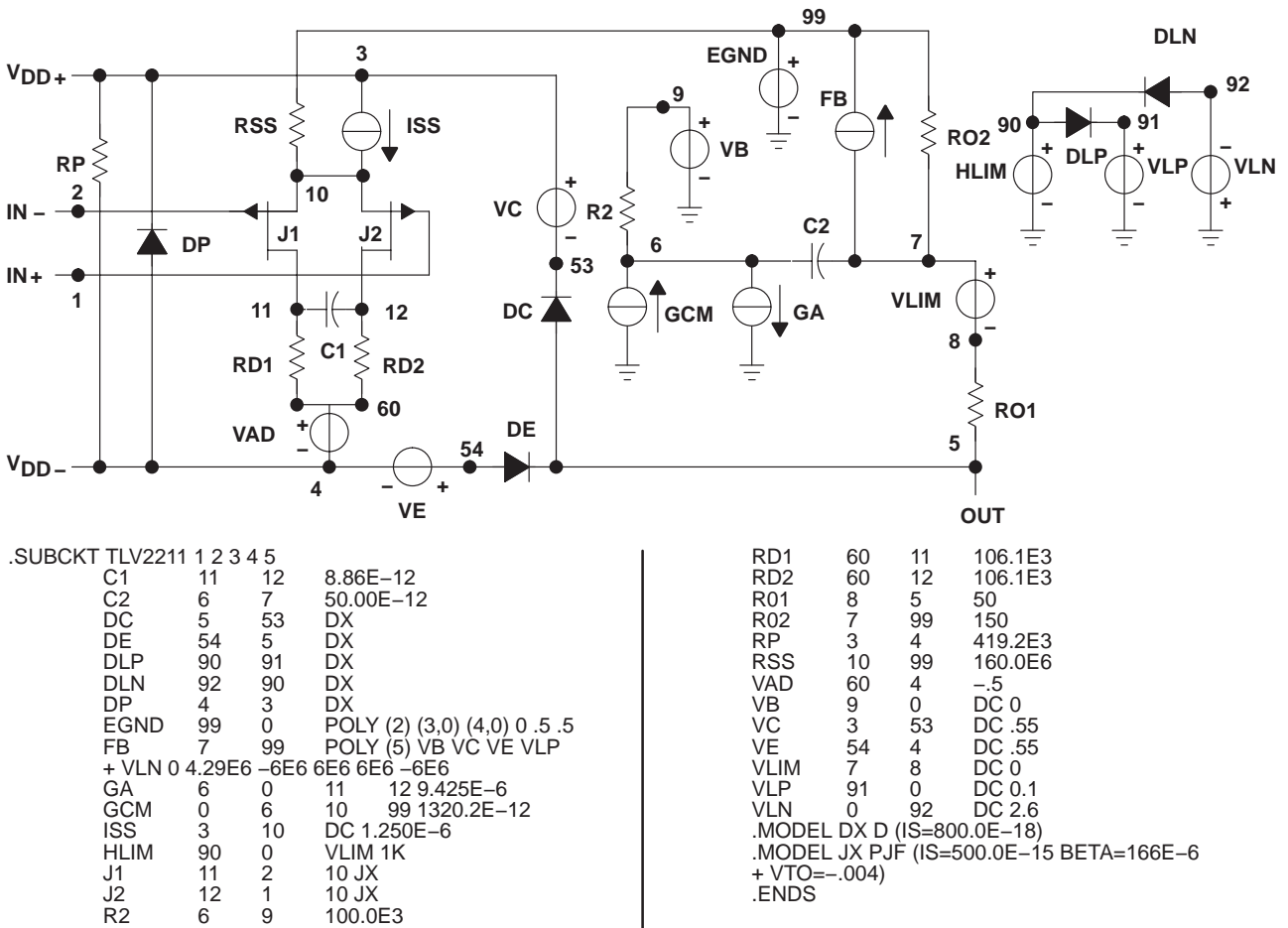


Figure 55. Boyle Macromodel and Subcircuit

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Macromodels, simulation models, or other models provided by TI, directly or indirectly, are not warranted by TI as fully representing all of the specification and operating characteristics of the semiconductor product to which the model relates.



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2211CDBVR	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	0 to 70	VACC
TLV2211CDBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	0 to 70	VACC
TLV2211IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VACI
TLV2211IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VACI
TLV2211IDBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLV2211IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VACI
TLV2211IDBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VACI
TLV2211IDBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

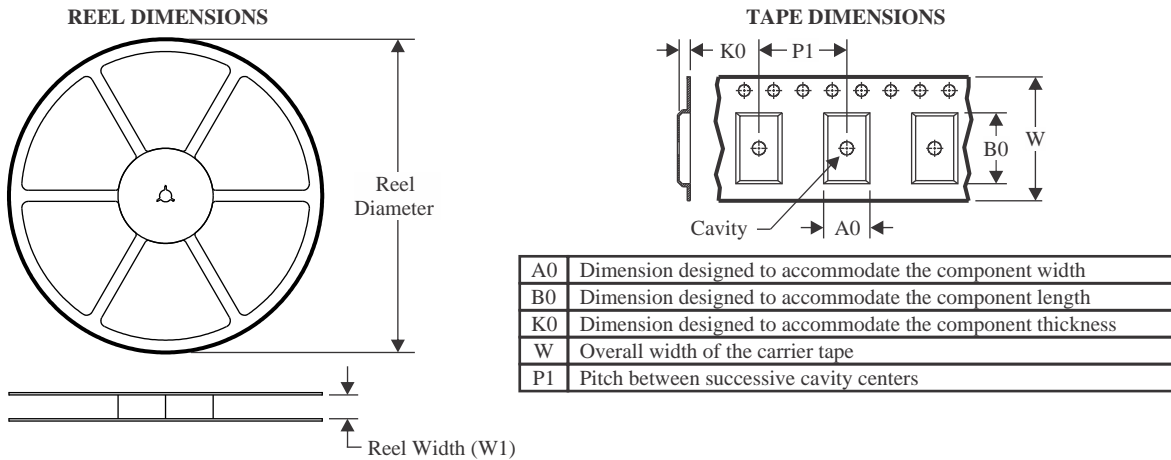
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

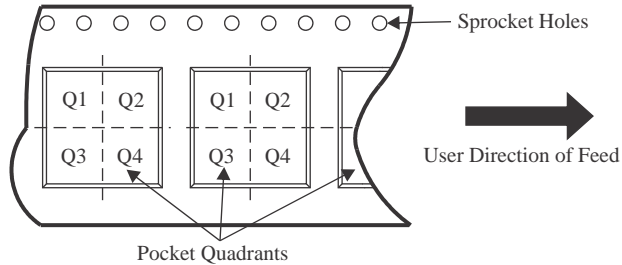
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TAPE AND REEL INFORMATION



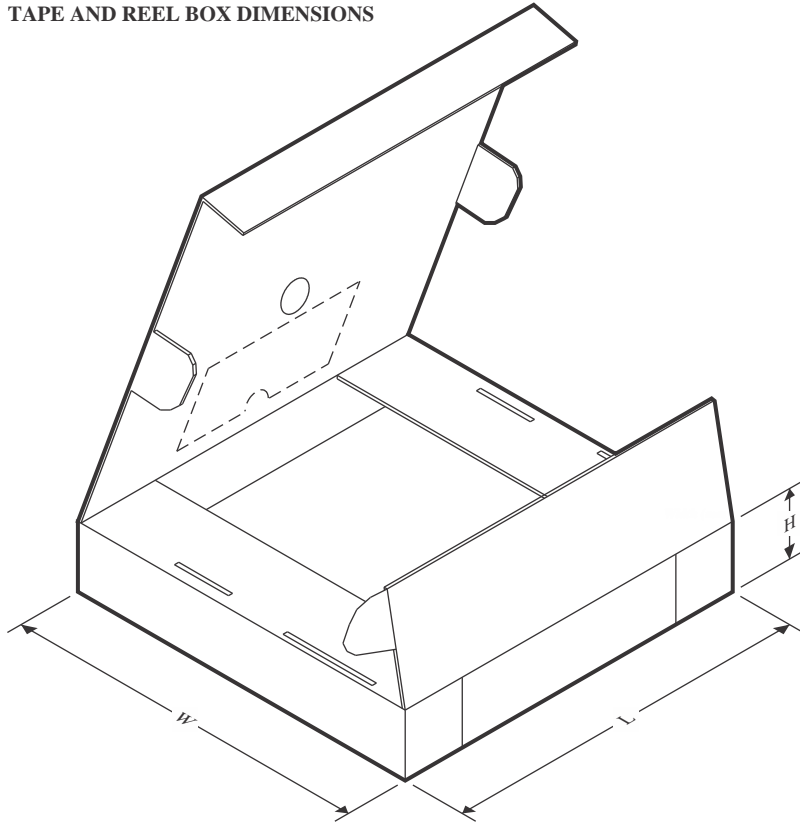
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2211IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2211IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

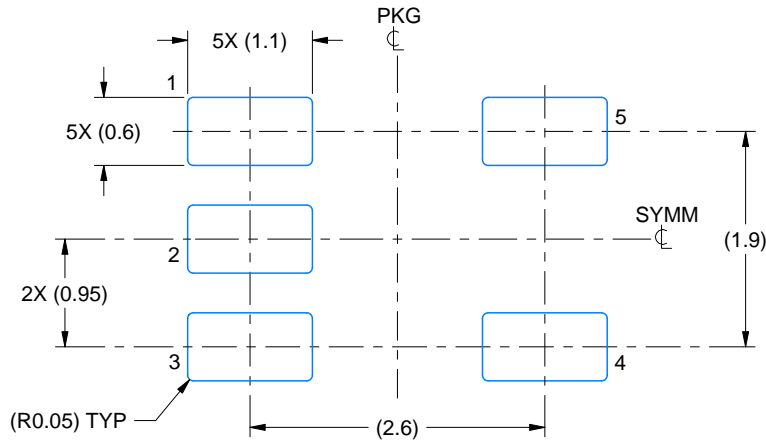
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2211IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2211IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

EXAMPLE BOARD LAYOUT

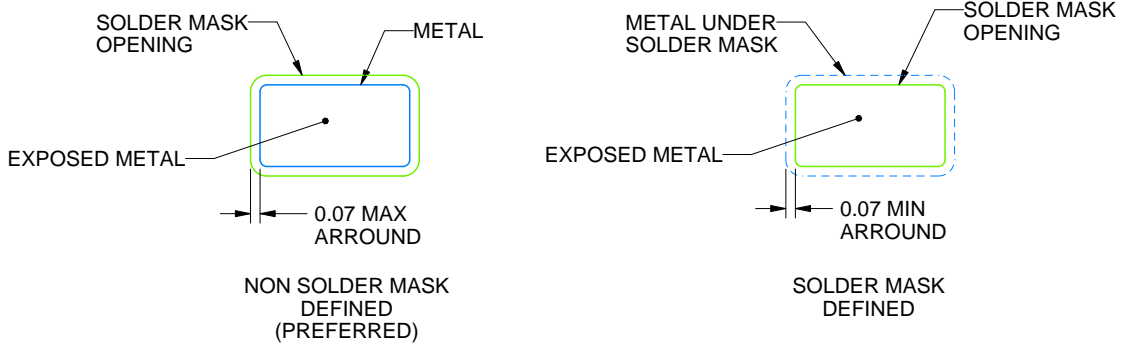
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

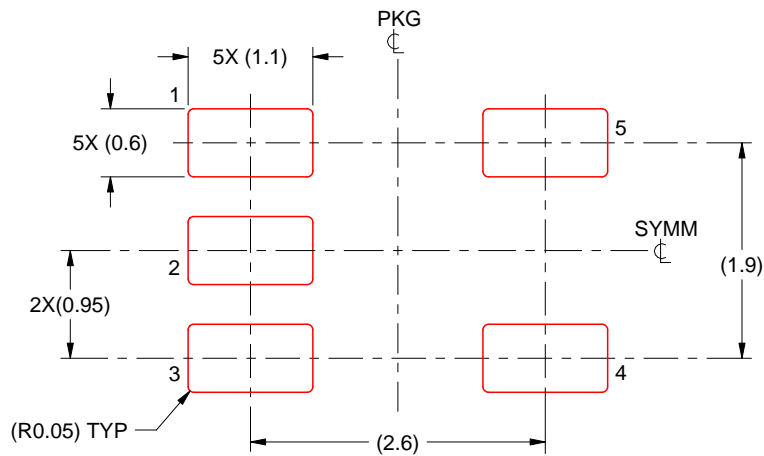
4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN**DBV0005A****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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