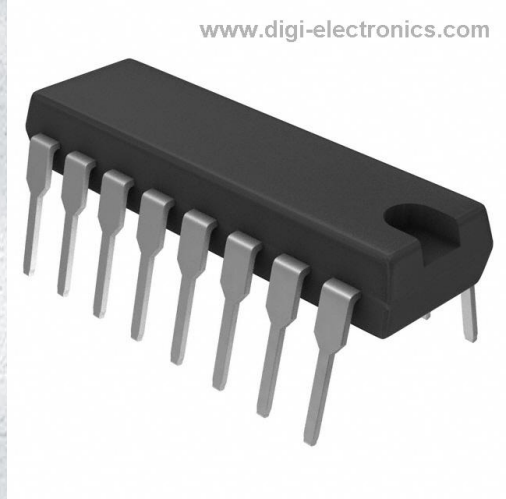
TRS232ECN Datasheet



DiGi Electronics Part Number	TRS232ECN-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	TRS232ECN
Description	IC TRANSCEIVER FULL 2/2 16DIP
Detailed Description	2/2 Transceiver Full RS232 16-PDIP

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
TRS232ECN	Texas Instruments
Series:	Product Status:
-	Obsolete
Type:	Protocol:
Transceiver	RS232
Number of Drivers/Receivers:	Duplex:
2/2	Full
Receiver Hysteresis:	Data Rate:
500 mV	250kbps
Voltage - Supply:	Operating Temperature:
4.5V ~ 5.5V	0°C ~ 70°C
Mounting Type:	Package / Case:
Through Hole	16-DIP (0.300", 7.62mm)
Supplier Device Package:	Base Product Number:
16-PDIP	TRS232

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	Not Applicable
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

Ordering & quality
TRS232ECN Texas Instruments IC TRANSCEIVER FULL 2/2 16DIP
Technical documentation
Design & development
Support & training

TRS232E Dual RS-232 Driver and Receiver with IEC61000-4-2 Protection

1 Features

- Meets or exceeds TIA/RS-232-F and ITU recommendation V.28
- Operates from a single 5V supply with 1µF charge-pump capacitors
- Operates up to 250kbit/s
- Two drivers and two receivers
- ±30V Input levels
- Low supply current: 8mA typical
- ESD protection for RS-232 bus pins
  - ±15-kV Human-body model (HBM)
  - ±8-kV IEC61000-4-2, Contact discharge
  - ±15-kV IEC61000-4-2, Air-gap discharge

2 Applications

- TIA/RS-232-F
- Battery-powered systems
- Terminals
- Modems
- Computers

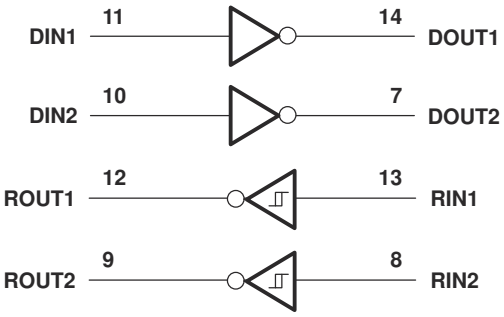
3 Description

The TRS232E is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/RS-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/RS-232-F inputs to 5V TTL/CMOS levels. This receiver has a typical threshold of 1.3V, a typical hysteresis of 0.5V, and can accept ±30V inputs. Each driver converts TTL/CMOS input levels into TIA/RS-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRS232E	SOIC (D, 16)	9.9mm x 6mm
	SOIC (DW, 16)	10.4mm x 10.3mm
	PDIP (N, 16)	19.3mm x 9.4mm
	TSSOP (PW, 16)	5mm x 6.4mm

(1) For more Information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

TRS232ECN Texas Instruments IC TRANSCEIVER FULL 2/2 16DIP

Table of Contents

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4 Pin Configuration and Functions

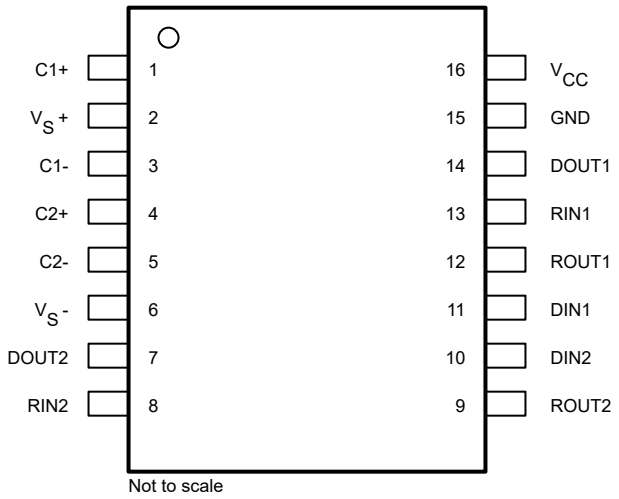

Figure 4-1. D, DW, N, NS or PW Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
V_S+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
V_S-	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 5V power supply

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TRS232ECN Texas Instruments IC TRANSCEIVER FULL 2/2 16DIP

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Input supply voltage range(2)		–0.3	6	V
V_{S+}	Positive output supply voltage range		V_{CC} – 0.3	15	V
$V_{S–}$	Negative output supply voltage range		–0.3	–15	V
V_I	Input voltage range	Driver	–0.3	V_{CC} + 0.3	V
		Receiver		±30	
V_O	Output voltage range	DOUT	$V_{S–}$ – 0.3	V_{S+} + 0.3	V
		ROUT	–0.3	V_{CC} + 0.3	
	Short-circuit duration	DOUT		Unlimited	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

PARAMETER	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	kV

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (DIN1, DIN2)		2			V
V_{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)				±30	V
T_A	Operating free-air temperature	TRS232EC	0		70	°C
		TRS232EI	–40		85	

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TRS232ECN Texas Instruments IC TRANSCEIVER FULL 2/2 16DIP

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	71.7	60.6	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	37.4	48.1	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	36.8	40.6	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.	27.5	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see (1) and Figure 8-1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5V,	All outputs open, T_A = 25°C		8	10	mA

(1) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.6 Driver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range(1)

PARAMETER			TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	R_L = 3kΩ to GND		5	7		V
V_{OL}	Low-level output voltage(3)	DOUT	R_L = 3kΩ to GND			–7	–5	V
r_o	Output resistance	DOUT	V_{S+} = V_{S-} = 0,	V_O = ±2V	300			Ω
I_{OS} (4)	Short-circuit output current	DOUT	V_{CC} = 5.5V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	DIN	V_I = 0				200	µA

(1) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4) Not more than one output should be shorted at a time.

5.7 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3kΩ to 7kΩ, See Figure 6-2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 6-3		3		V/µs
	Data rate	One DOUT switching		250		kbit/s

(1) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.

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5.8 Receiver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range (1)

PARAMETER			TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	ROUT	I_{OH} = –1mA		3.5			V
V_{OL}	Low-level output voltage(3)	ROUT	I_{OL} = 3.2mA				0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5V,	T_A = 25°C		1.7	2.4	V
$V_{IT–}$	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	RIN	V_{CC} = 5V		0.2	0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5V,	T_A = 25°C	3	5	7	kΩ

(1) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

5.9 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see (1) and Figure 6-1)

PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

(1) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.

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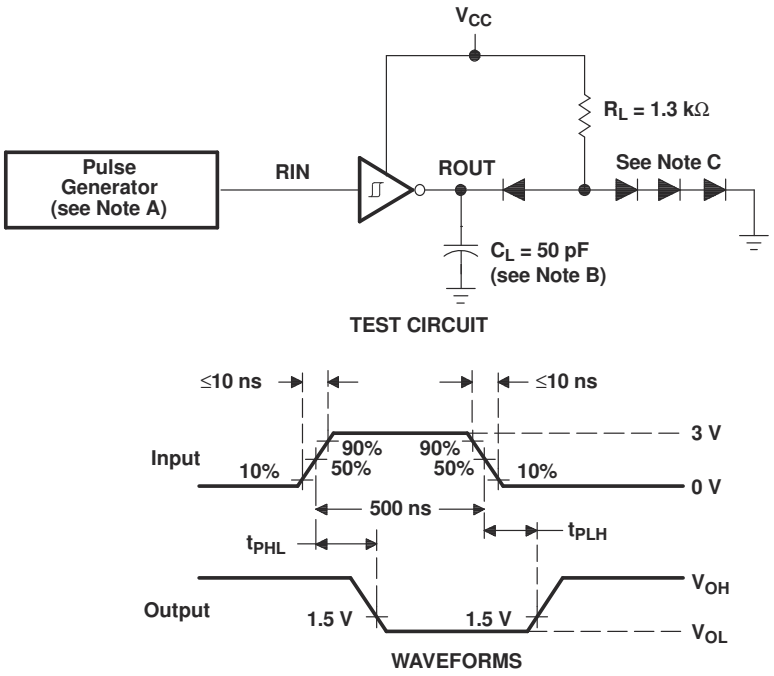
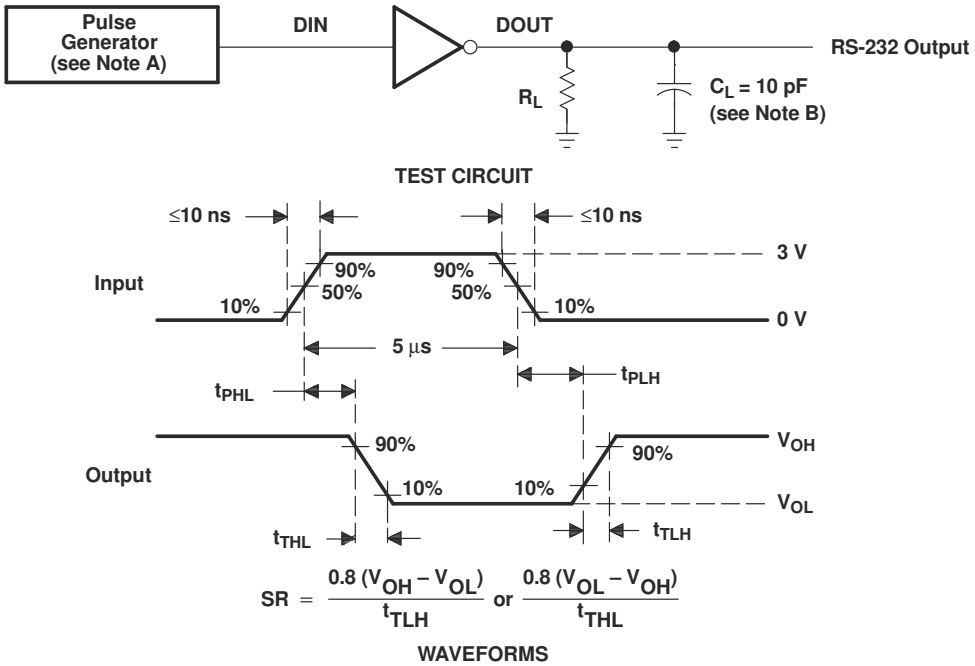
6 Parameter Measurement Information



A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements



A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5µs Input)

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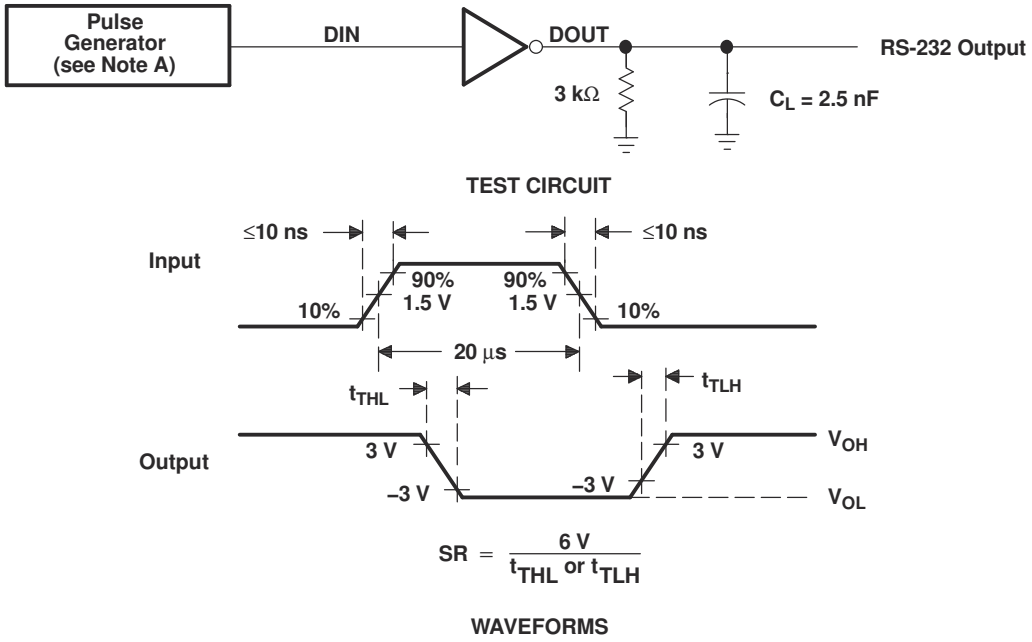

A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.

Figure 6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20µs Input)

7 Detailed Description

7.1 Device Functional Modes

Table 7-1. Function Tables: Each Driver

INPUT(1) DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 7-2. Each Receiver

INPUT(1) RIN	OUTPUT ROUT
L	H
H	L

(1) H = high level, L = low level

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TRS232ECN Texas Instruments IC TRANSCEIVER FULL 2/2 16DIP

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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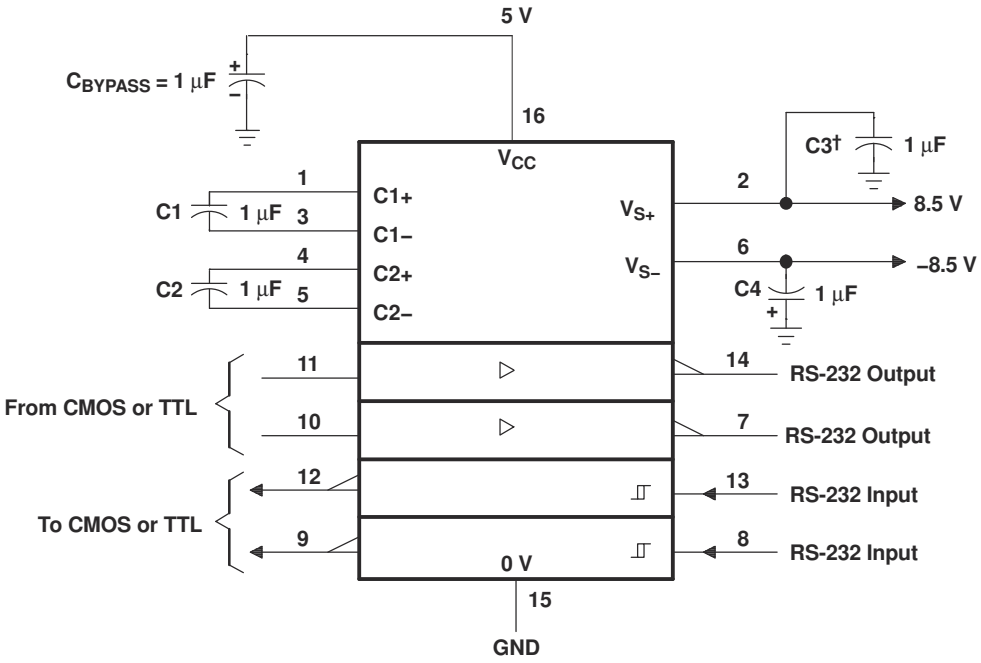
8.1 Application Information



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1µF capacitors shown, the TRS202E can operate with 0.1µF capacitors.

Figure 8-1. Typical Operating Circuit

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9 Device Documentation and Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2021) to Revision D (February 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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TEXAS INSTRUMENTS

PACKAGE OPTION ADDENDUM

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25-Sep-2024

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS232ECD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TRS232EC	
TRS232ECDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TRS232EC	
TRS232ECDWR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	TRS232EC	
TRS232ECPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	RU32EC	
TRS232EID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	TRS232EI	
TRS232EIDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	TRS232EI	
TRS232EIDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI	Samples
TRS232EIN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 85	TRS232EIN	
TRS232EIPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	RU32EI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

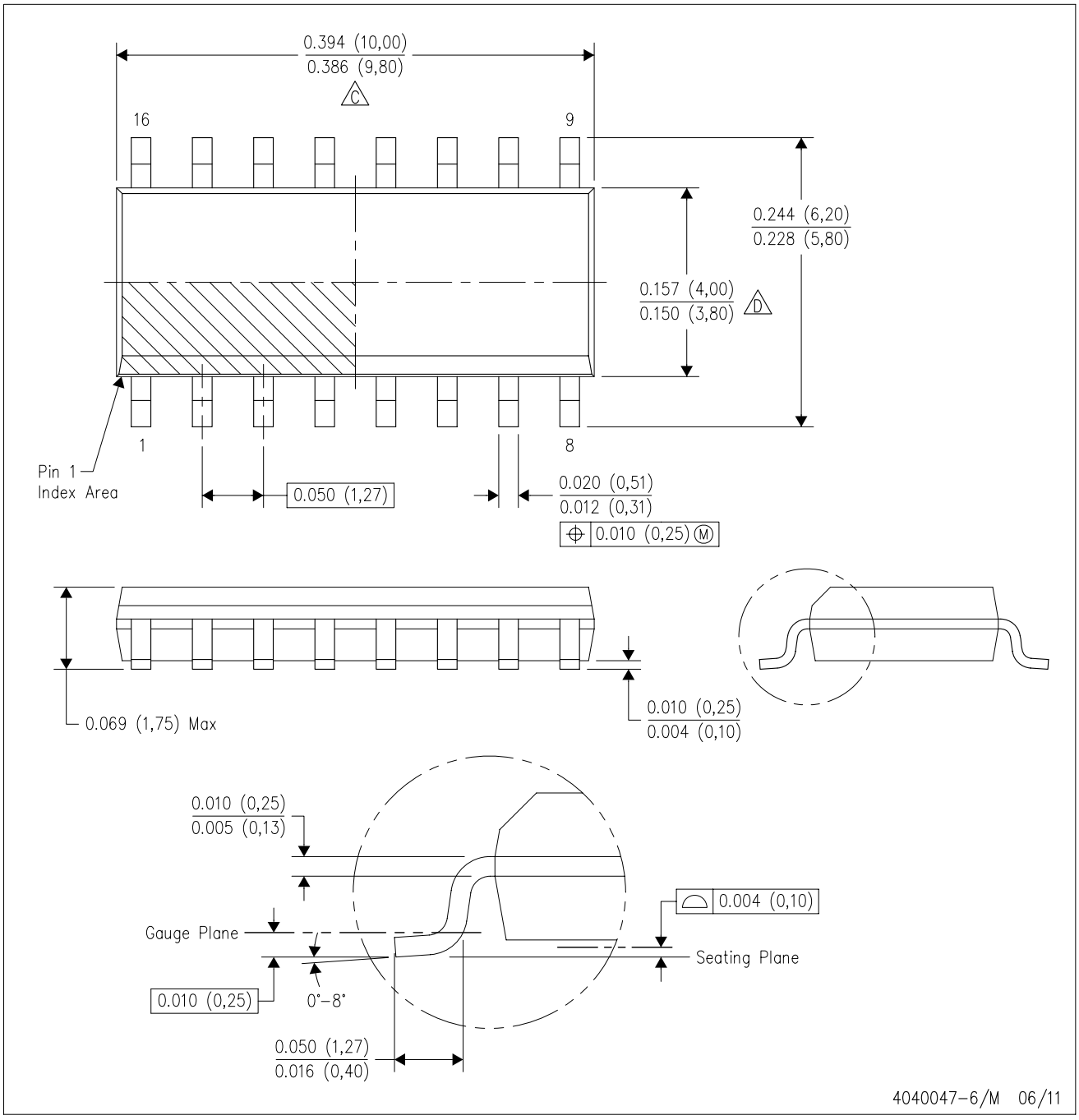
PACKAGE OPTION ADDENDUM

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

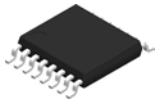
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

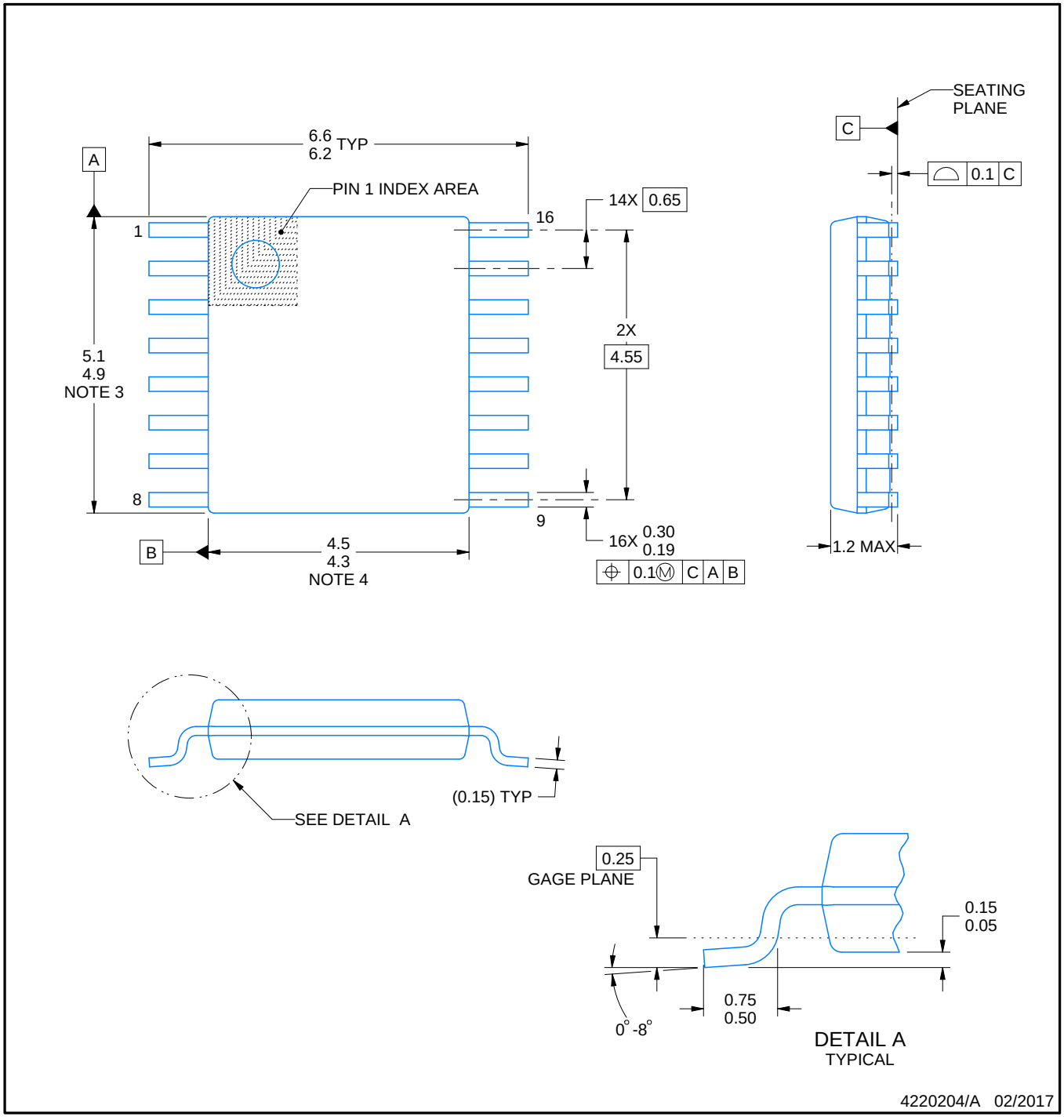


PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

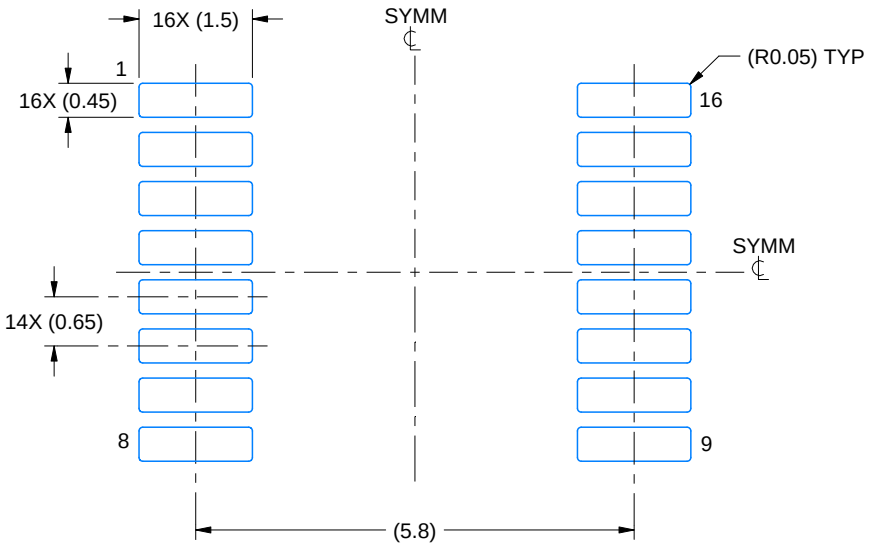
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

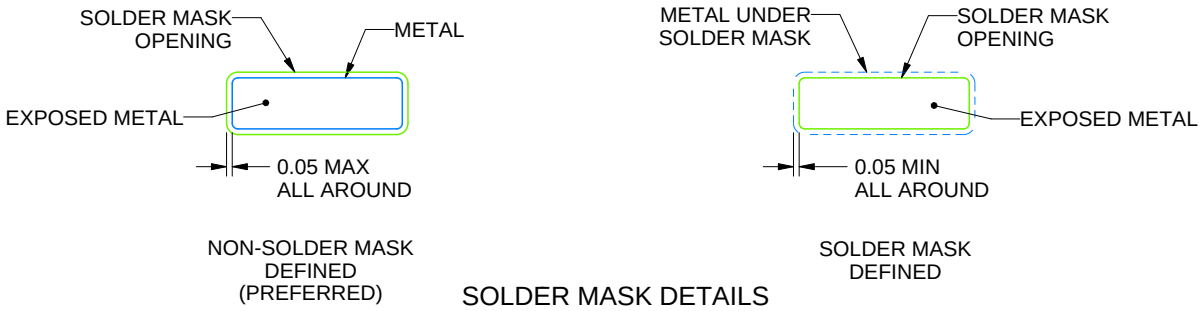
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

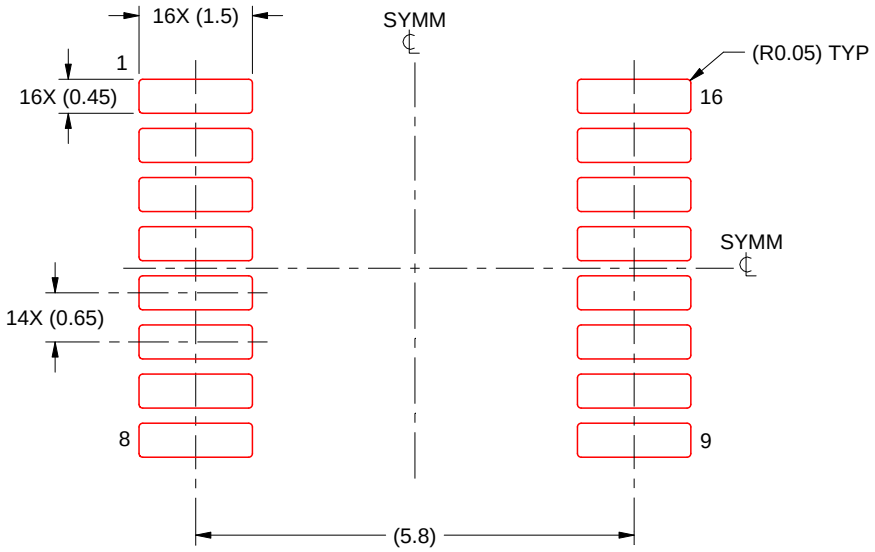
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

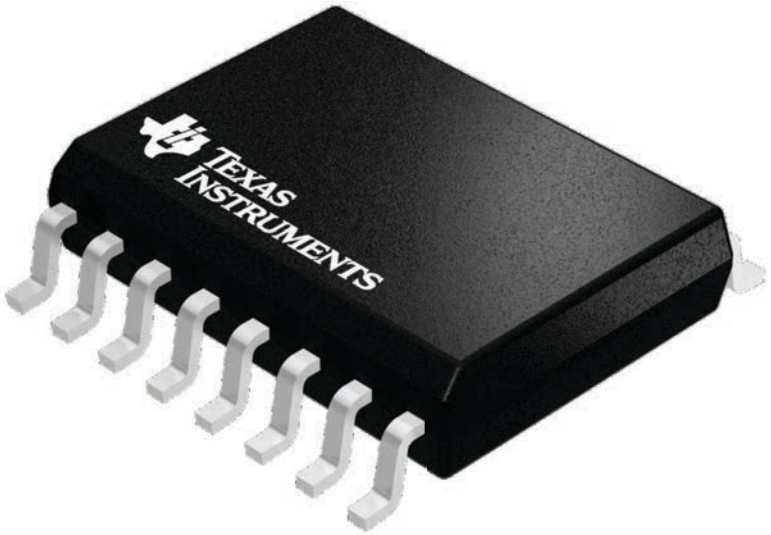
DW 16

SOIC - 2.65 mm max height

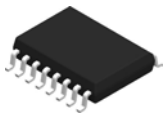
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

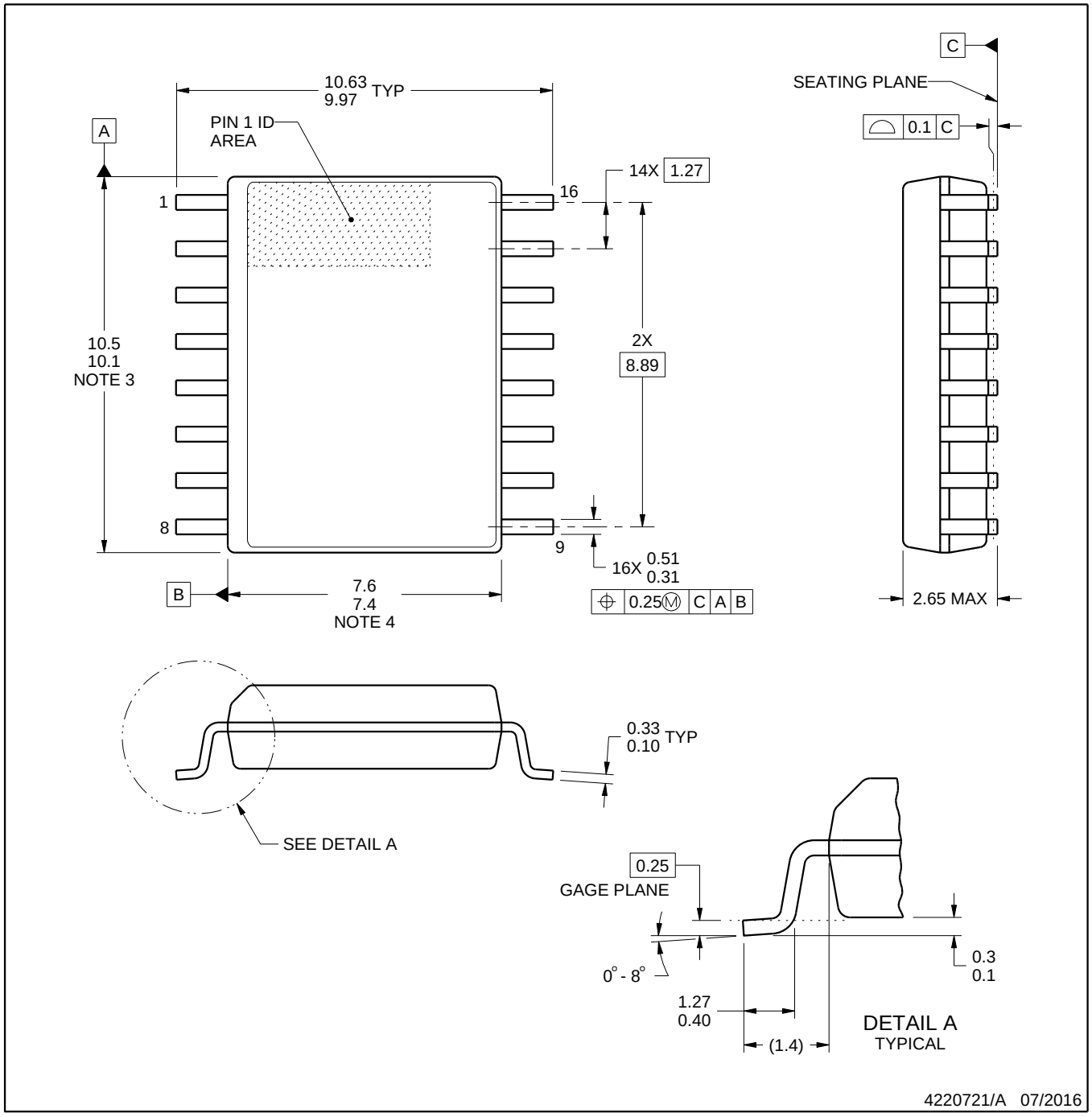


PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

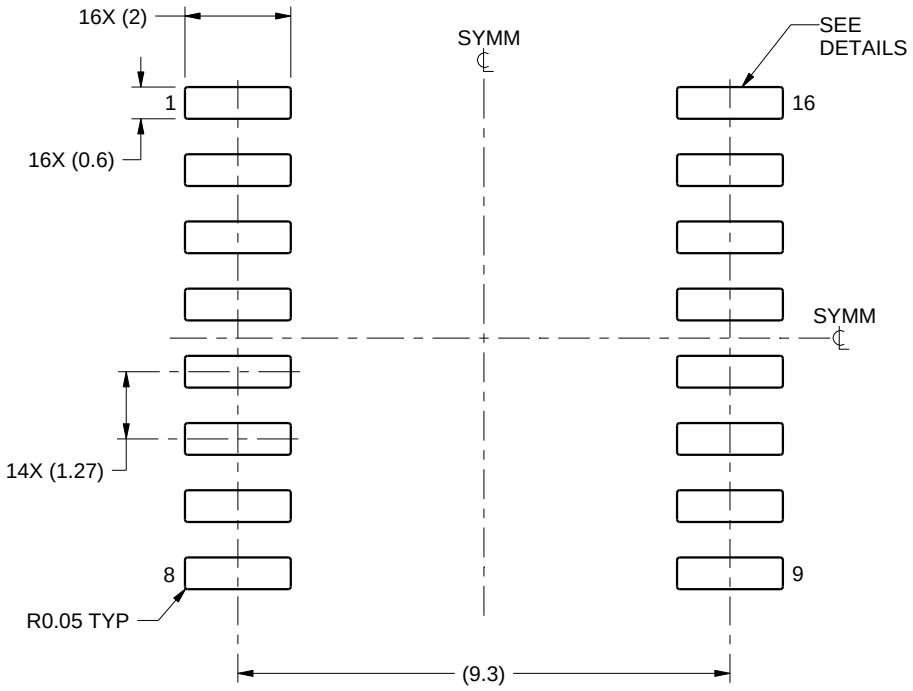
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

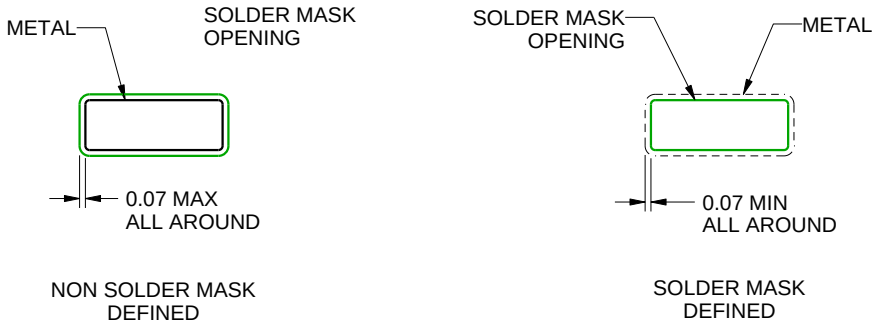
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

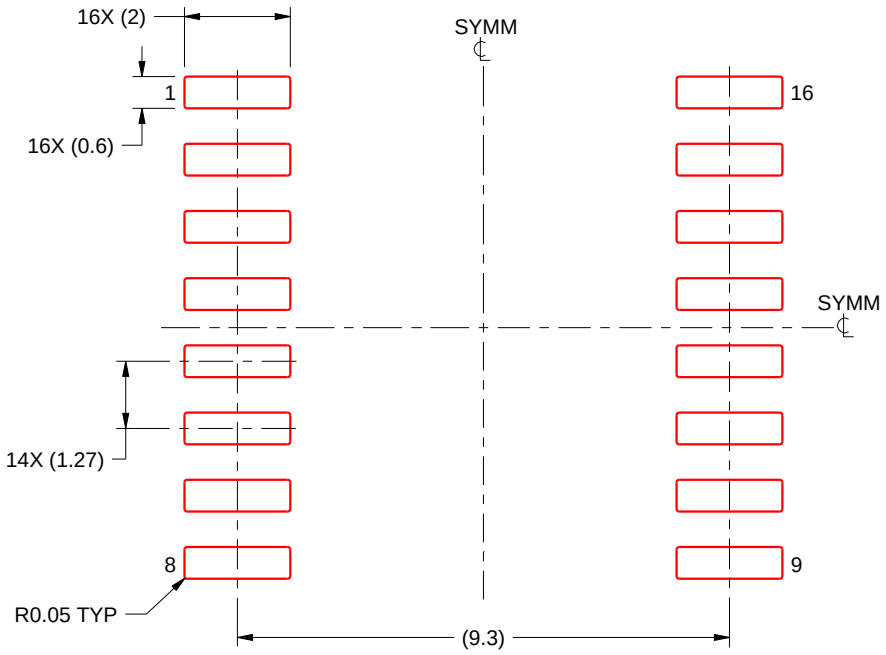
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

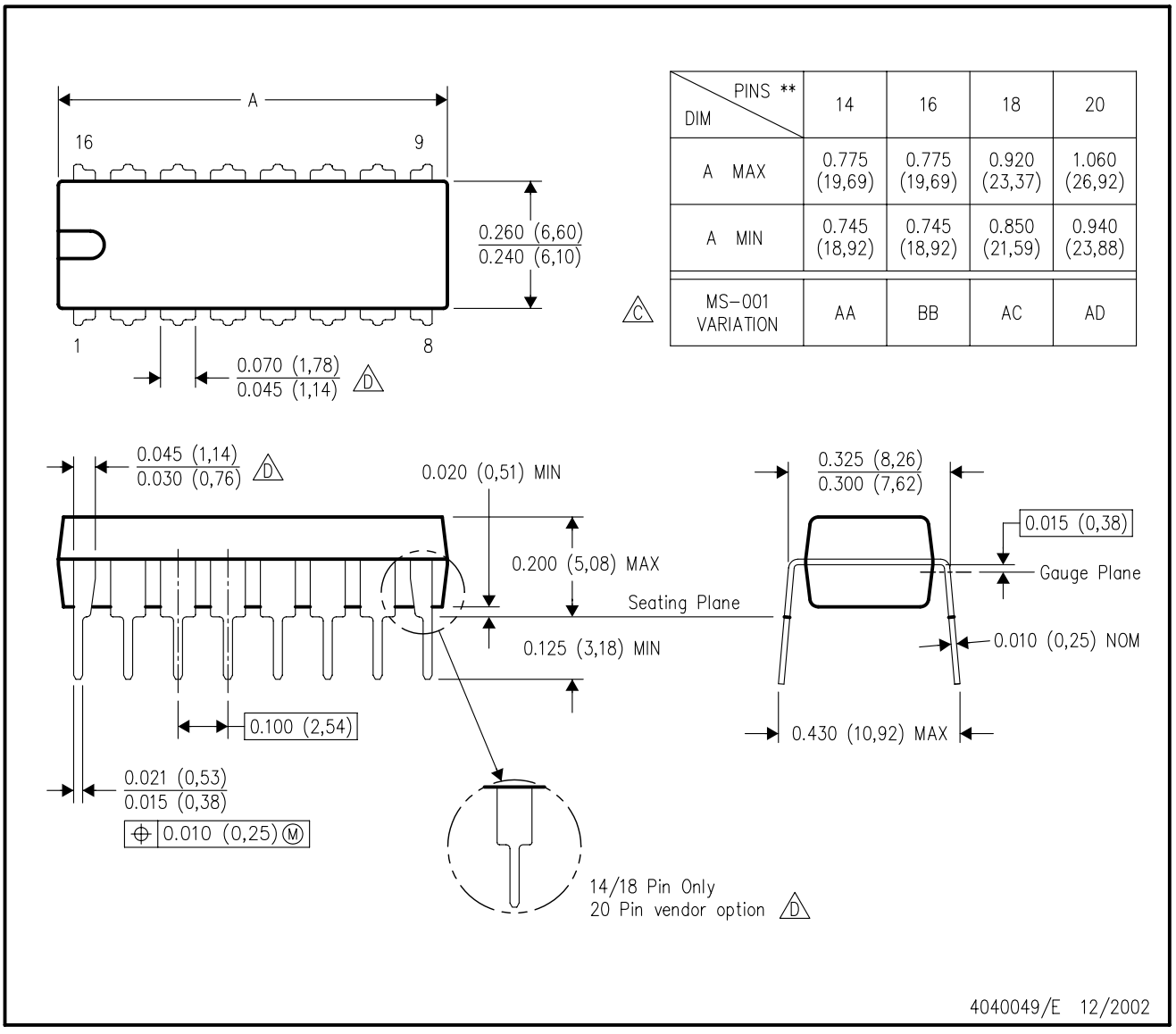
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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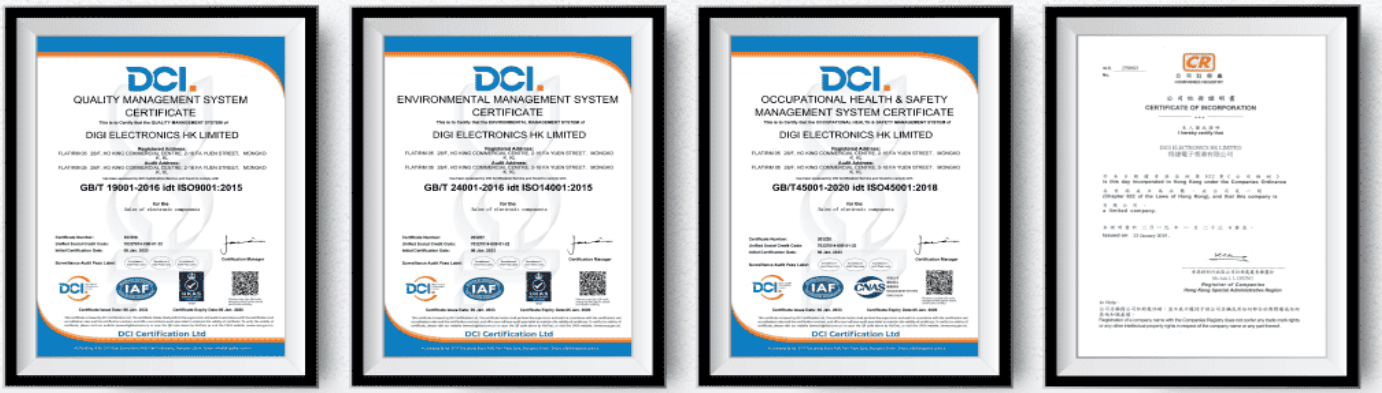

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