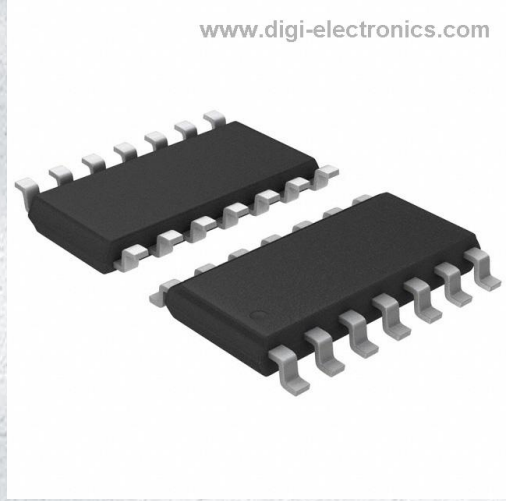
UA733CNSR Datasheet



DiGi Electronics Part Number	UA733CNSR-DG
Manufacturer	Texas Instruments
Manufacturer Product Number	UA733CNSR
Description	IC AMP DIFFERENTIAL 14SOP
Detailed Description	Video Amp 1 Differential 14-SO

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
UA733CNSR	Texas Instruments
Series:	Product Status:
-	Active
Applications:	Output Type:
Differential	Differential
Number of Circuits:	Slew Rate:
1	-
Current - Supply:	Current - Output / Channel:
16 mA	3.6 mA
Voltage - Supply, Single/Dual (±):	Mounting Type:
-	Surface Mount
Package / Case:	Supplier Device Package:
14-SOIC (0.209", 5.30mm Width)	14-SO
Base Product Number:	
UA733	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.33.0001	

μA733C, μA733M
DIFFERENTIAL VIDEO AMPLIFIERS

The μA733M is obsolete and no longer supplied.

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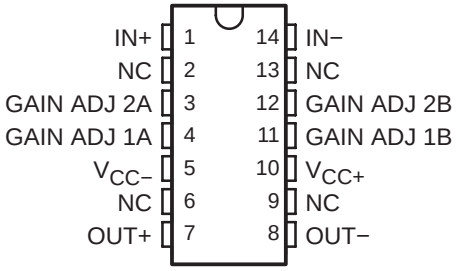
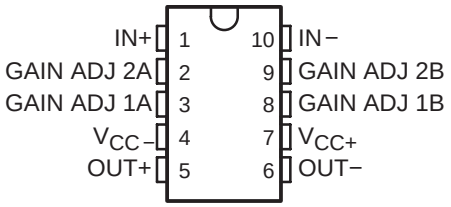
- **200-MHz Bandwidth**
- **250-kΩ Input Resistance**
- **Selectable Nominal Amplification of 10, 100, or 400**
- **No Frequency Compensation Required**

μA733C . . . D, N, OR NS PACKAGE
μA733M . . . J PACKAGE
(TOP VIEW)



NC — No internal connection

μA733M . . . U PACKAGE
(TOP VIEW)



description/ordering information

The μA733 is a monolithic two-stage video amplifier with differential inputs and differential outputs. Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads, and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 10 V/V, 100 V/V, or 400 V/V may be selected without external components, or amplification may be adjusted from 10 V/V to 400 V/V by the use of a single external resistor connected between 1A and 1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The μA733C is characterized for operation from 0°C to 70°C; the μA733M is characterized for operation over the full military temperature range of −55°C to 125°C.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	P-DIP (N)	Tube of 25	UA733CN	UA733CN
	SOIC (D)	Tube of 50	UA733CD	UA733C
		Reel of 2500	UA733CDR	
	SOP (NS)	Reel of 2000	UA733CNSR	UA733

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

μA733C, μA733M
DIFFERENTIAL VIDEO AMPLIFIERS

The μA733M is obsolete and no longer supplied.

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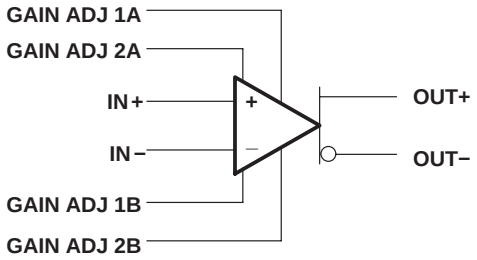
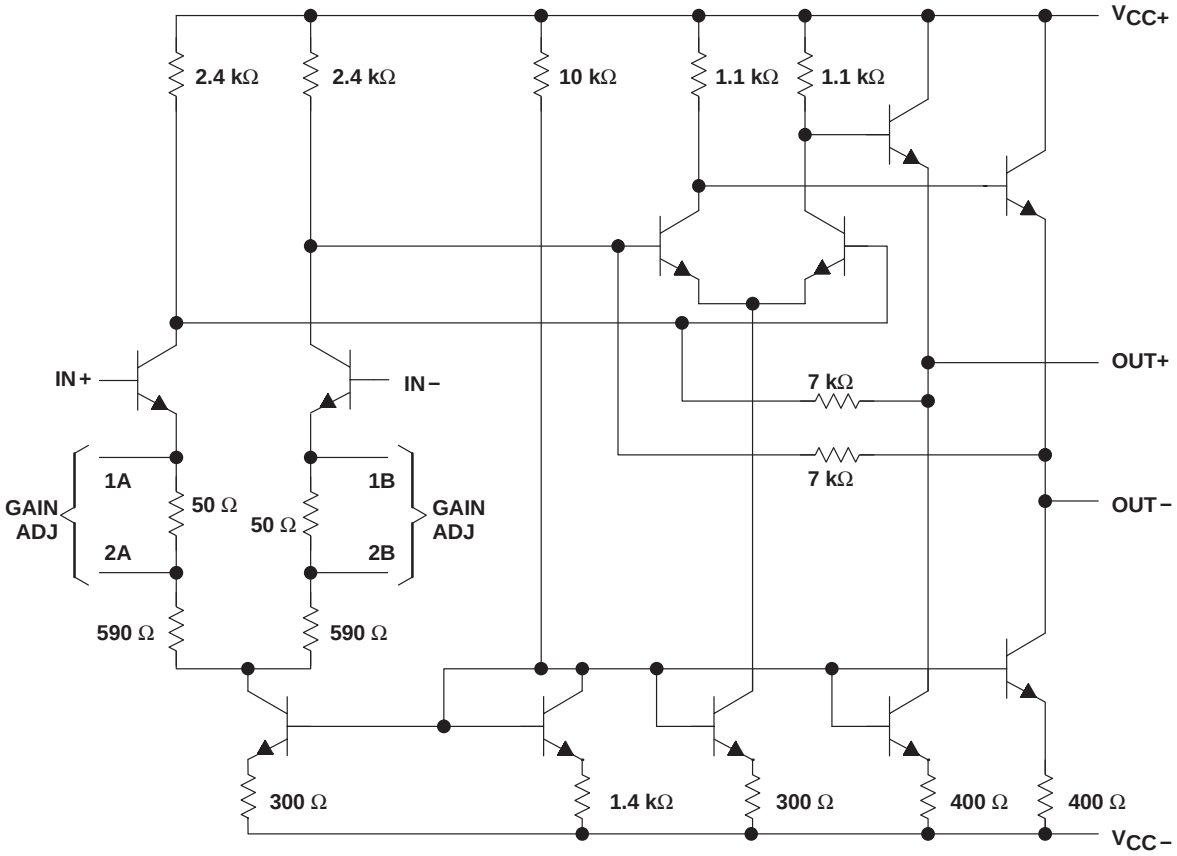
symbol



schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		μA733C	μA733M	UNIT
Supply voltage V_{CC+} (see Note 1)		8	8	V
Supply voltage V_{CC-} (see Note 1)		− 8	− 8	V
Differential input voltage		± 5	± 5	V
Common-mode input voltage		± 6	± 6	V
Output current		10	10	mA
Continuous total power dissipation		See Dissipation Rating Table		
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	D package	86		°C/W
	N package	80		
	NS package	76		
Maximum junction temperature, T_J		150		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package		300	°C
Storage temperature range, T_{stg}		− 65 to 150	− 65 to 150	°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
J (μA733M)	500 mW	11.0 mW/°C	104°C	500 mW	269 mW

μA733C, μA733M
DIFFERENTIAL VIDEO AMPLIFIERS

The μA733M is obsolete and no longer supplied.

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electrical characteristics, $V_{CC\pm}$ = ±6 V, T_A = 25°C

PARAMETER		FIGURE	TEST CONDITIONS	GAIN OPTION†	μA733C			μA733M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	250	400	600	300	400	500	V/V
				2	80	100	120	90	100	110	
				3	8	10	12	9	10	11	
BW	Bandwidth	2	R_S = 50 Ω	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	5		0.4	3	μA
I_{IB}	Input bias current			Any		9	30		9	20	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1.5		0.35	1	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	V_{OD} ≤ 1 V	1		4			4		kΩ
				2	10	24		20	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	V_{OD} ≤ 1 V	2		2			2		pF
CMRR	Common-mode rejection ration	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz	2		70			70		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	$\Delta V_{CC\pm}$ = ±0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	12		4.5	10	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, No signal	Any		16	24		16	24	mA

† The gain option is selected as follows:
Gain Option 1: Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2: Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3: All four gain-adjust pins are open.

The μA733M is obsolete and no longer supplied.

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electrical characteristics, $V_{CC\pm}$ = ±6 V, T_A = 0°C to 70°C for μA733C, − 55°C to 125°C for μA733M

PARAMETER		FIGURE	TEST CONDITIONS	GAIN OPTION†	μA733C		μA733M		UNIT
					MIN	MAX	MIN	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	250	600	200	600	V/V
				2	80	120	80	120	
				3	8	12	8	12	
I_{IO}	Input offset current			Any		6		5	μA
I_{IB}	Input bias current			Any		40		40	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1		±1		V
V_{OO}	Output offset voltage	1		1		1.5		1.5	V
				2 & 3		1.5		1.2	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	2.8		2.5		V
r_i	Input resistance	3	$V_{OD} \le 1$ V	2	8		8		kΩ
CMRR	Common-mode rejection ratio	4	V_{IC} = +1 V, f ≤ 100 kHz	2	50		50		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/(\Delta V_{IO})$	1	$\Delta V_{CC\pm}$ = ±0.5 V	2	50		50		dB
$I_{sink(max)}$	Maximum output sink current			Any	2.5		2.2		mA
I_{CC}	Supply current		No load, No signal	Any		27		27	mA

† The gain option is selected as follows:
Gain Option 1: Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2: Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3: All four gain-adjust pins are open.

PARAMETER MEASUREMENT INFORMATION

test circuits

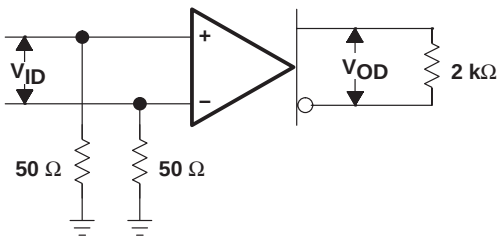


Figure 1

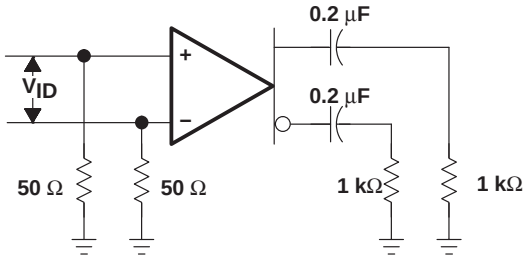


Figure 2

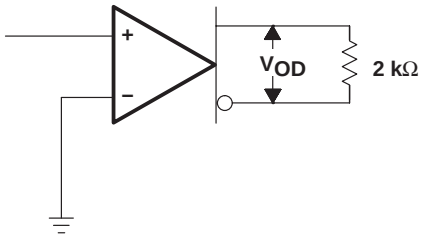


Figure 3

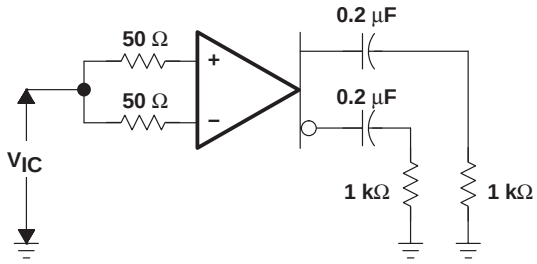


Figure 4

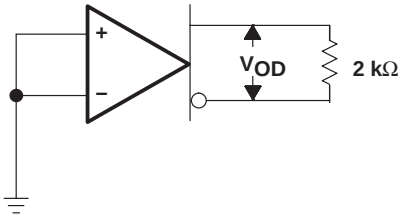
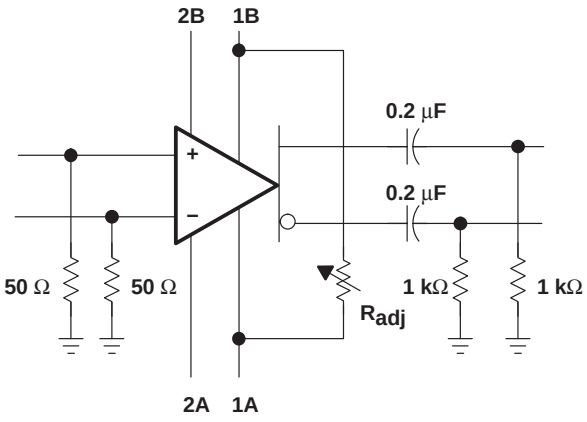


Figure 5



VOLTAGE AMPLIFICATION ADJUSTMENT

Figure 6

The μA733M is obsolete and no longer supplied.

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TYPICAL CHARACTERISTICS

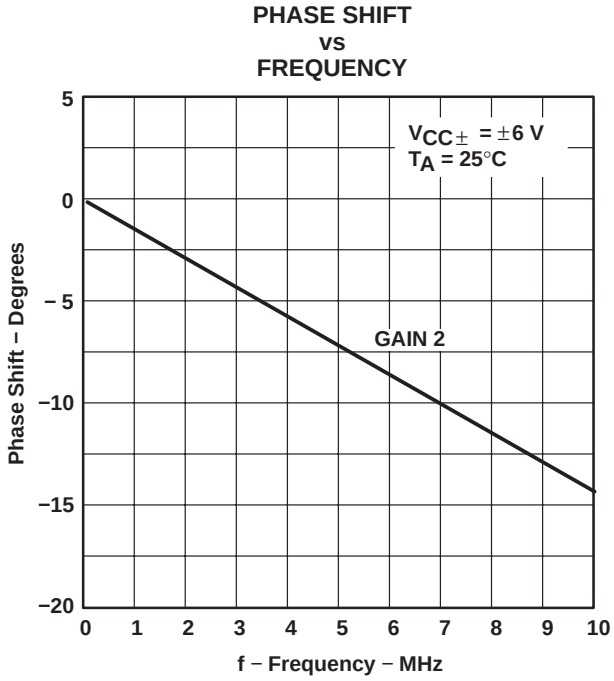

Figure 7

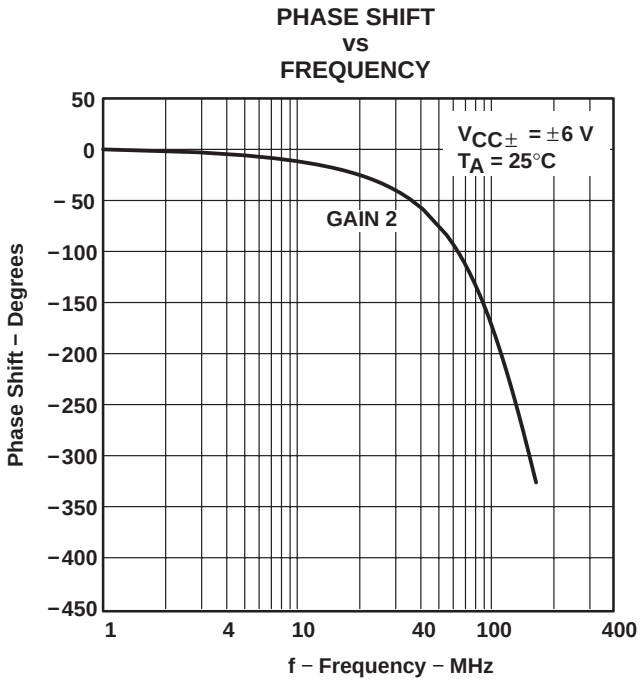

Figure 8

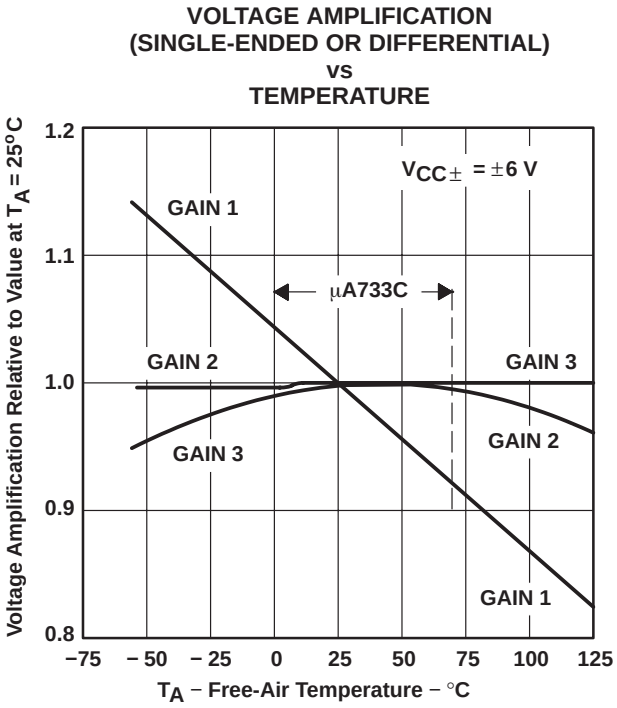

Figure 9

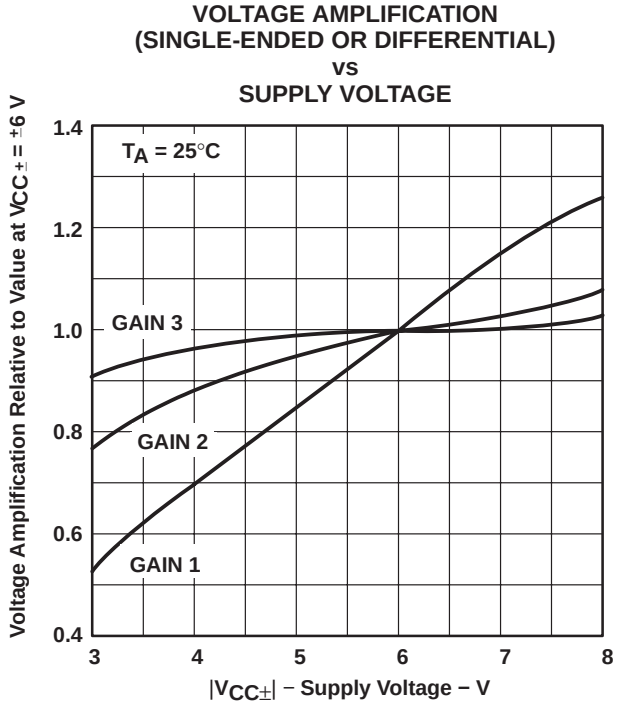

Figure 10

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION vs RESISTANCE BETWEEN G1A AND G1B

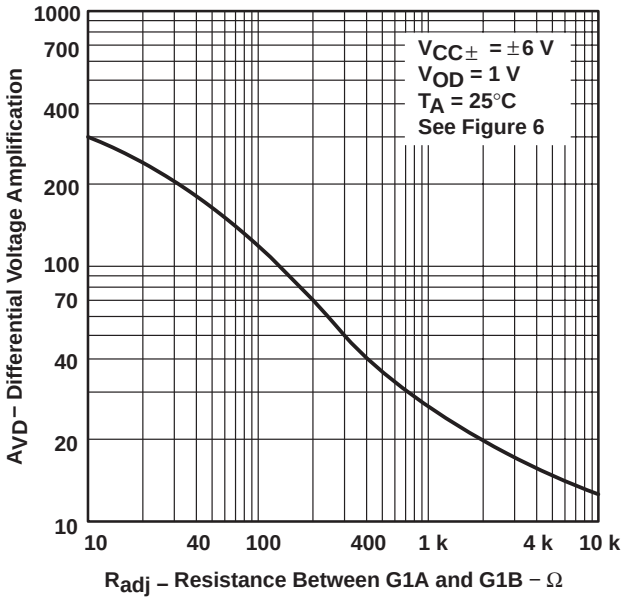

Figure 11

SINGLE-ENDED VOLTAGE AMPLIFICATION vs FREQUENCY

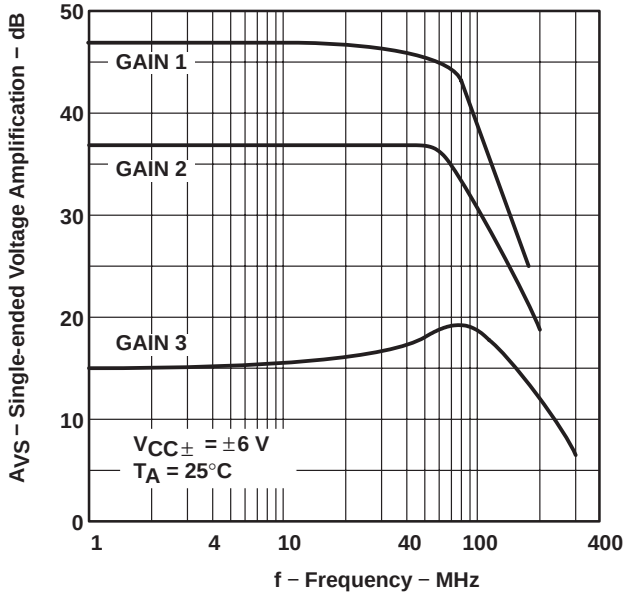

Figure 12

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

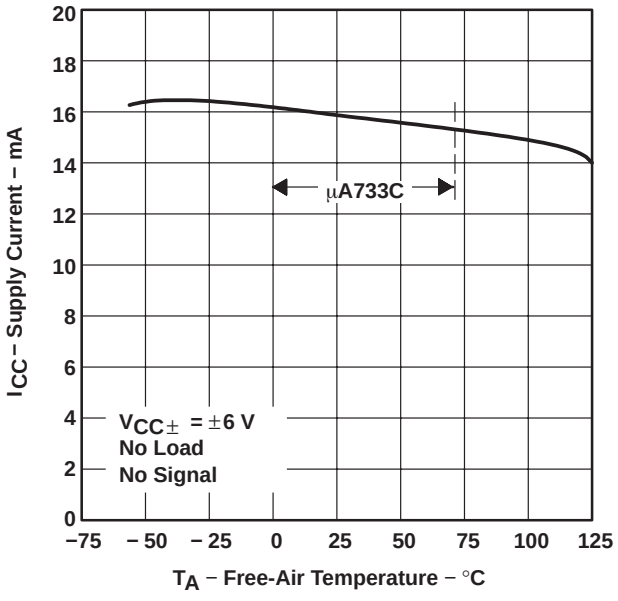

Figure 13

SUPPLY CURRENT vs SUPPLY VOLTAGE

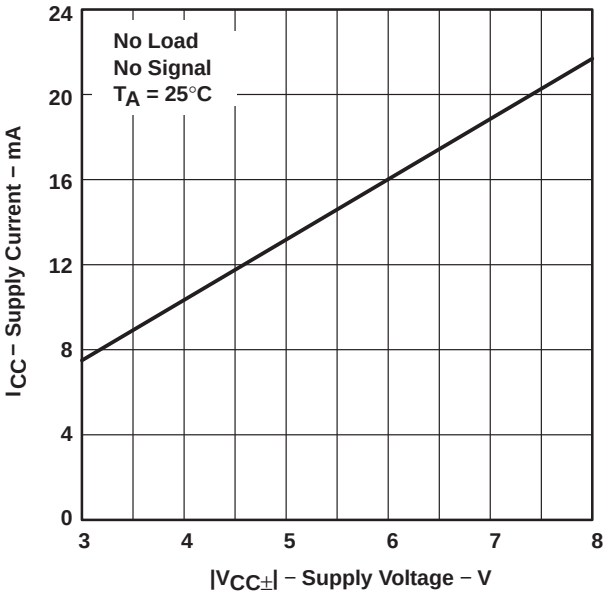

Figure 14

The μA733M is obsolete and no longer supplied.

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

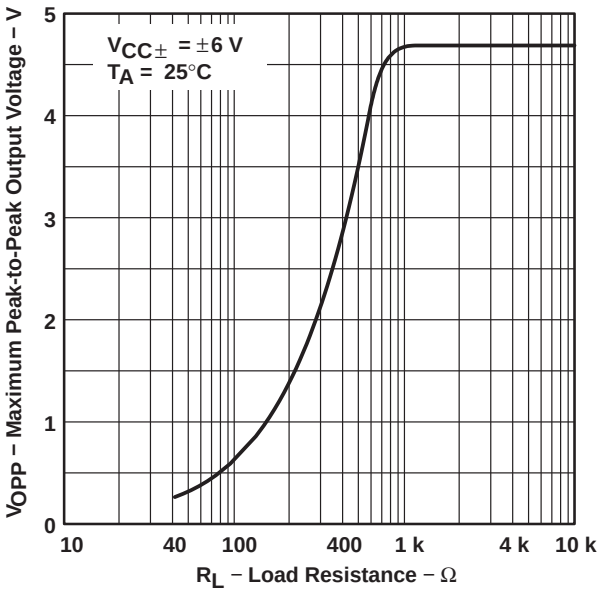


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

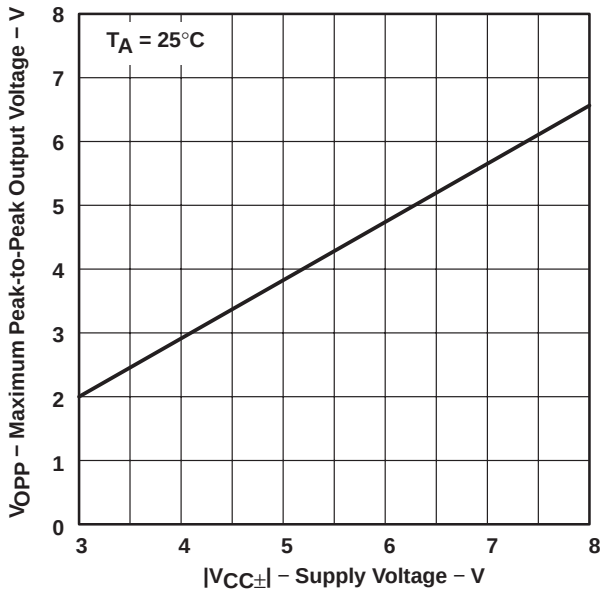


Figure 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

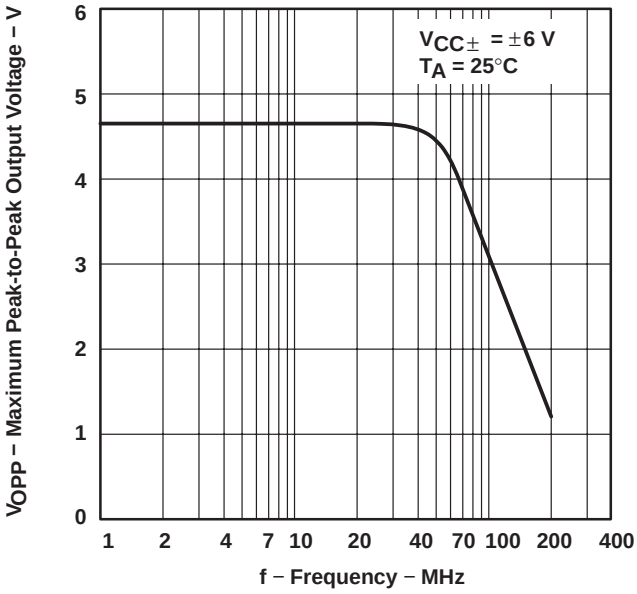


Figure 17

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

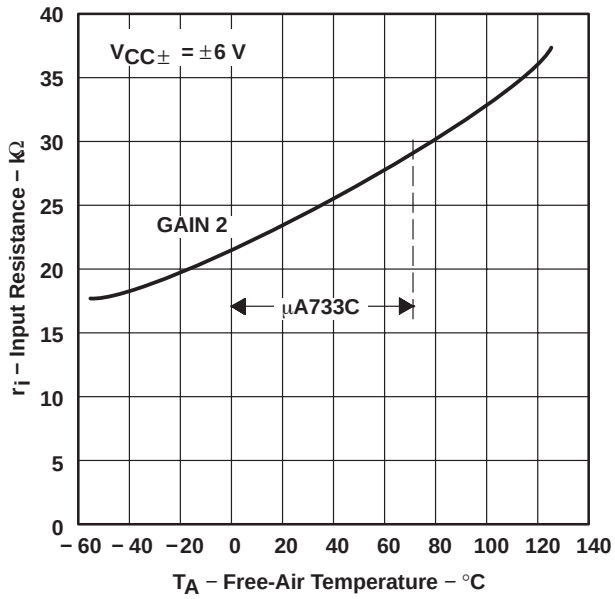


Figure 18

TEXAS INSTRUMENTS

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA733CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733C	Samples
UA733CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733C	Samples
UA733CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UA733CN	Samples
UA733CNSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

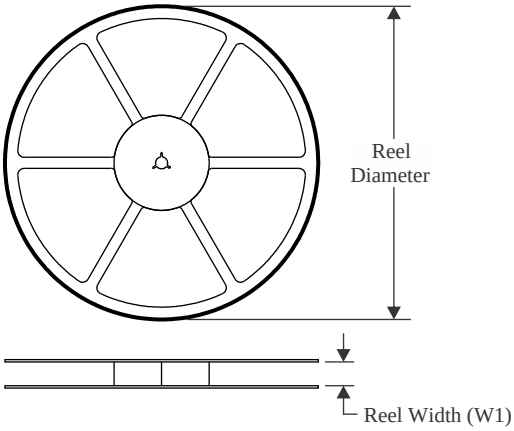
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

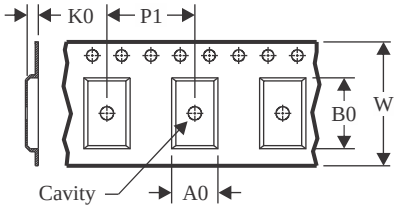
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

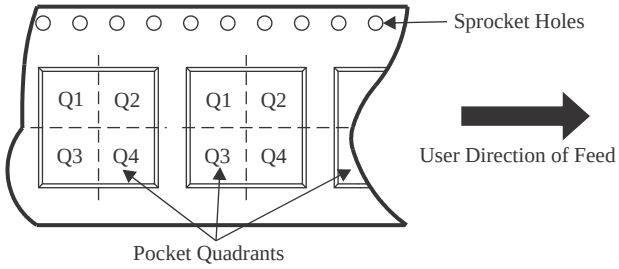


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

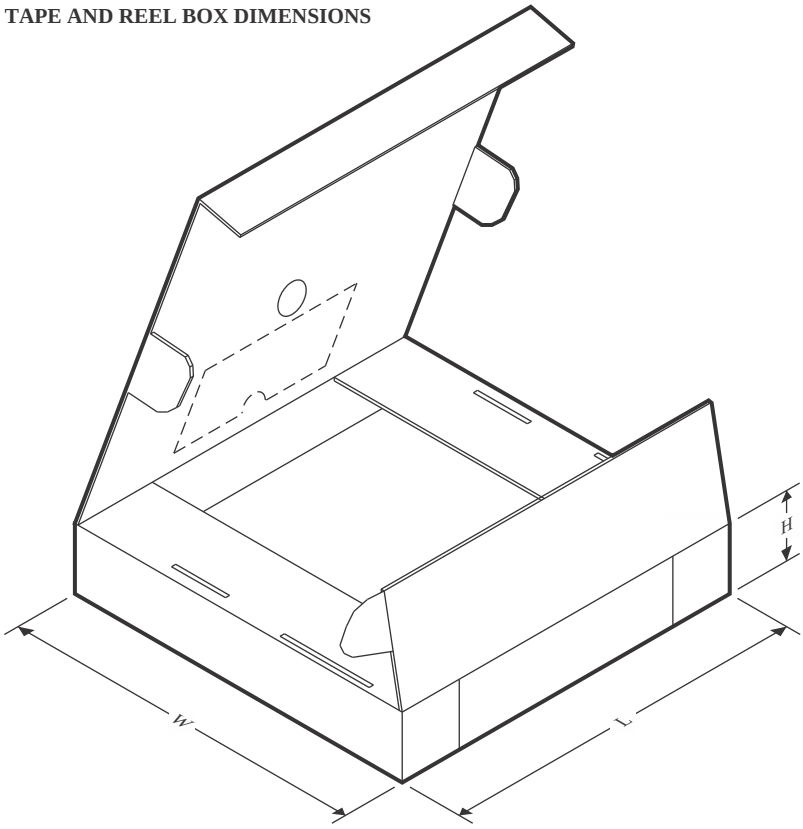


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA733CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UA733CNSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

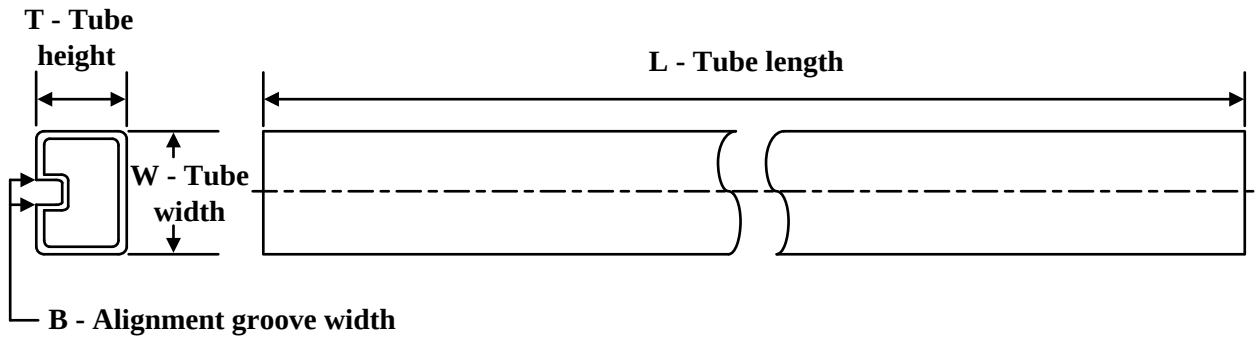


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA733CDR	SOIC	D	14	2500	356.0	356.0	35.0
UA733CNSR	SOP	NS	14	2000	356.0	356.0	35.0

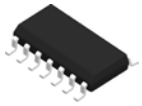
PACKAGE MATERIALS INFORMATION

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UA733CD	D	SOIC	14	50	506.6	8	3940	4.32
UA733CN	N	PDIP	14	25	506	13.97	11230	4.32

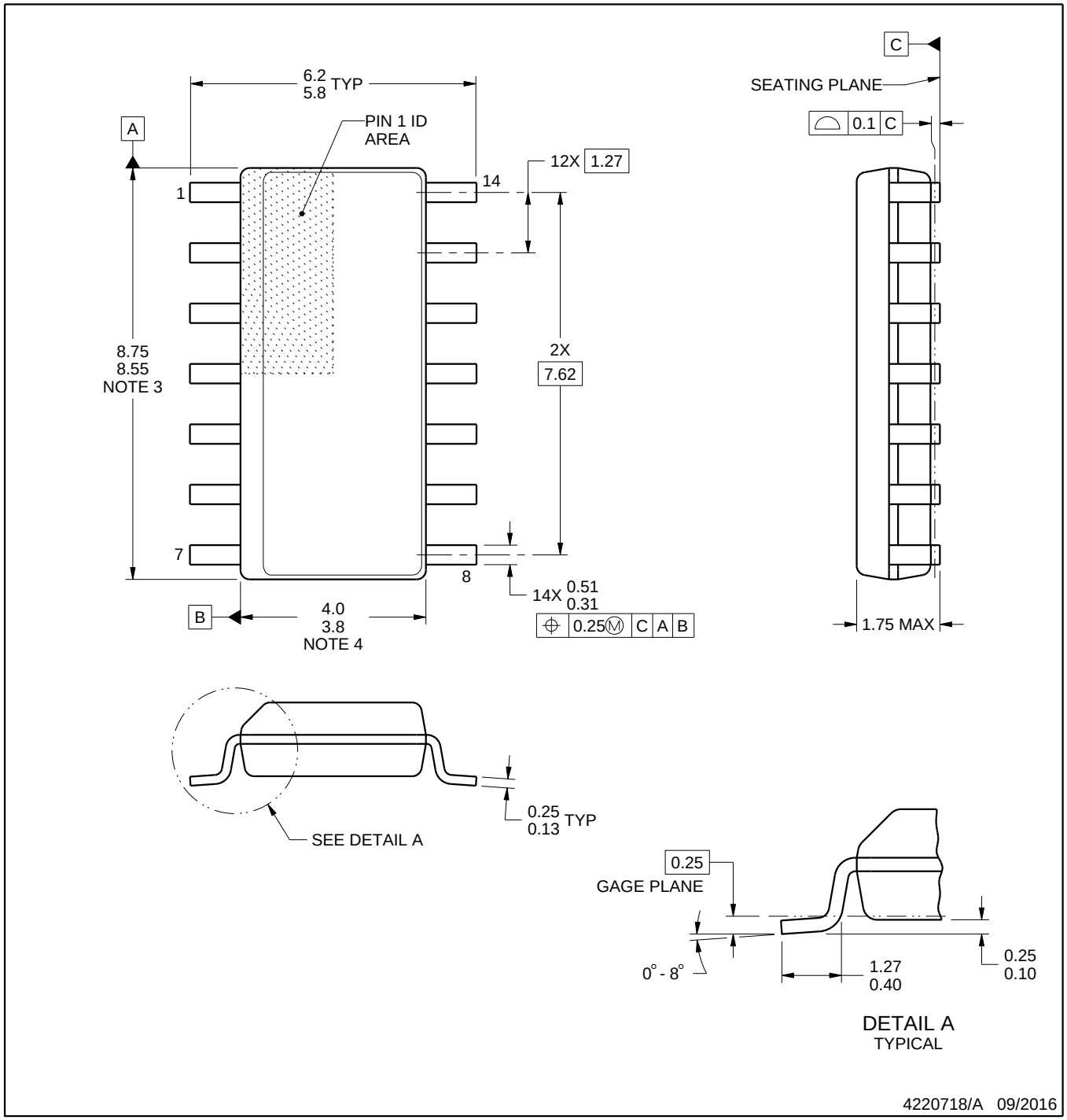


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

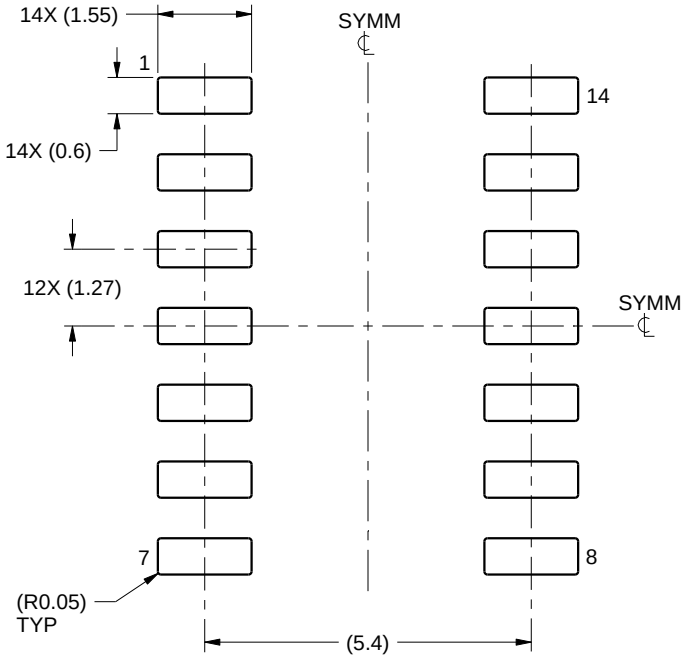
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

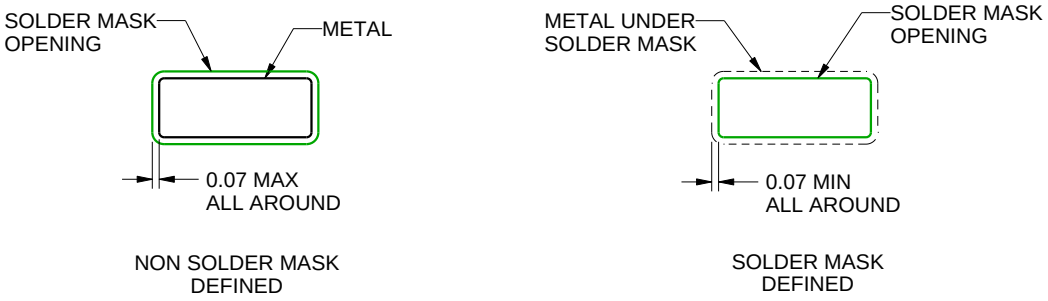
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

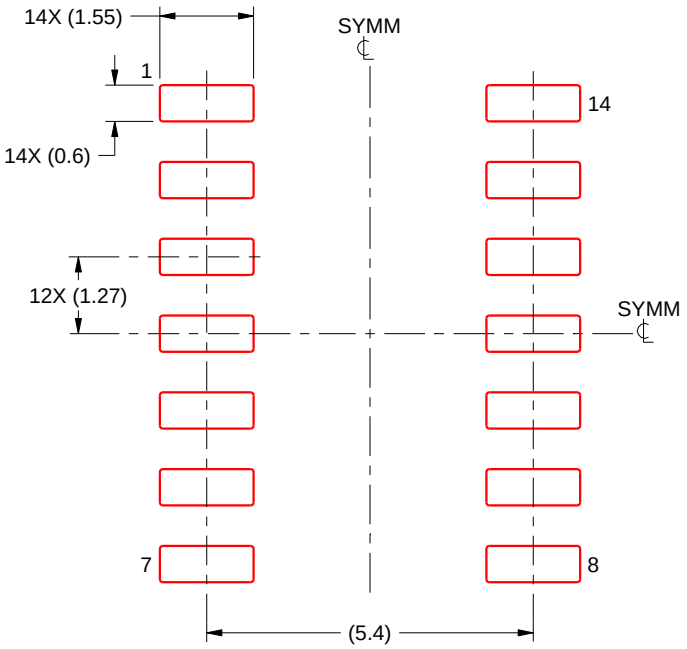
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

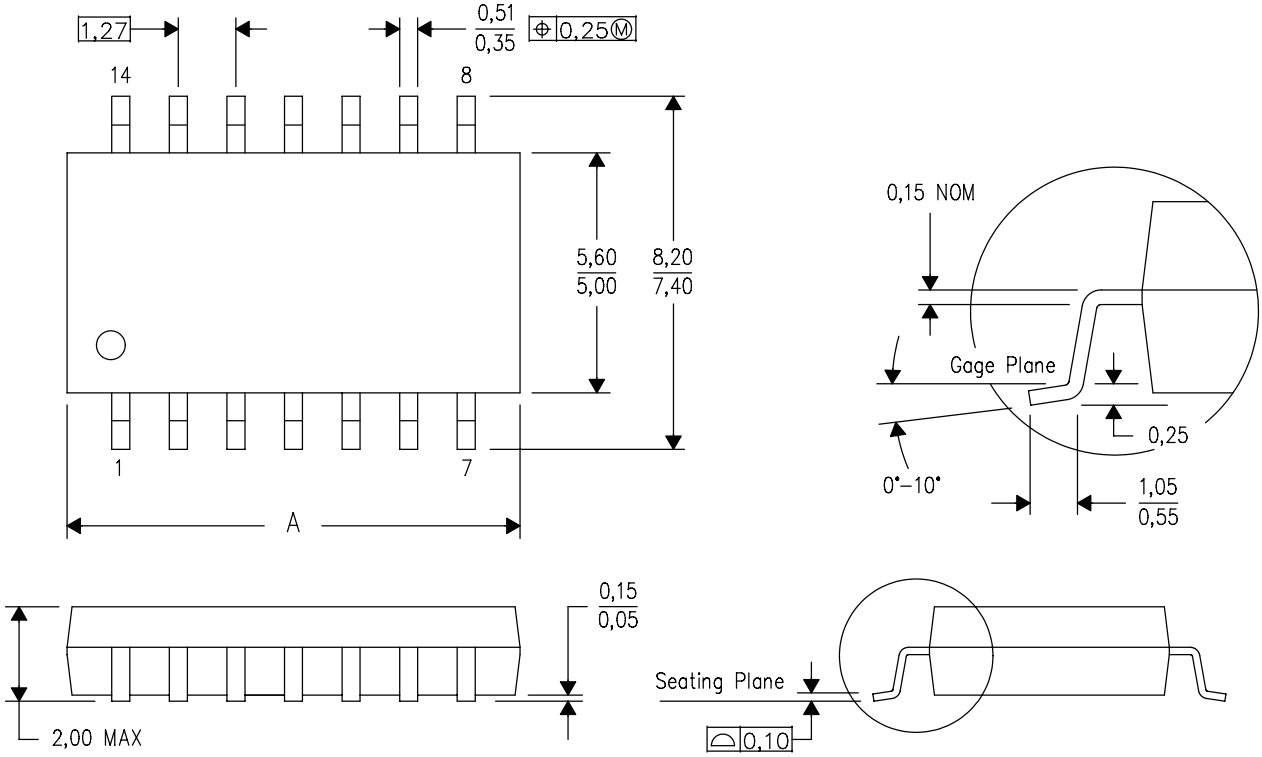
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

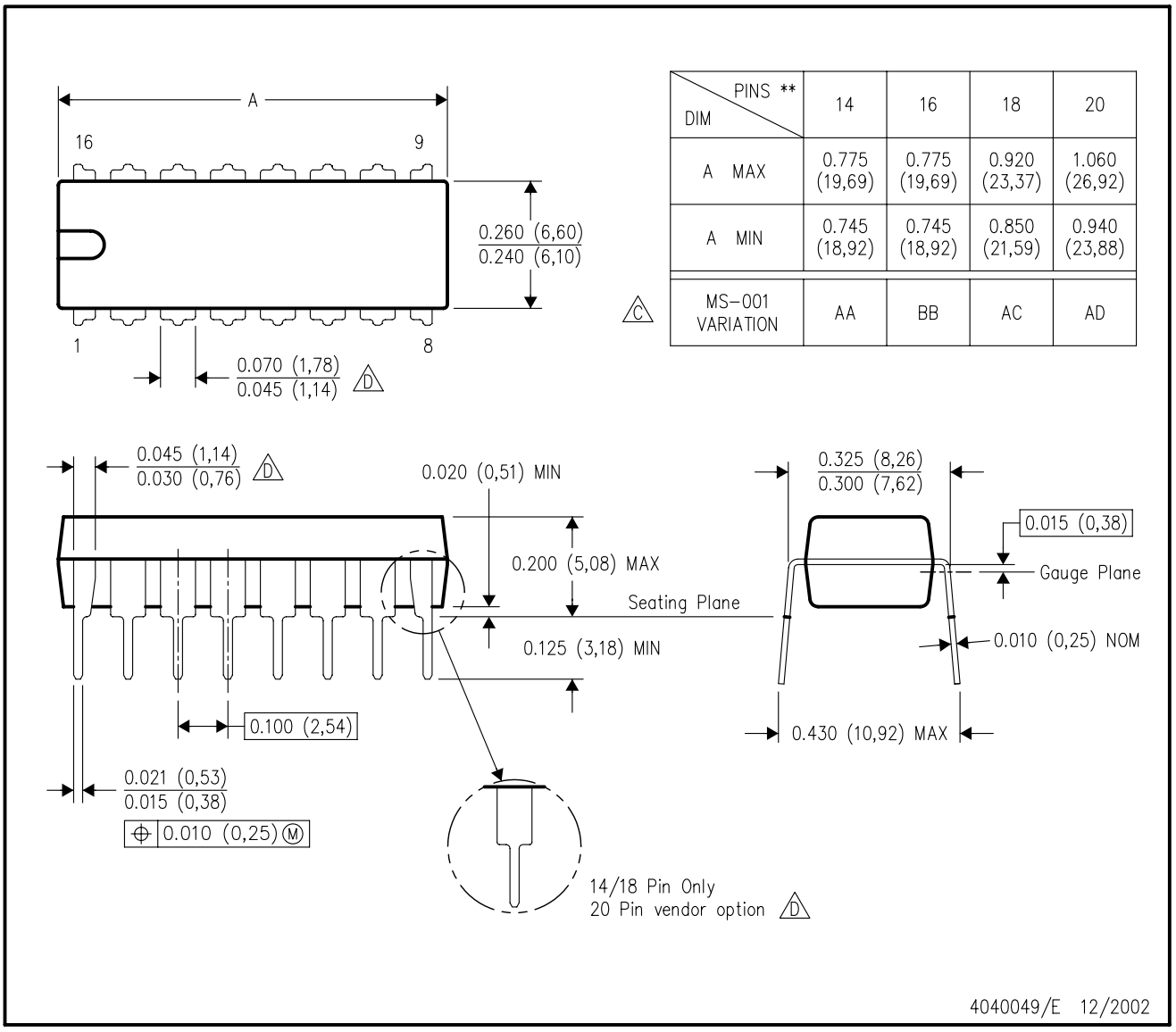
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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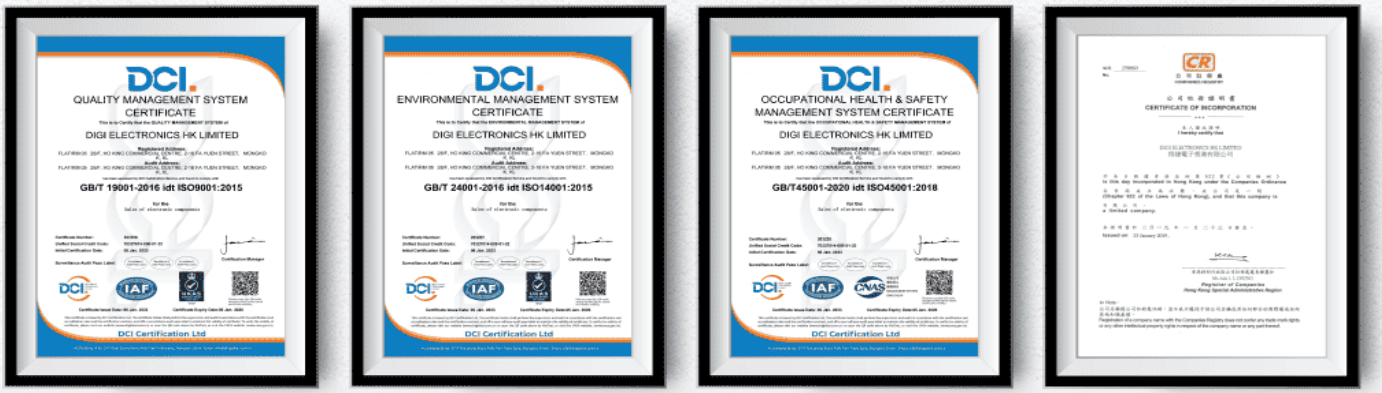

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