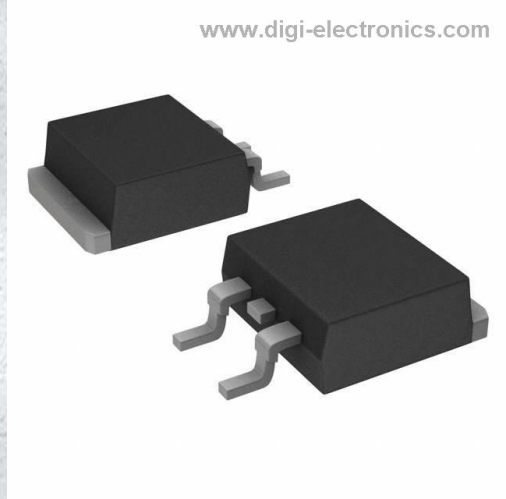
IRF540SPBF Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	IRF540SPBF-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	IRF540SPBF
Description	MOSFET N-CH 100V 28A D2PAK
Detailed Description	N-Channel 100 V 28A (Tc) 3.7W (Ta), 150W (Tc) Surface Mount TO-263 (D2PAK)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
IRF540SPBF	Vishay Siliconix
Series:	Product Status:
-	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
100 V	28A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	77mOhm @ 17A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 250µA	72 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	1700 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	3.7W (Ta), 150W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 175°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
TO-263 (D2PAK)	TO-263-3, D2PAK (2 Leads + Tab), TO-263AB
Base Product Number:	
IRF540	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Affected	EAR99
HTSUS:	
8541.29.0095	

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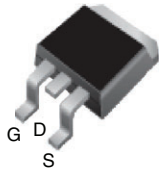
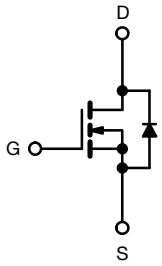
IRF540S, SiHF540S

Vishay Siliconix

Power MOSFET

D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available
HALOGEN FREE Available

Note
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.077
Q_g max. (nC)	72	
Q_{gs} (nC)	11	
Q_{gd} (nC)	32	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION			
Package	D²PAK (TO-263)	D²PAK (TO-263)	D²PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHF540S-GE3	SiHF540STRL-GE3 [a]	SiHF540STRR-GE3 [a]
Lead (Pb)-free	IRF540SPbF	IRF540STRLPbF [a]	IRF540STRRPbF [a]

Note
a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage			V_{DS}	100	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	28	A
		T_C = 100 °C		20	
Pulsed drain current [a]			I_{DM}	110	
Linear derating factor				1.0	W/°C
Linear derating factor (PCB mount) [e]				0.025	
Single pulse avalanche energy [b]			E_{AS}	230	mJ
Avalanche current [a]			I_{AR}	28	A
Repetitive avalanche energy [a]			E_{AR}	15	mJ
Maximum power dissipation	T_C = 25 °C		P_D	150	W
Maximum power dissipation (PCB mount) [e]	T_A = 25 °C			3.7	
Peak diode recovery dv/dt [c]			dv/dt	5.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d]	for 10 s			300	

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 440 µH, R_g = 25 Ω, I_{AS} = 28 A (see fig. 12)
c. I_{SD} ≤ 28 A, di/dt ≤ 170 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
d. 1.6 mm from case
e. When mounted on 1" square PCB (FR-4 or G-10 material)

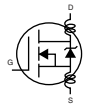
THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-ambient (PCB mount) [a]	R_{thJA}	-	40	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA	100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.13	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 17 A [b]	-	-	0.077	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 17 A [b]	8.7	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	1700	-	pF
Output capacitance	C_{oss}		-	560	-	
Reverse transfer capacitance	C_{rss}		-	120	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 17 A, V_{DS} = 80 V, see fig. 6 and 13 [b]	-	-	72	nC
Gate-source charge	Q_{gs}		-	-	11	
Gate-drain charge	Q_{gd}		-	-	32	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 17 A, R_g = 9.1 Ω, R_D = 2.9 Ω, see fig. 10 [b]	-	11	-	ns
Rise time	t_r		-	44	-	
Turn-off delay time	$t_{d(off)}$		-	53	-	
Fall time	t_f		-	43	-	
Gate input resistance	R_g	f = 1 MHz, open drain	0.5	-	3.6	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	28	A
Pulsed diode forward current [a]	I_{SM}		-	-	110	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 28 A, V_{GS} = 0 V [b]	-	-	2.5	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 17 A, dI/dt = 100 A/µs [b]	-	180	360	ns
Body diode reverse recovery charge	Q_{rr}		-	1.3	2.8	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

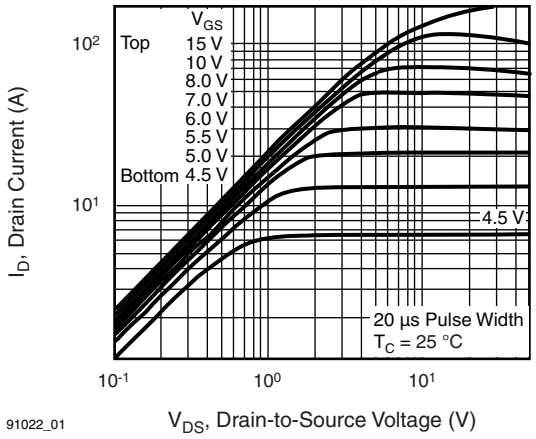


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

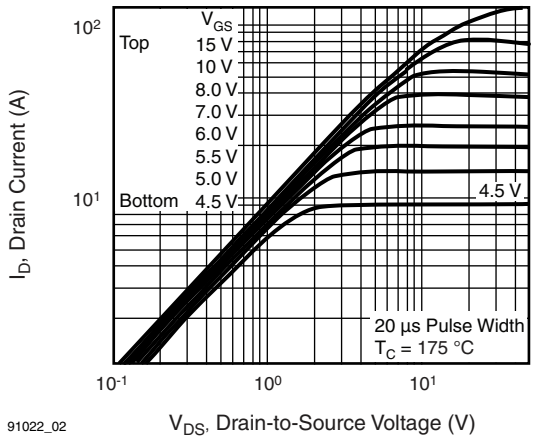


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

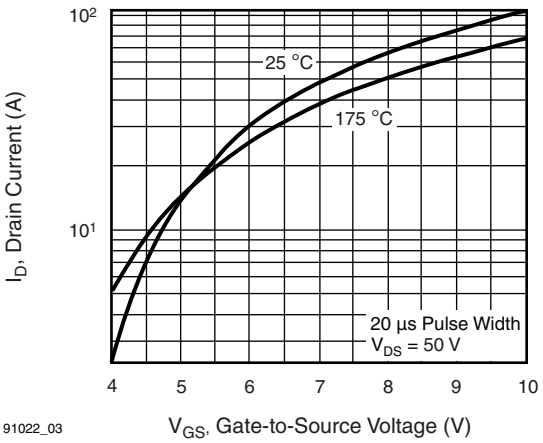


Fig. 3 - Typical Transfer Characteristics

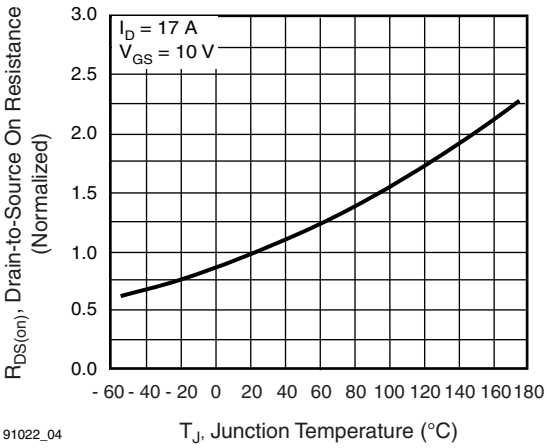


Fig. 4 - Normalized On-Resistance vs. Temperature

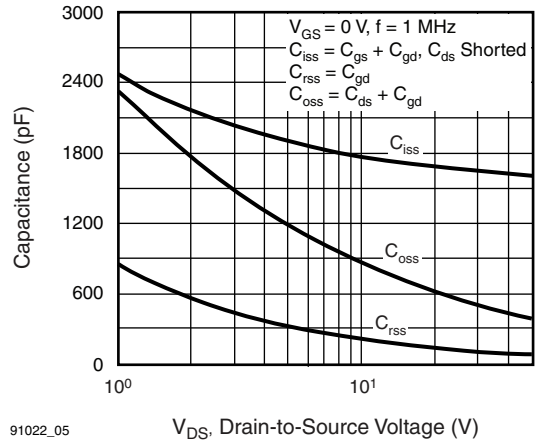


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

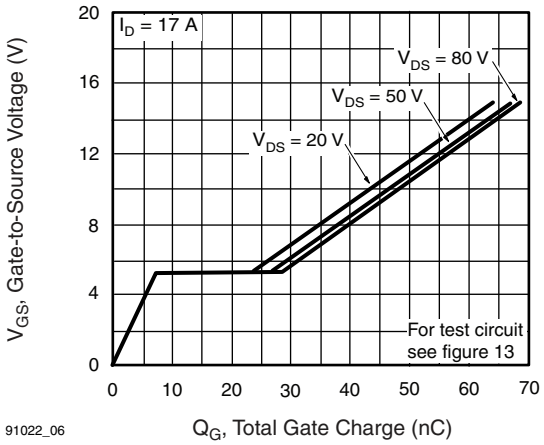


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

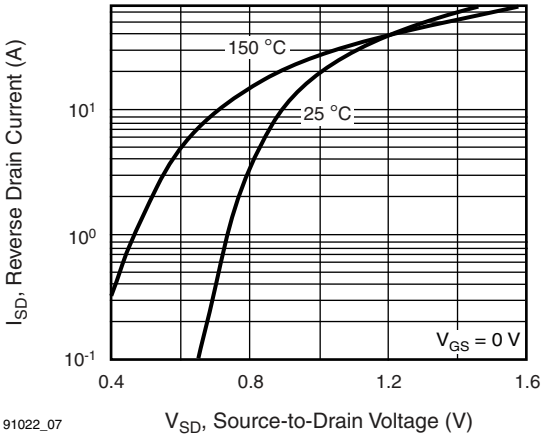


Fig. 7 - Typical Source-Drain Diode Forward Voltage

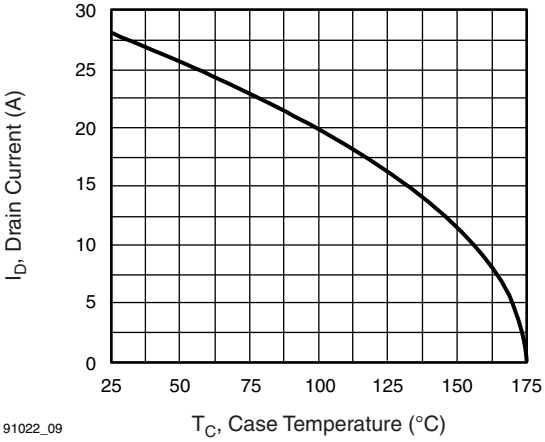


Fig. 9 - Maximum Drain Current vs. Case Temperature

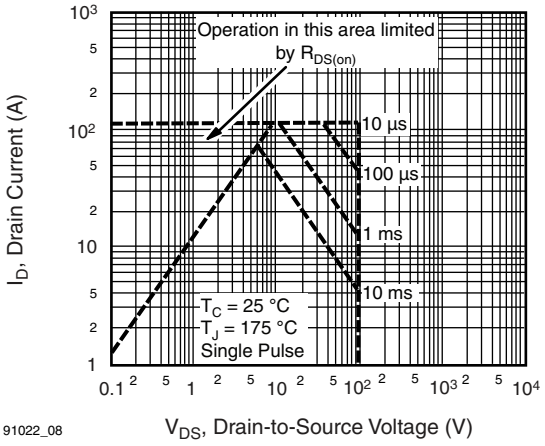


Fig. 8 - Maximum Safe Operating Area

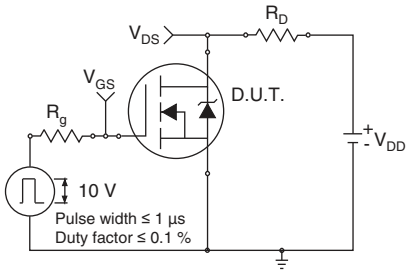


Fig. 10a - Switching Time Test Circuit

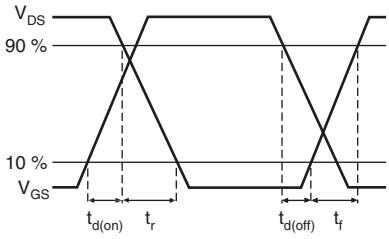


Fig. 10b - Switching Time Waveforms

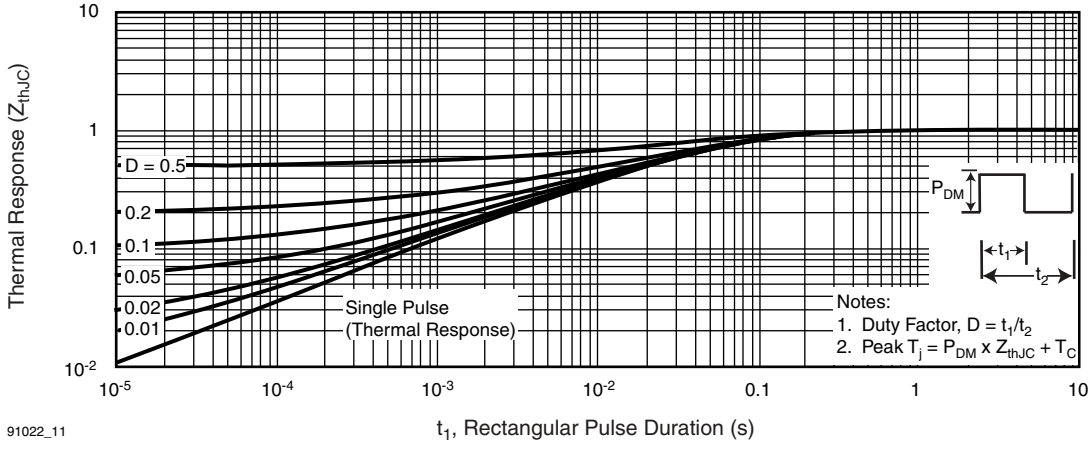


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

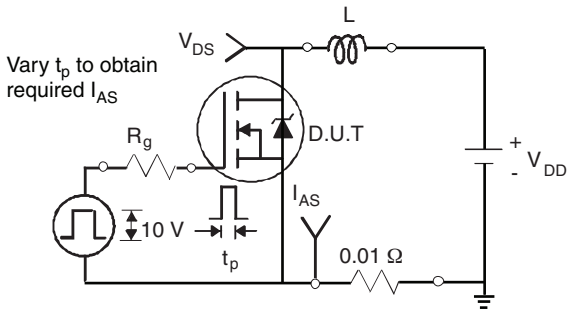


Fig. 12a - Unclamped Inductive Test Circuit

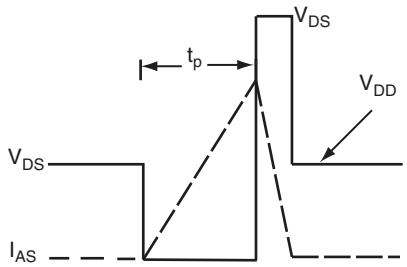


Fig. 12b - Unclamped Inductive Waveforms

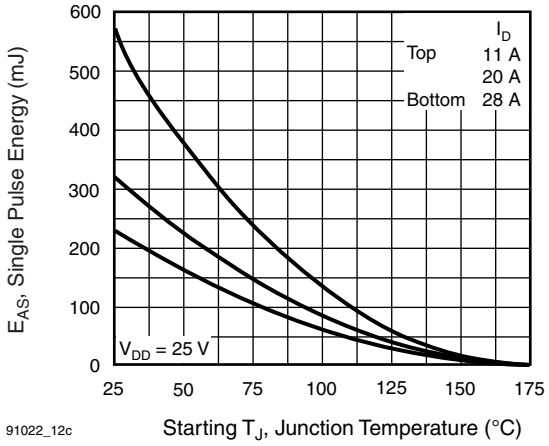


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

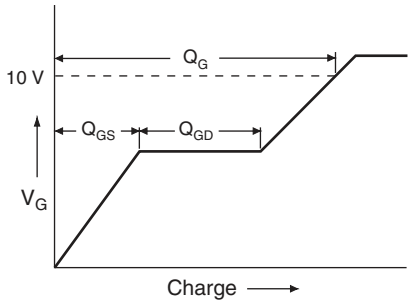


Fig. 13a - Basic Gate Charge Waveform

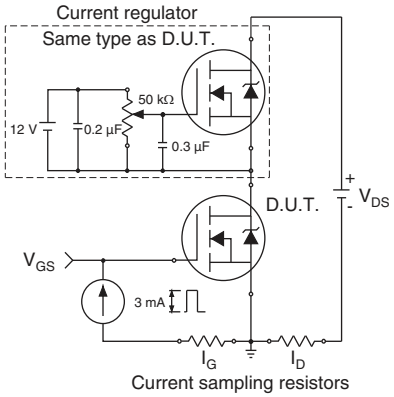
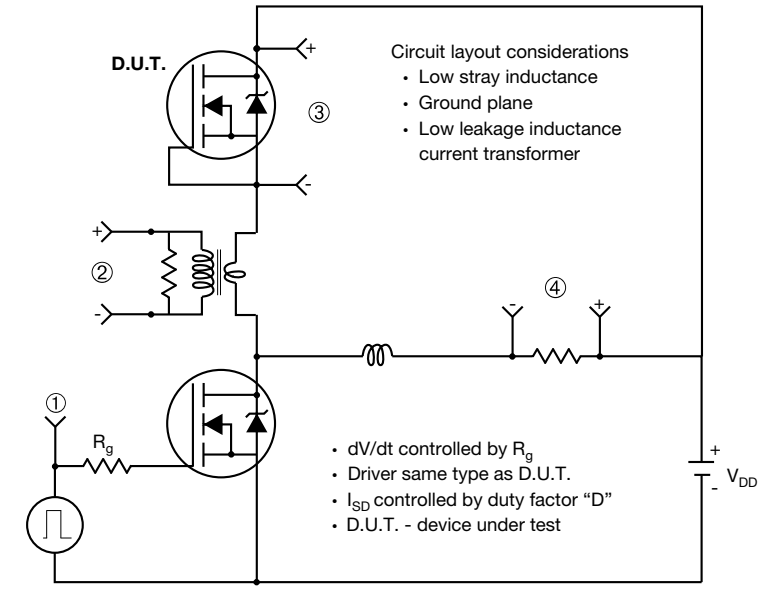
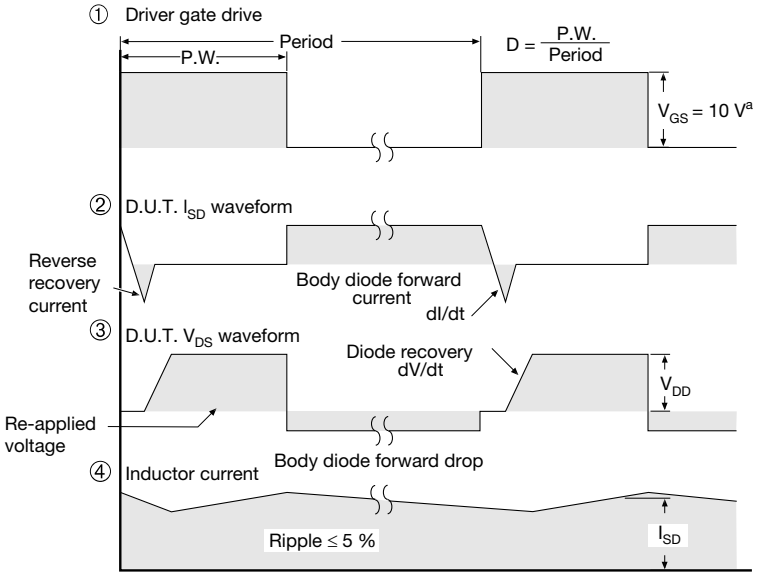


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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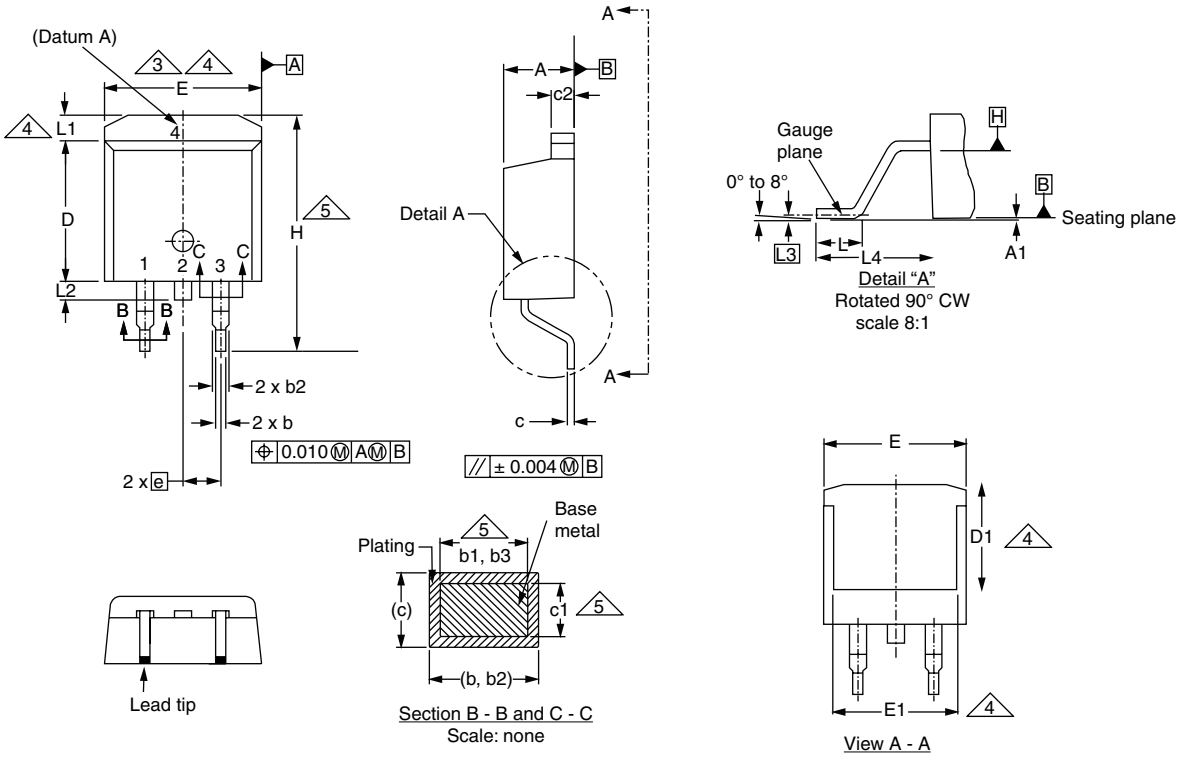
Package Information

Vishay Siliconix

TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

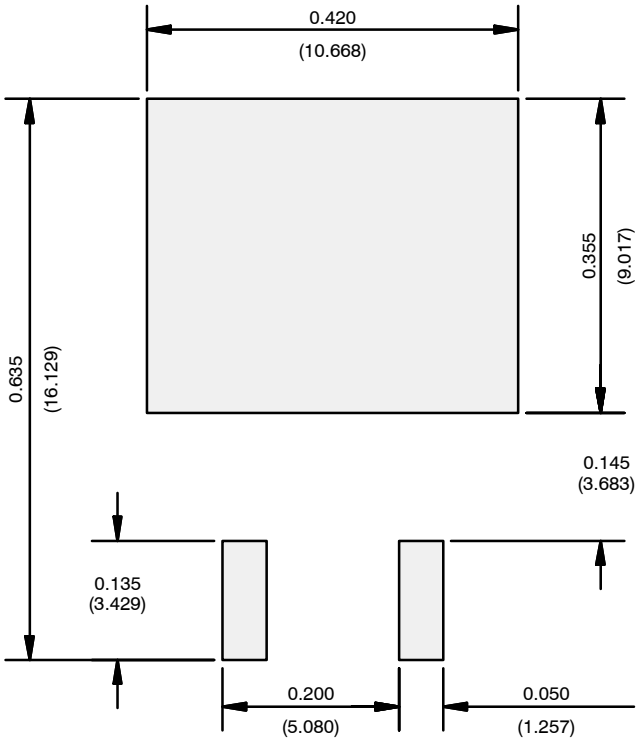
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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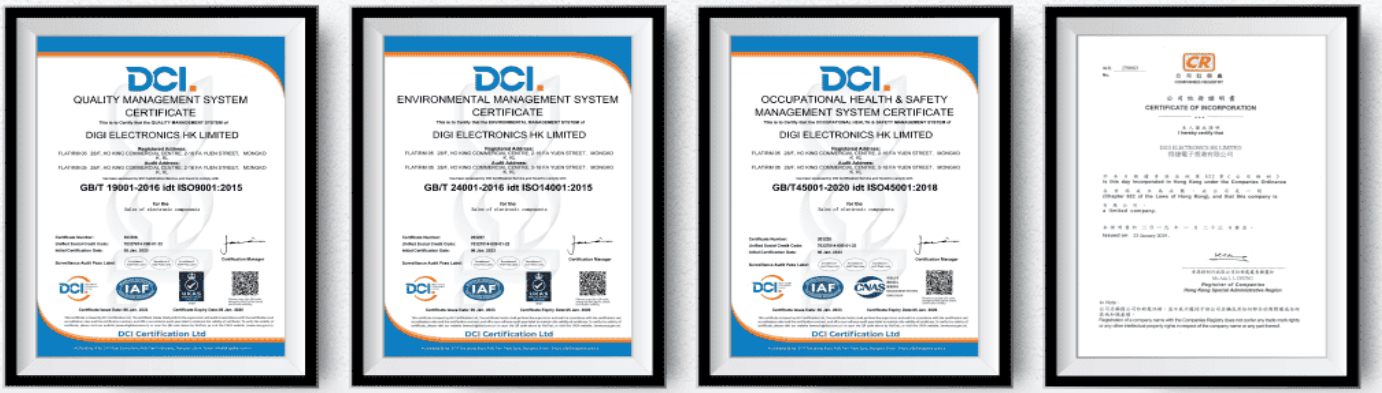

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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