IRF740APBF Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	IRF740APBF-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	IRF740APBF
Description	MOSFET N-CH 400V 10A TO220AB
Detailed Description	N-Channel 400 V 10A (Tc) 125W (Tc) Through Hole TO-220AB

Purchase and inquiry

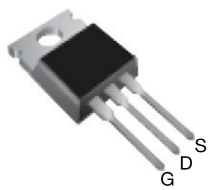
Manufacturer Product Number:	Manufacturer:
IRF740APBF	Vishay Siliconix
Series:	Product Status:
-	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
400 V	10A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	550mOhm @ 6A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 250μA	36 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±30V	1030 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	125W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Through Hole
Supplier Device Package:	Package / Case:
TO-220AB	TO-220-3
Base Product Number:	
IRF740	

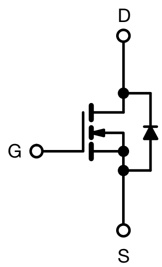
Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Affected	EAR99
HTSUS:	
8541.29.0095	

Power MOSFET

TO-220AB





N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	400	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.55
Q_g (Max.) (nC)	36	
Q_{gs} (nC)	9.9	
Q_{gd} (nC)	16	
Configuration	Single	

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche, and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Single transistor flyback Xfmr. reset
- Single transistor forward Xfmr. reset (both for US line input only)

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF740APbF
Lead (Pb)-free and halogen-free	IRF740APbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

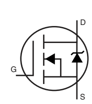
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	400	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	10	A
		T_C = 100 °C		6.3	
Pulsed drain current [a]			I_{DM}	40	
Linear derating factor				1.0	W/°C
Single pulse avalanche energy [b]			E_{AS}	630	mJ
Repetitive avalanche current [a]			I_{AR}	10	A
Repetitive avalanche energy [a]			E_{AR}	12.5	mJ
Maximum power dissipation	T_C = 25 °C		P_D	125	W
Peak diode recovery dV/dt [c]			dV/dt	5.9	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	- 55 to + 150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300[d]	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 12.6 mH, R_g = 25 Ω, I_{AS} = 10 A (see fig. 12)
c. $I_{SD} \leq$ 10 A, dV/dt $\leq$ 330 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C
d. 1.6 mm from case

For technical questions, contact: hvm@vishay.com

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		400	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.48	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V		-	-	25	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 6.0 A[b]	-	-	0.55	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 6.0 A[b]		4.9	-	-	S
Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1030	-	pF
Output capacitance	C_{oss}			-	170	-	
Reverse transfer capacitance	C_{rss}			-	7.7	-	
Output capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 1.0 V, f = 1.0 MHz		-	1490	-	
		V_{GS} = 0 V, V_{DS} = 320 V, f = 1.0 MHz		-	52	-	
Effective output capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 0 V to 320 V		-	61	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 10 A, V_{DS} = 320 V, see fig. 6 and 13[b]	-	-	36	nC
Gate-source charge	Q_{gs}			-	-	9.9	
Gate-drain charge	Q_{gd}			-	-	16	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 200 V, I_D = 10 A, R_g = 10 Ω, R_D = 19.5 Ω, see fig. 10[b]		-	10	-	ns
Rise time	t_r			-	35	-	
Turn-off delay time	$t_{d(off)}$			-	24	-	
Fall time	t_f			-	22	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	10	A
Pulsed diode forward current [a]	I_{SM}			-	-	40	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 10 A, V_{GS} = 0 V[b]		-	-	2.0	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 10 A, dI/dt = 100 A/μs[b]		-	240	360	ns
Body diode reverse recovery charge	Q_{rr}			-	1.9	2.9	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

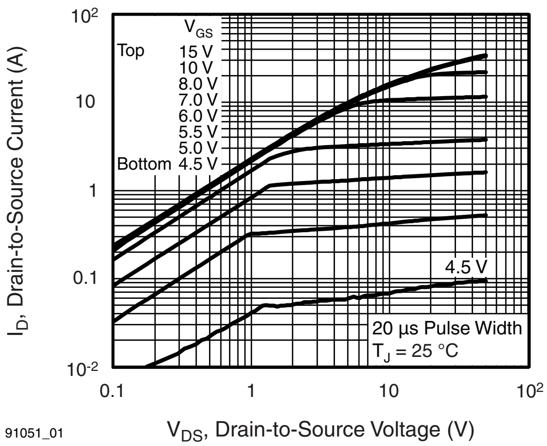


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

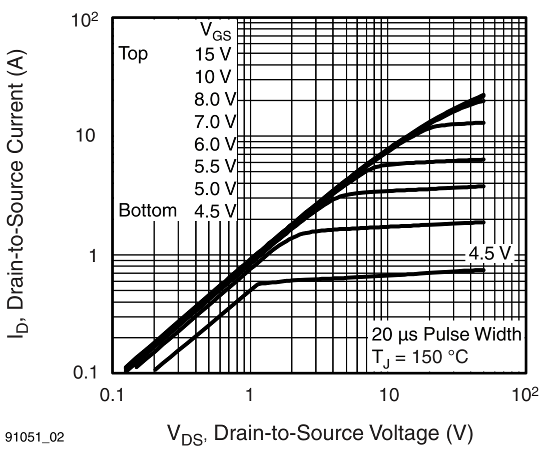


Fig. 1 - Typical Output Characteristics, T_C = 150 °C

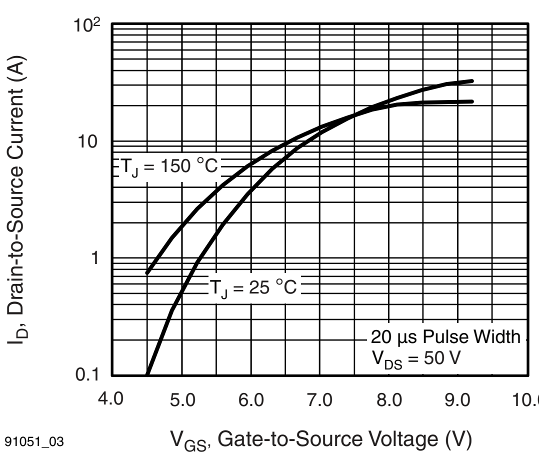


Fig. 2 - Typical Transfer Characteristics

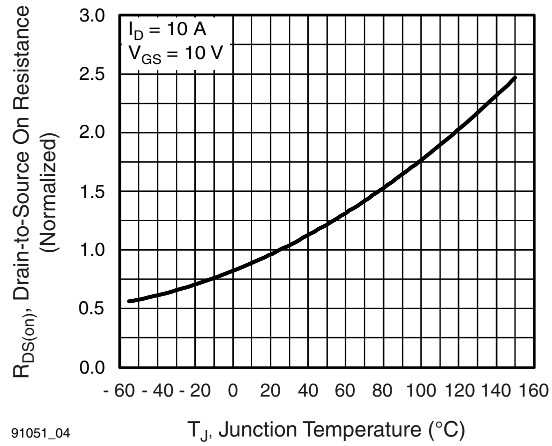


Fig. 3 - Normalized On-Resistance vs. Temperature

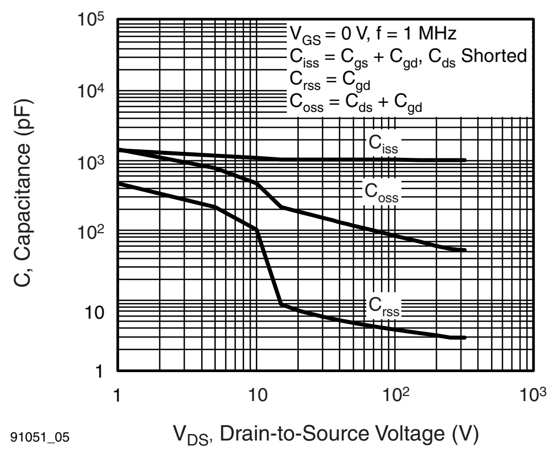


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

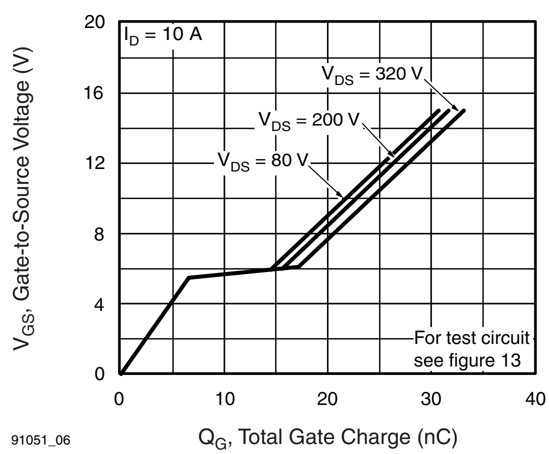


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

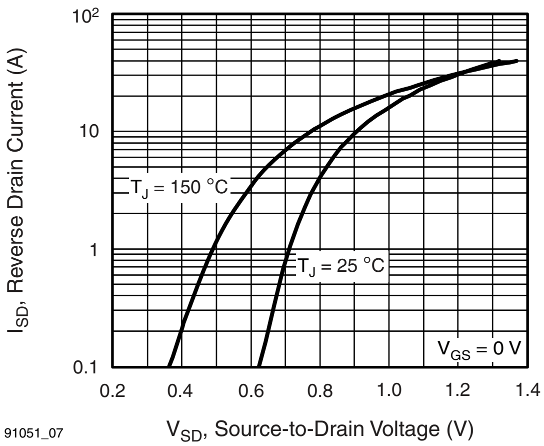


Fig. 6 - Typical Source-Drain Diode Forward Voltage

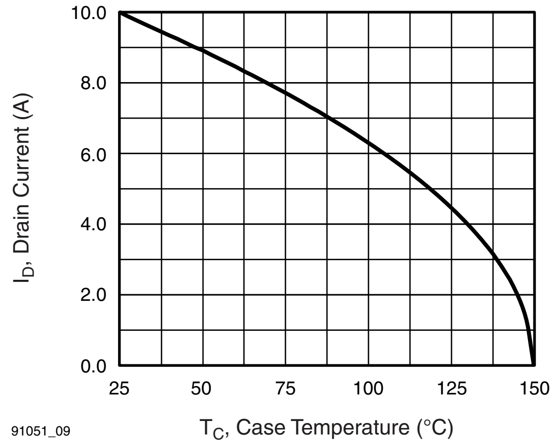


Fig. 8 - Maximum Drain Current vs. Case Temperature

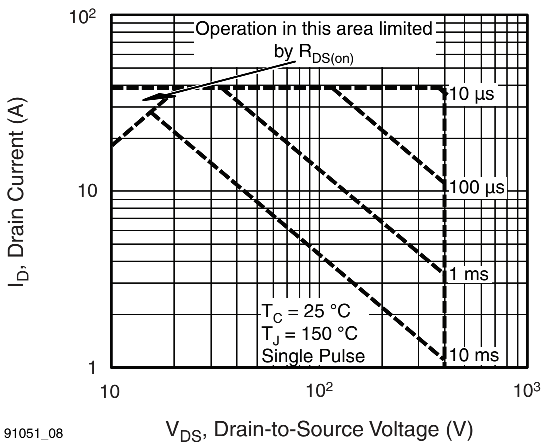


Fig. 7 - Maximum Safe Operating Area

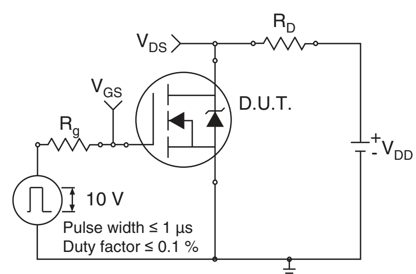


Fig. 9 - Switching Time Test Circuit

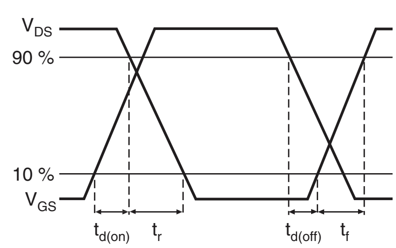


Fig. 10 - Switching Time Waveforms

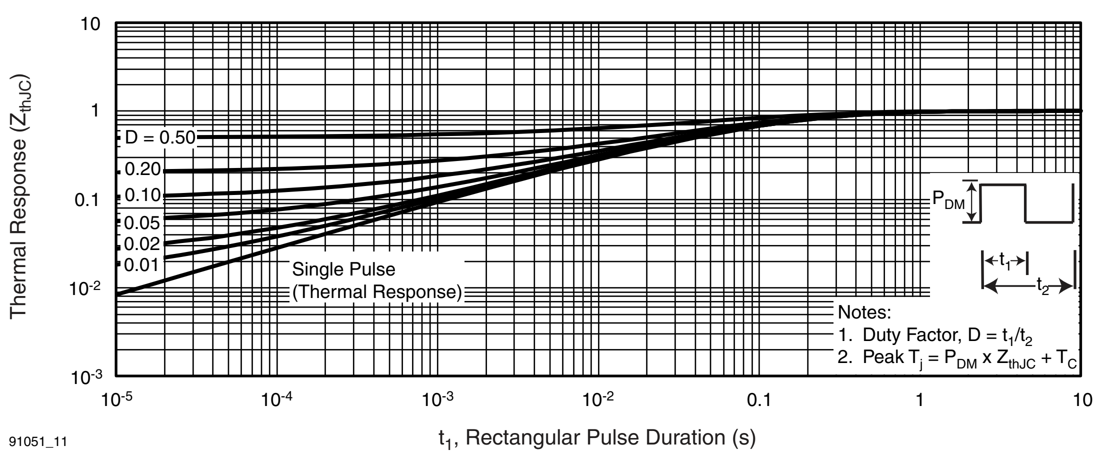


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

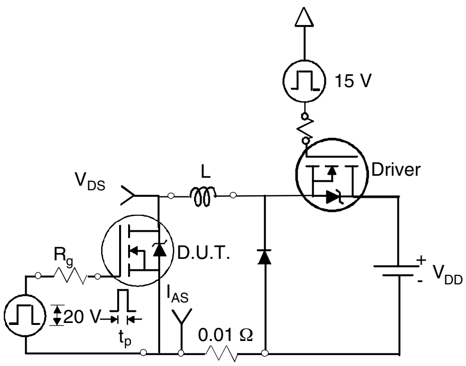


Fig. 12 - Unclamped Inductive Test Circuit

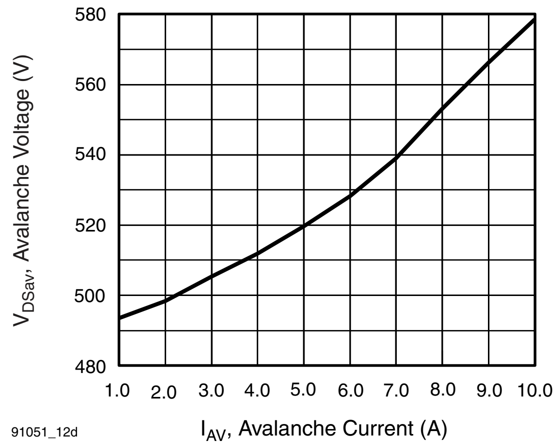


Fig. 15 - Typical Drain-to-Source Voltage vs. Avalanche Current

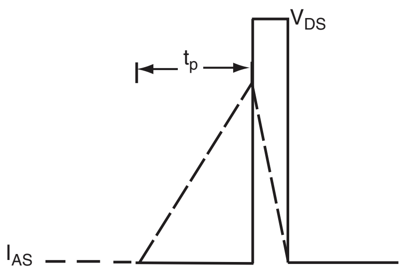


Fig. 13 - Unclamped Inductive Waveforms

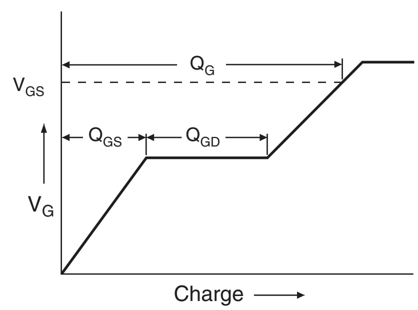


Fig. 16 - Basic Gate Charge Waveform

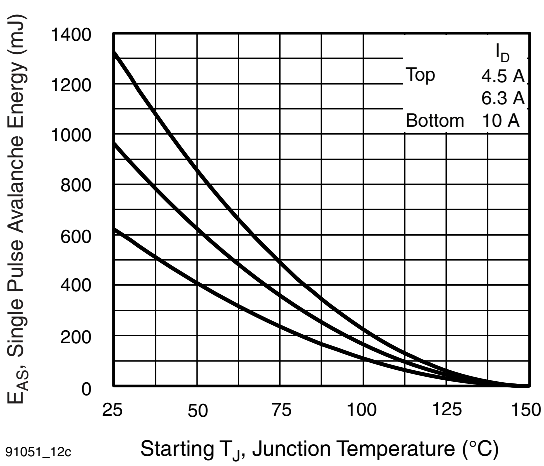


Fig. 14 - Maximum Avalanche Energy vs. Drain Current

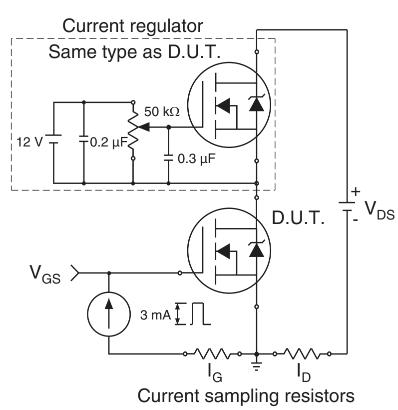
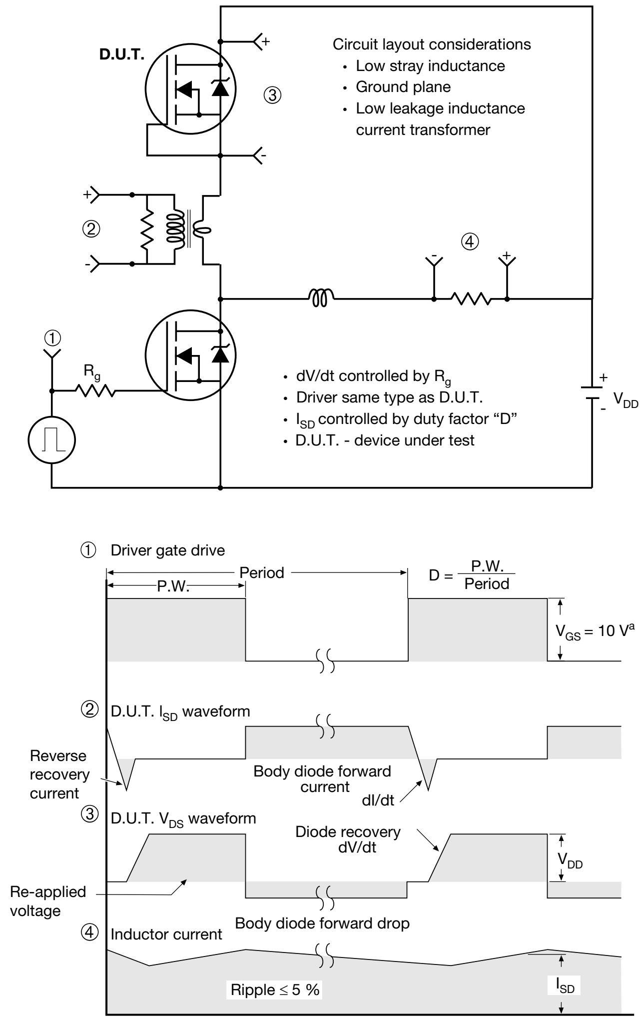


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

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