IRF9620 Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	IRF9620-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	IRF9620
Description	MOSFET P-CH 200V 3.5A TO220AB
Detailed Description	P-Channel 200 V 3.5A (Tc) 40W (Tc) Through Hole TO-220AB

Purchase and inquiry

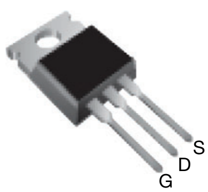
Manufacturer Product Number:	Manufacturer:
IRF9620	Vishay Siliconix
Series:	Product Status:
-	Obsolete
FET Type:	Technology:
P-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
200 V	3.5A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	1.5Ohm @ 1.5A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 250µA	22 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	350 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	40W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Through Hole
Supplier Device Package:	Package / Case:
TO-220AB	TO-220-3
Base Product Number:	
IRF9620	

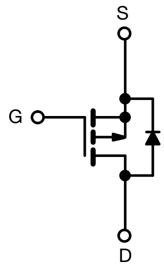
Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
RoHS non-compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

Power MOSFET

TO-220AB





P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Available
RoHS* Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY		
V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	1.5
Q_g max. (nC)	22	
Q_{gs} (nC)	12	
Q_{gd} (nC)	10	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF9620PbF
Lead (Pb)-free and halogen-free	IRF9620PbF-BE3

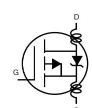
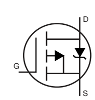
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	-200	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at -10 V	T_C = 25 °C	I_D	-3.5	A
		T_C = 100 °C		-2.0	
Pulsed srain current [a]			I_{DM}	-14	
Linear serating factor				0.32	W/°C
Maximum power dissipation	T_C = 25 °C		P_D	40	W
Peak diode recovery dV/dt [b]			dV/dt	-5.0	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]	For 10 s			300	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. $I_{SD} \leq$ -3.5 A, dI/dt ≤ 95 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C
c. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	3.1	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 μA	-200	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = -1 mA	-	-0.22	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	-	-4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -200 V, V_{GS} = 0 V	-	-	-100	μA
		V_{DS} = -160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = -10 V; I_D = -1.5 A [b]	-	-	1.5	Ω
Forward transconductance	g_{fs}	V_{DS} = -50 V, I_D = -1.5 A [b]	1.0	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 5	-	350	-	pF
Output capacitance	C_{oss}		-	100	-	
Reverse transfer capacitance	C_{rss}		-	30	-	
Total gate charge	Q_g	V_{GS} = -10 V; I_D = -4.0 A, V_{DS} = -160 V, see fig. 11 and 18 [b]	-	-	22	nC
Gate-source charge	Q_{gs}		-	-	12	
Gate-drain charge	Q_{gd}		-	-	10	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -100 V, I_D = -1.5 A, R_g = 50 Ω, R_D = 67 Ω, see fig. 17 [b]	-	15	-	ns
Rise time	t_r		-	25	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	t_f		-	15	-	
Gate input resistance	R_g	f = 1 MHz, open drain	0.9	-	5.7	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-3.5	A
Pulsed diode forward current [a]	I_{SM}		-	-	-14	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = -3.5 A, V_{GS} = 0 V [b]	-	-	-7.0	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = -3.5 A, dI/dt = 100 A/μs [b]	-	300	450	ns
Body diode reverse recovery charge	Q_{rr}		-	1.9	2.9	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

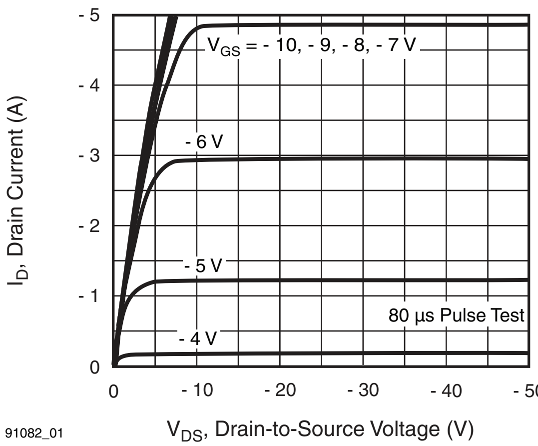


Fig. 1 - Typical Output Characteristics

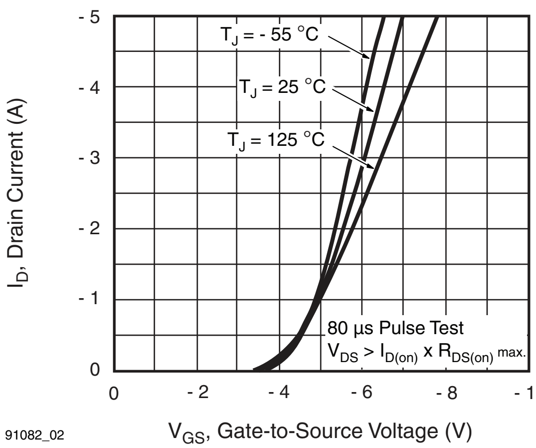


Fig. 2 - Typical Transfer Characteristics

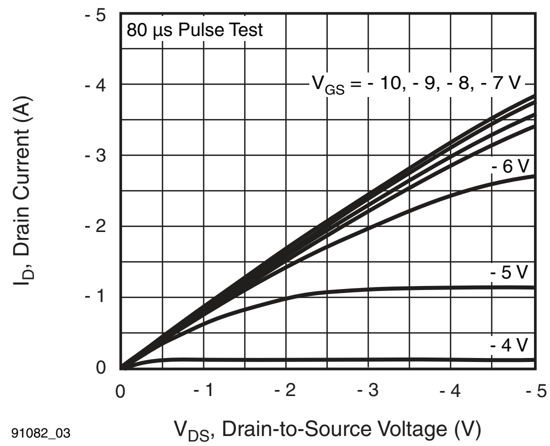


Fig. 3 - Typical Saturation Characteristics

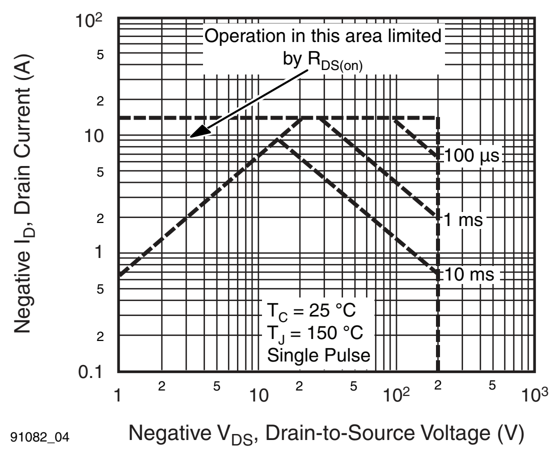


Fig. 4 - Maximum Safe Operating Area

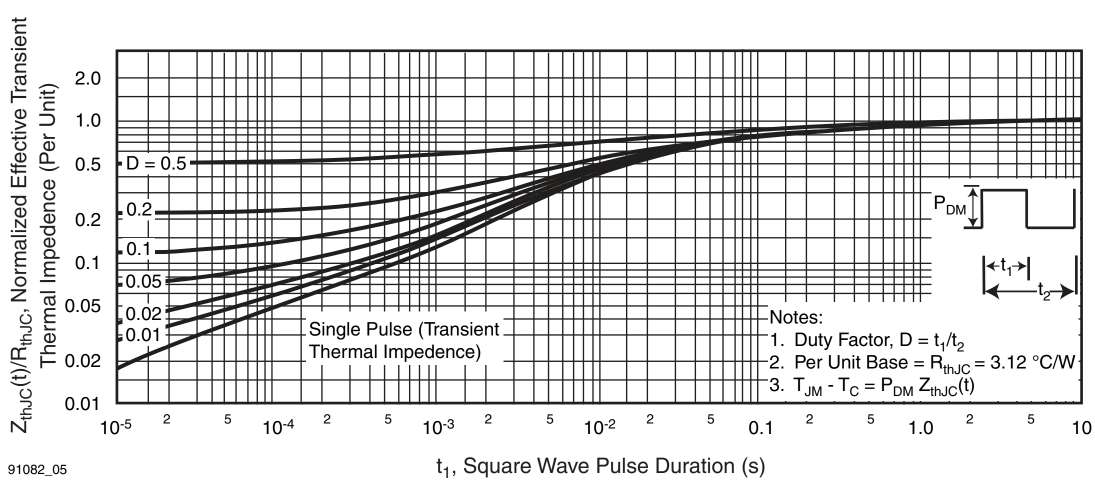


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

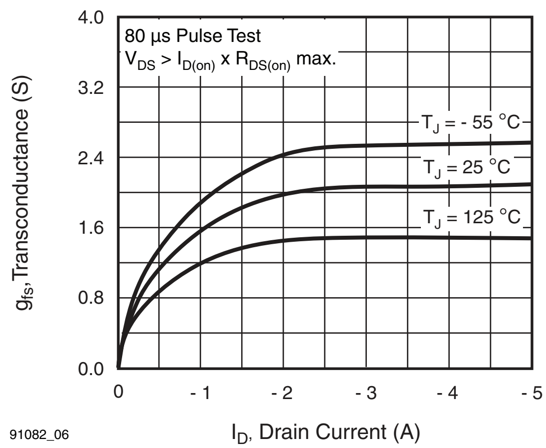


Fig. 6 - Typical Transconductance vs. Drain Current

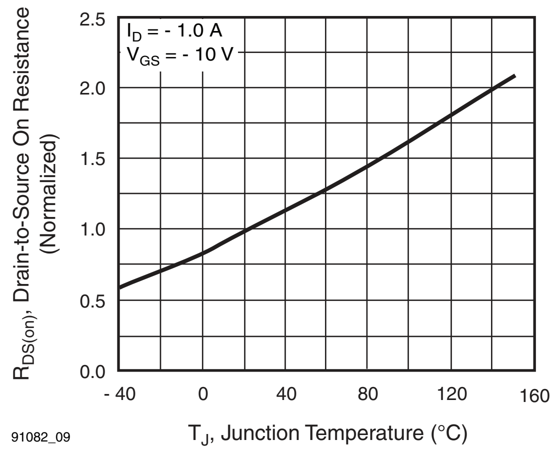


Fig. 9 - Normalized On-Resistance vs. Temperature

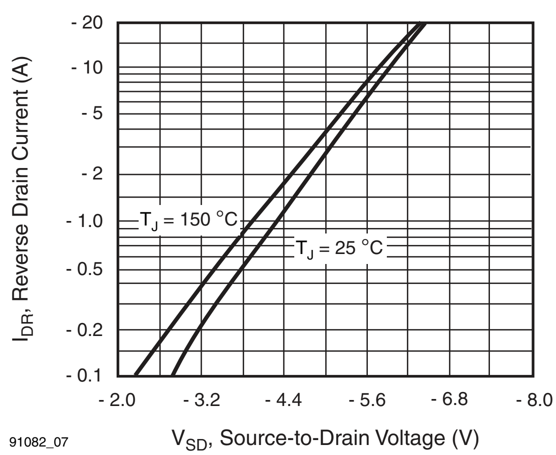


Fig. 7 - Typical Source-Drain Diode Forward Voltage

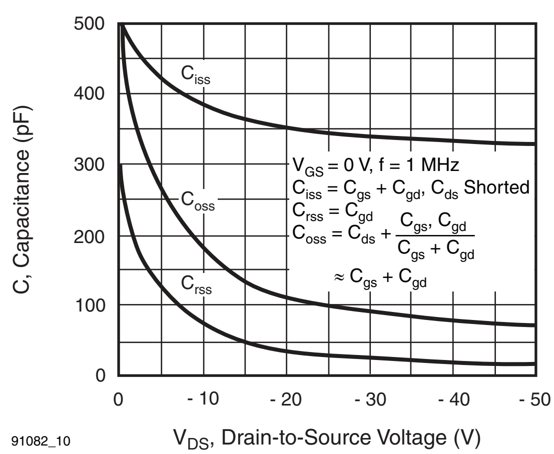


Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

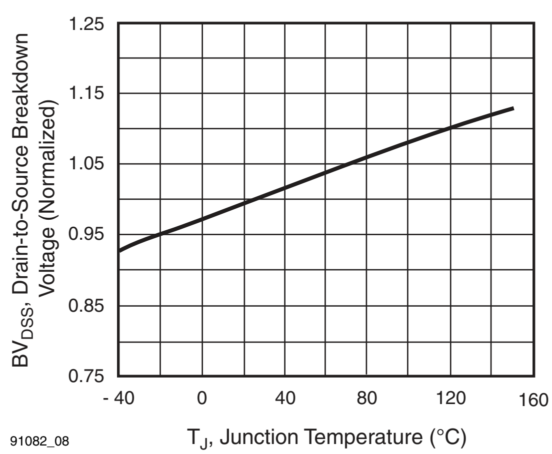


Fig. 8 - Breakdown Voltage vs. Temperature

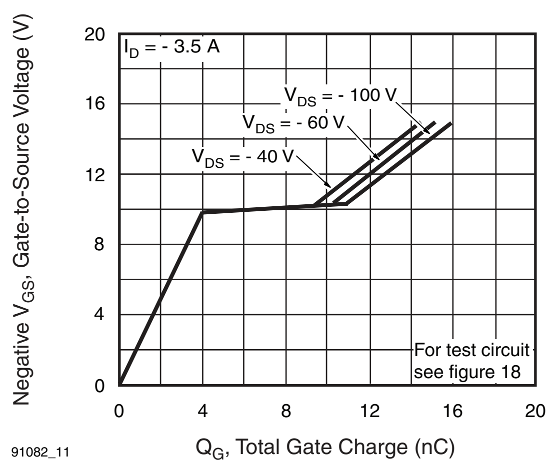


Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

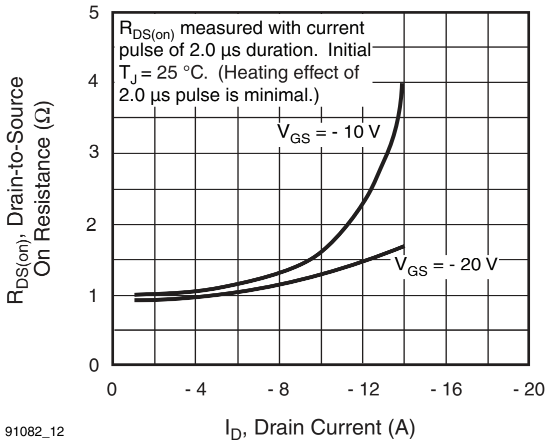


Fig. 12 - Typical On-Resistance vs. Drain Current

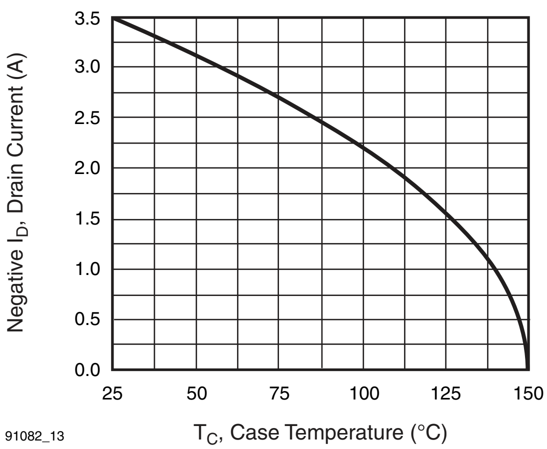


Fig. 13 - Maximum Drain Current vs. Case Temperature

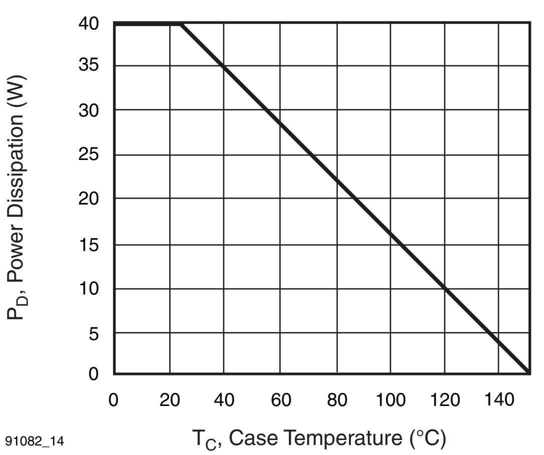


Fig. 14 - Power vs. Temperature Derating Curve

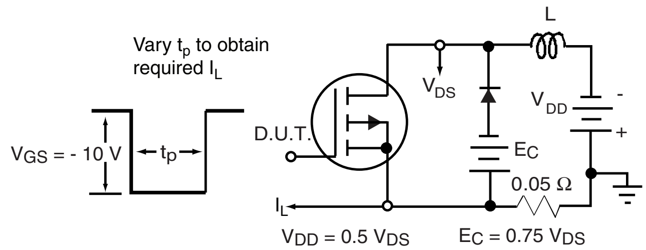


Fig. 15 - Clamped Inductive Test Circuit

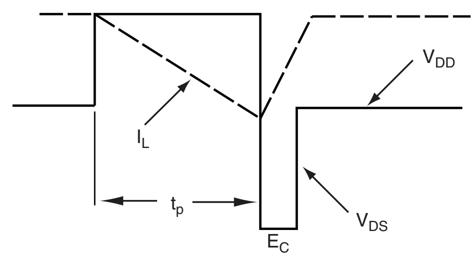


Fig. 16 - Clamped Inductive Waveforms

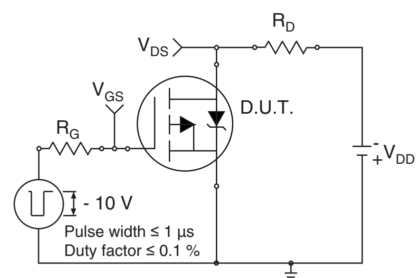


Fig. 17a - Switching Time Test Circuit

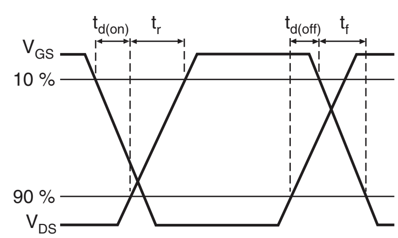


Fig. 17b - Switching Time Waveforms

For technical questions, contact: hvm@vishay.com

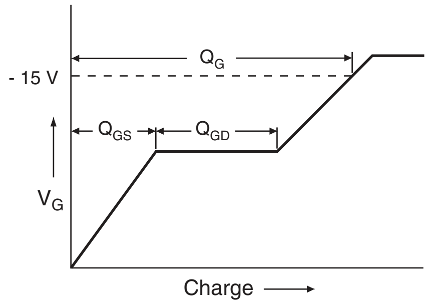


Fig. 18a - Basic Gate Charge Waveform

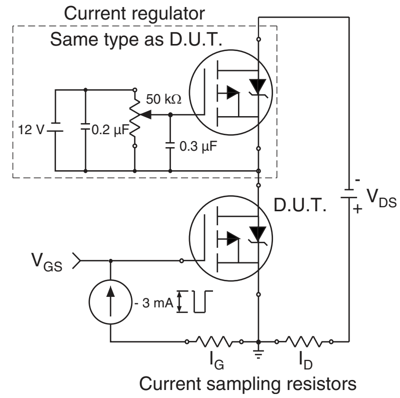
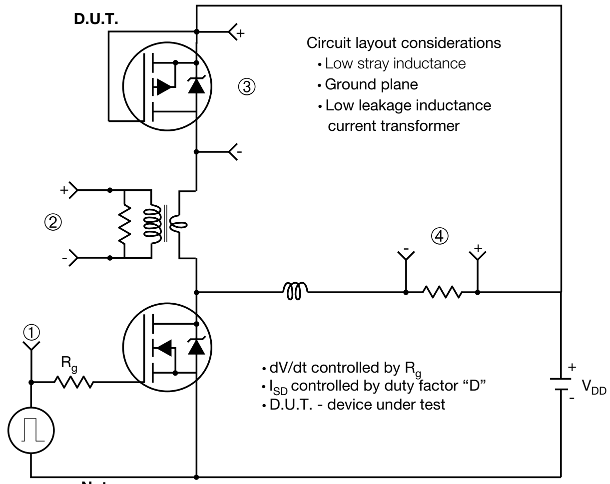
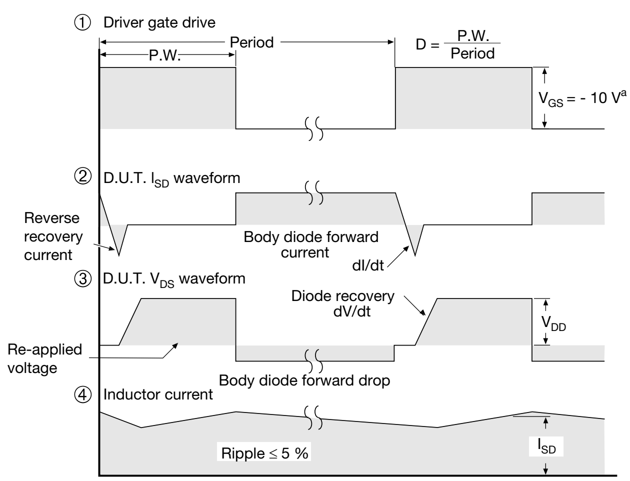


Fig. 18b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
- Compliment N-Channel of D.U.T. for driver



Note
a. V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 19 - For P-Channel

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