IRFIB8N50K Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	IRFIB8N50K-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	IRFIB8N50K
Description	MOSFET N-CH 500V 6.7A TO220-3
Detailed Description	N-Channel 500 V 6.7A (Tc) 45W (Tc) Through Hole TO-220-3

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	IRFIB8N50K	Manufacturer:	Vishay Siliconix
Series:	-	Product Status:	Obsolete
FET Type:	N-Channel	Technology:	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	500 V	Current - Continuous Drain (Id) @ 25°C:	6.7A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	10V	Rds On (Max) @ Id, Vgs:	350mOhm @ 4A, 10V
Vgs(th) (Max) @ Id:	5V @ 250µA	Gate Charge (Qg) (Max) @ Vgs:	89 nC @ 10 V
Vgs (Max):	±30V	Input Capacitance (Ciss) (Max) @ Vds:	2160 pF @ 25 V
FET Feature:	-	Power Dissipation (Max):	45W (Tc)
Operating Temperature:	-55°C ~ 150°C (TJ)	Mounting Type:	Through Hole
Supplier Device Package:	TO-220-3	Package / Case:	TO-220-3 Full Pack, Isolated Tab
Base Product Number:	IRFIB8		

Environmental & Export classification

RoHS Status:	RoHS non-compliant	Moisture Sensitivity Level (MSL):	1 (Unlimited)
REACH Status:	REACH Unaffected	ECCN:	EAR99
HTSUS:	8541.29.0095		

PD - 94444

International
IOR Rectifier

SMPS MOSFET

IRFIB8N50K

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	**290mΩ**	**6.7A**

Applications

- Switch Mode Power Supply (SMPS)
- UninterruptIble Power Supply
- High Speed Power Switching

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current

TO-220
FULL-PAK

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	6.7	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	4.2	
I_{DM}	Pulsed Drain Current ①	27	
P_D @T_C = 25°C	Power Dissipation	45	W
	Linear Derating Factor	0.36	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
dv/dt	Peak Diode Recovery dv/dt ③	17	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	1.1(10)	N•m (lbf•in)

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	290	mJ
I_{AR}	Avalanche Current ①	—	6.7	A
E_{AR}	Repetitive Avalanche Energy ①	—	4.5	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.76	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

4/21/04

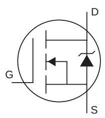
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.59	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	290	350	mΩ	V_{GS} = 10V, I_D = 4.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	µA	V_{DS} = 500V, V_{GS} = 0V
		—	—	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	4.7	—	—	V	V_{DS} = 50V, I_D = 4.0A
Q_g	Total Gate Charge	—	—	89	nC	I_D = 6.7A
Q_{gs}	Gate-to-Source Charge	—	—	24		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	44		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 250V
t_r	Rise Time	—	16	—		I_D = 6.7A
$t_{d(off)}$	Turn-Off Delay Time	—	28	—		R_G = 38Ω
t_f	Fall Time	—	8.4	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	2160	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	240	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz
C_{oss}	Output Capacitance	—	2600	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	62	—		V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	120	—		V_{GS} = 0V, V_{DS} = 0V to 400V ③

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	27		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J = 25°C, I_S = 6.7A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	430	640	ns	T_J = 25°C, I_F = 6.7A
Q_{rr}	Reverse RecoveryCharge	—	2840	4270	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11).

② Starting T_J = 25°C, L = 13mH, R_G = 25Ω, I_{AS} = 6.7A, dv/dt = 17V/ns (See Figure 12a).

③ $I_{SD} \leq 6.7$A, di/dt ≤ 330A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150$°C.

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

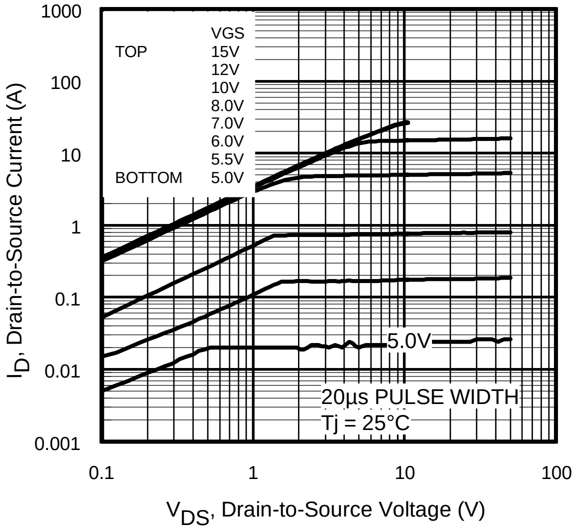


Fig 1. Typical Output Characteristics

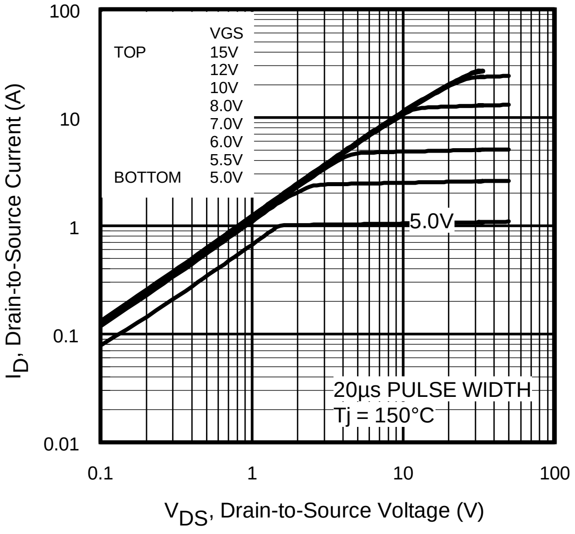


Fig 2. Typical Output Characteristics

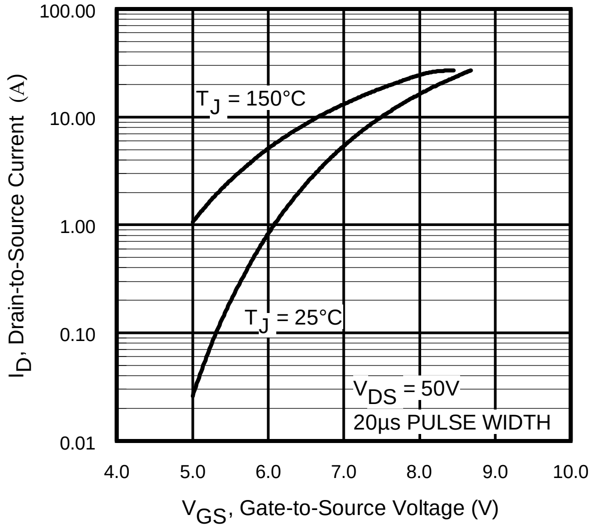


Fig 3. Typical Transfer Characteristics

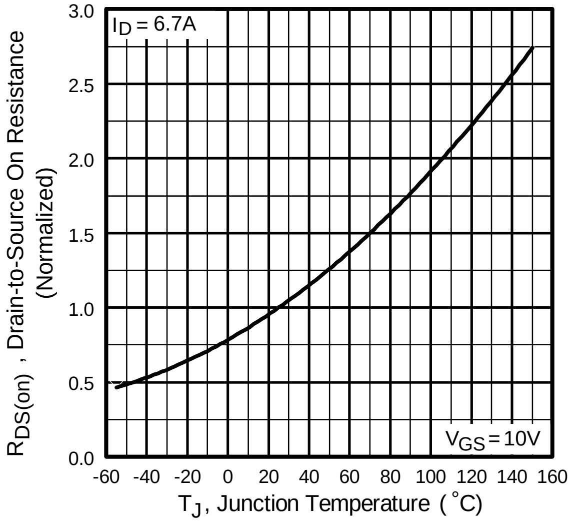


Fig 4. Normalized On-Resistance
Vs. Temperature

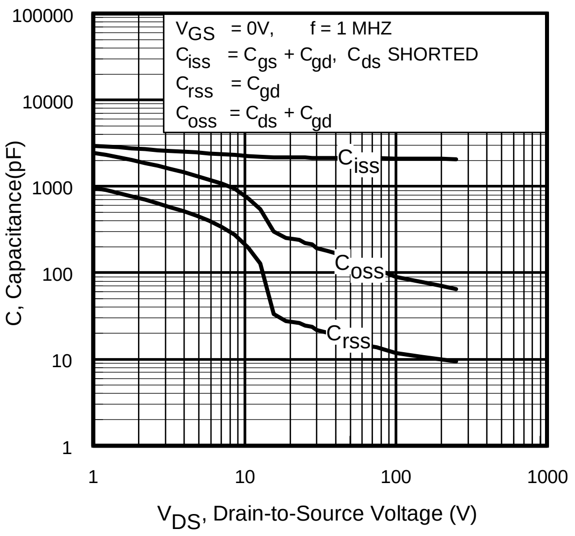


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

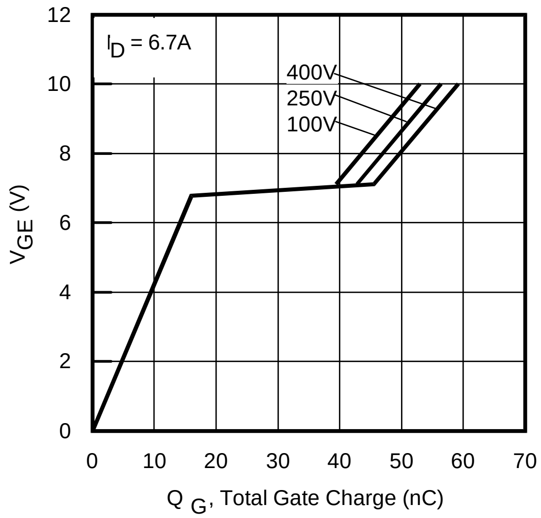


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

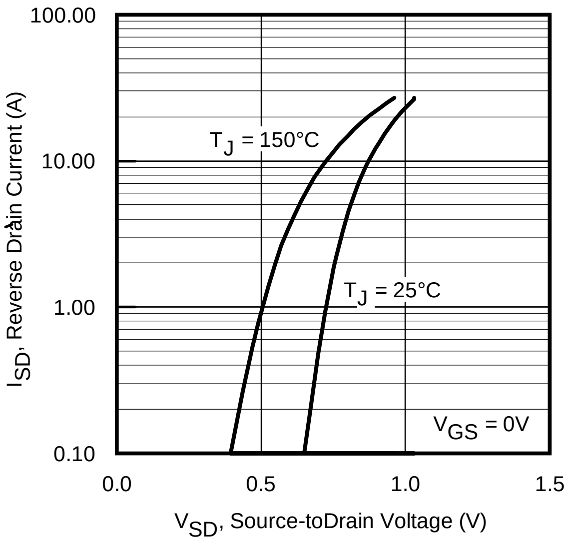


Fig 7. Typical Source-Drain Diode Forward Voltage

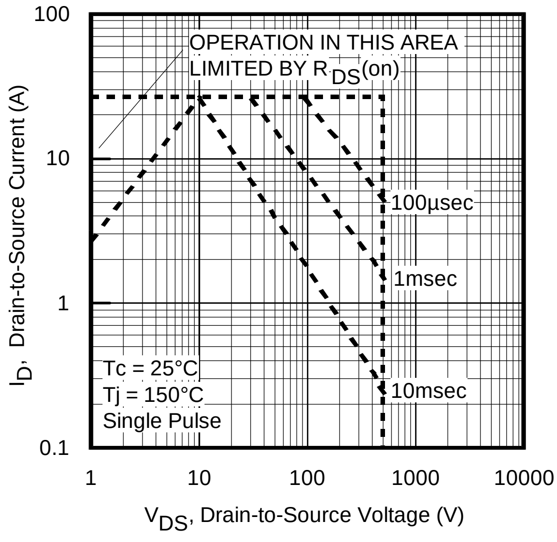


Fig 8. Maximum Safe Operating Area

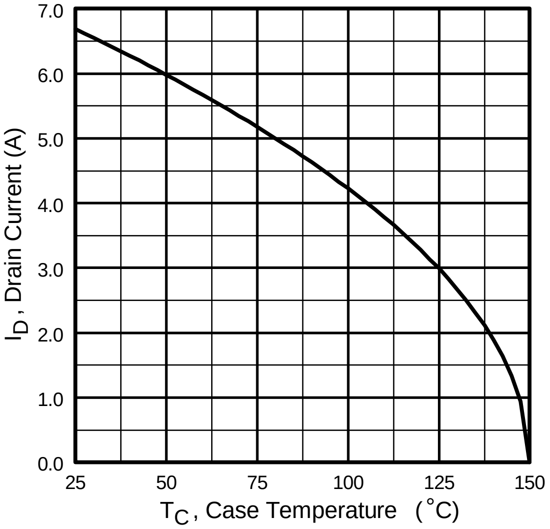


Fig 9. Maximum Drain Current Vs. Case Temperature

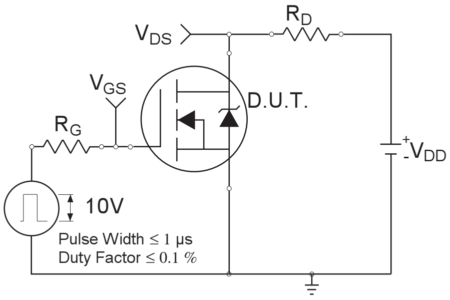


Fig 10a. Switching Time Test Circuit

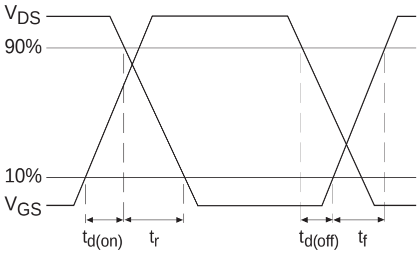


Fig 10b. Switching Time Waveforms

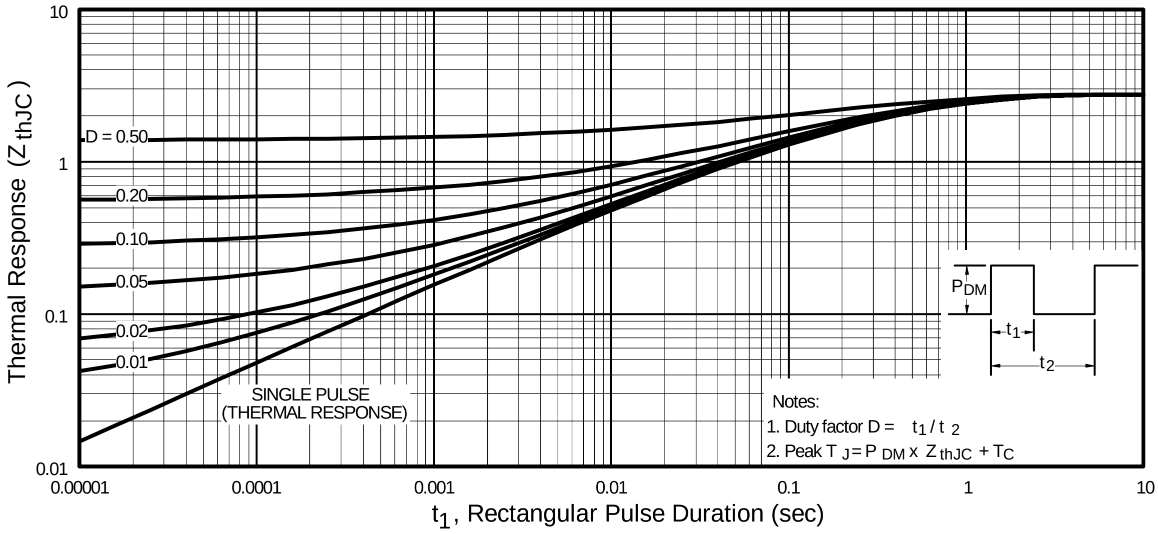


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

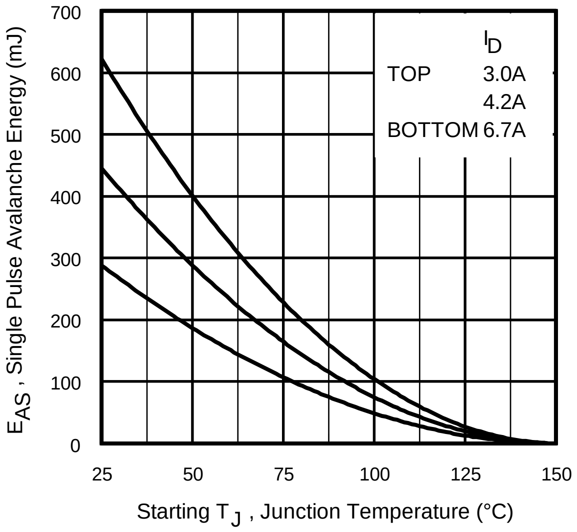


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

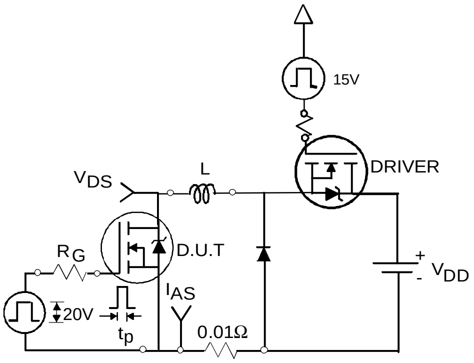


Fig 12c. Unclamped Inductive Test Circuit

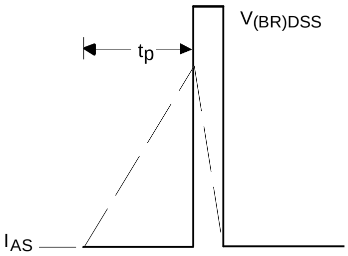


Fig 12d. Unclamped Inductive Waveforms

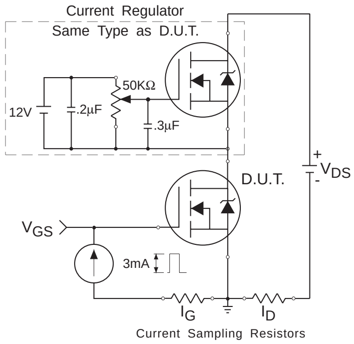


Fig 13a. Gate Charge Test Circuit

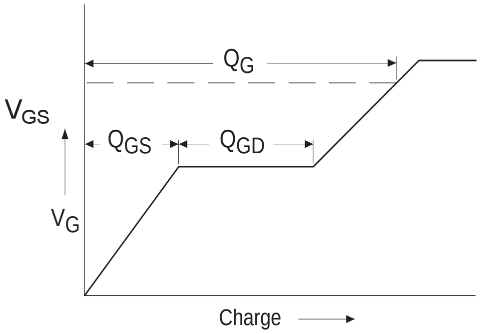
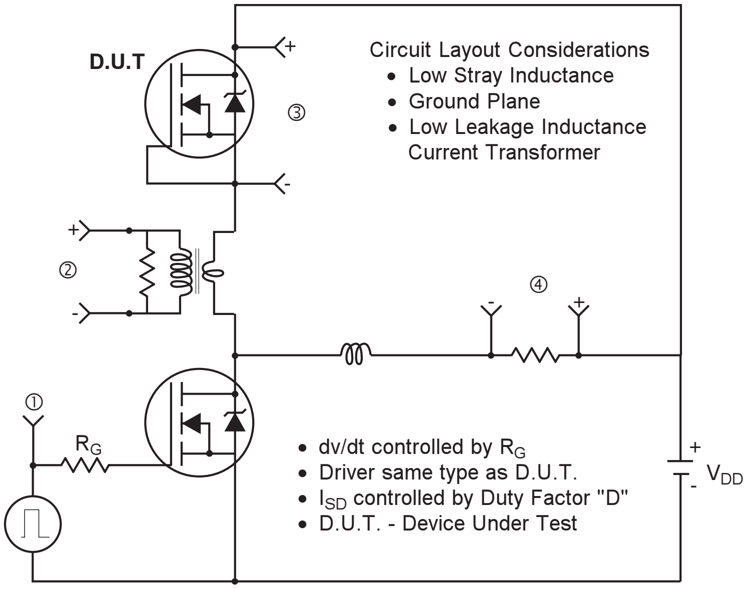


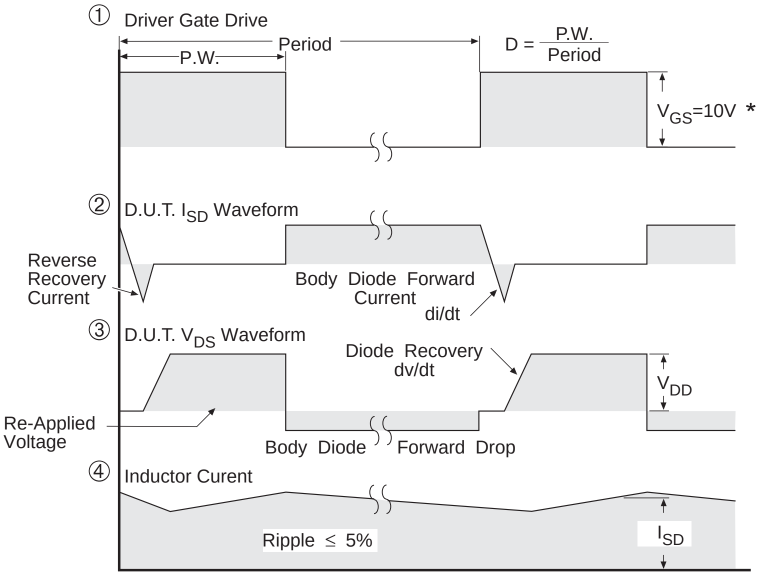
Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

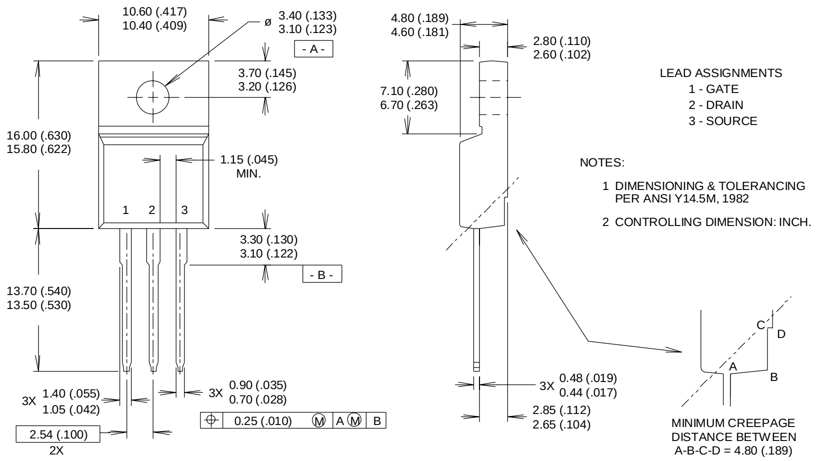


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

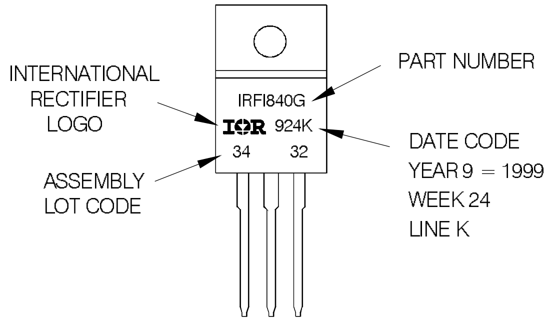
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982

2 CONTROLLING DIMENSION: INCH.

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"



TO-22O Full-Pak package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR’s Web site.

International
Rectifier

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