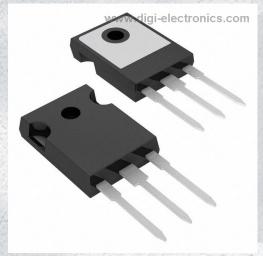


IRFP460LC Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number

IRFP460LC-DG

Manufacturer

Vishay Siliconix

Manufacturer Product Number

IRFP460LC

Description

MOSFET N-CH 500V 20A TO247-3

Detailed Description

N-Channel 500 V 20A (Tc) 280W (Tc) Through Hole

TO-247AC



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
IRFP460LC	Vishay Siliconix
Series:	Packaging:
	Tube
Part Status:	FET Type:
Active	N-Channel
Technology:	Drain to Source Voltage (Vdss):
MOSFET (Metal Oxide)	500 V
Current - Continuous Drain (Id) @ 25°C:	Drive Voltage (Max Rds On, Min Rds On):
20A (Tc)	10V
Rds On (Max) @ Id, Vgs:	Vgs(th) (Max) @ Id:
270mOhm @ 12A, 10V	4V @ 250μA
Gate Charge (Qg) (Max) @ Vgs:	Vgs (Max):
120 nC @ 10 V	±30V
Input Capacitance (Ciss) (Max) @ Vds:	FET Feature:
3600 pF @ 25 V	
Power Dissipation (Max):	Operating Temperature:
280W (Tc)	-55°C ~ 150°C (TJ)
Mounting Type:	Supplier Device Package:
Through Hole	TO-247AC
Package / Case:	Base Product Number:
TO-247-3	IRFP460

Environmental & Export classification

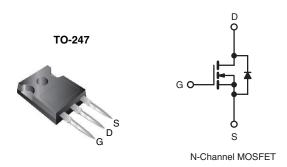
RoHS Status:	Moisture Sensitivity Level (MSL):	
RoHS non-compliant	1 (Unlimited)	
ECCN:	HTSUS:	
EAR99	8541.29.0095	



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Power MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	50	500			
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	V _{GS} = 10 V 0.27			
Q _g (max.) (nC)	12	120			
Q _{gs} (nC)	32	32			
Q _{gd} (nC)	49	49			
Configuration	Sino	Single			

FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V V_{GS} rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Isolated central mounting hole
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Power MOSFETs technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole.

ORDERING INFORMATION		
Package	TO-247	
Lead (Pb)-free	IRFP460LCPbF	

ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	500	V
Gate-source voltage			V_{GS}	± 30	V
Continuous drain current	Vec at 10 V	$T_C = 25 \degree C$ $T_C = 100 \degree C$	I _D	20	
Continuous drain current	VGS at 10 V	T _C = 100 °C	טו	12	Α
Pulsed drain current a			I_{DM}	80	
Linear derating Factor				2.2	W/°C
Single pulse avalanche energy b			E _{AS}	960	mJ
Repetitive avalanche currenta			I _{AR}	20	Α
Repetitive avalanche energy ^a			E _{AR}	28	mJ
Maximum power dissipation	T _C = 25 °C		P_{D}	280	W
Peak diode recovery dV/dtc			dV/dt	3.5	V/ns
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) for 10 s				300 ^d	
Mounting torque 6-32 or M3 screw			10	lbf ⋅ in	
Mounting torque	0-32 Of IVIS SCREW			1.1	N⋅m

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 4.3 mH, R_G = 25 Ω , I_{AS} = 20 A (see fig. 12)
- c. $I_{SD} \le 20$ A, $dI/dt \le 160$ A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case



IRFP460LC

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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	=	-	
Case-to-sink, flat, greased surface	R _{thCS}	0.24	-	°C/W
Maximum junction-to-case (Drain)	R _{thJC}	-	0.45	

PARAMETER	SYMBOL	TEST (CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 2$	50 μΑ	500	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25	°C, I _D = 1 mA	-	0.59	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 2$	250 μΑ	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 500 \text{ V}, V_{GS}$ $V_{DS} = 400 \text{ V}, V_{GS}$	_S = 0 V _S = 0 V, T _J = 125 °C	-	-	25 250	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12 A b	-	-	0.27	Ω
Forward transconductance	9fs	$V_{DS} = 50 \text{ V}, I_{D} =$	12 A ^b	12	-	-	S
Dynamic					L		
Input capacitance	C _{iss}	V _{GS} = 0 V,		-	3600	-	
Output capacitance	C _{oss}	$V_{DS} = 25 \text{ V},$		-	440	-	pF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, see	fig. 5	-	39	-	
Total gate charge	Qg			-	-	120	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 20 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 b		-	32	nC
Gate-drain charge	Q _{gd}	see lig. 0 and 13		-	-	49	
Turn-on delay time	t _{d(on)}			-	18	-	
Rise time	t _r	V _{DD} = 250 V, I _D =	V_{DD} = 250 V, I_D = 20 A R_G = 4.3 Ω, R_D = 12 Ω, see fig. 10 b		77	-]
Turn-off delay time	t _{d(off)}	$R_G = 4.3 \Omega, R_D =$			40	-	ns
Fall time	t _f	1			43	-	1
Internal drain inductance	L _D	Between lead,	ئے ۔	-	5.0	-	
Internal source inductance	L _S	6 mm (0.25") from package and center of die contact		-	13	-	nH
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	,	MOSFET symbol		=	20	
Pulsed diode forward current ^a	I _{SM}	showing the integral reverse p - n junction diode		-	-	80	А
Body diode voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 25 ^{\circ}\text{C}$	20 A, V _{GS} = 0 V ^b	-	-	1.8	V
Body diode reverse recovery time	t _{rr}	T = 0F °C 0	20 A dl/dt = 100 A/v.c h	-	570	860	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}$, $I_F = 20 \text{A}$, $dI/dt = 100 \text{A/µs}^{ \text{b}}$		-	6.6	9.9	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300 \ \mu s$; duty cycle $\leq 2 \ \%$

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

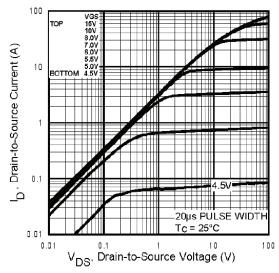


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

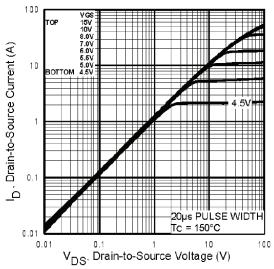


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

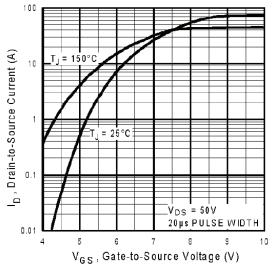


Fig. 3 - Typical Transfer Characteristics

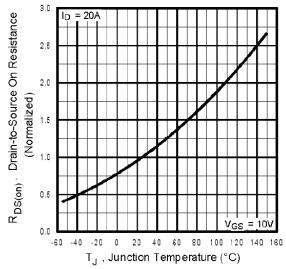


Fig. 4 - Normalized On-Resistance vs. Temperature

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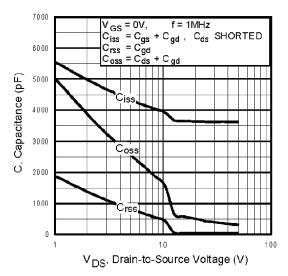


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

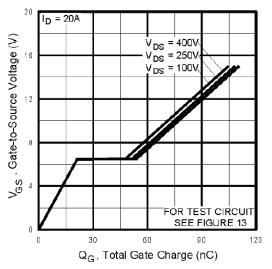


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

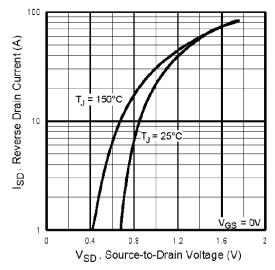


Fig. 7 - Typical Source-Drain Diode Forward Voltage

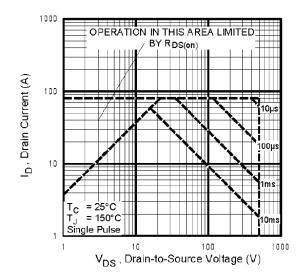


Fig. 8 - Maximum Safe Operating Area



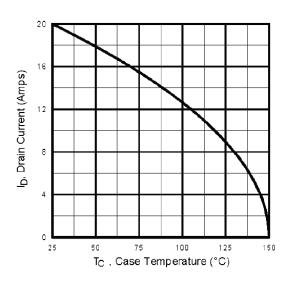


Fig. 9 - Maximum Drain Current vs. Case Temperature

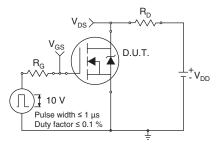


Fig. 10 - Switching Time Test Circuit

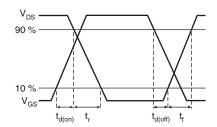


Fig. 11 - Switching Time Waveforms

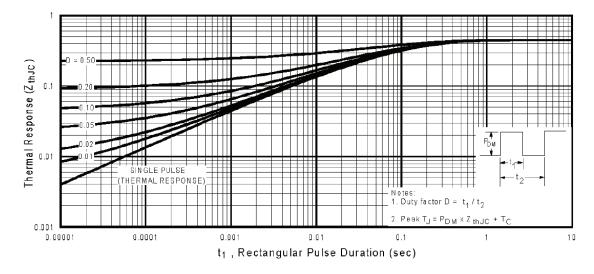


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

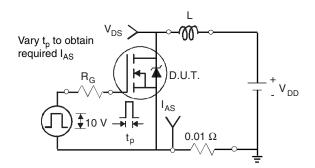


Fig. 13 - Unclamped Inductive Test Circuit

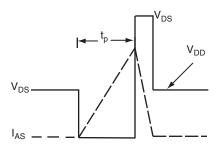


Fig. 14 - Unclamped Inductive Waveforms

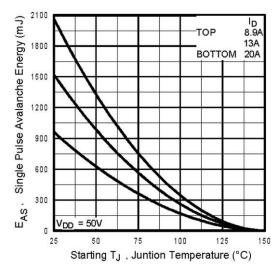


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

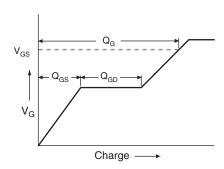


Fig. 16 - Basic Gate Charge Waveform

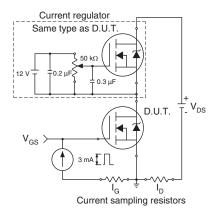
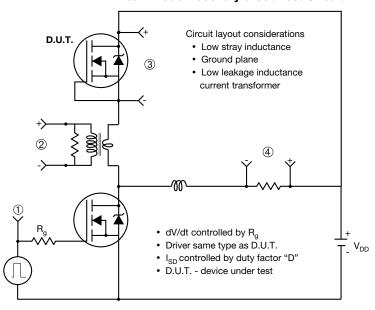


Fig. 17 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



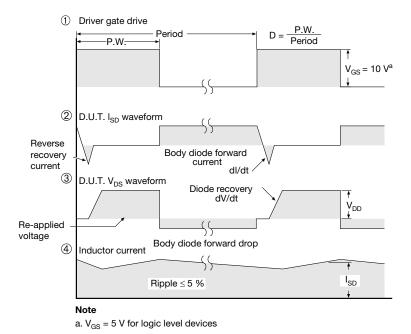


Fig. 18 - For N-Channel

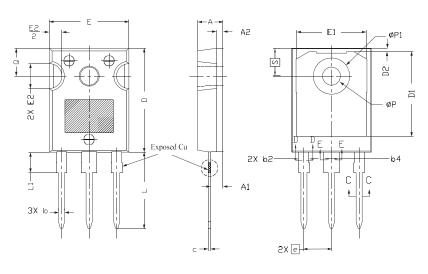
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Package Information

Vishay Siliconix

TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D-D,E-E

DIM.	MIN.	NOM.	MAX.	NOTES
Α	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
С	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
Е	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
е	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
ØΡ	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

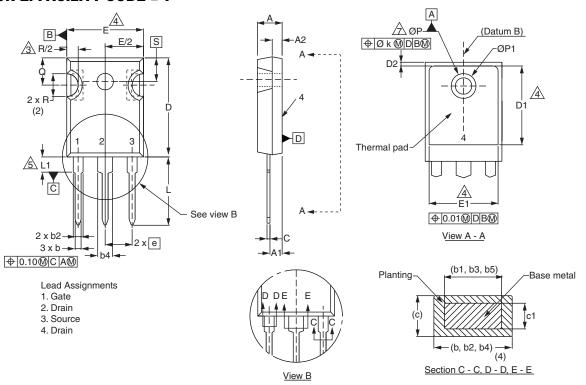
- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



Package Information

Vishay Siliconix

VERSION 2: FACILITY CODE = Y



	MILLIM		
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIM	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES	
D2	0.51	1.30		
Е	15.29	15.87		
E1	13.72	-		
е	5.46	BSC		
Øk	0.2	254		
L	14.20	16.25		
L1	3.71	4.29		
ØР	3.51	3.66		
Ø P1	-	7.39		
Q	5.31	5.69		
R	4.52	5.49		
S	5.51 BSC			

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

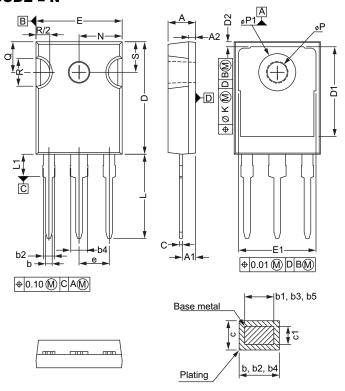


Package Information

Vishay Siliconix

VERSION 3: FACILITY CODE = N

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	MILLIMETERS	
DIM.	MIN.	MAX.
Α	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
С	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

	MILLIMETERS	
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	ı
е	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
Р	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022

DWG: 5971

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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