IRLD014PBF Datasheet

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DiGi Electronics Part Number	IRLD014PBF-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	IRLD014PBF
Description	MOSFET N-CH 60V 1.7A 4DIP
Detailed Description	N-Channel 60 V 1.7A (Ta) 1.3W (Ta) Through Hole 4 -HVMDIP

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

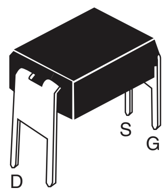
Manufacturer Product Number:	Manufacturer:
IRLD014PBF	Vishay Siliconix
Series:	Packaging:
-	Tube
Part Status:	FET Type:
Last Time Buy	N-Channel
Technology:	Drain to Source Voltage (Vdss):
MOSFET (Metal Oxide)	60 V
Current - Continuous Drain (Id) @ 25°C:	Drive Voltage (Max Rds On, Min Rds On):
1.7A (Ta)	4V, 5V
Rds On (Max) @ Id, Vgs:	Vgs(th) (Max) @ Id:
200mOhm @ 1A, 5V	2V @ 250µA
Gate Charge (Qg) (Max) @ Vgs:	Vgs (Max):
8.4 nC @ 5 V	±10V
Input Capacitance (Ciss) (Max) @ Vds:	FET Feature:
400 pF @ 25 V	-
Power Dissipation (Max):	Operating Temperature:
1.3W (Ta)	-55°C ~ 175°C (TJ)
Mounting Type:	Supplier Device Package:
Through Hole	4-HVMDIP
Package / Case:	Base Product Number:
4-DIP (0.300", 7.62mm)	IRLD014

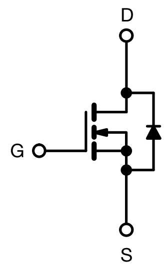
Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
ECCN:	HTSUS:
EAR99	8541.29.0095

Power MOSFET

HVMDIP





N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- For automatic insertion
- End stackable
- Logic-level gate drive
- $R_{DS(on)}$ specified at V_{GS} = 4 V and 5 V
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	V_{GS} = 5 V	0.20
Q_g (Max.) (nC)	8.4	
Q_{gs} (nC)	2.6	
Q_{gd} (nC)	6.4	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertiable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain servers as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRLD014PbF

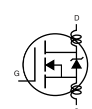
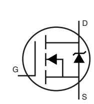
ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	60	V
Gate-source voltage			V_{GS}	± 10	
Continuous drain current	V_{GS} at 5.0 V	T_A = 25 °C	I_D	1.7	A
		T_A = 100 °C		1.2	
Pulsed drain current [a]			I_{DM}	14	
Linear derating factor				0.0083	W/°C
Single pulse avalanche energy [b]			E_{AS}	490	mJ
Maximum power dissipation	T_A = 25 °C		P_D	1.3	W
Peak diode recovery dV/dt [c]			dV/dt	4.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	- 55 to + 175	°C
Soldering recommendations (peak temperature)	For 10 s			300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 197 mH, R_g = 25 Ω, I_{AS} = 1.7 A (see fig. 12)
c. $I_{SD} \leq$ 10 A, dI/dt $\leq$ 90 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 175 °C
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.070	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 5.0 V, I_D = 1.0 A[b]	-	-	0.20	Ω
		V_{GS} = 4.0 V, I_D = 0.85 A[b]	-	-	0.28	
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 1.0 A[b]	1.9	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1.0 MHz, see fig. 5	-	400	-	pF
Output Capacitance	C_{oss}		-	170	-	
Reverse Transfer Capacitance	C_{rss}		-	42	-	
Total Gate Charge	Q_g	V_{GS} = 5.0 V; I_D = 10 A, V_{DS} = 48 V see fig. 6 and 13[b]	-	-	8.4	nC
Gate-Source Charge	Q_{gs}		-	-	2.6	
Gate-Drain Charge	Q_{gd}		-	-	6.4	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 10 A R_g = 12 Ω, R_D = 2.8 Ω, see fig. 10[b]	-	9.3	-	ns
Rise Time	t_r		-	110	-	
Turn-Off Delay Time	$t_{d(off)}$		-	17	-	
Fall Time	t_f		-	26	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.0	-	nH
Internal Source Inductance	L_S		-	6.0	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	1.7	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	14	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 1.7 A, V_{GS} = 0 V[b]	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 10 A, dI/dt = 100 A/μs[b]	-	93	130	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.34	0.65	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

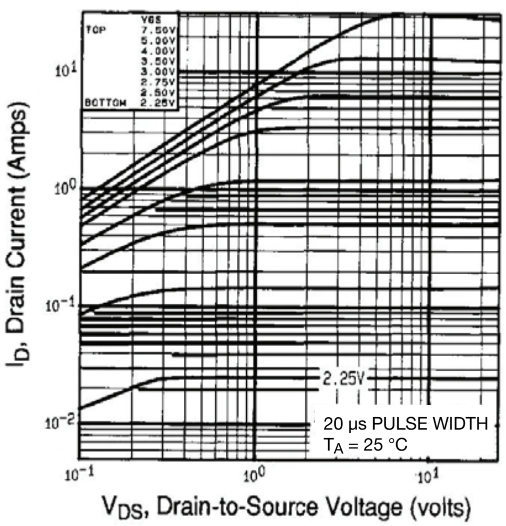


Fig. 1 - Typical Output Characteristics, T_A = 25 °C

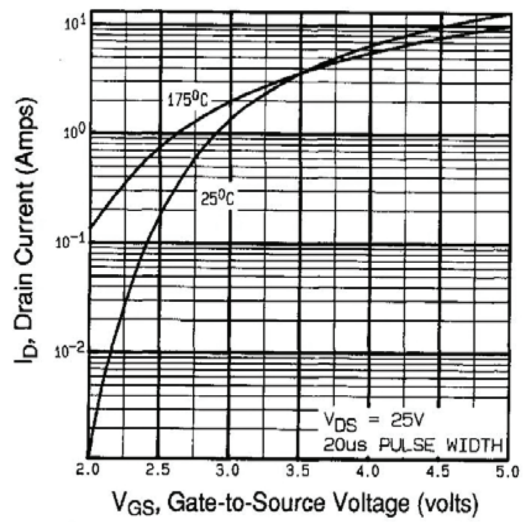


Fig. 3 - Typical Transfer Characteristics

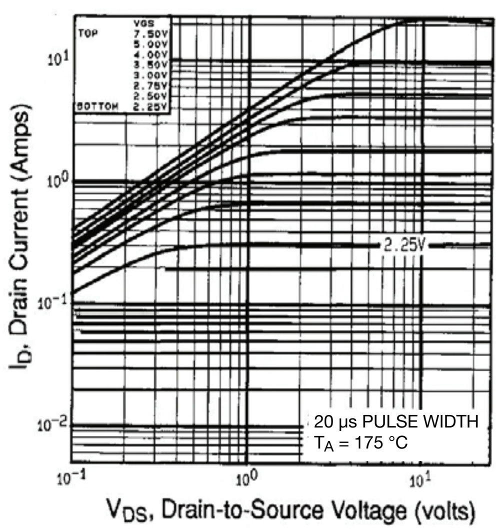


Fig. 2 - Typical Output Characteristics, T_A = 175 °C

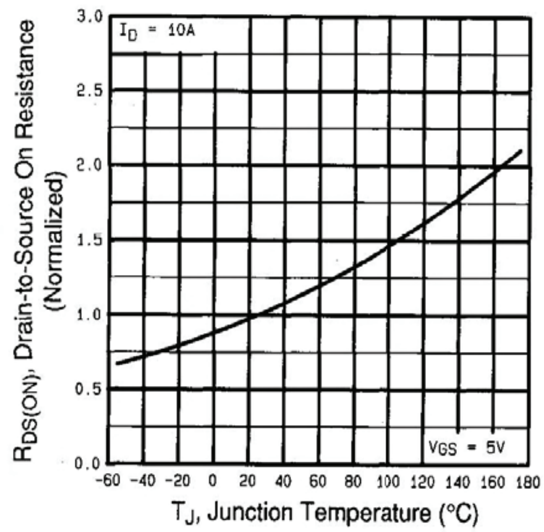


Fig. 4 - Normalized On-Resistance vs. Temperature

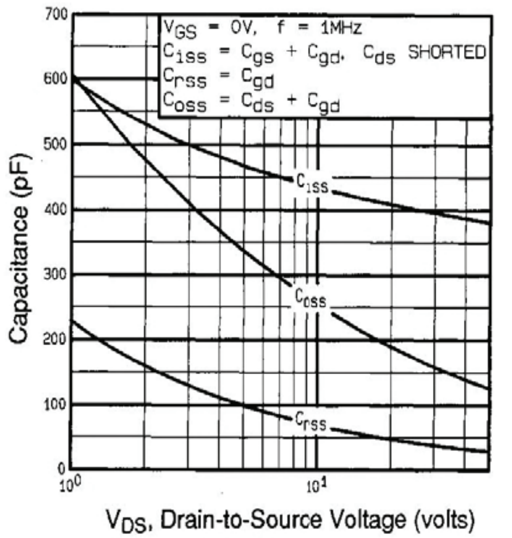


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

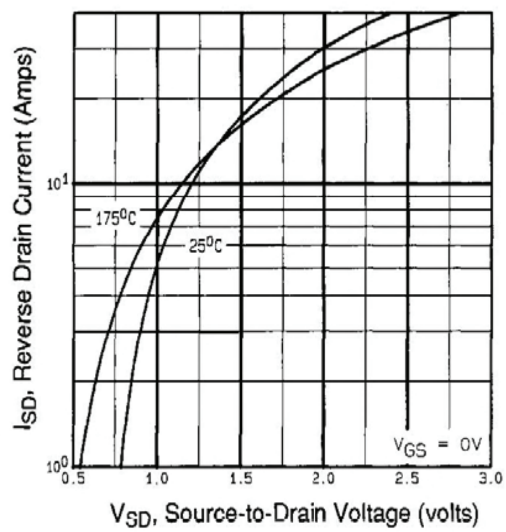


Fig. 7 - Typical Source-Drain Diode Forward Voltage

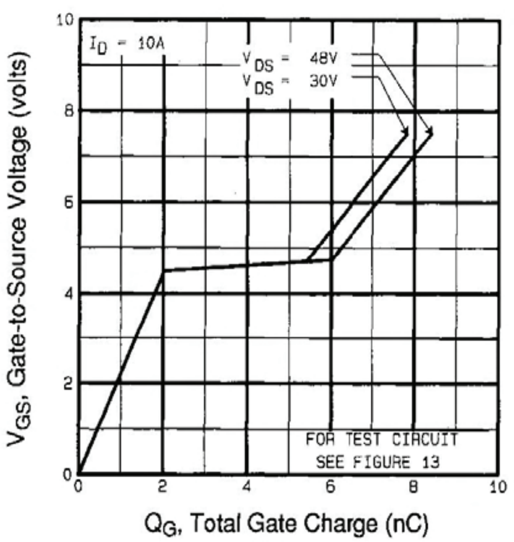


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

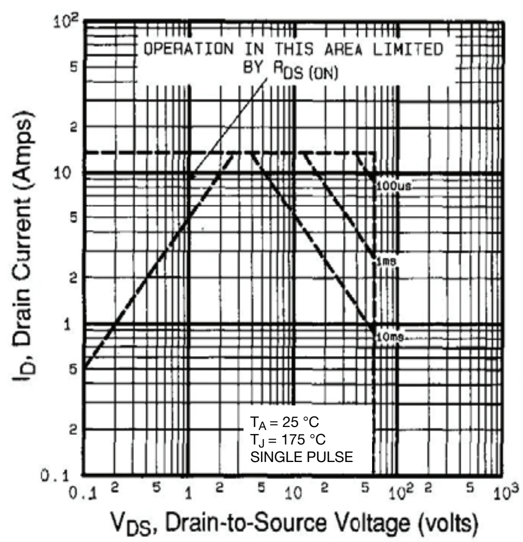


Fig. 8 - Maximum Safe Operating Area

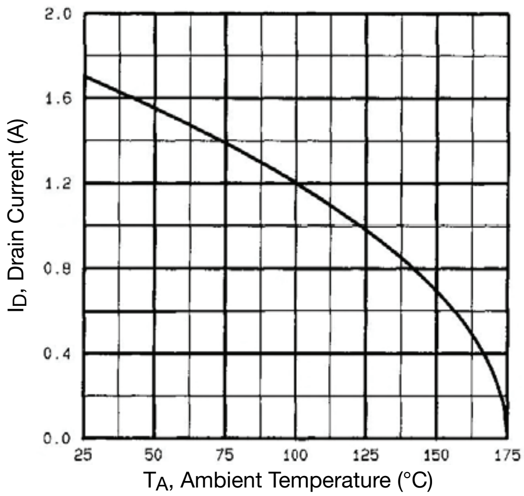


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

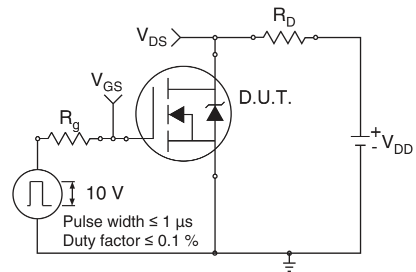


Fig. 10a - Switching Time Test Circuit

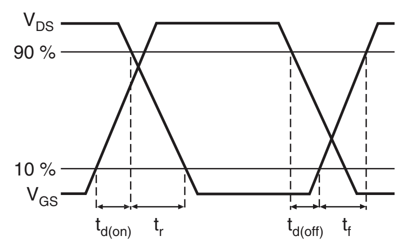


Fig. 10b - Switching Time Waveforms

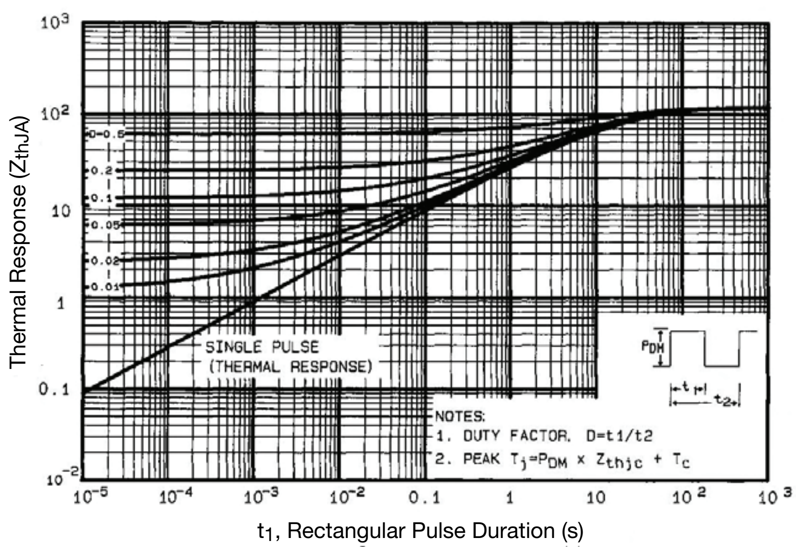


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

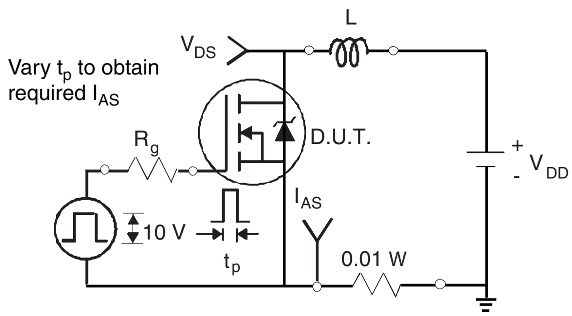


Fig. 12a - Unclamped Inductive Test Circuit

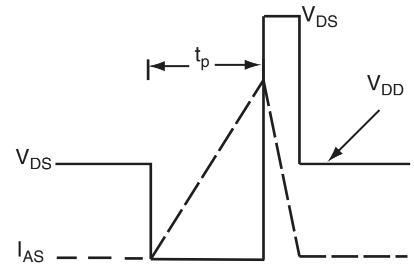


Fig. 12b - Unclamped Inductive Waveforms

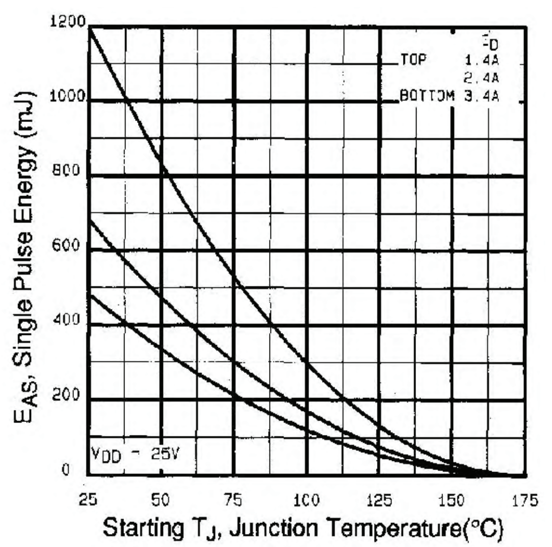


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

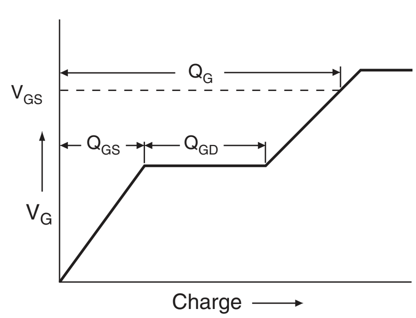


Fig. 13a - Basic Gate Charge Waveform

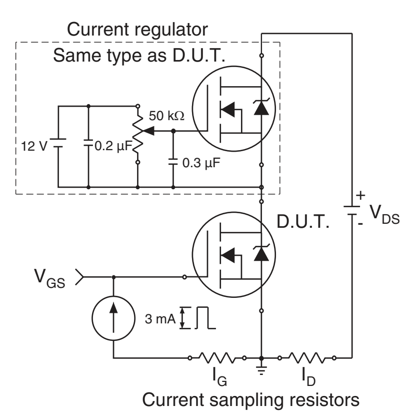
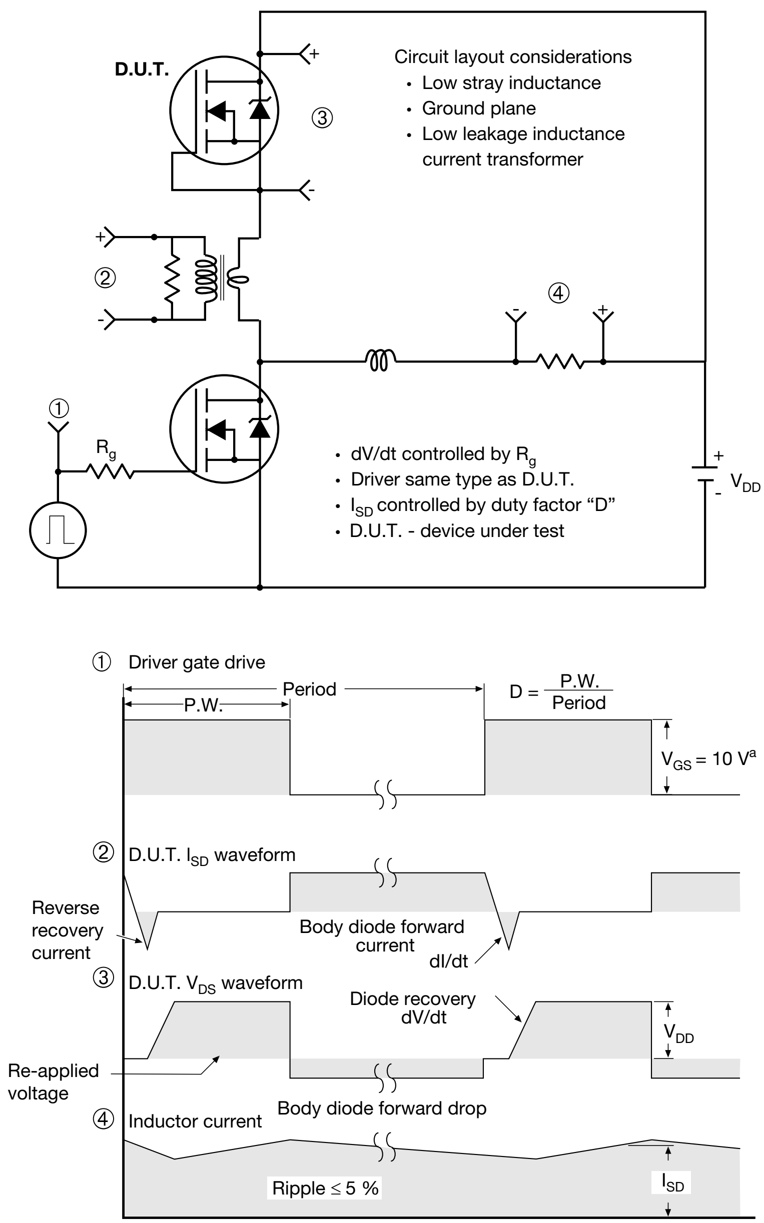


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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