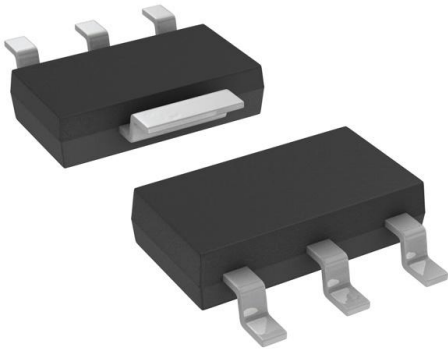


IRLL014TR Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	IRLL014TR-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	IRLL014TR
Description	MOSFET N-CH 60V 2.7A SOT223
Detailed Description	N-Channel 60 V 2.7A (Tc) 2W (Ta), 3.1W (Tc) Surface Mount SOT-223



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

IRLL014TR

Series:

-

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

60 V

Drive Voltage (Max Rds On, Min Rds On):

4V, 5V

Vgs(th) (Max) @ Id:

2V @ 250µA

Vgs (Max):

±10V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

SOT-223

Base Product Number:

IRLL014

Manufacturer:

Vishay Siliconix

Product Status:

Obsolete

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

2.7A (Tc)

Rds On (Max) @ Id, Vgs:

200mOhm @ 1.6A, 5V

Gate Charge (Qg) (Max) @ Vgs:

8.4 nC @ 5 V

Input Capacitance (Ciss) (Max) @ Vds:

400 pF @ 25 V

Power Dissipation (Max):

2W (Ta), 3.1W (Tc)

Mounting Type:

Surface Mount

Package / Case:

TO-261-4, TO-261AA

Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

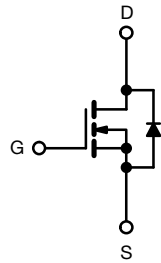
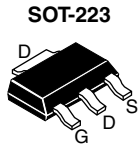
1 (Unlimited)

ECCN:

EAR99



Power MOSFET



N-Channel MOSFET

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Logic-level gate drive
- $R_{DS(on)}$ specified at $V_{GS} = 4\text{ V}$ and 5 V
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

Marking code: LA

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0\text{ V}$ 0.20
Q_g max. (nC)	8.4
Q_{gs} (nC)	3.5
Q_{gd} (nC)	6.0
Configuration	Single

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Lead (Pb)-free and halogen-free	SiHLL014TR-GE3 IRLL014TRPbF-BE3 a, b
Lead (Pb)-free	IRLL014TRPbF a

Notes

- See device orientation
- “-BE3” denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 10	
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	22	W/ $^\circ\text{C}$
Linear derating factor		0.025	
Linear derating factor (PCB mount) ^e		0.017	
Single pulse avalanche energy ^b	E_{AS}	100	mJ
Avalanche current ^a	I_{AR}	2.7	A
Repetitive avalanche energy ^a	E_{AR}	0.31	mJ
Maximum power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	W
		$T_A = 25\text{ }^\circ\text{C}$	
Peak diode recovery dv/dt ^c	dV/dt	4.5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 16\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.7\text{ A}$ (see fig. 12)
- $I_{SD} \leq 10\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	-	60	°C/W	
Maximum junction-to-case (drain)	R_{thJC}	-	-	40		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.073	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 10\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	$I_D = 1.6\text{ A}^b$	-	-	0.20	Ω
		$V_{GS} = 4.0\text{ V}$	$I_D = 1.4\text{ A}^b$	-	-	0.28	
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 1.6\text{ A}$		3.2	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$, see fig. 5		-	400	-	μF
Output capacitance	C_{oss}			-	170	-	
Reverse transfer capacitance	C_{rss}			-	42	-	
Total gate charge	Q_g	$V_{GS} = 5.0\text{ V}$	$I_D = 10\text{ A}, V_{DS} = 48\text{ V},$ see fig. 6 and 13 ^b	-	-	8.4	nC
Gate-source charge	Q_{gs}			-	-	3.5	
Gate-drain charge	Q_{gd}			-	-	6.0	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 10\text{ A},$ $R_g = 12\text{ }\Omega, R_D = 2.8\text{ }\Omega$, see fig. 10 ^b		-	9.3	-	ns
Rise time	t_r			-	110	-	
Turn-off delay time	$t_{d(off)}$			-	17	-	
Fall time	t_f			-	26	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal source inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.7	A
Pulsed diode forward current ^a	I_{SM}			-	-	22	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 2.7\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 10\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	65	130	ns
Body diode reverse recovery charge	Q_{rr}			-	0.33	0.65	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

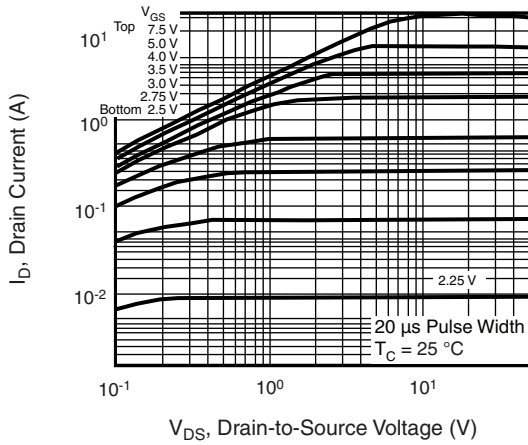


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

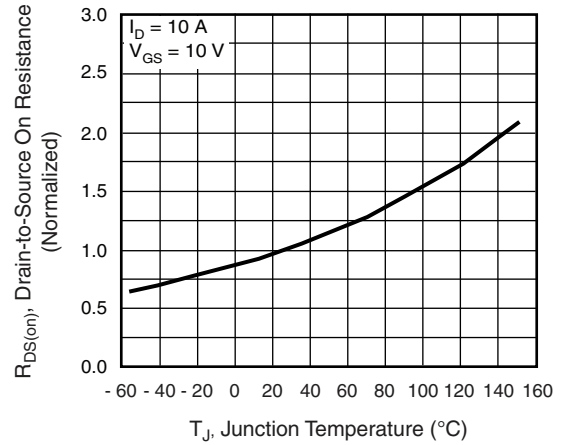


Fig. 4 - Normalized On-Resistance vs. Temperature

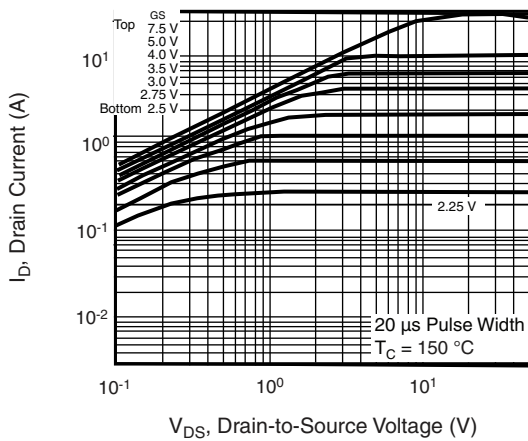


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

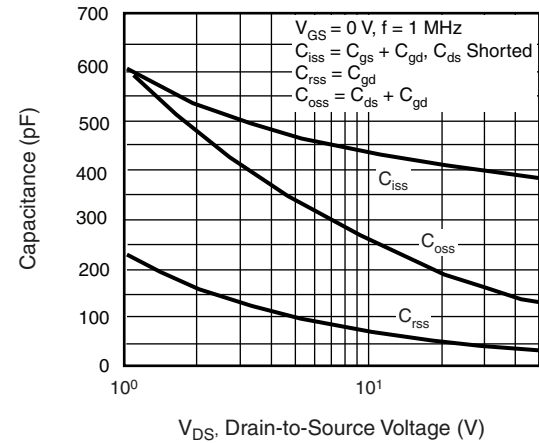


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

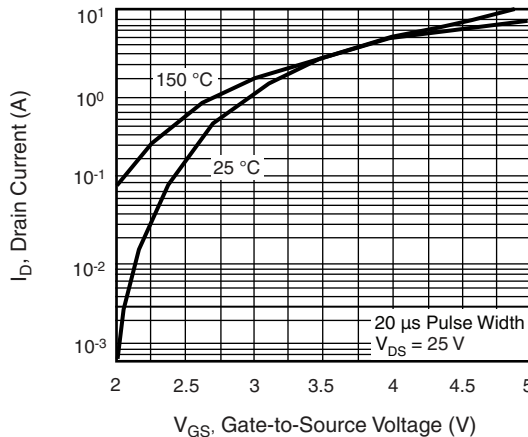


Fig. 3 - Typical Transfer Characteristics

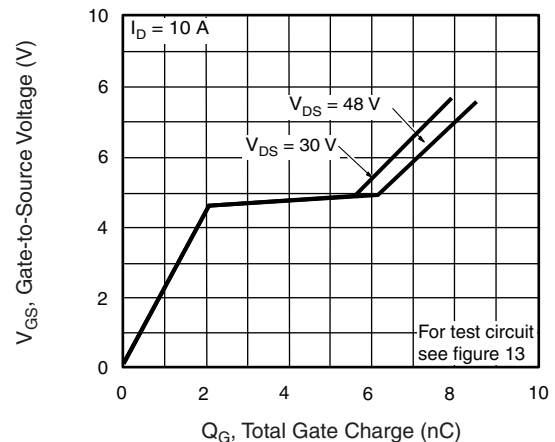


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

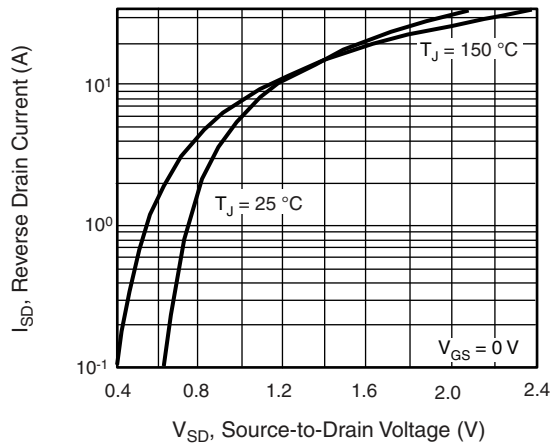


Fig. 7 - Typical Source-Drain Diode Forward Voltage

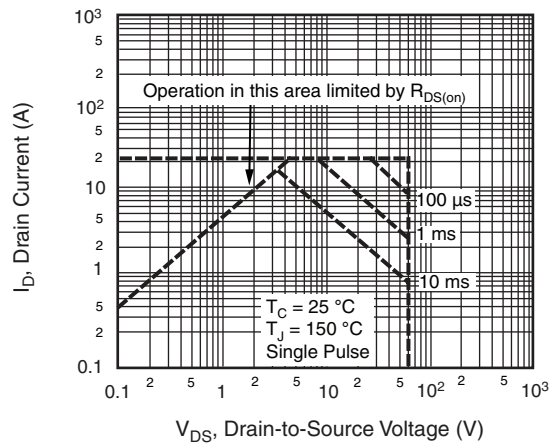


Fig. 8 - Maximum Safe Operating Area

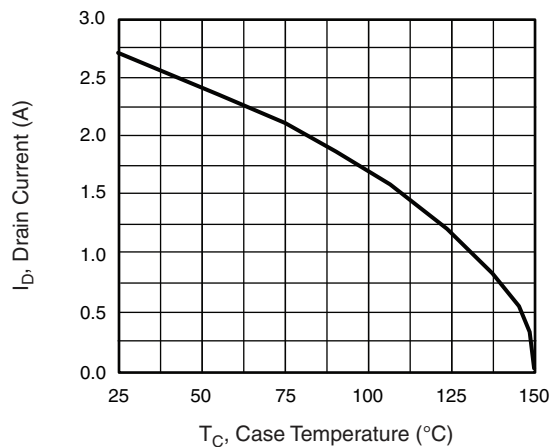


Fig. 9 - Maximum Drain Current vs. Case Temperature

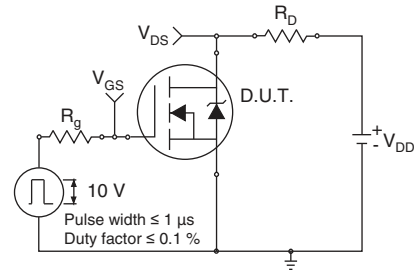


Fig. 10a - Switching Time Test Circuit

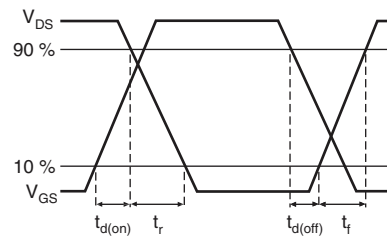


Fig. 10b - Switching Time Waveforms

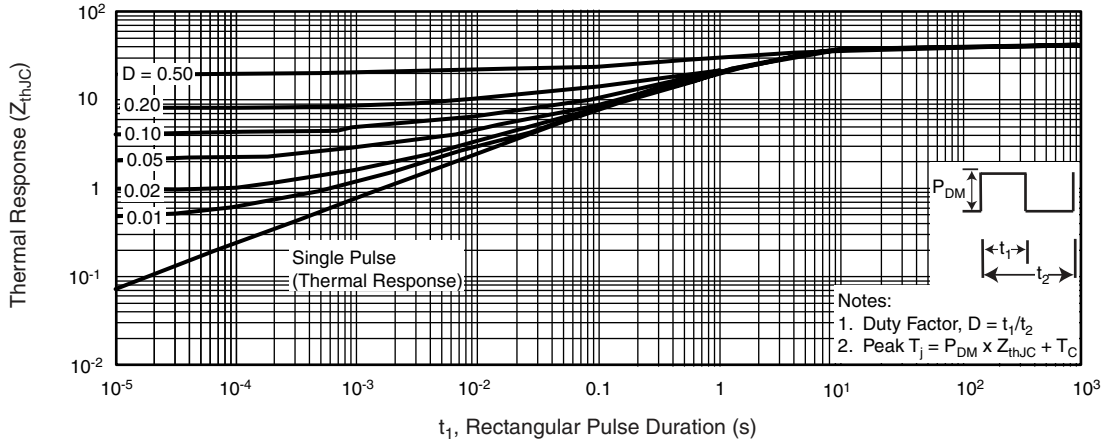


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

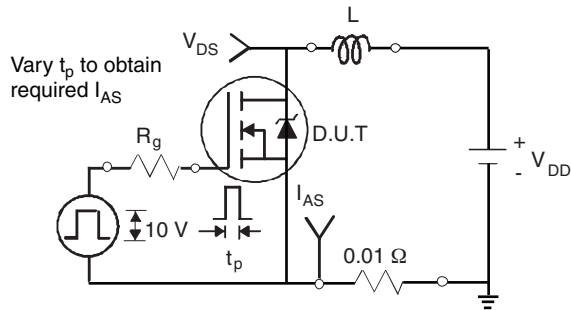


Fig. 12a - Unclamped Inductive Test Circuit

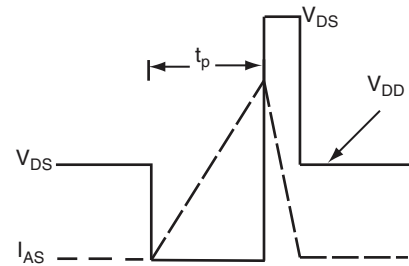


Fig. 12b - Unclamped Inductive Waveforms

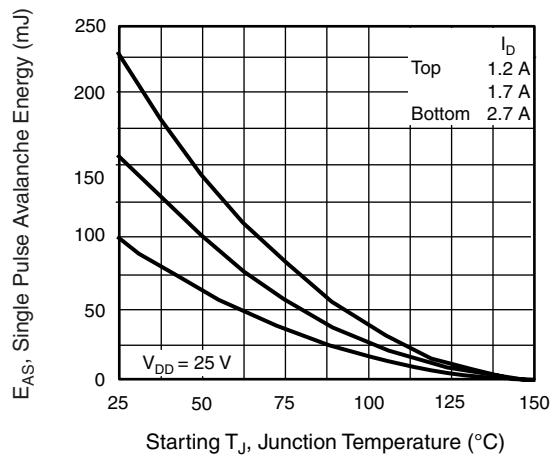


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

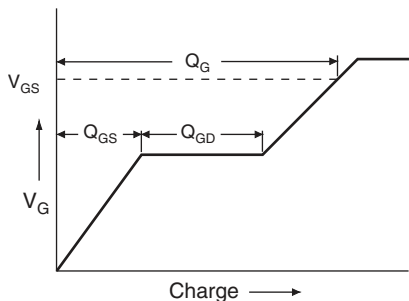


Fig. 13a - Basic Gate Charge Waveform

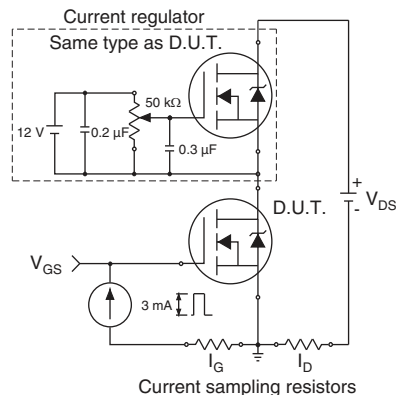
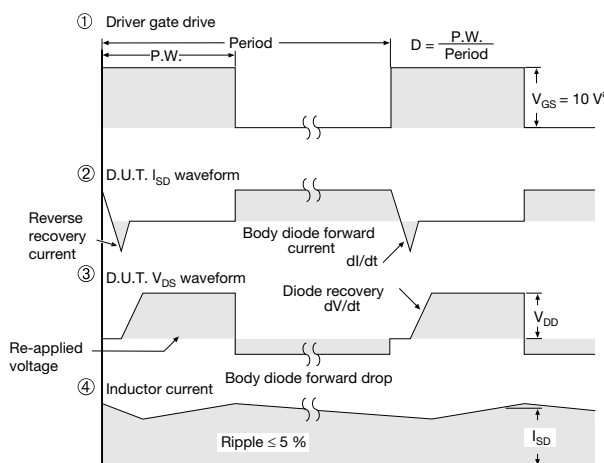
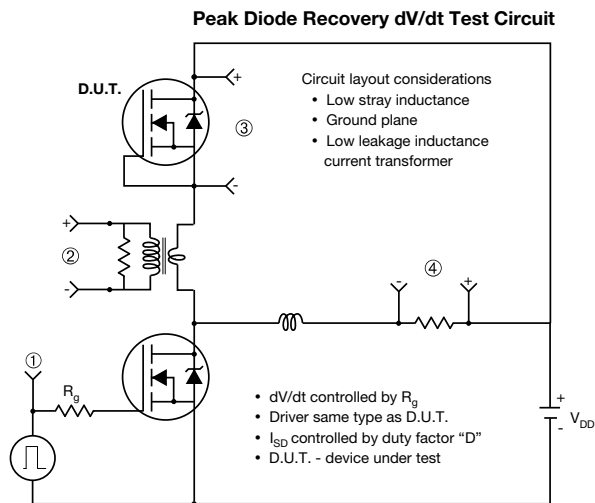


Fig. 13b - Gate Charge Test Circuit



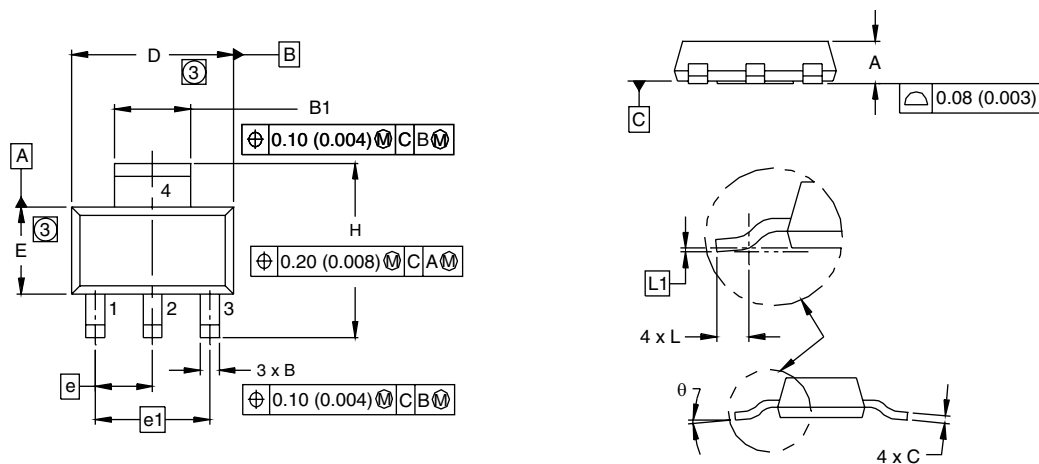
Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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SOT-223 (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10°	-	10°
ECN: S-82109-Rev. A, 15-Sep-08 DWG: 5969				

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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