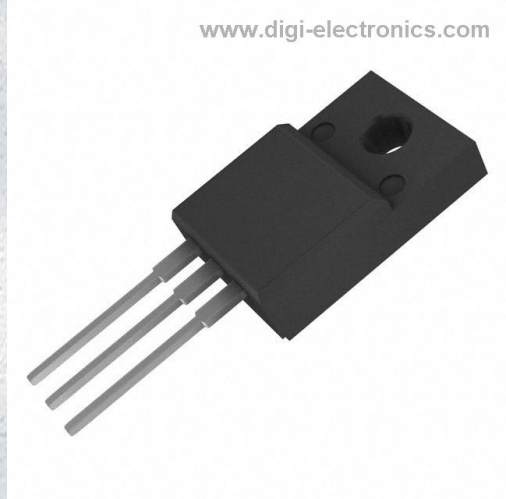
SIHA17N80AE-GE3 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	SIHA17N80AE-GE3-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	SIHA17N80AE-GE3
Description	MOSFET N-CH 800V 7A TO220
Detailed Description	N-Channel 800 V 7A (Tc) 34W (Tc) Through Hole TO-220 Full Pack

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
SIHA17N80AE-GE3	Vishay Siliconix
Series:	Product Status:
-	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
800 V	7A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	290mOhm @ 8.5A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 250µA	62 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±30V	1260 pF @ 100 V
FET Feature:	Power Dissipation (Max):
-	34W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Through Hole
Supplier Device Package:	Package / Case:
TO-220 Full Pack	TO-220-3 Full Pack
Base Product Number:	
SIHA17	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
ECCN:	HTSUS:
EAR99	8541.29.0095

VISHAY
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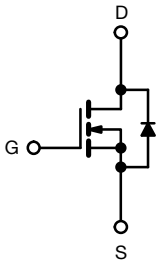
SiHA17N80AE

Vishay Siliconix

E Series Power MOSFET

Thin-Lead TO-220 FULLPAK



N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) R_{on} x Q_g
- Low effective capacitance (Co(er))
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	850	
$R_{DS(on)}$ typ. (Ω) at 25 °C	V_{GS} = 10 V	0.25
Q_g max. (nC)	62	
Q_{gs} (nC)	8	
Q_{gd} (nC)	18	
Configuration	Single	

ORDERING INFORMATION	
Package	Thin-Lead TO-220 FULLPAK
Lead (Pb)-free and halogen-free	SiHA17N80AE-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	800	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current (T_J = 150 °C) [e]	V_{GS} at 10 V	T_C = 25 °C	I_D	7	A
		T_C = 100 °C		4	
Pulsed drain current [a]			I_{DM}	32	
Linear derating factor				0.27	W/°C
Single pulse avalanche energy [b]			E_{AS}	127	mJ
Maximum power dissipation			P_D	34	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	T_J = 125 °C		dV/dt	100	V/ns
Reverse diode dV/dt [d]				17	
Soldering recommendations (peak temperature) [c]	For 10 s			260	°C
Mounting torque	M3 screw			0.6	Nm

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 3.0 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, dI/dt = 100 A/µs, starting T_J = 25 °C
e. Limited by maximum junction temperature

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	3.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	800	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.8	-	V/°C
Gate-source threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	µA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 800 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 640 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 8.5 A	-	0.25	0.29	Ω
Forward transconductance	g_{fs}	V_{DS} = 10 V, I_D = 8.5 A	-	7.1	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	1260	-	pF
Output capacitance	C_{oss}		-	56	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	40	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$		-	245	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 8.5 A, V_{DS} = 640 V	-	41	62	nC
Gate-source charge	Q_{gs}		-	8	-	
Gate-drain charge	Q_{gd}		-	18	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 640 V, I_D = 8.5 A, V_{GS} = 10 V, R_g = 9.1 Ω	-	21	42	ns
Rise time	t_r		-	23	46	
Turn-off delay time	$t_{d(off)}$		-	45	90	
Fall time	t_f		-	31	62	
Gate input resistance	R_g	f = 1 MHz, open drain	0.2	0.5	1.1	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	7	A
Pulsed diode forward current	I_{SM}		-	-	32	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 8.5 A, V_{GS} = 0 V	-	-	1.2	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 8.5 A, dI/dt = 100 A/µs, V_R = 25 V	-	314	628	ns
Reverse recovery charge	Q_{rr}		-	4	8	µC
Reverse recovery current	I_{RRM}		-	21	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

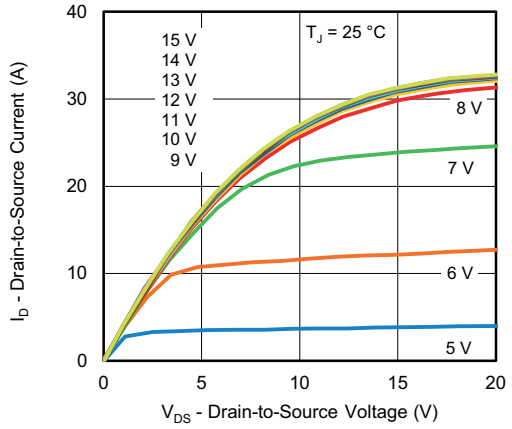


Fig. 1 - Typical Output Characteristics

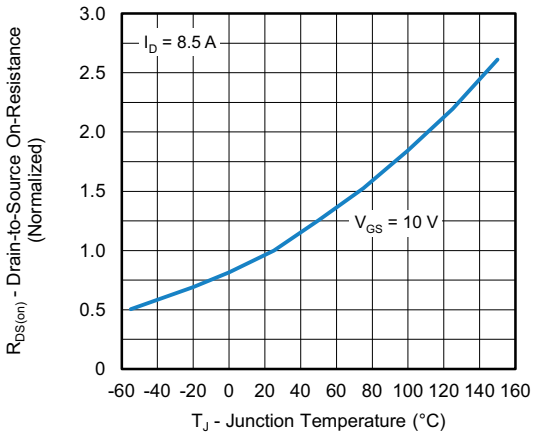


Fig. 4 - Normalized On-Resistance vs. Temperature

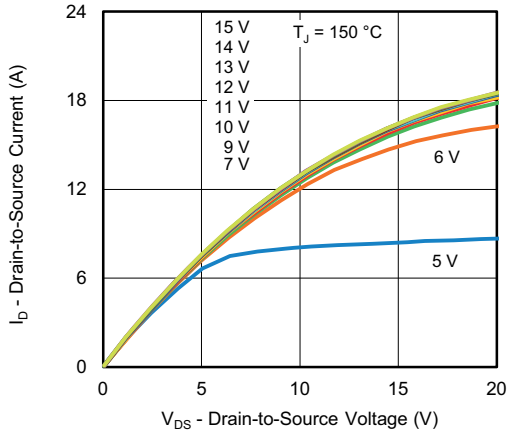


Fig. 2 - Typical Output Characteristics

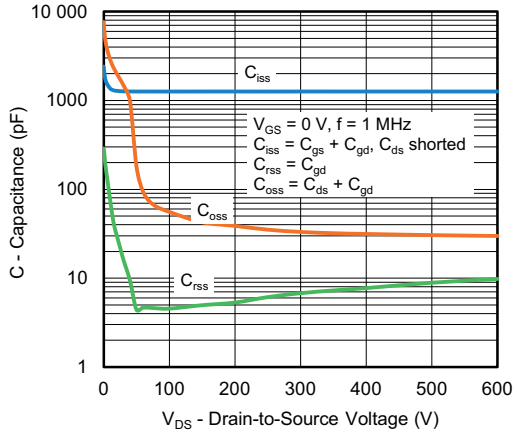


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

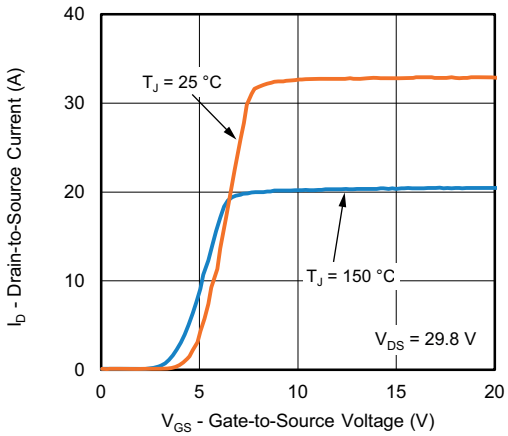


Fig. 3 - Typical Transfer Characteristics

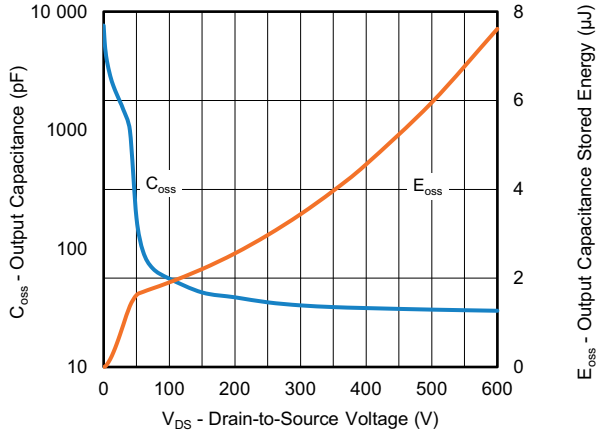


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

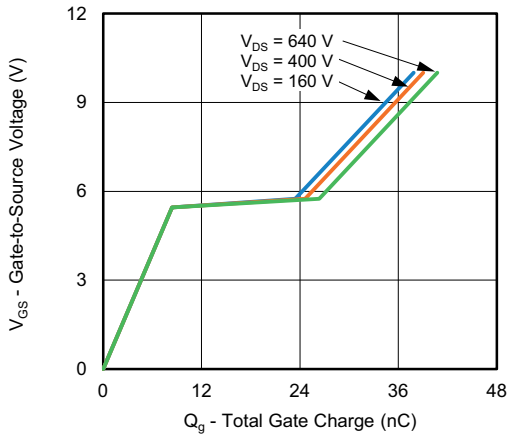


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

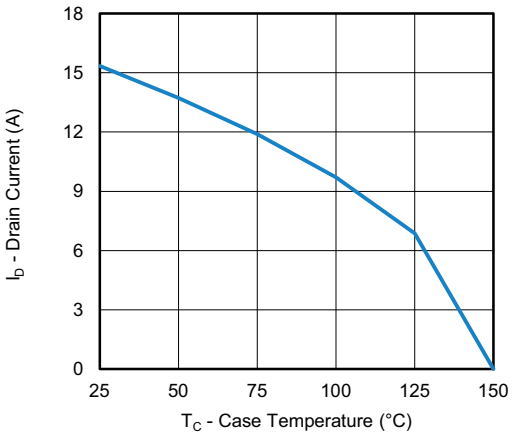


Fig. 10 - Maximum Drain Current vs. Case Temperature

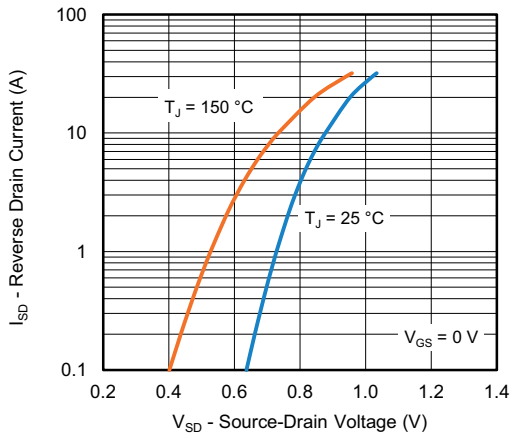


Fig. 8 - Typical Source-Drain Diode Forward Voltage

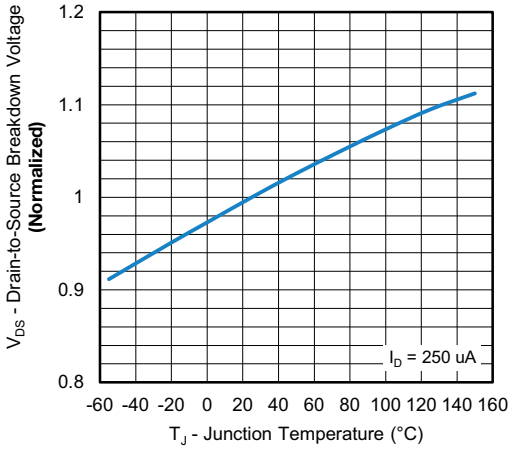


Fig. 11 - Temperature vs. Drain-to-Source Voltage

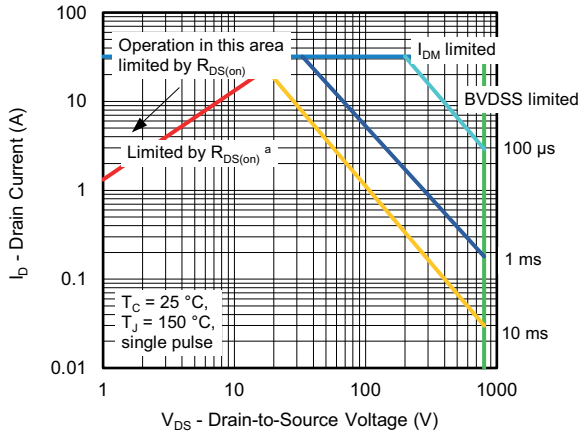


Fig. 9 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

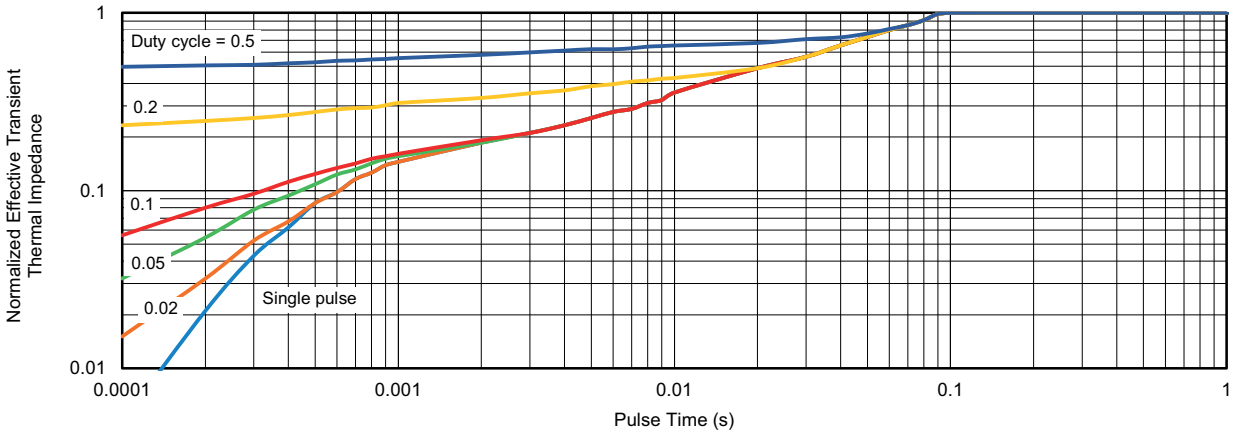


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

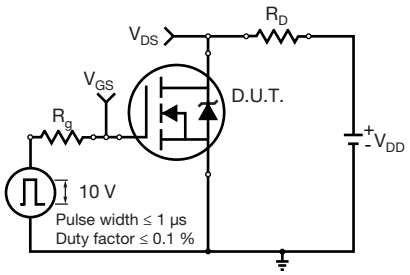


Fig. 13 - Switching Time Test Circuit

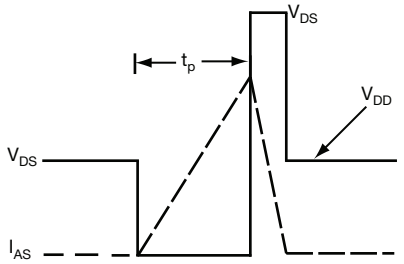


Fig. 16 - Unclamped Inductive Waveforms

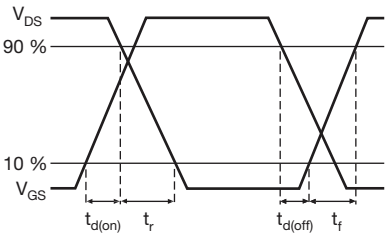


Fig. 14 - Switching Time Waveforms

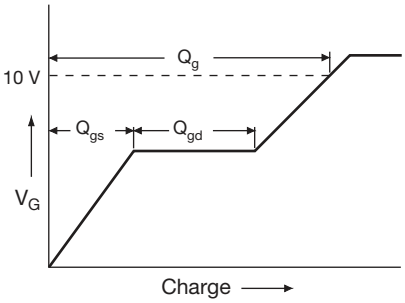


Fig. 17 - Basic Gate Charge Waveform

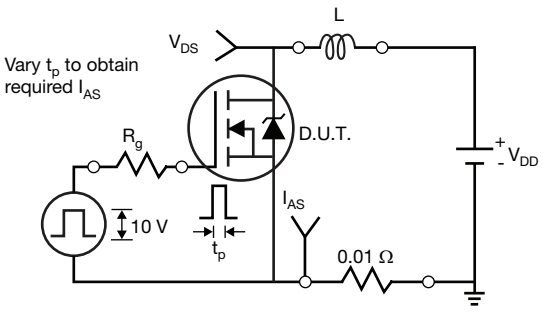


Fig. 15 - Unclamped Inductive Test Circuit

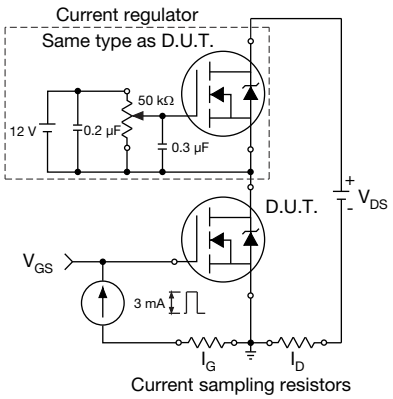
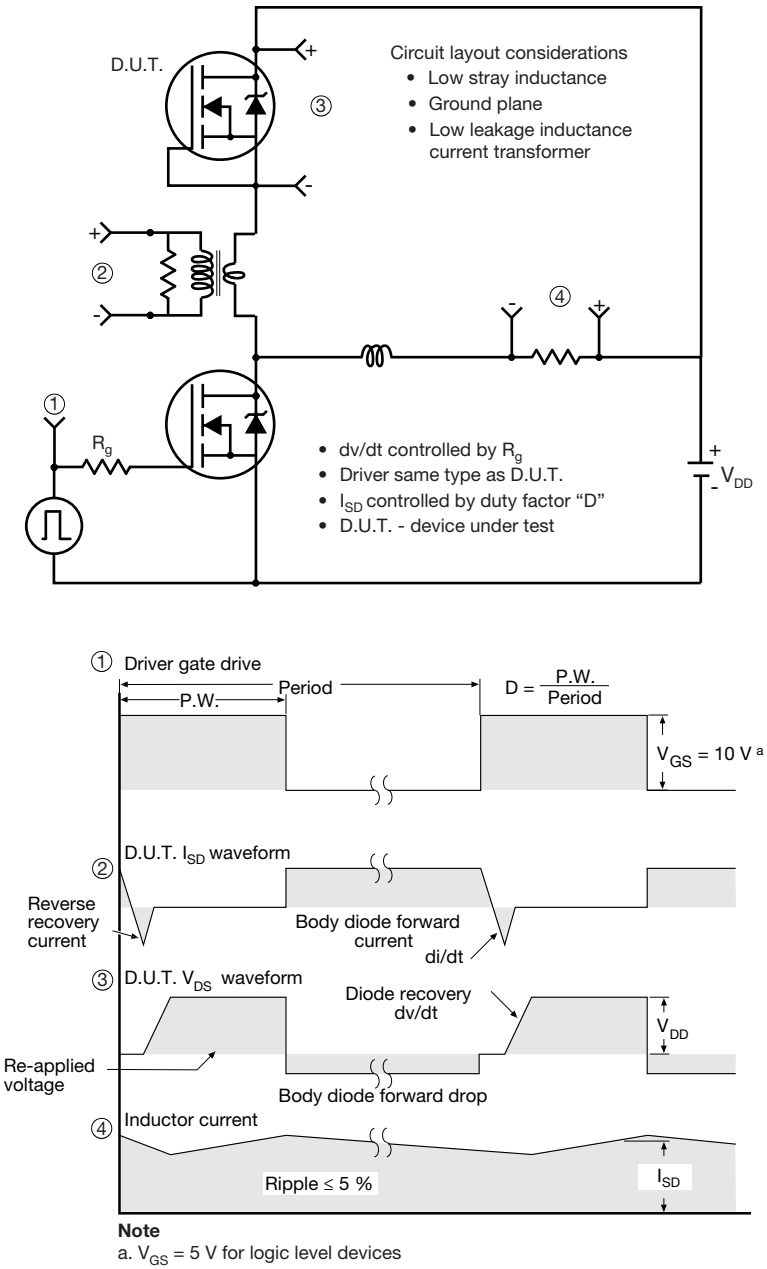


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

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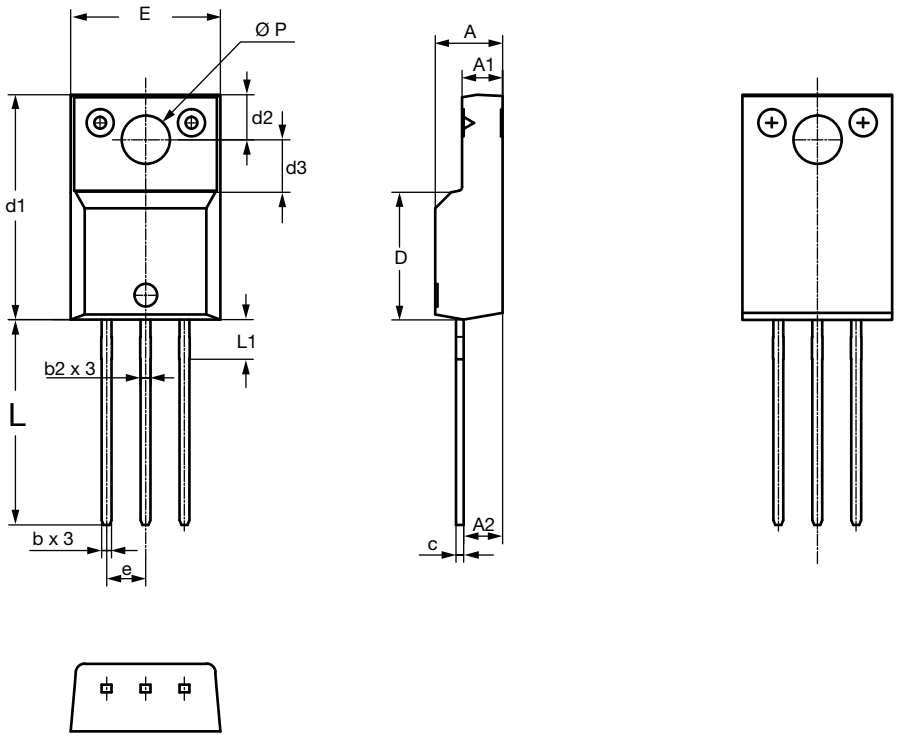
Package Information

Vishay Siliconix

TO-220 FULLPAK Thin Lead



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.30	4.70	0.169	0.185
A1	2.50	2.90	0.098	0.114
A2	2.40	2.80	0.094	0.110
b	0.60	0.80	0.024	0.031
b2	0.60	0.90	0.024	0.035
c	-	0.60	-	0.024
D	8.30	8.70	0.327	0.342
d1	14.70	15.30	0.579	0.602
d2	2.90	3.10	0.114	0.122
d3	3.30	3.70	0.130	0.146
E	9.70	10.30	0.382	0.406
e	2.50	2.70	0.098	0.106
L	13.40	13.80	0.528	0.543
L1	1.00	2.80	0.039	0.110
Ø P	3.00	3.40	0.118	0.134

ECN: E20-0684-Rev. D, 28-Dec-2020
DWG: 6021

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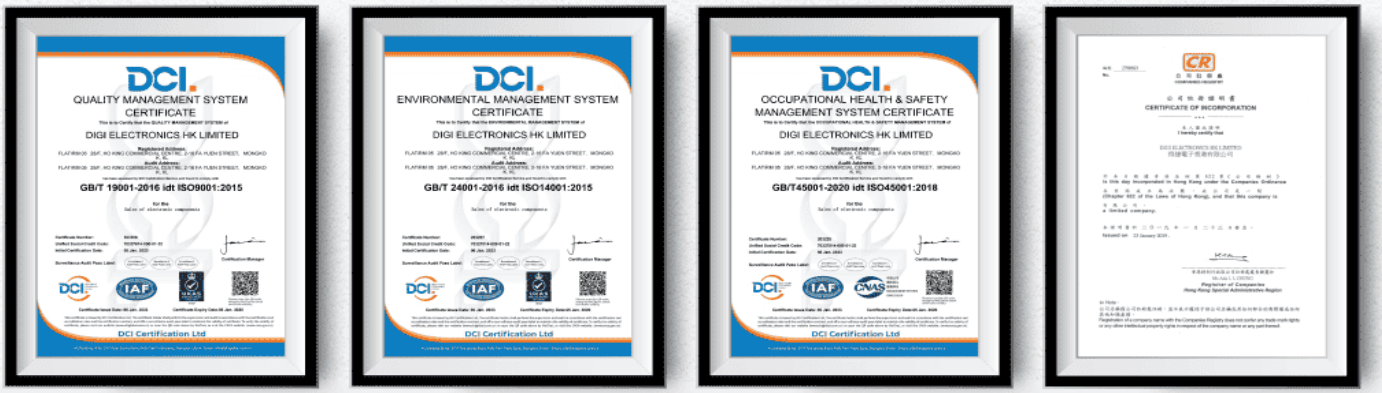

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