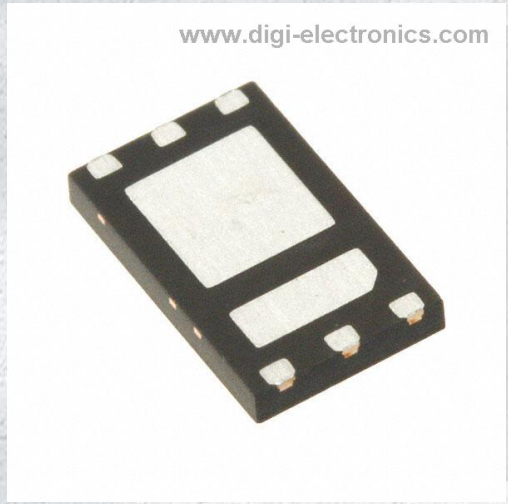
SIZ900DT-T1-GE3 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	SIZ900DT-T1-GE3-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	SIZ900DT-T1-GE3
Description	MOSFET 2N-CH 30V 24A 6PWRPAIR
Detailed Description	Mosfet Array 30V 24A, 28A 48W, 100W Surface Mount 6-PowerPair™

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
SIZ900DT-T1-GE3	Vishay Siliconix
Series:	Product Status:
TrenchFET®	Obsolete
Technology:	Configuration:
MOSFET (Metal Oxide)	2 N-Channel (Half Bridge)
FET Feature:	Drain to Source Voltage (Vdss):
Logic Level Gate	30V
Current - Continuous Drain (Id) @ 25°C:	Rds On (Max) @ Id, Vgs:
24A, 28A	7.2mOhm @ 19.4A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2.4V @ 250µA	45nC @ 10V
Input Capacitance (Ciss) (Max) @ Vds:	Power - Max:
1830pF @ 15V	48W, 100W
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Package / Case:	Supplier Device Package:
6-PowerPair™	6-PowerPair™
Base Product Number:	
SIZ900	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
ECCN:	HTSUS:
EAR99	8541.29.0095

SiZ900DT

Vishay Siliconix

Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
Channel-1	30	0.0072 at V_{GS} = 10 V	24[a]	13.5 nC
		0.0092 at V_{GS} = 4.5 V	24[a]	
Channel-2	30	0.0039 at V_{GS} = 10 V	28[a]	34 nC
		0.0047 at V_{GS} = 4.5 V	28[a]	

FEATURES

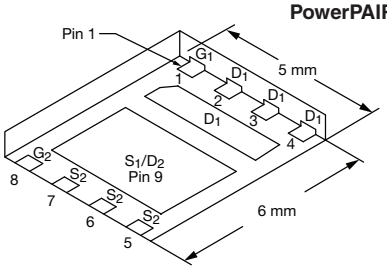
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

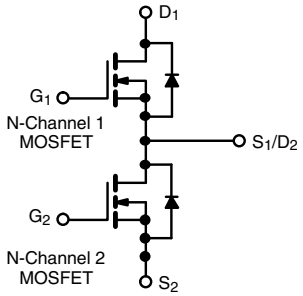
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Notebook System Power
- POL
- Synchronous Buck Converter

PowerPAIR® 6 x 5





Ordering Information: SiZ900DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**Channel-1**	**Channel-2**	**Unit**
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	24[a]	28[a]	A
	T_C = 70 °C		24[a]	28[a]	
	T_A = 25 °C		19[b, c]	28[b, c]	
	T_A = 70 °C		15.5[b, c]	22[b, c]	
Pulsed Drain Current		I_{DM}	90	110	
Continuous Source Drain Diode Current	T_C = 25 °C	I_S	24[a]	28[a]	
	T_A = 25 °C		3.8[b, c]	4.3[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	20	35	
Single Pulse Avalanche Energy		E_{AS}	20	61	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	48	100	W
	T_C = 70 °C		31	64	
	T_A = 25 °C		4.6[b, c]	5.2[b, c]	
	T_A = 70 °C		3[b, c]	3.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[d, e]			260		

THERMAL RESISTANCE RATINGS							
			Channel-1		**Channel-2**		
Parameter		**Symbol**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	22	27	19	24	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.1	2.6	1	1.25	

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 62 °C/W for channel-1 and 55 °C/W for channel-2.

SiZ900DT

Vishay Siliconix

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	Ch-1	30			V
		V_{GS} = 0 V, I_D = 250 µA	Ch-2	30			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	Ch-1		32		mV/°C
		I_D = 250 µA	Ch-2		32		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	Ch-1		- 6		
		I_D = 250 µA	Ch-2		- 6.5		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	1.2		2.4	V
		V_{DS} = V_{GS}, I_D = 250 µA	Ch-2	1		2.2	
Gate Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	Ch-1			± 100	nA
			Ch-2			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	Ch-1			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V	Ch-2			1	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-1			5	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-2			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	Ch-1	20			A
		$V_{DS} \geq$ 5 V, V_{GS} = 10 V	Ch-2	25			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 19.4 A	Ch-1		0.0059	0.0072	Ω
		V_{GS} = 10 V, I_D = 20 A	Ch-2		0.0032	0.0039	
		V_{GS} = 4.5 V, I_D = 17.2 A	Ch-1		0.0075	0.0092	
		V_{GS} = 4.5 V, I_D = 20 A	Ch-2		0.0038	0.0047	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 19.4 A	Ch-1		76		S
		V_{DS} = 10 V, I_D = 20 A	Ch-2		120		
Dynamic[a]							
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1		1830		pF
			Ch-2		4900		
Output Capacitance	C_{oss}		Ch-1		300		
		Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-2		710		
Reverse Transfer Capacitance	C_{rss}		Ch-1		120		
			Ch-2		280		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 19.4 A	Ch-1		29	45	nC
		V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	Ch-2		73	110	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 19.4 A	Ch-1		13.5	21	
			Ch-2		34	51	
Gate-Source Charge	Q_{gs}		Ch-1		5.8		
		Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	Ch-2		15		
Gate-Drain Charge	Q_{gd}		Ch-1		3.1		
			Ch-2		7.3		
Gate Resistance	R_g	f = 1 MHz	Ch-1	0.5	2.4	4.8	Ω
			Ch-2	0.2	0.9	1.8	

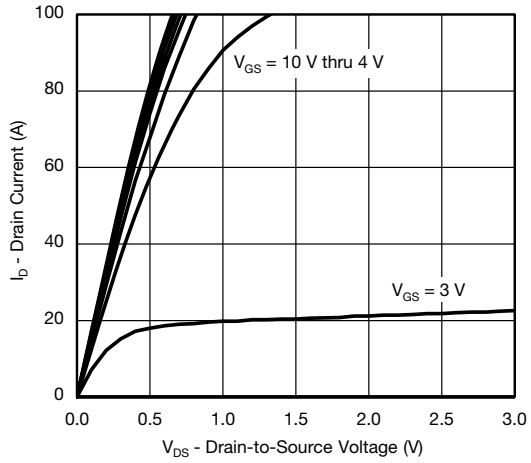
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1		20	40	ns
			Ch-2		35	70	
Rise Time	t_r		Ch-1		10	20	
			Ch-2		10	20	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1		25	50	
			Ch-2		35	70	
Fall Time	t_f		Ch-1		10	20	
			Ch-2		10	20	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1		15	30	
			Ch-2		15	30	
Rise Time	t_r		Ch-1		10	20	
			Ch-2		7	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1		30	60	
			Ch-2		40	80	
Fall Time	t_f		Ch-1		10	20	
			Ch-2		10	20	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	Ch-1			24	A
			Ch-2			28	
Pulse Diode Forward Current[a]	I_{SM}		Ch-1			90	
			Ch-2			110	
Body Diode Voltage	V_{SD}	I_S = 10 A, V_{GS} = 0 V	Ch-1		0.8	1.2	V
		I_S = 10 A, V_{GS} = 0 V	Ch-2		0.8	1.2	
Body Diode Reverse Recovery Time	t_{rr}	Channel-1 I_F = 10 A, dI/dt = 100 A/µs, T_J = 25 °C	Ch-1		16	30	ns
			Ch-2		30	60	
Body Diode Reverse Recovery Charge	Q_{rr}		Ch-1		6	12	nC
			Ch-2		21	40	
Reverse Recovery Fall Time	t_a	Channel-2 I_F = 10 A, dI/dt = 100 A/µs, T_J = 25 °C	Ch-1		9		ns
			Ch-2		17		
Reverse Recovery Rise Time	t_b		Ch-1		7		
			Ch-2		13		

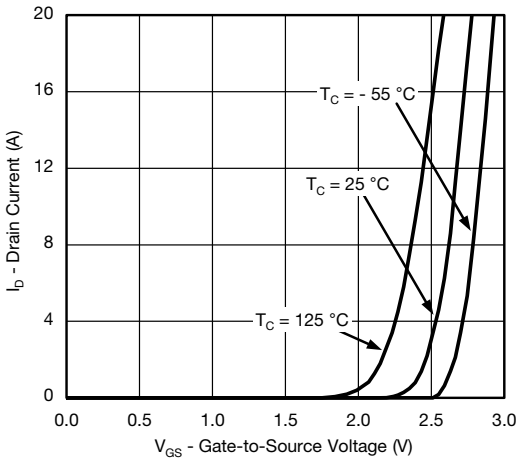
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

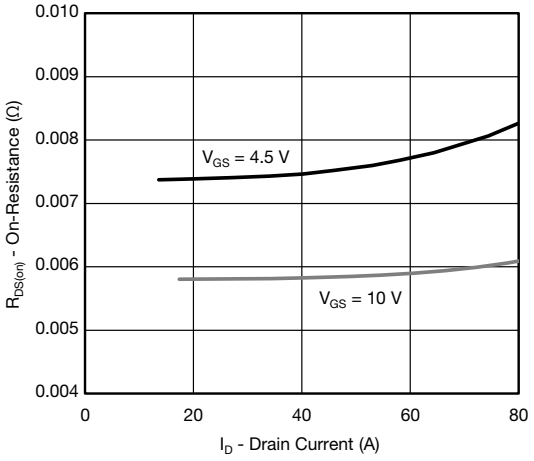
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



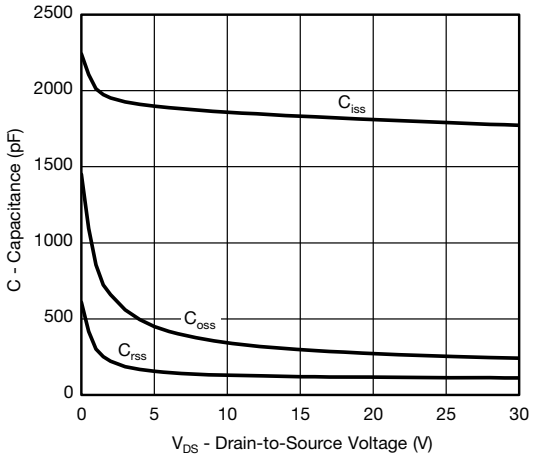
Output Characteristics



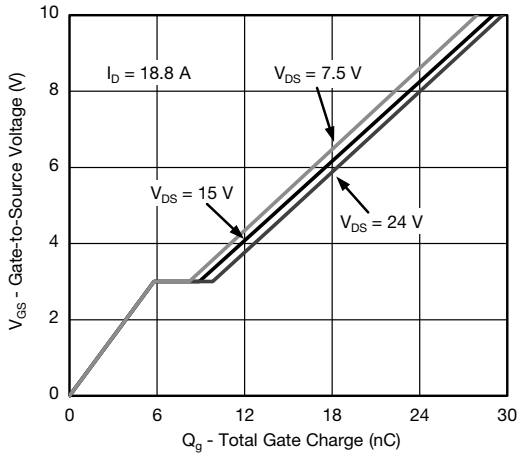
Transfer Characteristics



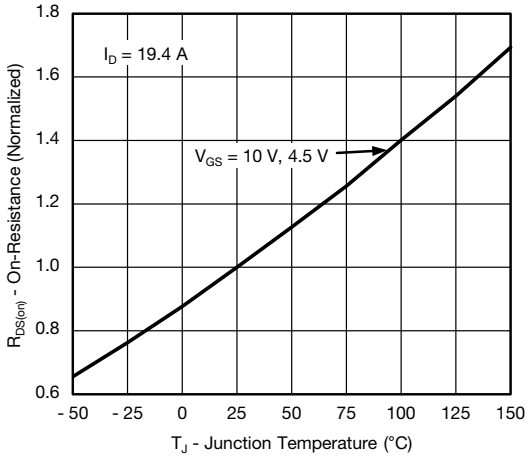
On-Resistance vs. Drain Current



Capacitance

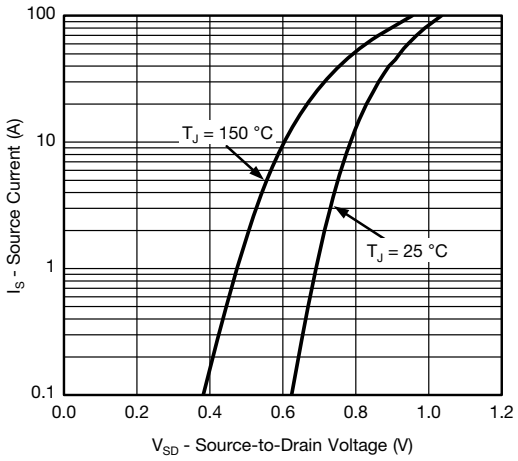


Gate Charge

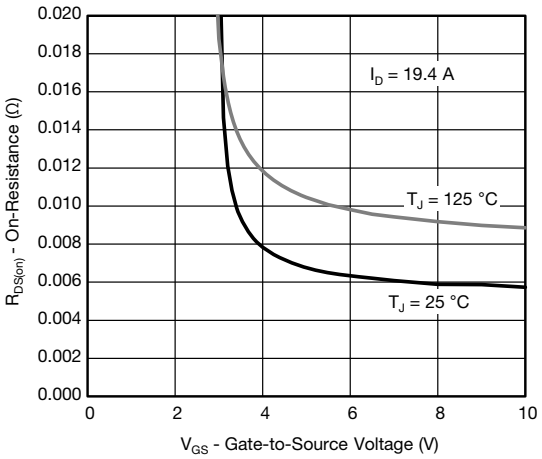


On-Resistance vs. Junction Temperature

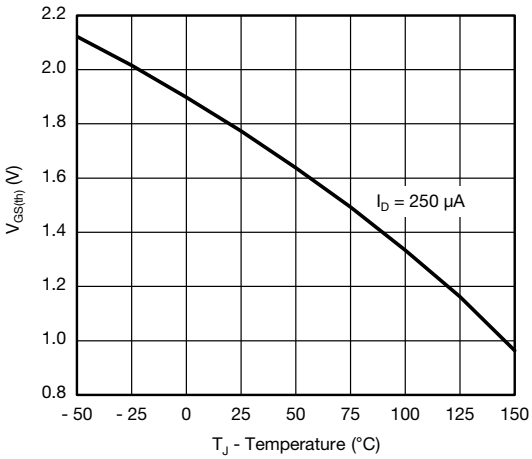
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



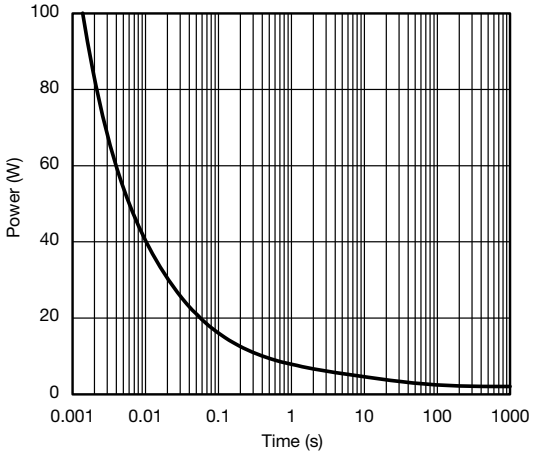
Source-Drain Diode Forward Voltage



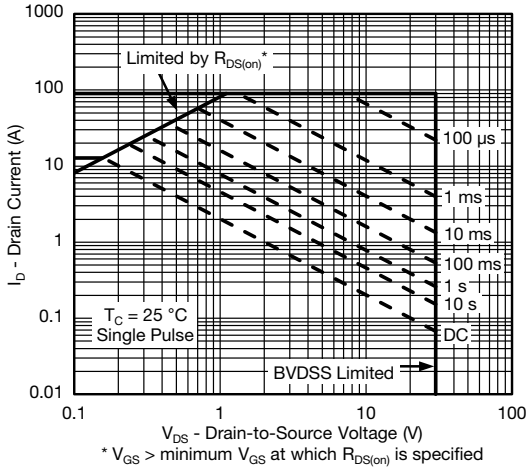
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

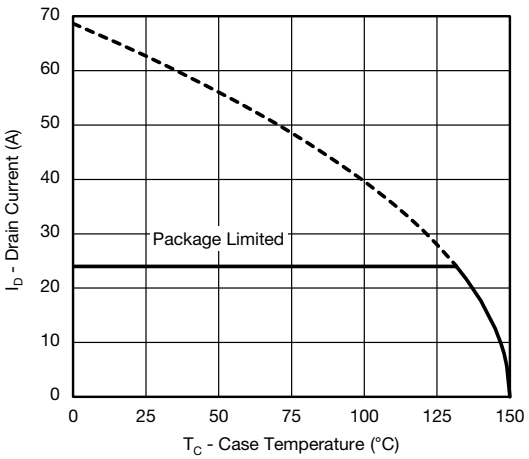


Single Pulse Power

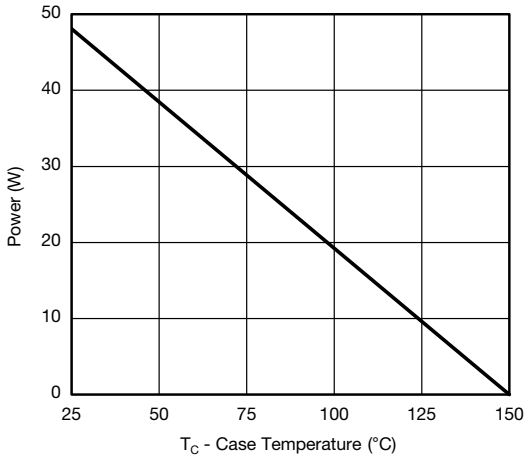


Safe Operating Area, Junction-to-Ambient

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



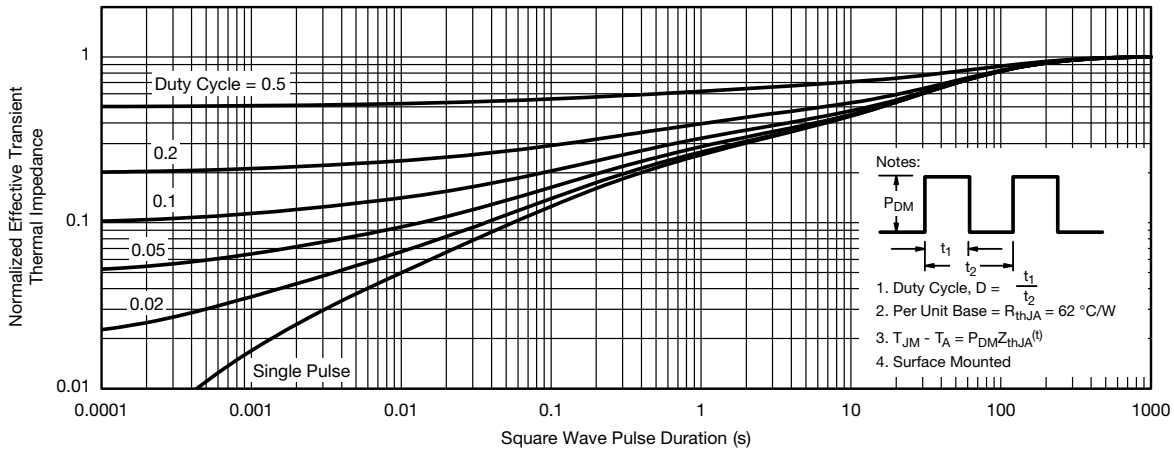
Current Derating*



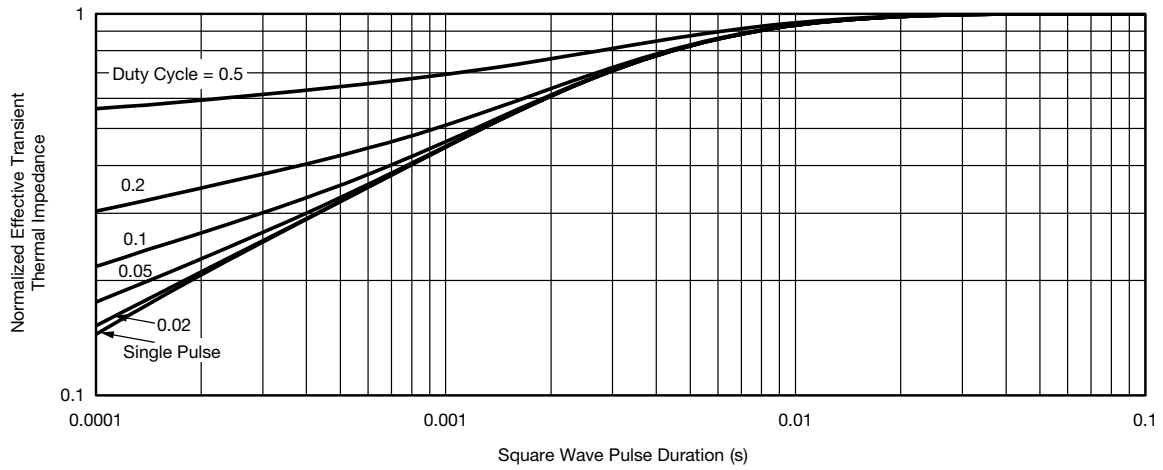
Power, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

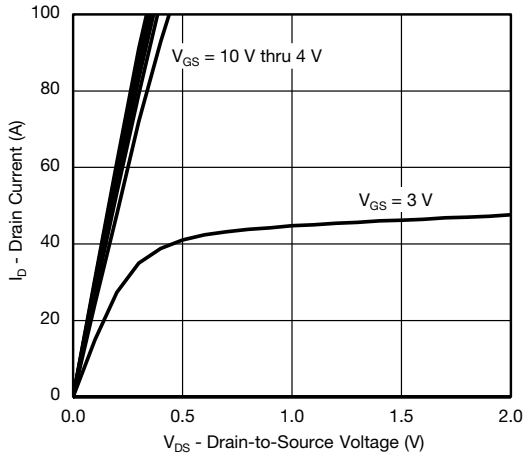


Normalized Thermal Transient Impedance, Junction-to-Ambient

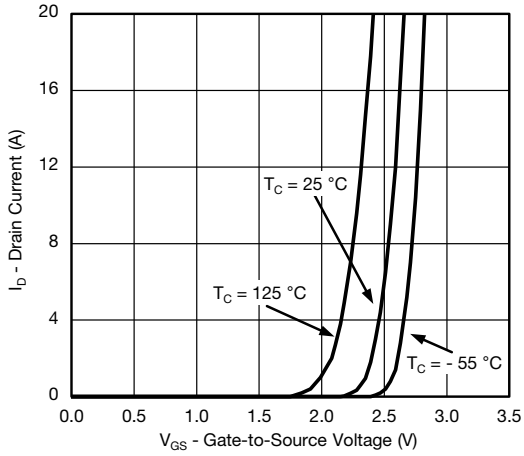


Normalized Thermal Transient Impedance, Junction-to-Case

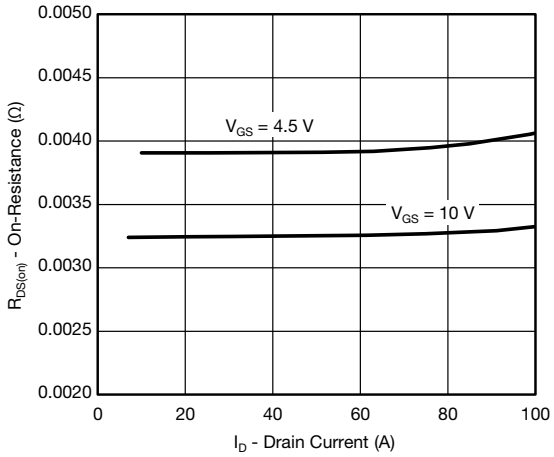
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



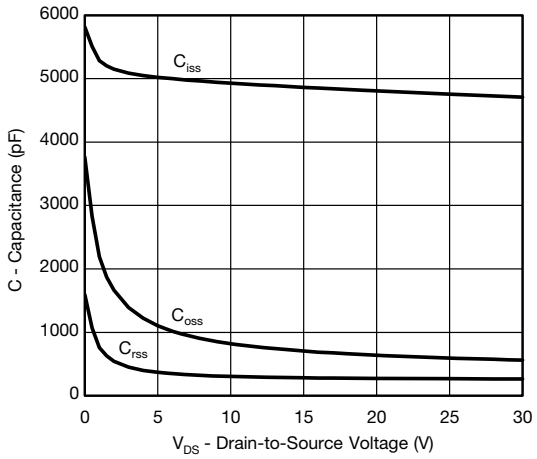
Output Characteristics



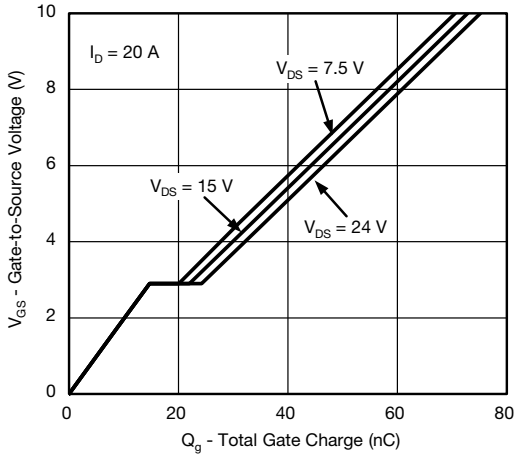
Transfer Characteristics



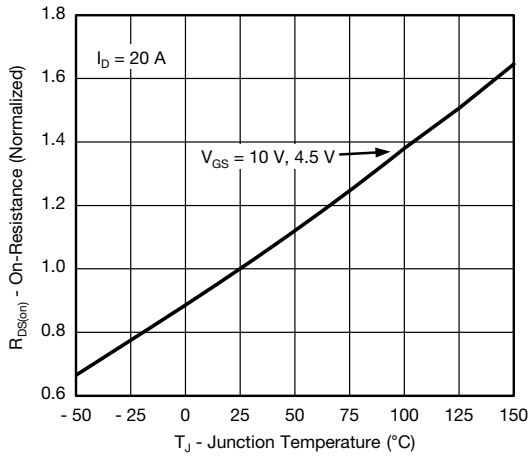
On-Resistance vs. Drain Current



Capacitance



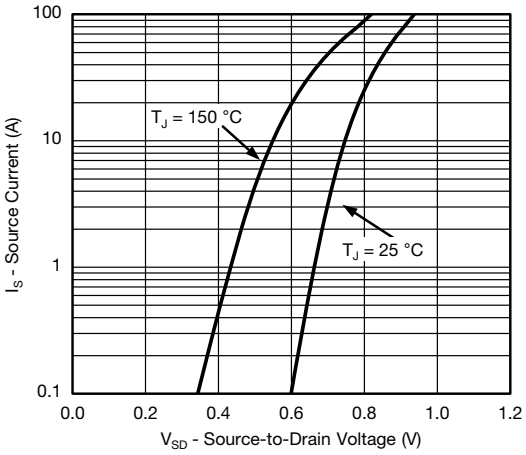
Gate Charge



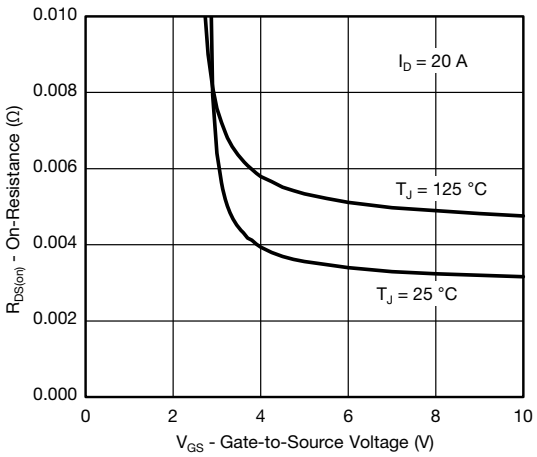
On-Resistance vs. Junction Temperature

Document Number: 67344
S11-2380-Rev. C, 28-Nov-11

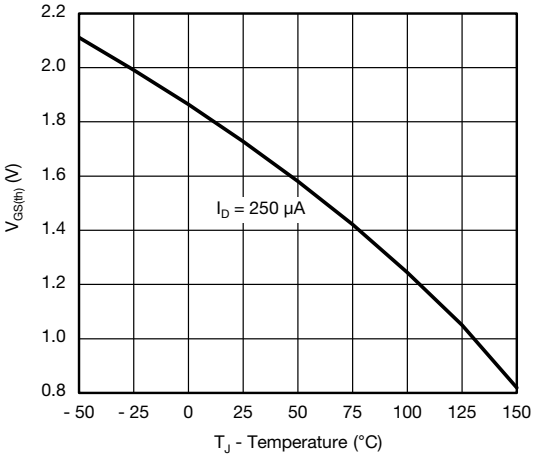
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



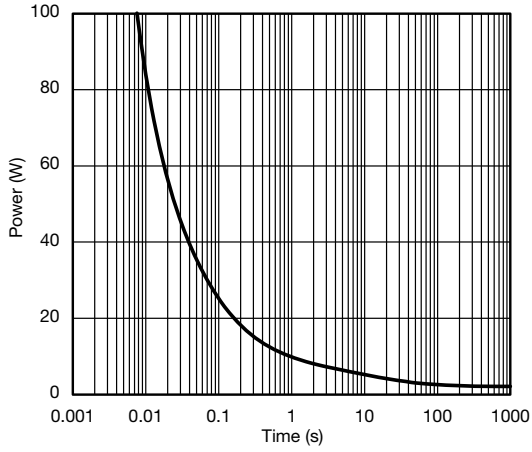
Source-Drain Diode Forward Voltage



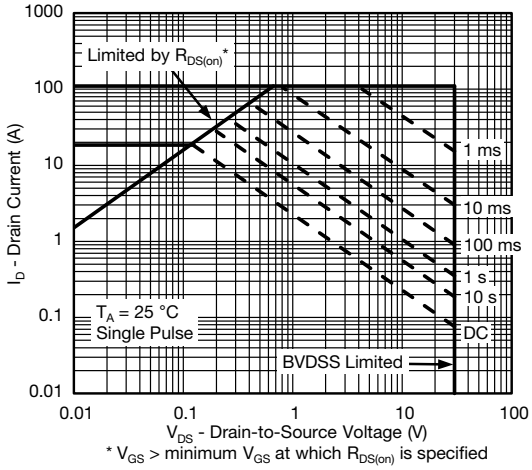
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

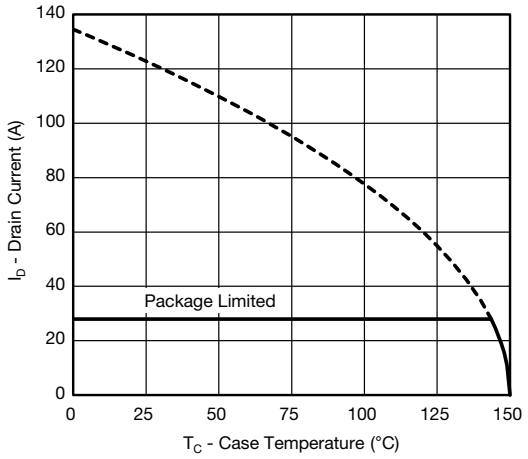


Single Pulse Power

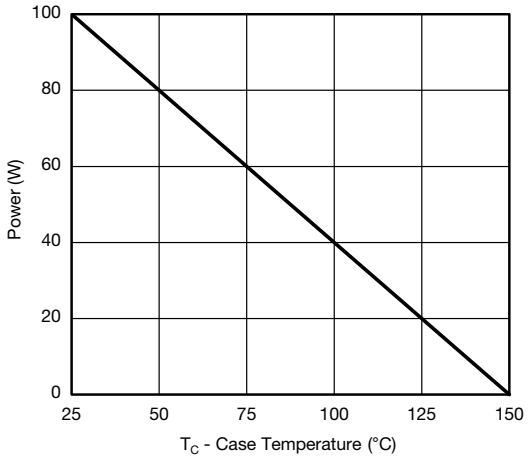


Safe Operating Area, Junction-to-Ambient

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*

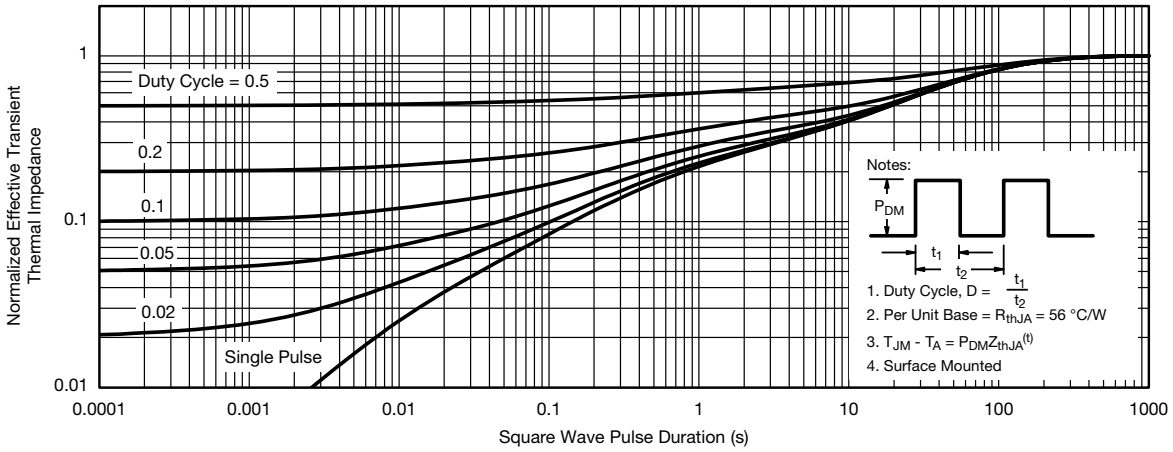


Power, Junction-to-Case

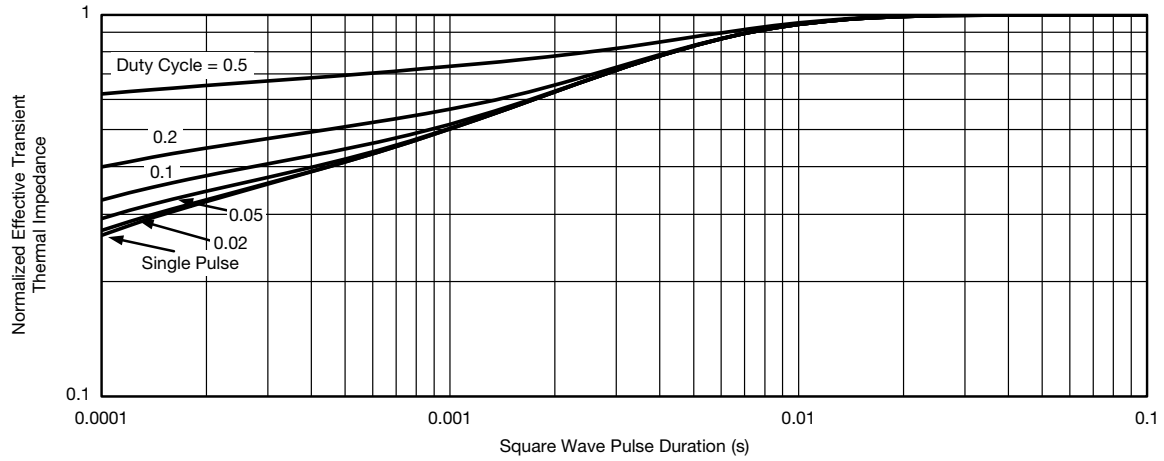
* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Document Number: 67344
S11-2380-Rev. C, 28-Nov-11

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67344.

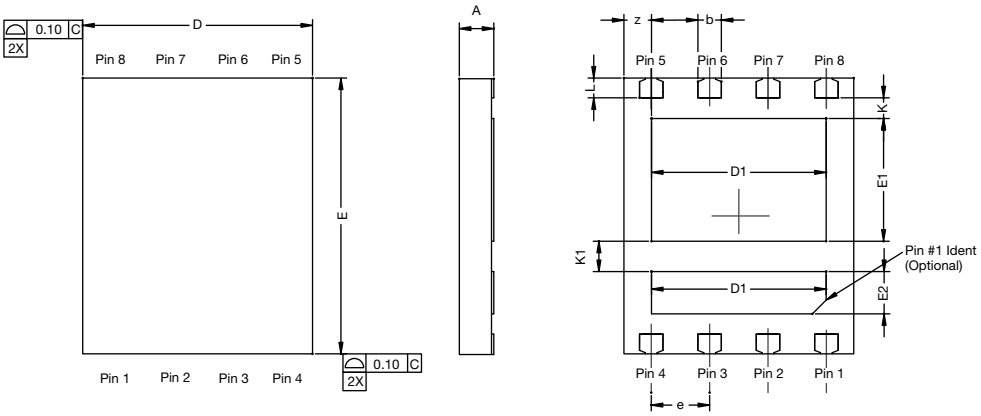
www.vishay.com

Package Information

Vishay Siliconix

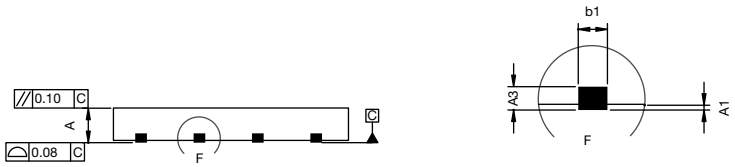
PowerPAIR® 6 x 5 BW Case Outline

(for SiZ900DT only)



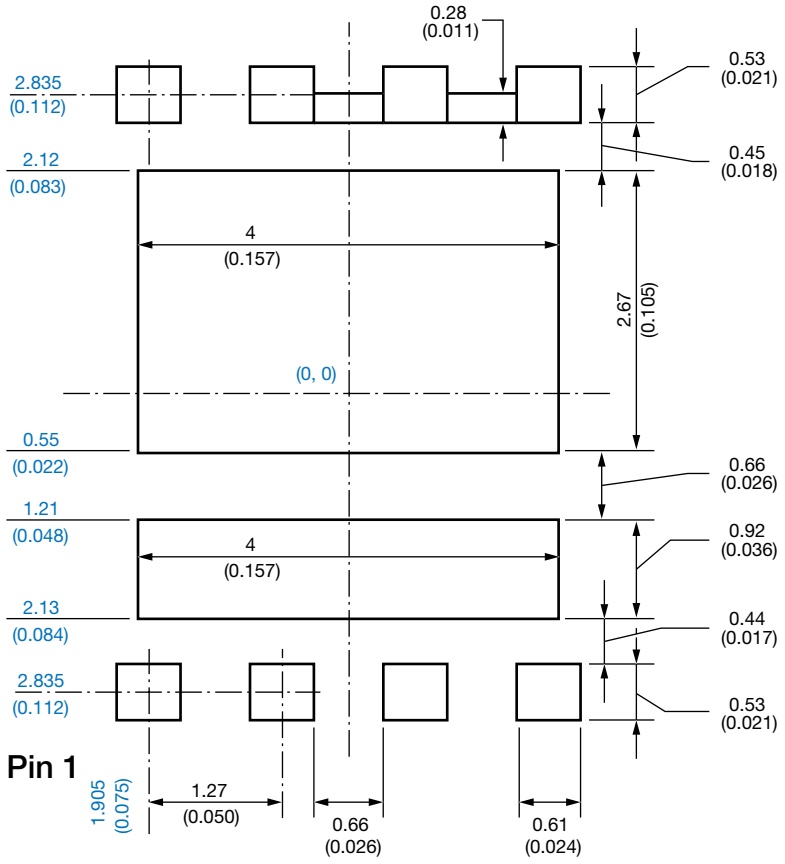
TOP SIDE VIEW

BACK SIDE VIEW



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.10	0.000	-	0.004
A3	0.20 REF			0.008 REF		
b	0.51 BSC			0.020 BSC		
b1	0.25 BSC			0.010 BSC		
D	5.00 BSC			0.197 BSC		
D1	3.75	3.80	3.85	0.148	0.150	0.152
E	6.00 BSC			0.236 BSC		
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.005 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
L	0.43 BSC			0.017 BSC		
z	0.34 BSC			0.013 BSC		
ECN: C11-1247-Rev. D, 31-Oct-11 DWG: 5978						

Recommended Minimum PAD for PowerPAIR® 6 x 5



Dimensions in millimeters (inch)

Note

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.

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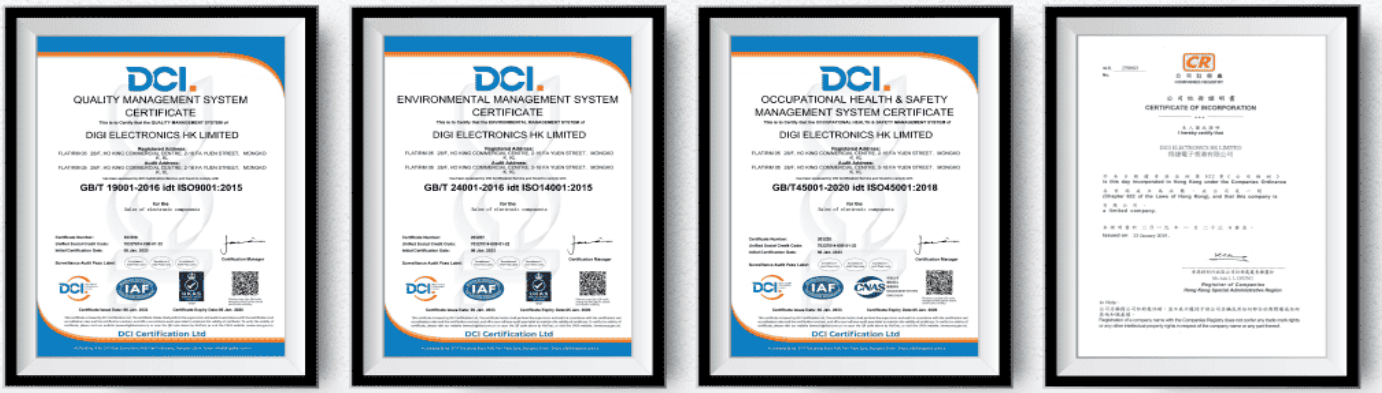

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